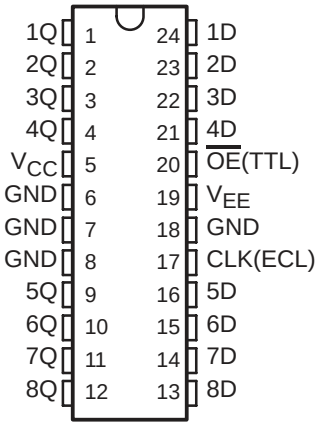
SN10KHT5574
OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS

SDZS010 − JANUARY 1990 − REVISED OCTOBER 1990

- **10KH Compatible**
- **ECL Clock and TTL Control Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight flip-flops of the SN10KHT5574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

A buffered output-enable input ($\overline{OE}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable input $\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN10KHT5574 is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

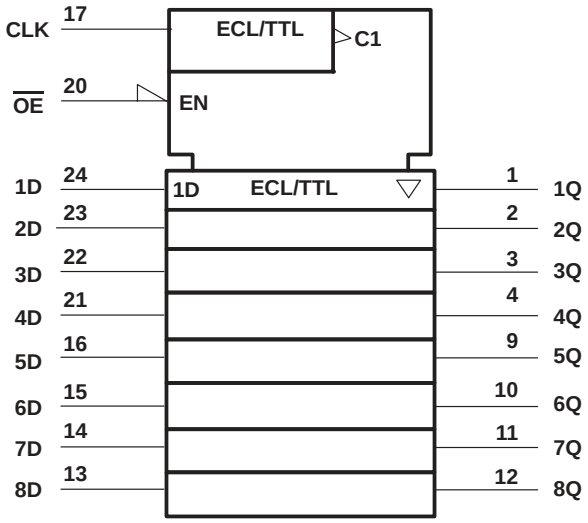
INPUTS			OUTPUT (TTL)
$\overline{OE}$	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q_0
H	X	X	Z

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1990, Texas Instruments Incorporated

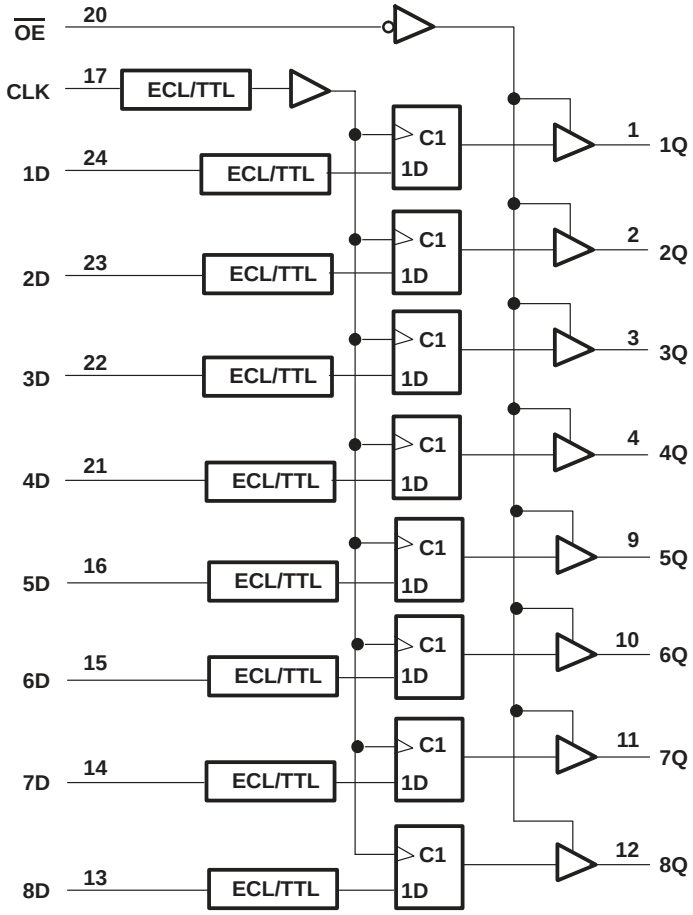
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251−1443

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Supply voltage range, V_{EE} . . . . . −8 V to 0 V
Input voltage range: TTL (see Note 1) . . . . . −1.2 V to 7 V
ECL . . . . . V_{EE} to 0 V
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Input current range, (TTL) . . . . . −30 mA to 5 mA
Current into any output in the low state . . . . . 96 mA
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage		4.5	5	5.5	V
V_{EE}	ECL supply voltage		−4.94	−5.2	−5.46	V
V_{IH}	TTL high-level input voltage		2			V
V_{IL}	TTL low-level input voltage				0.8	V
V_{IH}	ECL high-level input voltage‡	T_A = 0°C	−1170		−840	mV
		T_A = 25°C	−1130		−810	
		T_A = 75°C	−1070		−735	
V_{IL}	ECL low-level input voltage‡	T_A = 0°C	−1950		−1480	mV
		T_A = 25°C	−1950		−1480	
		T_A = 75°C	−1950		−1450	
I_{IK}	TTL input clamp current				−18	mA
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current				48	mA
T_A	Operating free-air temperature range		0		75	°C

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{OE}$ only	V_{CC} = 4.5 V,	V_{EE} = −4.94 V,	I_I = −18 mA				−1.2	V
V_{OH}		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ±5%,	I_{OH} = −3 mA		2.4	3.3		V
		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ±5%,	I_{OH} = −15 mA		2	3.1		
V_{OL}		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ±5%,	I_{OL} = 48 mA			0.38	0.55	V
I_I	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 7 V				0.1	mA
I_{IH}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 2.7 V				20	µA
I_{IL}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 0.5 V				−0.5	mA
I_{IH}	Data inputs and CLK	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −840 mV	T_A = 0°C			350	µA
		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −810 mV	T_A = 25°C			350	
		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −735 mV	T_A = 75°C			350	
I_{IL}	Data inputs and CLK	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −1950 mV	T_A = 0°C	0.5			µA
					T_A = 25°C	0.5			
					T_A = 75°C	0.5			
I_{OZH}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_O = 2.7 V				50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_O = 0.5 V				−50	µA
I_{OS}‡		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_O = 0 V		−100		−225	mA
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				66	95	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				76	110	mA
I_{CCZ}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				74	106	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				−43	−61	mA
C_i		V_{CC} = 5.5 V,	V_{EE} = −5.2 V,	f = 10 MHz			5		pF
C_o		V_{CC} = 5.5 V,	V_{EE} = −5.2 V,	f = 10 MHz			7		pF

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements

			V_{CC} = 4.5 V to 5.5 V, V_{EE} = −4.94 V to −5.46 V, T_A = MIN to MAX§		UNIT
			MIN	MAX	
t_w	Pulse duration	CLK high	4		ns
		CLK low	4		
t_{su}	Setup time before CLK↑	Data high	1		ns
		Data low	1		
t_h	Hold time after CLK↑	Data high	1		ns
		Data low	1		

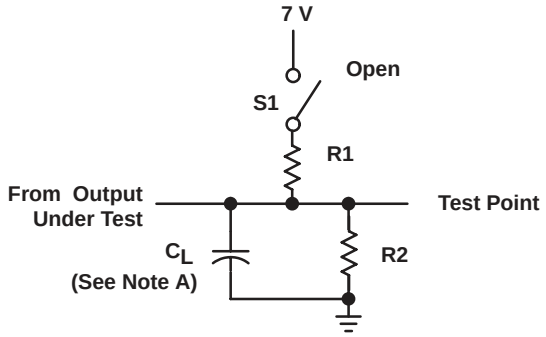
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
f_{max}			200	300		MHz
t_{PLH}	CLK	Q	2.3	4.1	7	ns
t_{PHL}			2.9	4.6	7.4	
t_{PZH}	$\overline{OE}$	Q	1.9	3.6	6.3	ns
t_{PZL}			2.7	4.8	7.7	
t_{PHZ}	$\overline{OE}$	Q	2.1	3.9	6.1	ns
t_{PLZ}			0.5	3.4	6.3	

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.

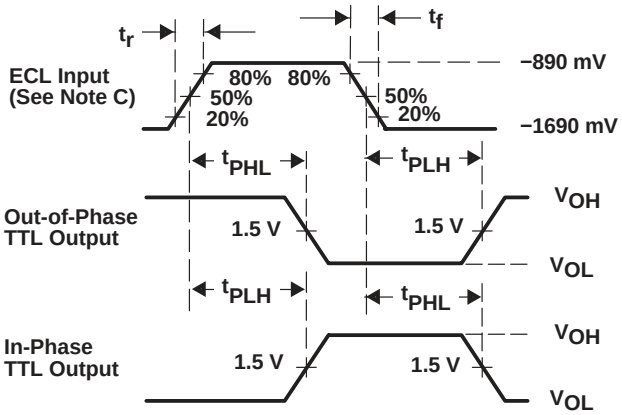
PARAMETER MEASUREMENT INFORMATION



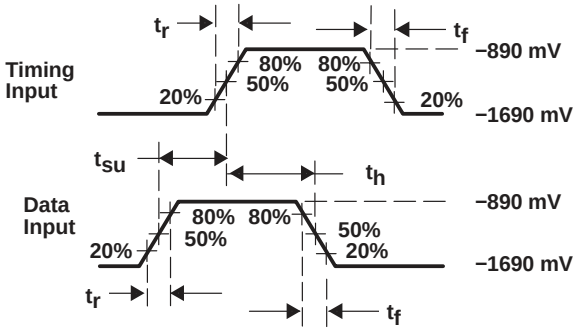
LOAD CIRCUIT

SWITCH POSITION TABLE

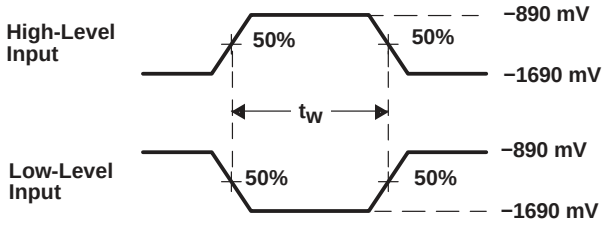
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



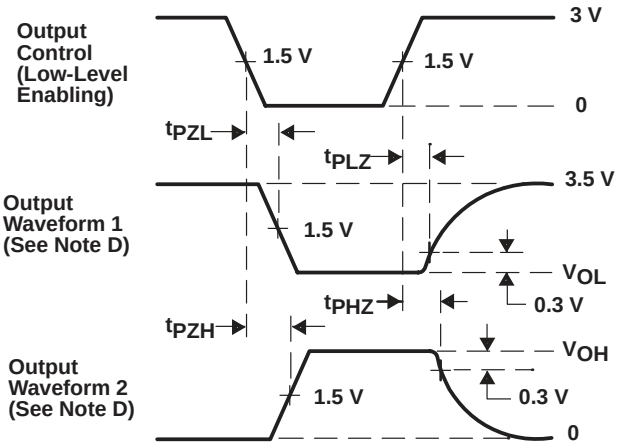
VOLTAGE WAVEFORMS
ECL-INPUT PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
TTL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. For TTL inputs, input pulses are supplied by generators having the following characteristics PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1.5 ns, t_f ≤ 1.5 ns.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load circuit and voltage waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN10KHT5574DW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	10KHT5574	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

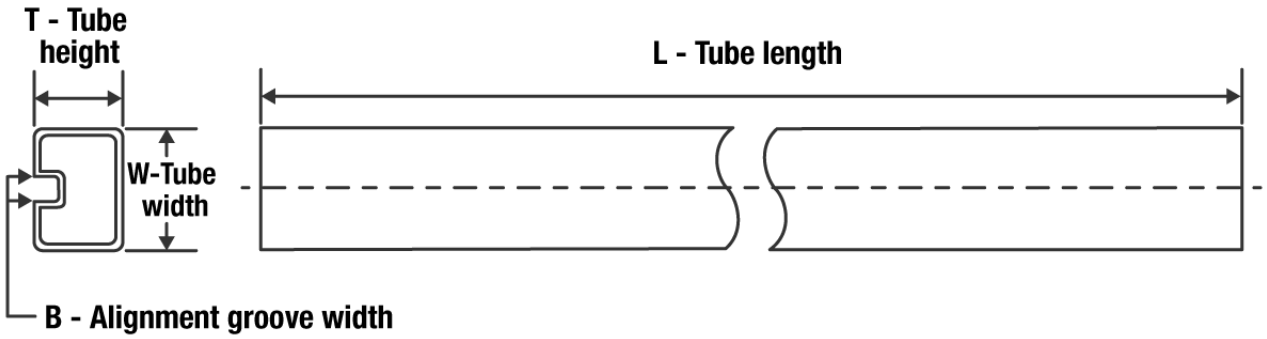
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

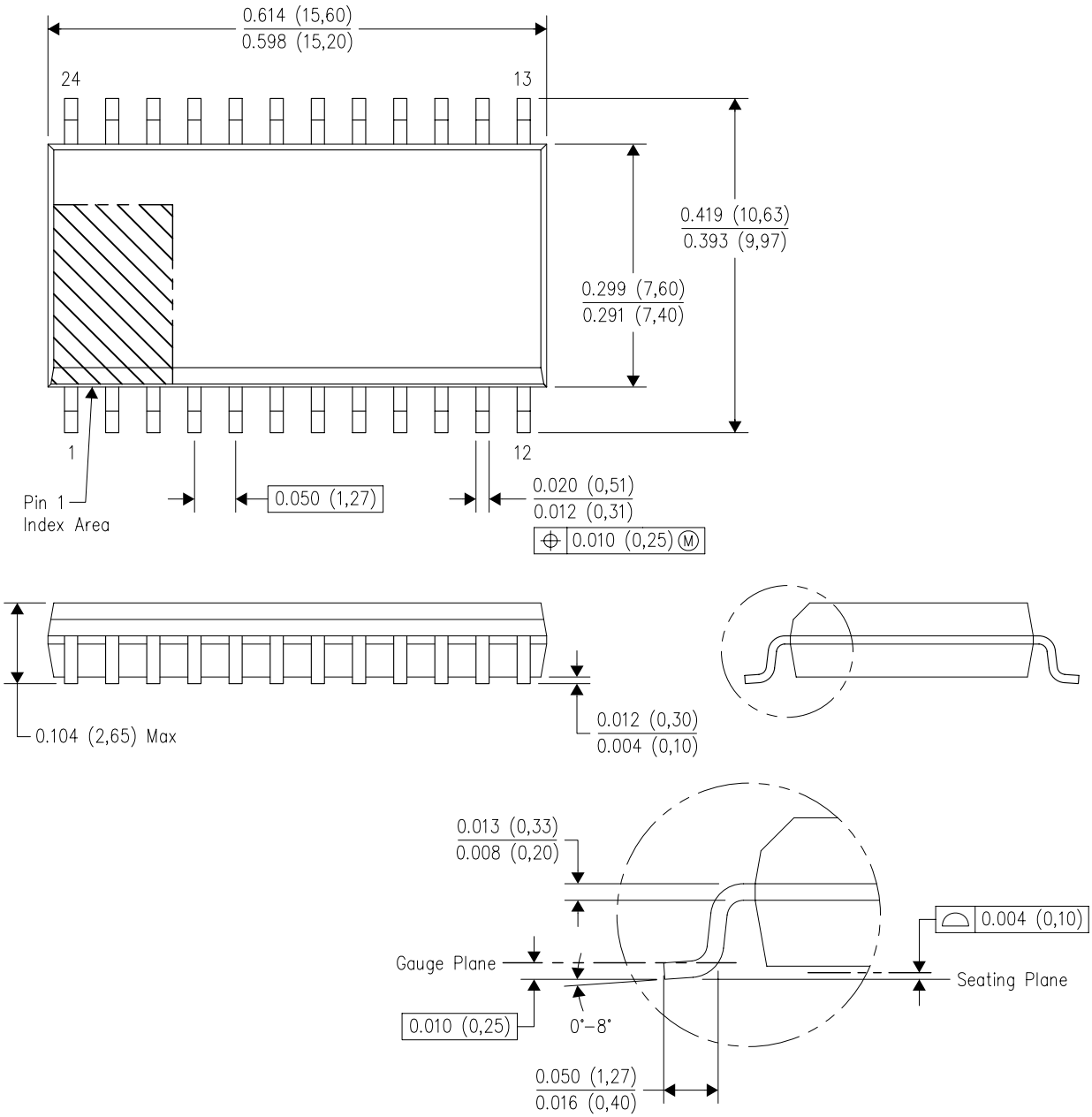
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN10KHT5574DW	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated