ZL30166
Triple Clock Translator
Product Brief

October 2014

Features

- Three programmable digital PLLs/Numerically Controlled Oscillators (NCOs)
- Synchronize to any clock rate from 1 KHz to 750 MHz
- Four programmable synthesizers generate any clock rate from 1 Hz to 750 MHz with low jitter for 10G PHYs
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Digital PLLs filter jitter from 5.2 Hz up to 1 kHz
- Automatic hitless reference switching and digital holdover on reference fail
- Eight input references configurable as single ended or differential
- Any input reference can be fed with sync (frame pulse) or clock
- Programmable DPLLs can synchronize to sync pulse and sync pulse/clock pair

Ordering Information

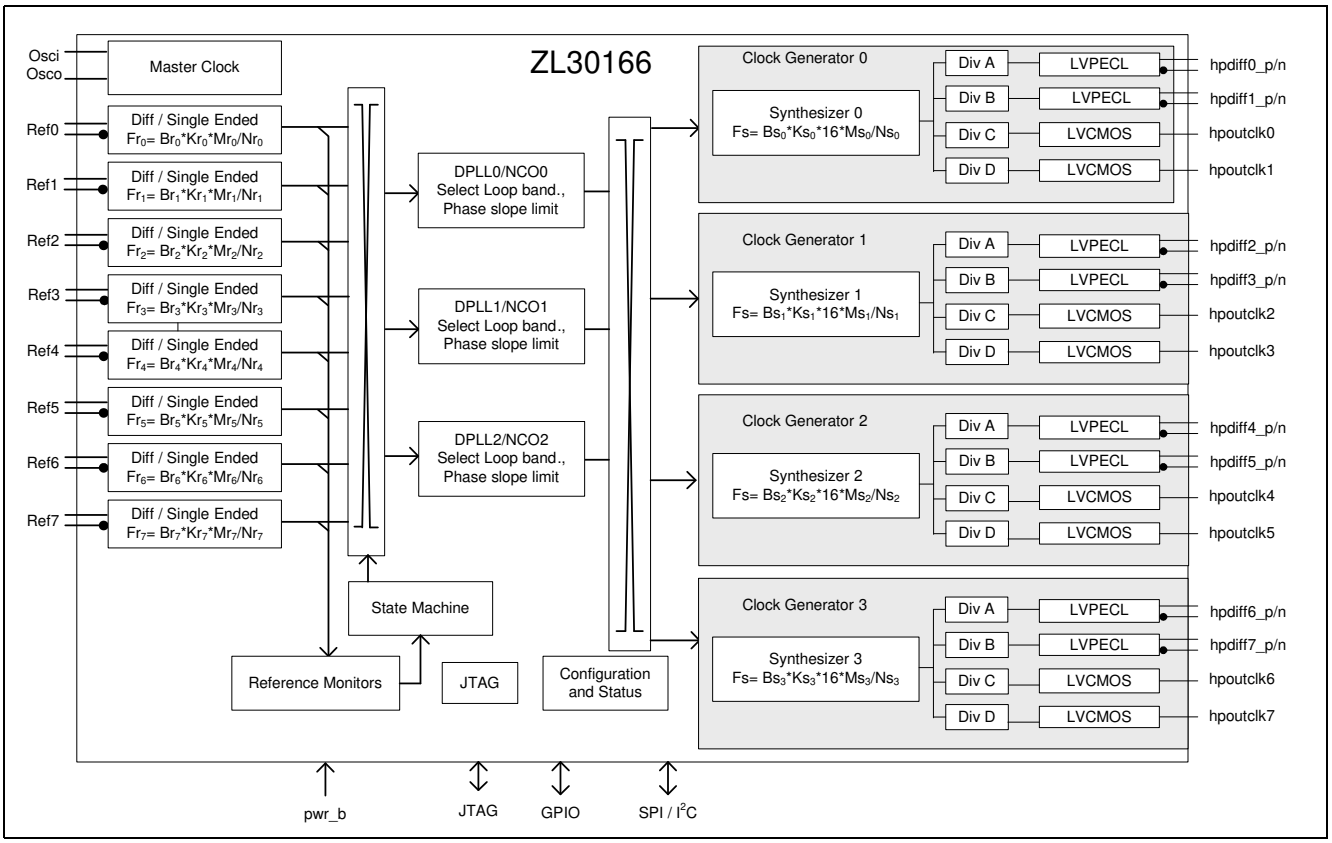
ZL30166GDG2 144 Pin LBGA Trays

Pb Free Tin/Silver/Copper
-40°C to +85°C
Package Size: 13 x 13 mm

- Eight LVPECL outputs and eight LVCMOS outputs
- Operates from a single crystal resonator or clock oscillator
- Field programmable via SPI/I^2C interface

Applications

- OTN muxponders and transponders
- 10 Gigabit line cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
- SONET/SDH, Fibre Channel, XAUI



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