GiGa

an Intel company

140/155 Mbit/s CMI Shaper and Equaliser for E4/STM-1/OC-3 GD16360

Preliminary

General Description

The GD16360 is a dual transceiver for transmitting and receiving CMI–signals, according to the ITU-T G.703 standard. Basically the chip is used as an interface between the internal system signals and the outside world.

The internal system signals are CMI coded, though distorted and attenuated. The outside world signals should fully meet ITU-T G.703.
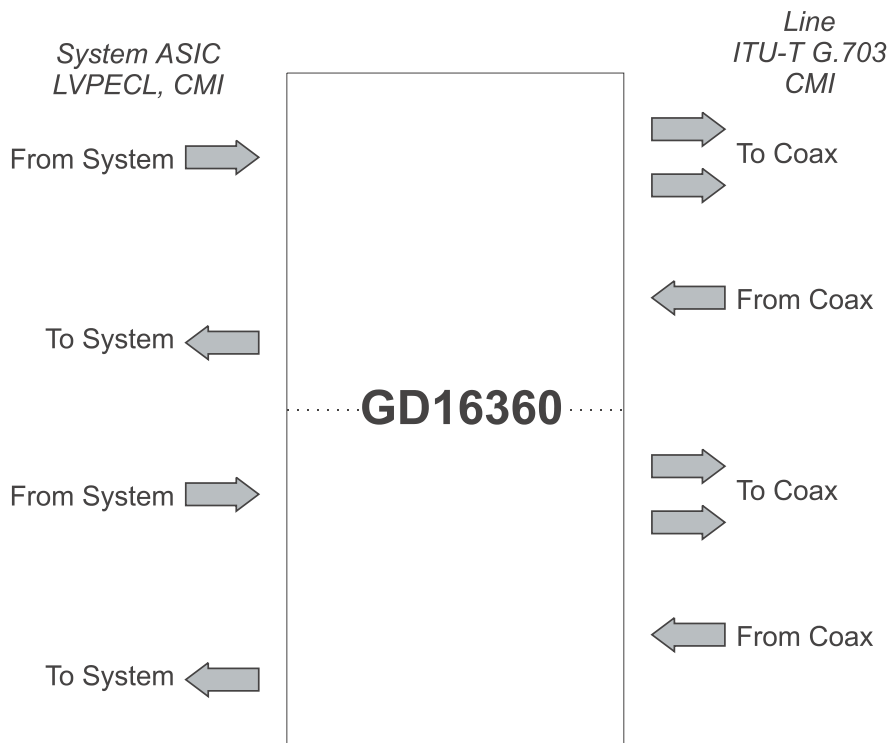
On the receive side the GD16360 receives an attenuated signal after passing through a 75 Ω coax cable with a 12.7 dB attenuation at 78 MHz.

This signal is fed into an equalizer circuit, which compensates for the frequency dependant attenuation and reshapes the signal levels into digital, differential LVPECL levels.

The transmit path receives a distorted signal usually improperly terminated and with high reflections. This signal is originally a differential LVPECL signal from the system ASIC.
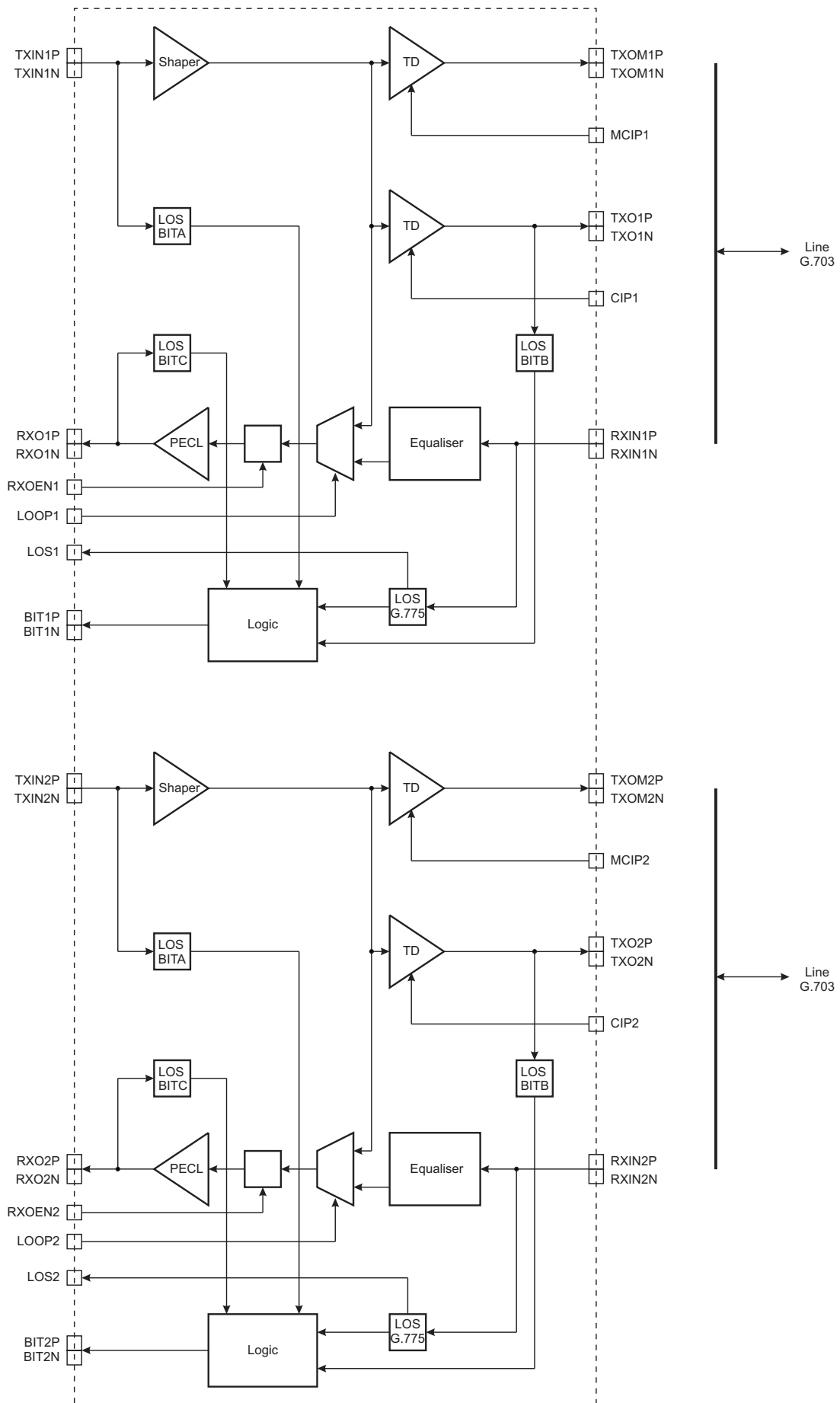
Features

- Fully dual transmit/receive IC for E4/STM-1/OC-3 operations.

- Meet G.703 for 140 and 155 Mbit/s CMI interface:
  - Return loss
  - Receive sensitivity
  - Transmit power

- Meet G.775 for LOS detection.

- 3.3 V LVPECL High speed I/O's.

- CMOS configuration signals.

- Power consumption: 500 mW <target>.

- Supply voltage: 3.3 V (5 V for external cabledriver connection.)

- Package: 48 pin TQFP (7×7×1.4 mm).

- Designed for low cost and volume production.

Applications

- STM-1 or E4 CMI electrical line interfaces

System ASIC LVPECL, CMI

From System →

To System ←

GD16360

From System →

To System ←

Line ITU-T G.703 CMI

→ To Coax

← From Coax

→ To Coax

← From Coax

Block Diagram

Functional Details

Functionally the GD16360 consists of two identical blocks, each containing:
- A transmit channel
- A receive channel

Transmit Channel

Each transmit channel comprises:
- One differential LVPECL signal input (shaper)
- Two cable drivers, providing G.703 interface signals.

The cable drivers can be adjusted individually, allowing optimum performance, with minimum power consumption.

The shaper takes the distorted LVPECL CMI signals and restores them to a near square waveform internally. This signal is sent out through the cable drivers. Both of which are differential open collector outputs. Both cable drivers are adjustable by use of a current control pin (current mirroring).

Receive Channel

Each receive channel comprises:
- A cable equaliser and a LOS (ITU-T G.775 compliant Loss Of Signal detector)
- A selector and an LVPECL output buffer.

The Equaliser takes the differential analogue input signals, which have been √f-attenuated through the coax, equalises the signal, and send it to a selector. From the selector the signal goes to the output LVPECL buffer. This buffer drives the signal outputs from circuit intended for interconnection to the system ASIC.

The LOS function monitors the input signal amplitude and generates a signal according to ITU-T G.775.

Loopback Mode

The selector can be used to take the signal from the transmit channel and send it out through RXOxx to the system ASIC by setting the LOOPx high.

Build in Test

The build in test is a monitoring circuit, which looks at the two input signals as well as both output signals.

For the input signals for the receiver the detection is determined by the use of the ITU-T G.775 LOS function.

For the remaining three I/O signals (BITA/B/C), the criteria for signal detection is set by the presence of transitions. If there are no transitions for more than 100 bit periods this signal will go high internally. Otherwise it will stay low.

The determination of the output open collector signal BITxP/N, will be generated according to the logic table below.

BITA/B/C/G.775		
	Receive Channel	
	CMI Digital Output	CMI Analog Input
OK	Signal ON	Signal ON
FAIL	Signal ON	NO Signal
FAIL	NO Signal	Signal ON
OK	NO Signal	NO Signal
	Transmit Channel	
	CMI Analog Output	CMI Digital Input
OK	Signal ON	Signal ON
FAIL	Signal ON	NO Signal
FAIL	NO Signal	Signal ON
OK	NO Signal	NO Signal

Hence if there is one or more FAIL conditions, then the overall (-external BITxP/N monitoring signals) will be low (voltage).

The internal signals BITA, BITB, BITC, G.775 are OR'ed together.

Pin List

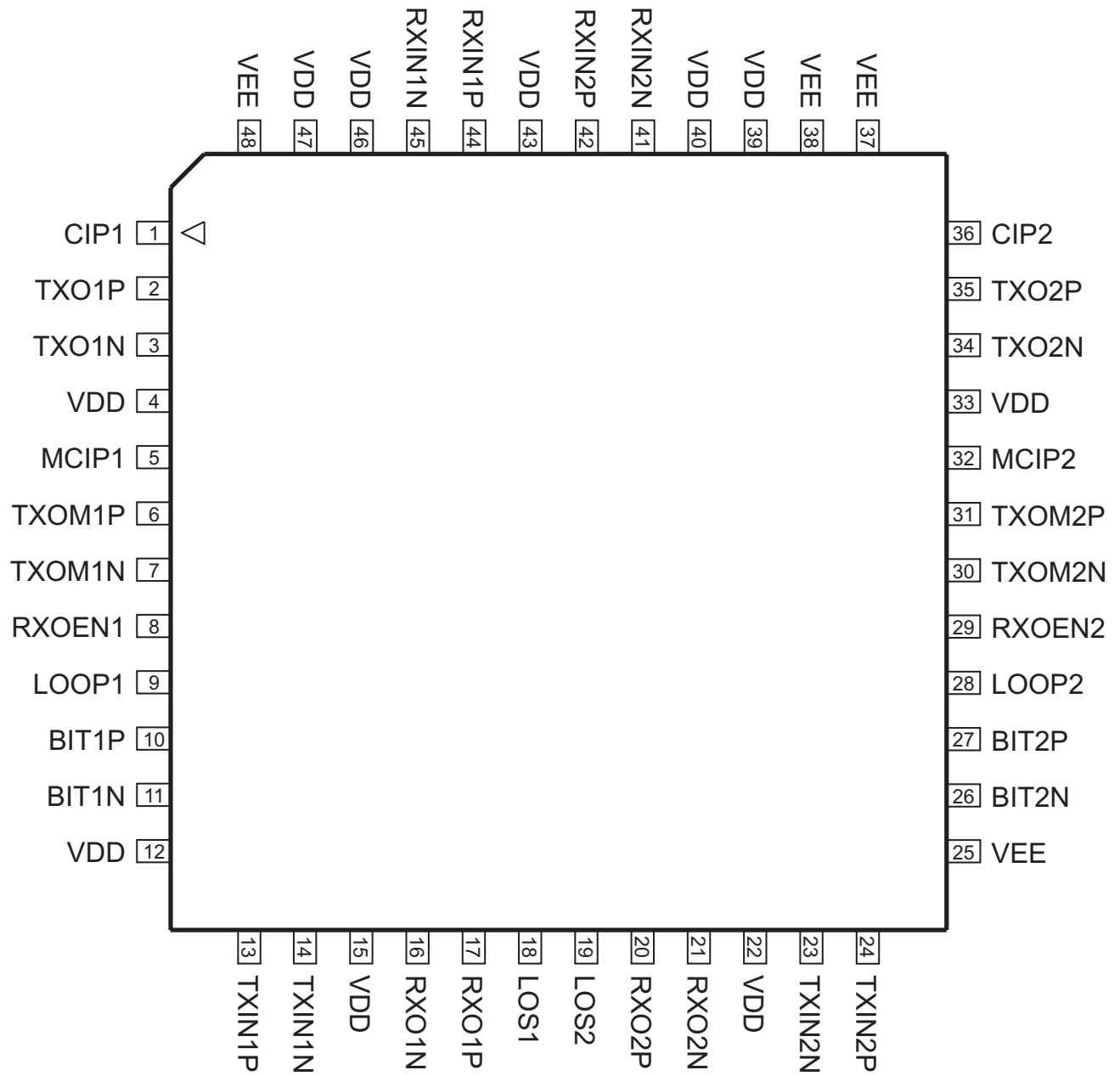| Mnemonic:	Pin Number:	Pin Type:	Description:
TXIN1P, TXIN1N	13, 14	LVPECL-IN	Distorted, LVPECL signal input, 100 - 1000 mV$_{PP}$
TXIN2P, TXIN2N	24, 23	LVPECL-IN	Distorted, LVPECL signal input, 100 – 1000 mV$_{PP}$
TXO1P, TXO1N	2, 3	ANL-OUT	ITU-T G.703 interface, open collector output 26.7 mA nominally
TXO2P, TXO2N	35, 34	ANL-OUT	ITU-T G.703 interface, open collector output 26.7 mA nominally
TXOM1P, TXOM1N	6, 7	ANL-OUT	ITU-T G.703 interface, open collector output 26.7 mA nominally. Monitor cable driver.
TXOM2P, TXOM2N	31, 30	ANL-OUT	ITU-T G.703 interface, open collector output 26.7 mA nominally. Monitor cable driver.
CIP1, CIP2	1, 36	ANL	CML open collector current control input. Connect resistor TBD Ω to VDD + 1.7 V.
MCIP1, MCIP2	5, 32	ANL	CML open collector current control input for Monitor cabledrivers. Connect resistor TBD Ω to VDD + 1.7 V
RXIN1P, RXIN1N	44, 45	ANL-IN	ITU-T G.703 input. $\sqrt{f}$ - Attenuated from coax.
RXIN2P, RXIN2N	42, 41	ANL-IN	ITU-T G.703 input. $\sqrt{f}$ - Attenuated from coax.
RXO1P, RXO1N	17, 16	LVPECL-OUT	LVPECL output to system ASIC.
RXO2P, RXO2N	20, 21	LVPECL-OUT	LVPECL output to system ASIC.
RXOEN1	8	CMOS-IN	When LOW, RXO1P is forced LOW.
RXOEN2	29	CMOS-IN	When LOW, RXO2P is forced LOW.
LOS1	18	CMOS-OUT	ITU-T G.775 LOS detected from RXIN1P/N input. When LOS flagged, output is LOW.
LOS2	19	CMOS-OUT	ITU-T G.775 LOS detected from RXIN2P/N input. When LOS flagged, output is LOW.
LOOP1	9	CMOS-IN	Loop-back selector. When HIGH loop-back in transceiver 1 is enabled.
LOOP2	28	CMOS-IN	Loop-back selector. When HIGH loop-back in transceiver 2 is enabled.
BIT1P, BIT1N	10, 11	OPEN-COLLECTOR	Build in test for transceiver 1. Determines status of GD16360 and I/O signals determined from logic table above. If one or more fails the positive output is low (voltage).
BIT2P, BIT2N	27, 26	OPEN-COLLECTOR	Build in test for transceiver 2. Determines status of GD16360 and I/O signals determined from logic table above. If one or more fails the positive output is low (voltage).
VDD	4, 12, 15, 22, 33	PWR	Positive power supply 3.3 V for transceiver 1.
VDD	39, 40, 43, 46, 47	PWR	Positive power supply 3.3 V for transceiver 2.
VEE	25, 37	PWR	0 V power, GND.
VEE	38, 48	PWR	0 V power, GND.
Heat sink			Connected to VEE.

Package Pinout

Figure 1. *Package 48 pin, Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages are referenced to VEE unless otherwise noted.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{DD}	Supply Voltage		0		5	V
$V_{O\ max}$	Output Voltage	LVPECL/CMOS	-0.5		V_{DD} + 0.5	V
$I_{O,PECL\ max}$	Output Current	LVPECL			40	mA
$I_{O,CMOS\ max}$	Output Current	CMOS	-10		10	mA
$V_{I\ max}$	Input Voltage	LVPECL/CMOS	-0.5		V_{DD} + 0.5	V
$I_{I\ max}$	Input Current	LVPECL/CMOS	-1.0		1.0	mA
T_O	Operating Temperature	Junction	-55		+150	°C
T_s	Storage Temperature	Junction	-65		+175	°C
V_{ESD}	ESD Voltage	Note 1	500			V
FIT				TBD		

Note 1: Human body model (100 pF, 1500 Ω) MIL 883 std.

Thermal Characteristics

$T_{AMBIENT}$ = -5 °C to 85 °C.
Thermal resistance θ_{J-C} = TBD
Thermal resistance θ_{J-A} = TBD

Note: Heat sink will be used, see package outline.

DC Characteristics

All voltages in table are referred to VEE unless otherwise noted.
All input signal and power currents in the table are defined positive into the pin.
All output signal currents are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{DD}	Supply Voltage		3.15	3.30	3.45	V
I_{DD}	Supply Current	Note 3			TBD	mA
$V_{IC,LVPECL}$	LVPECL Input Common Mode Voltage	Shaper Input	V_{DD}-1.5		V_{DD}-1.1	V
$V_{IDIFF,LVPECL}$	LVPECL Differential Input Voltage	Shaper Input, Note 2	0.100		1.000	V
$I_{IH,LVPECL}$	LVPECL Input HI Current	V_{IH} LVPECL, max			100	µA
$I_{IL,LVPECL}$	LVPECL Input LO Current	V_{IL} LVPECL, min	-100			µA
$V_{OH,LVPECL}$	LVPECL Output HI Voltage	Note 1	V_{DD}-1.1		V_{DD}-0.70	V
$V_{OL,LVPECL}$	LVPECL Output LO Voltage	Note 1	V_{DD}-2.00		V_{DD}-1.62	V
$V_{ODIFF,LVPECL}$	LVPECL Output Differential Voltage	Note 1	600		1300	mV
$V_{IH,CMOS}$	CMOS Input HI Voltage		V_{DD}x0.8		V_{DD}	V
$V_{IL,CMOS}$	CMOS Input LO Voltage		0		V_{DD}x0.2	V
$I_{IH,CMOS}$	CMOS Input HI Current	V_{IH} CMOS, max			100	µA
$I_{IL,CMOS}$	CMOS Input LO Current	V_{IL} CMOS, min	-100			µA
$V_{OH,CMOS}$	CMOS Output HI Voltage	I_{OH} = 1mA	V_{DD}- 0.1		V_{DD}	V
$V_{OL,CMOS}$	CMOS Output LO Voltage	I_{OL} = -1mA	0		0.1	V

Note 1:   50 Ω termination to V_{DD}-2.0 V.
Note 2:   Although $V_{IDIFF,PECL}$ may vary within $V_{IH,MAX}$ and $V_{IL,MIN}$, it must not exceed $V_{IDIFF,MAX}$.

Analog Characteristics

All specifications according to the CMI ITU-T interface are to be kept according to this standard.
The 'shaper' block is to be considered as a LVPECL input, with an external biasing according to note 1 above.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
$OVLD_{IN}$	Input Overload	G.703 interface	1000			mV_{PP}
$SENS_{IN}$	Input Sensitivity	G.703 interface			-15	dB
RL_{IN}	Input Return Loss	Note 1			-17	dB
RL_{OUT}	Output Return Loss	Note 1			-17	dB
$V_{OH\ G.703}$	G.703 Output Voltage HI	Note 2	0.45		0.55	V
$V_{OL\ G.703}$	G.703 Output Voltage LO	Note 2	-0.55		-0.45	V

Note 1:   G.703 interface open collector type. Actual value depends on discrete external circuitry.
Note 2:   Measured in 75 Ω load via AC- or pulse transformer coupling

AC Characteristics

All voltages in table are referred to VEE unless otherwise noted.
All input signal and power currents in the table are defined positive into the pin.
All output signal currents are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
T_{R-PECL}	PECL Rise Time	Note 1			800	ps
T_{F-PECL}	PECL Fall Time	Note 1			800	ps
T_{R-CMOS}	CMOS Rise Time	Note 2			4	ns
T_{F-CMOS}	CMOS Fall Time	Note 2			4	ns

Note 1: 20 - 80 %, 50 Ω to V_{DD} - 2.0 V.
Note 2: 20 - 80 %, 10 pF and 100 μA load.
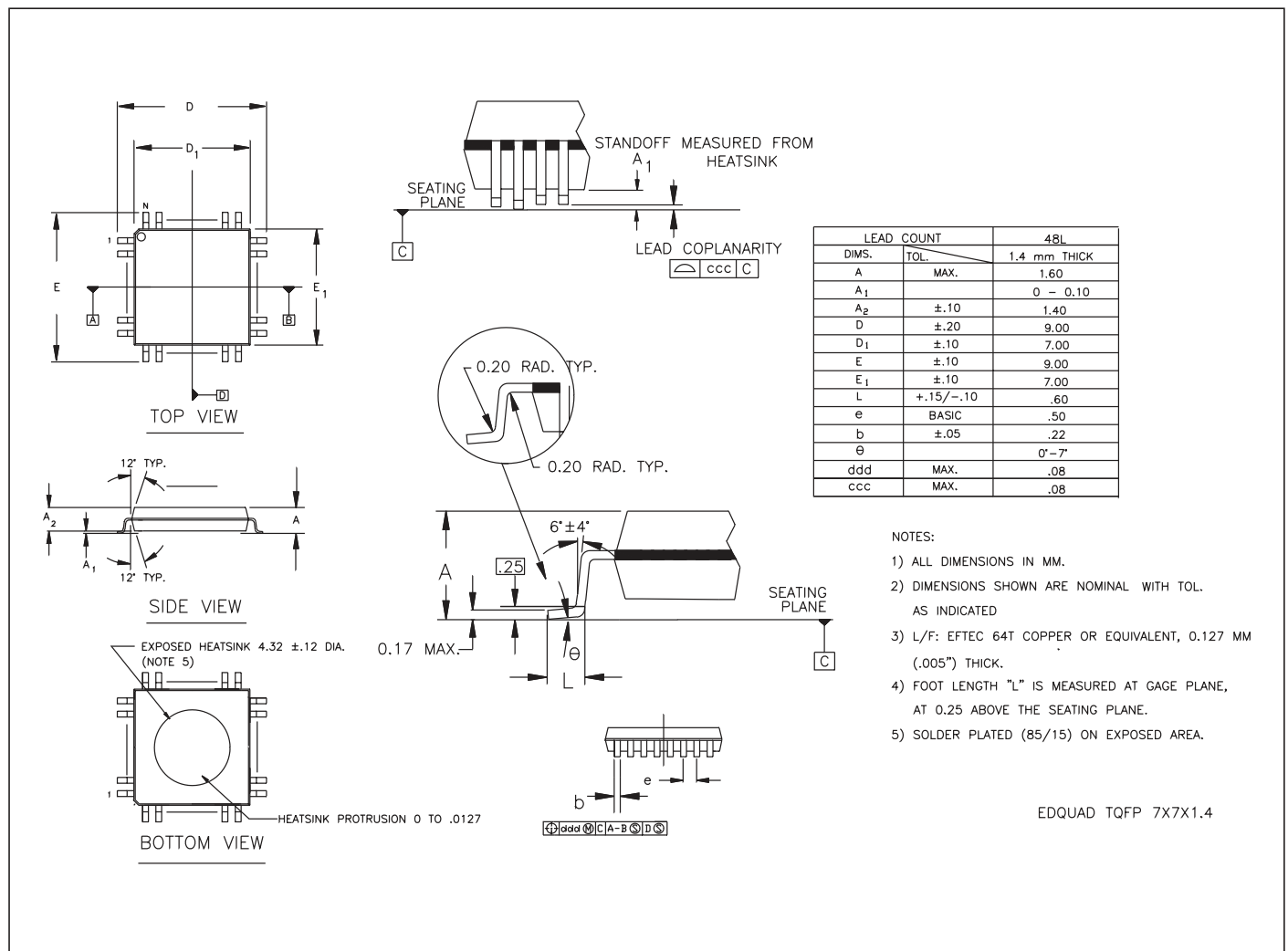
Package Outline

Figure 2. *Package 48 pin TQFP, EDQUAD*

Device Marking

Figure 3. *Device Marking, Top View*

External References

ITU-T G.703 (04/91): General Aspects of Digital transmissionsystems, terminal equipments.
ITU-T G.775 (11/94): LOS and AIS defect detection criteria.

Ordering Information

To order, please specify as shown below:

Product Name:	Intel Order number:	Package Type:	Ambient Temperature Range:
GD16360-48BA	**FAGD1636048BA** MM#: 836046	48 Lead TQFP, EDQUAD	-5..85 °C

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GD16360, Data Sheet Rev.: 6 - Date: 24 July 2001

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