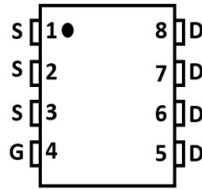
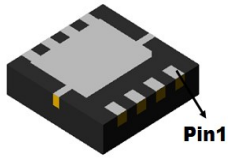
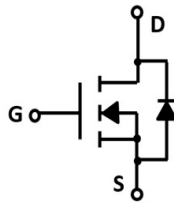


## N-Channel Enhancement Mode Field Effect Transistor



DFN3.3X3.3



### Product Summary

- $V_{DS}$  100V
- $I_D$  40A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ ) < 18.5 mohm
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ ) < 22.5 mohm
- 100% UIS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

### Applications

- Consumer electronic power supply
- Motor control
- Synchronous-rectification
- Isolated DC/DC convertor
- Invertors

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	100	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_c=25^\circ C$	$I_D$	40	A
	$T_c=100^\circ C$		25.3	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	160	A
Avalanche energy <sup>B</sup>		$E_{AS}$	81	mJ
Total Power Dissipation <sup>C</sup>	$T_c=25^\circ C$	$P_D$	43	W
	$T_c=100^\circ C$		17.2	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ C$

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	$t \leq 10S$	$R_{\theta JA}$	20	25	$^\circ C/W$
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State		45	55	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	2.4	2.9	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ40G10A	F1	Q40G10A	5000	10000	100000	13" reel



# YJQ40G10A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	100			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		15	18.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		18	22.5	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V			1.3	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				40	A
Gate resistance	R <sub>G</sub>	f=1MHz, Open drain		1		Ω
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, f=1MHZ		1051		pF
Output Capacitance	C <sub>oss</sub>			399		
Reverse Transfer Capacitance	C <sub>rss</sub>			18		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =25A		16		nC
Gate-Source Charge	Q <sub>gs</sub>			5.6		
Gate-Drain Charge	Q <sub>gd</sub>			2.4		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=100A/us		42		ns
Reverse Recovery Time	t <sub>rr</sub>			39.8		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =50V, I <sub>DS</sub> =25A R <sub>GEN</sub> =2.2Ω		39.2		ns
Turn-on Rise Time	t <sub>r</sub>			11		
Turn-off Delay Time	t <sub>D(off)</sub>			53.2		
Turn-off fall Time	t <sub>f</sub>			15.8		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V<sub>DD</sub>=50V, R<sub>G</sub>=25Ω, L=0.5mH.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R<sub>θJA</sub> is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25° C. The Power dissipation PDSM is based on R<sub>θJA</sub> ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.



# YJQ40G10A

## ■ Typical Performance Characteristics

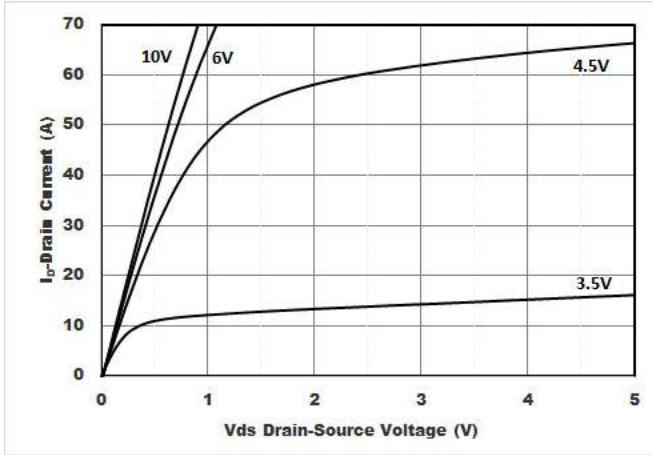


Figure1. Output Characteristics

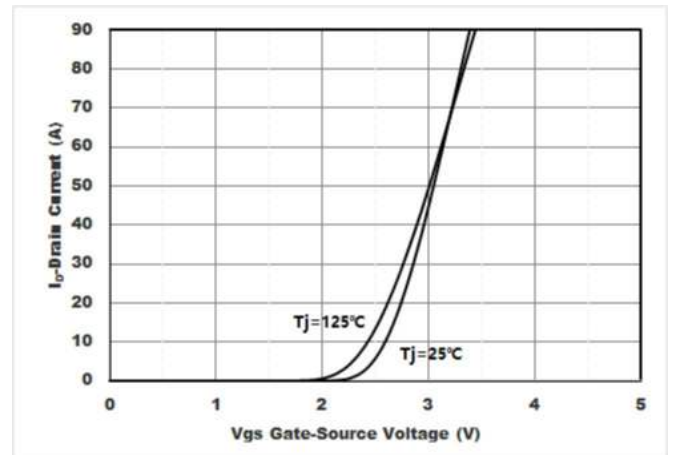


Figure2. Transfer Characteristics

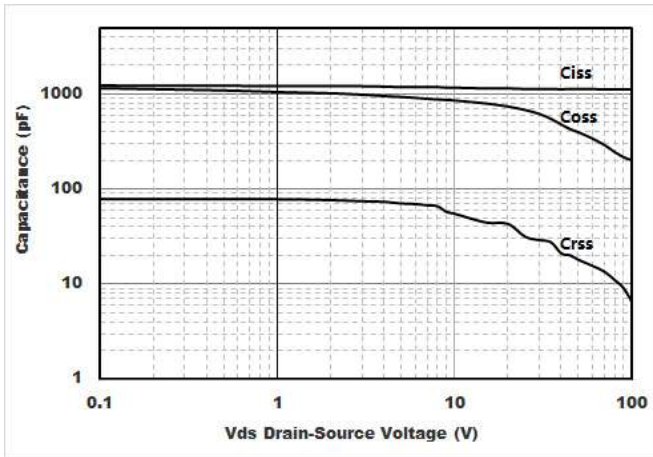


Figure3. Capacitance Characteristics

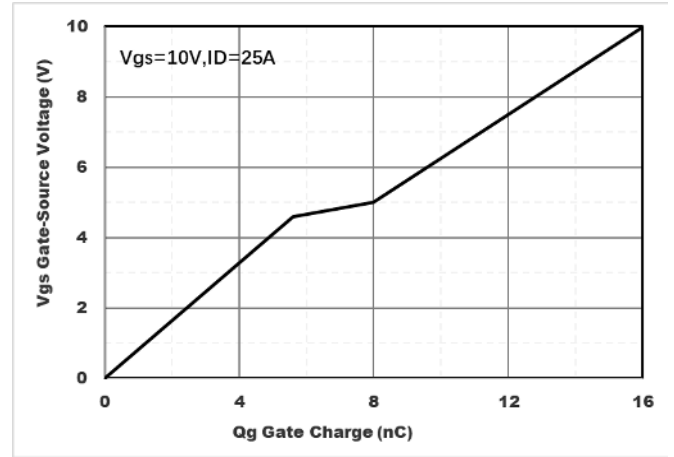


Figure4. Gate Charge

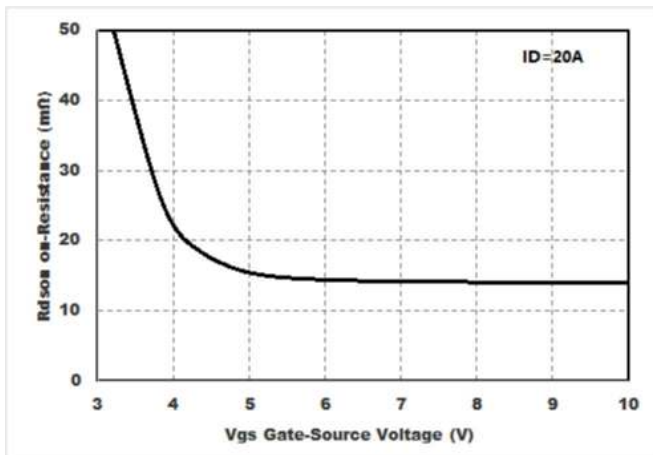


Figure5. : On-Resistance vs. Gate to Source Voltage

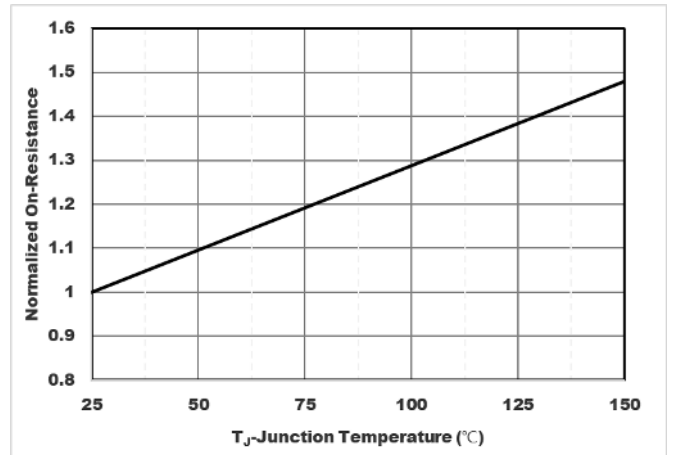


Figure6. Normalized On-Resistance



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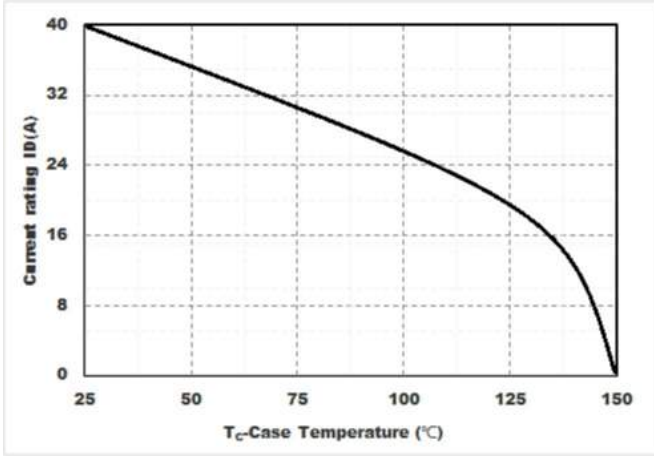


Figure7. Drain current

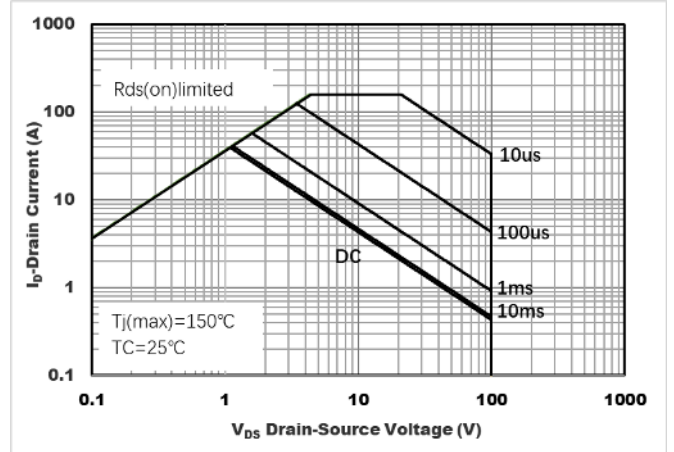


Figure8.Safe Operation Area

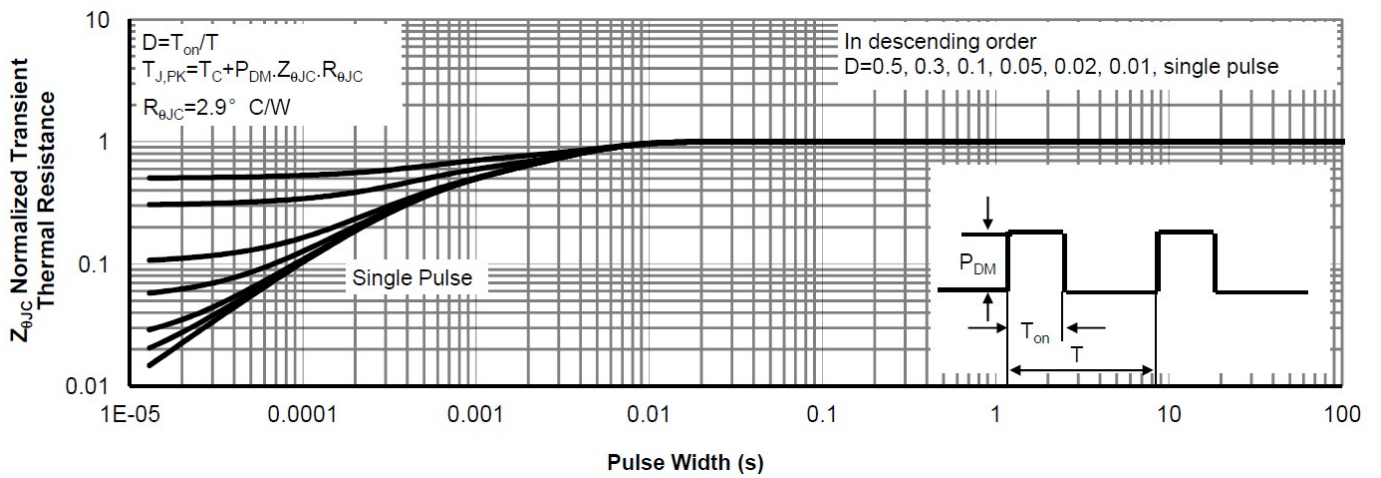
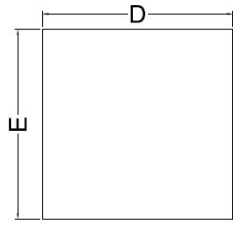


Figure9.Normalized Maximum Transient thermal impedance

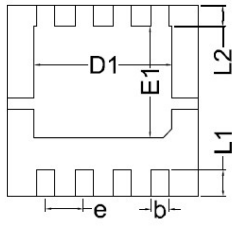


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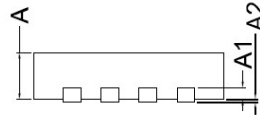
## ■ DFN3.3x3.3 Package information



Top View  
正面视图

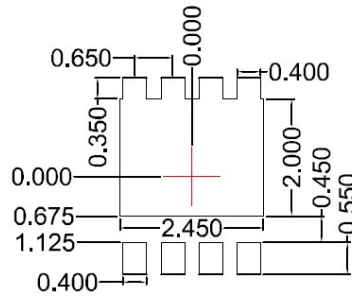


Bottom View  
背面视图



Side View  
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout  
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10\text{mm}$ .
3. The pad layout is for reference purposes only.



# YJQ40G10A

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