

1. General description

High voltage, high speed, planar passivated NPN power switching transistor with integrated anti-parallel E-C diode in a SOT428 (DPAK) surface mountable plastic package.

2. Features and benefits

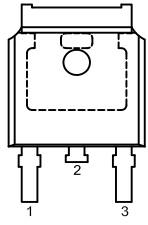
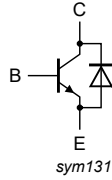
- Fast switching
- High voltage capability
- Integrated anti-parallel E-C diode
- Surface mountable plastic package
- Very low switching and conduction losses

3. Applications

- DC-to-DC converters
- Electronic lighting ballasts
- Inverters
- Motor control systems

4. Pinning information

Table 1. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base	 <p>DPAK (SOT428)</p>	 <p>sym131</p>
2	C	collector ^[1]		
3	E	emitter		

[1] It is not possible to make a connection to pin 2 of the SOT428 (DPAK) package.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BUJD105AD	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

6. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0\text{ V}$	-	700	V
V_{CBO}	collector-base voltage	$I_E = 0\text{ A}$	-	700	V
V_{CEO}	collector-emitter voltage	$I_B = 0\text{ A}$	-	400	V
I_C	collector current	DC; Fig. 1; Fig. 2	-	8	A
I_{CM}	peak collector current	Fig. 1; Fig. 2	-	16	A
I_B	base current	DC	-	4	A
I_{BM}	peak base current		-	8	A
P_{tot}	total power dissipation	$T_{mb} \leq 25\text{ °C}$; Fig. 3	-	80	W
T_{stg}	storage temperature		-65	150	°C
T_j	junction temperature		-	150	°C

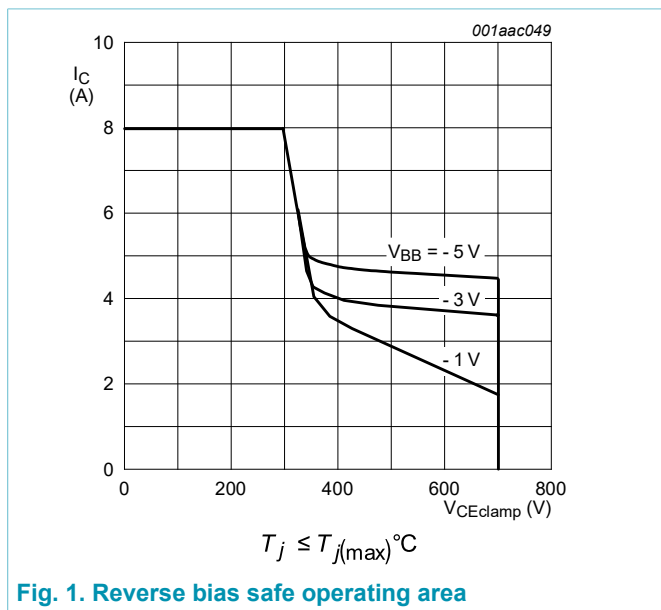


Fig. 1. Reverse bias safe operating area

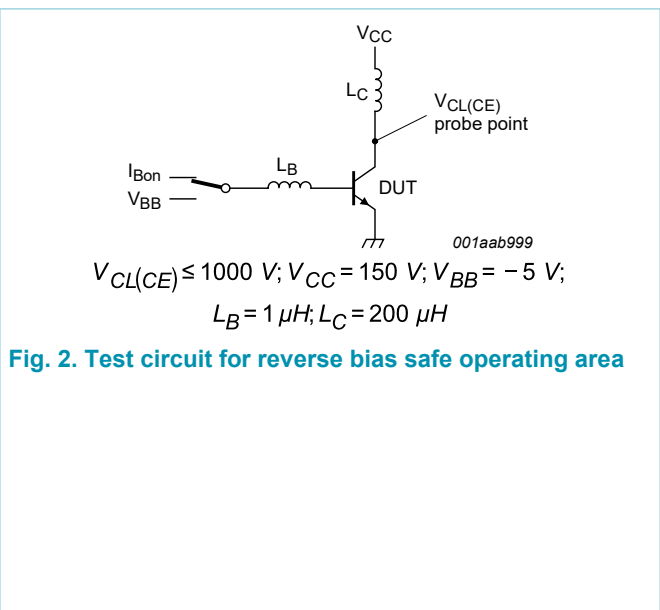
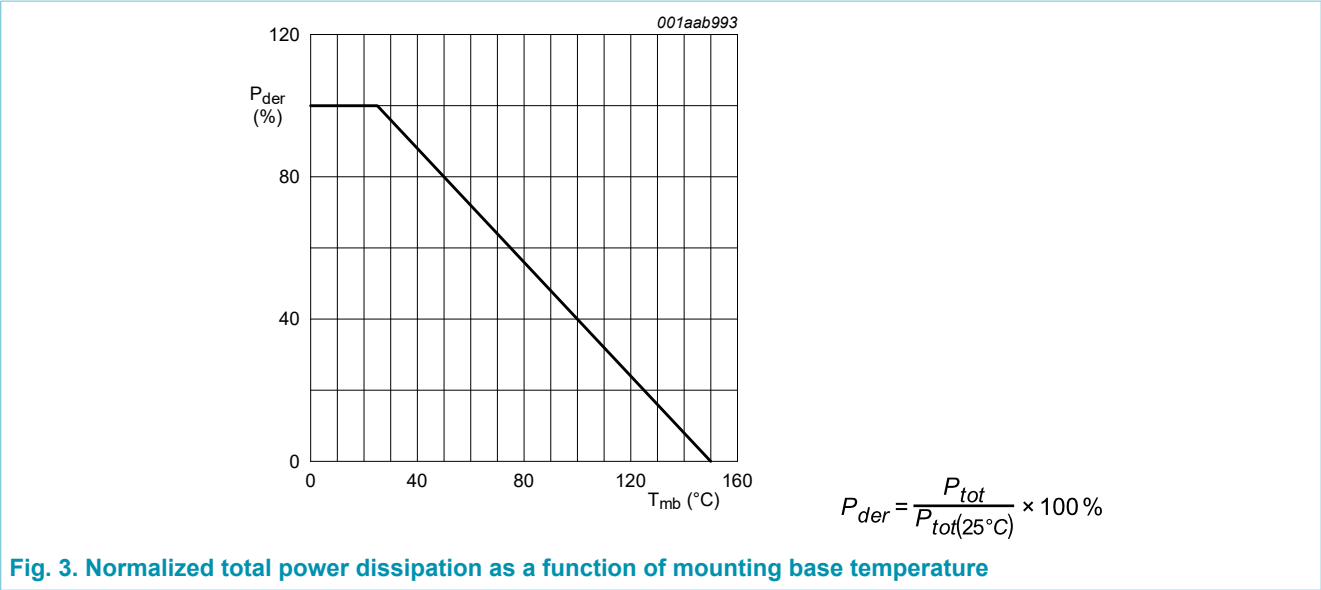


Fig. 2. Test circuit for reverse bias safe operating area



7. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	-	1.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board (FR4) mounted; minimum footprint; Fig. 5	-	75	-	K/W

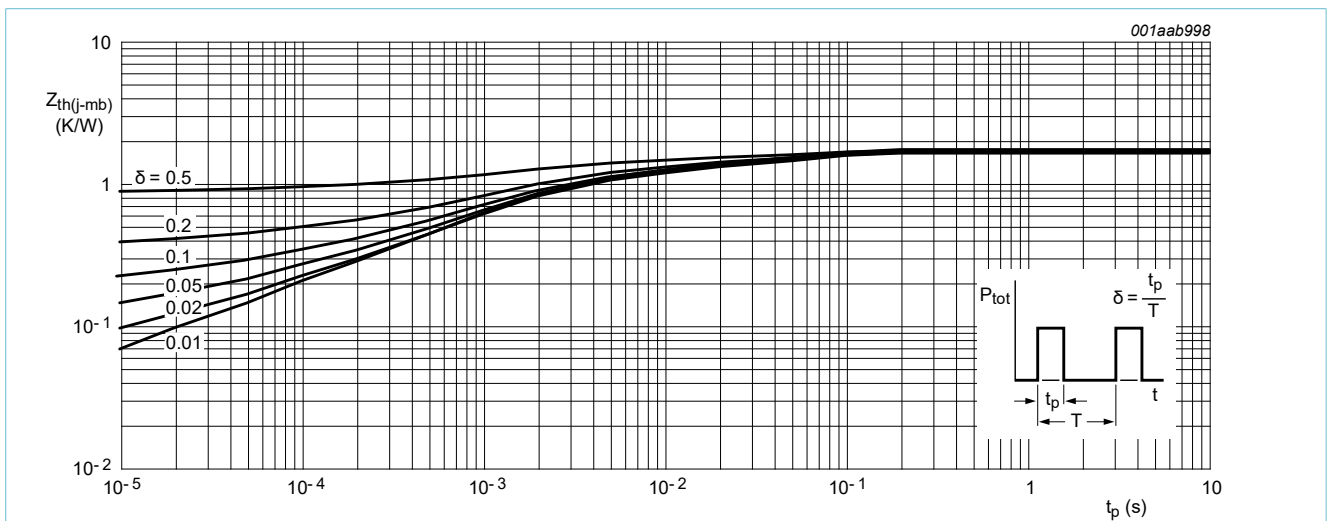


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse width

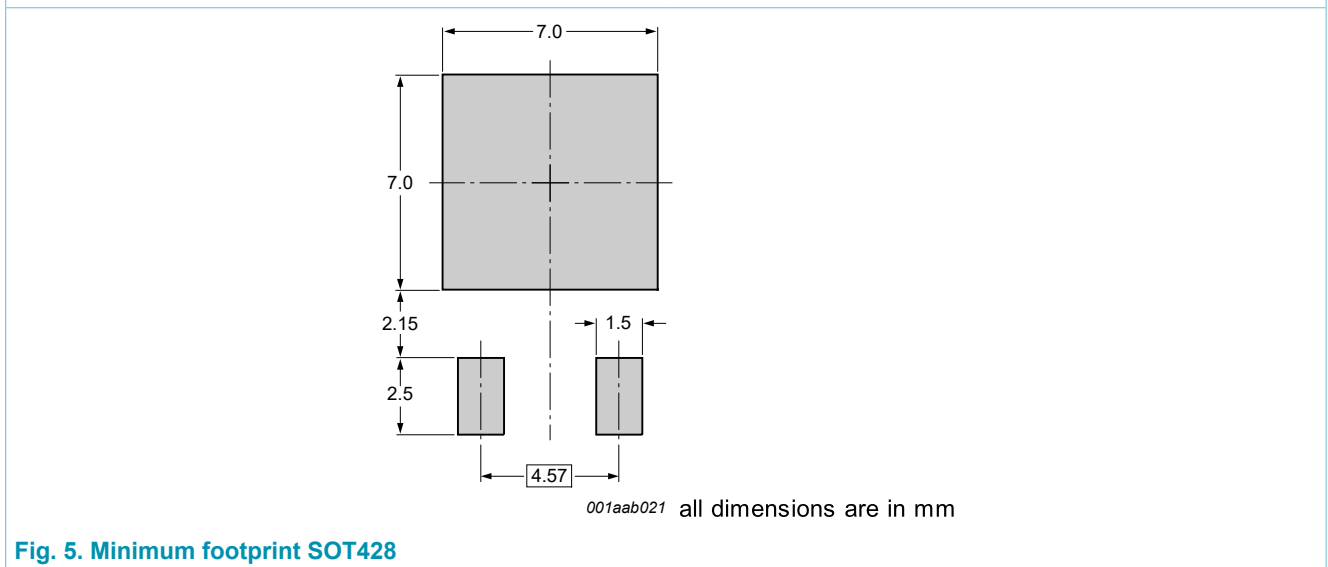


Fig. 5. Minimum footprint SOT428

8. Characteristics

Table 5. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit		
Static characteristics								
I_{CES}	collector-emitter cut-off current (base shorted)	$V_{BE} = 0\text{ V}; V_{CE} = 700\text{ V}; T_j = 25\text{ }^\circ\text{C}$	[1]	-	-	0.2	mA	
		$V_{BE} = 0\text{ V}; V_{CE} = 700\text{ V}; T_j = 125\text{ }^\circ\text{C}$	[1]	-	-	0.5	mA	
I_{CBO}	collector-base cut-off current (emitter open)	$V_{CB} = 700\text{ V}; I_E = 0\text{ A}$	[1]	-	-	0.2	mA	
I_{CEO}	collector-emitter cut-off current (base open)	$V_{CE} = 400\text{ V}; I_B = 0\text{ A}$	[1]	-	-	0.1	mA	
I_{EBO}	emitter-base cut-off current (collector open)	$V_{EB} = 9\text{ V}; I_C = 0\text{ A}$		-	-	10	mA	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 4\text{ A}; I_B = 0.8\text{ A};$ Fig. 6 ; Fig. 7		-	0.35	1	V	
V_{BEsat}	base-emitter saturation voltage	$I_C = 4\text{ A}; I_B = 0.8\text{ A};$ Fig. 8		-	1	1.5	V	
V_F	forward voltage	$I_F = 4\text{ A}; T_j = 25\text{ }^\circ\text{C}$		-	1.07	1.5	V	
h_{FE}	DC current gain	$I_C = 4\text{ A}; V_{CE} = 5\text{ V}; T_{mb} = 25\text{ }^\circ\text{C};$ Fig. 9 ; Fig. 10		8	12.5	-		
		$I_C = 1\text{ mA}; V_{CE} = 5\text{ V}; T_{mb} = 25\text{ }^\circ\text{C}$		10	17	34		
		$I_C = 500\text{ mA}; V_{CE} = 5\text{ V}; T_{mb} = 25\text{ }^\circ\text{C}$		13	22	36		
Dynamic characteristics								
t_{on}	turn-on time	$I_C = 5\text{ A}; I_{Bon} = 1\text{ A}; I_{Boff} = -1\text{ A}; R_L = 75\text{ }\Omega; T_j = 25\text{ }^\circ\text{C};$ resistive load; Fig. 11 ; Fig. 12		-	0.65	1	μs	
t_s	storage time		$I_C = 5\text{ A}; I_{Bon} = 1\text{ A}; V_{BB} = -5\text{ V}; L_B = 1\text{ }\mu\text{H}; T_j = 25\text{ }^\circ\text{C};$ inductive load; Fig. 13 ; Fig. 14		-	1.2	1.7	μs
			$I_C = 5\text{ A}; I_{Bon} = 1\text{ A}; V_{BB} = -5\text{ V}; L_B = 1\text{ }\mu\text{H}; T_j = 100\text{ }^\circ\text{C};$ inductive load; Fig. 13 ; Fig. 14		-	1.4	1.9	μs
t_f	fall time	$I_C = 5\text{ A}; I_{Bon} = 1\text{ A}; V_{BB} = -5\text{ V}; L_B = 1\text{ }\mu\text{H}; T_{mb} = 25\text{ }^\circ\text{C};$ inductive load; Fig. 13 ; Fig. 14		-	0.02	0.05	μs	
		$I_C = 5\text{ A}; I_{Bon} = 1\text{ A}; V_{BB} = -5\text{ V}; L_B = 1\text{ }\mu\text{H}; T_{mb} = 100\text{ }^\circ\text{C};$ inductive load; Fig. 13 ; Fig. 14		-	0.025	0.1	μs	
		$I_C = 5\text{ A}; I_{Bon} = 1\text{ A}; I_{Boff} = -1\text{ A}; R_L = 75\text{ }\Omega;$ resistive load; Fig. 11 ; Fig. 12		-	0.3	0.5	μs	

[1] Measured with half-sine wave voltage (curve tracer).

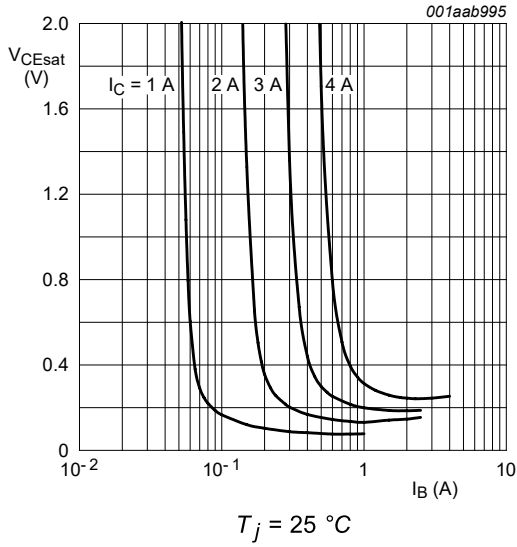


Fig. 6. Collector-emitter saturation voltage as a function of base current; typical values

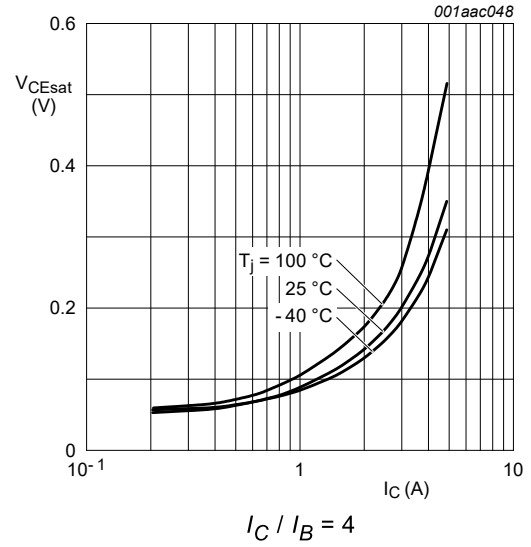


Fig. 7. Collector-emitter saturation voltage as a function of collector current; typical values

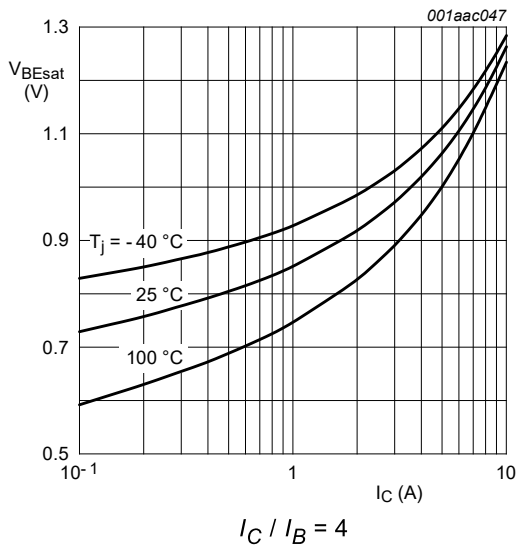


Fig. 8. Base-emitter saturation voltage as a function of collector current; typical values

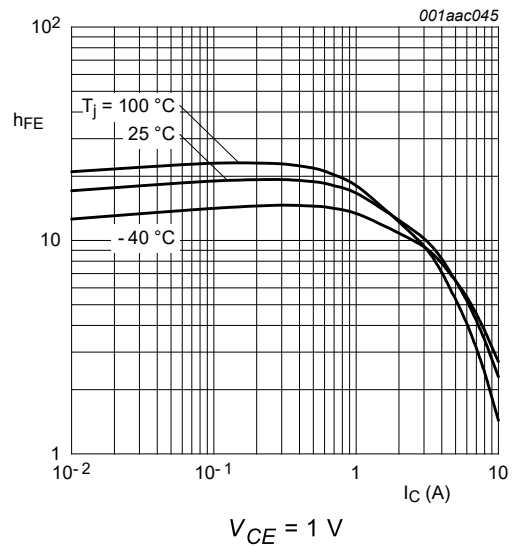


Fig. 9. DC current gain as a function of collector current; typical values

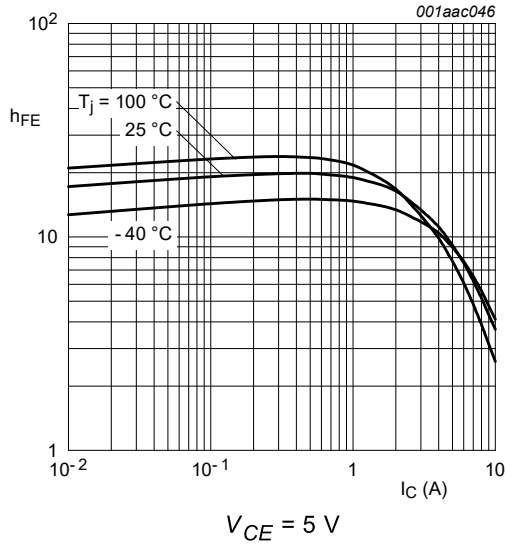
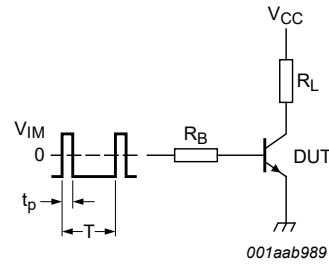


Fig. 10. DC current gain as a function of collector current; typical values



$V_{IM} = -6 \text{ to } +8 \text{ V}; V_{CC} = 250 \text{ V}; t_p = 20 \mu\text{s}; \delta = \frac{t_p}{T} = 0.01$
 R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig. 11. Test circuit for resistive load switching

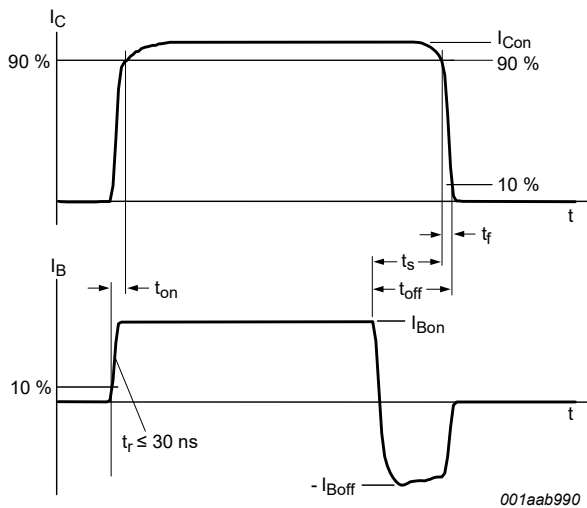
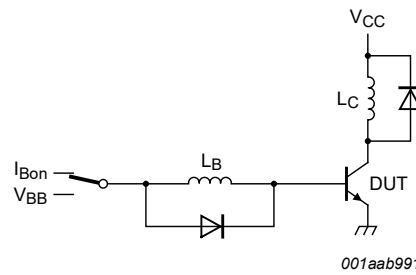


Fig. 12. Switching times waveforms for resistive load



$V_{CC} = 300 \text{ V}; V_{BB} = -5 \text{ V}; L_C = 200 \mu\text{H}; L_B = 1 \mu\text{H}$

Fig. 13. Test circuit for inductive load switching

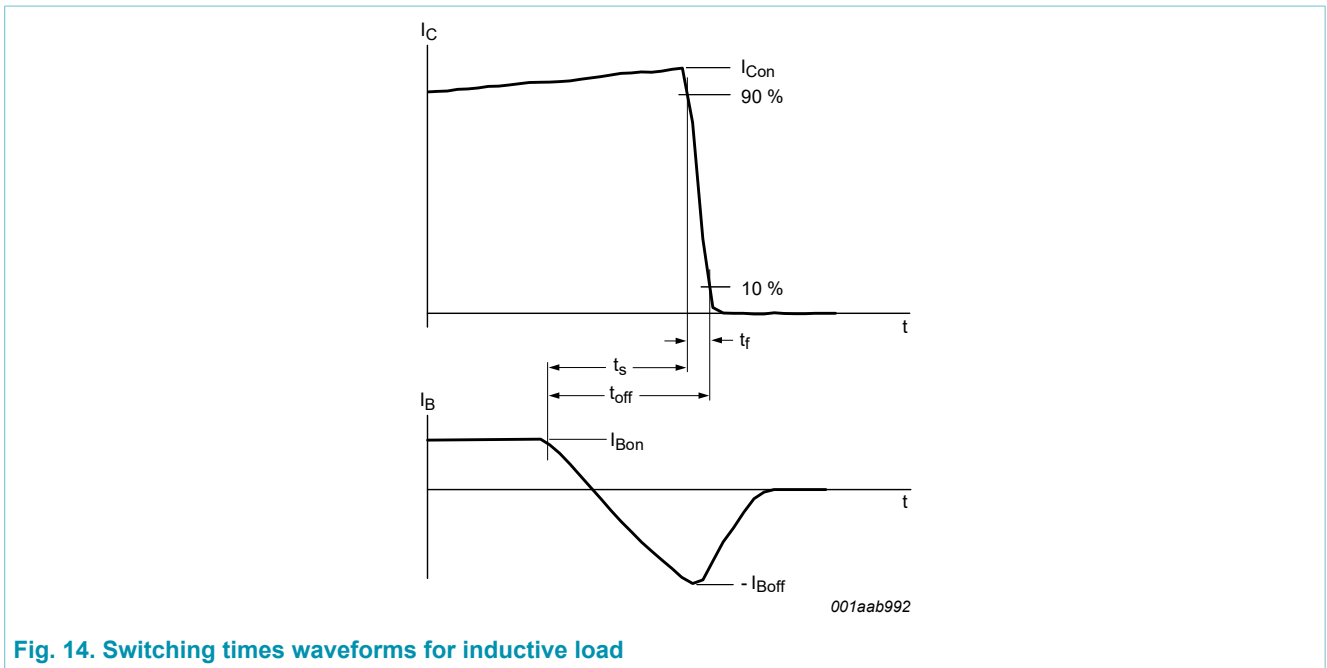


Fig. 14. Switching times waveforms for inductive load

9. Package outline

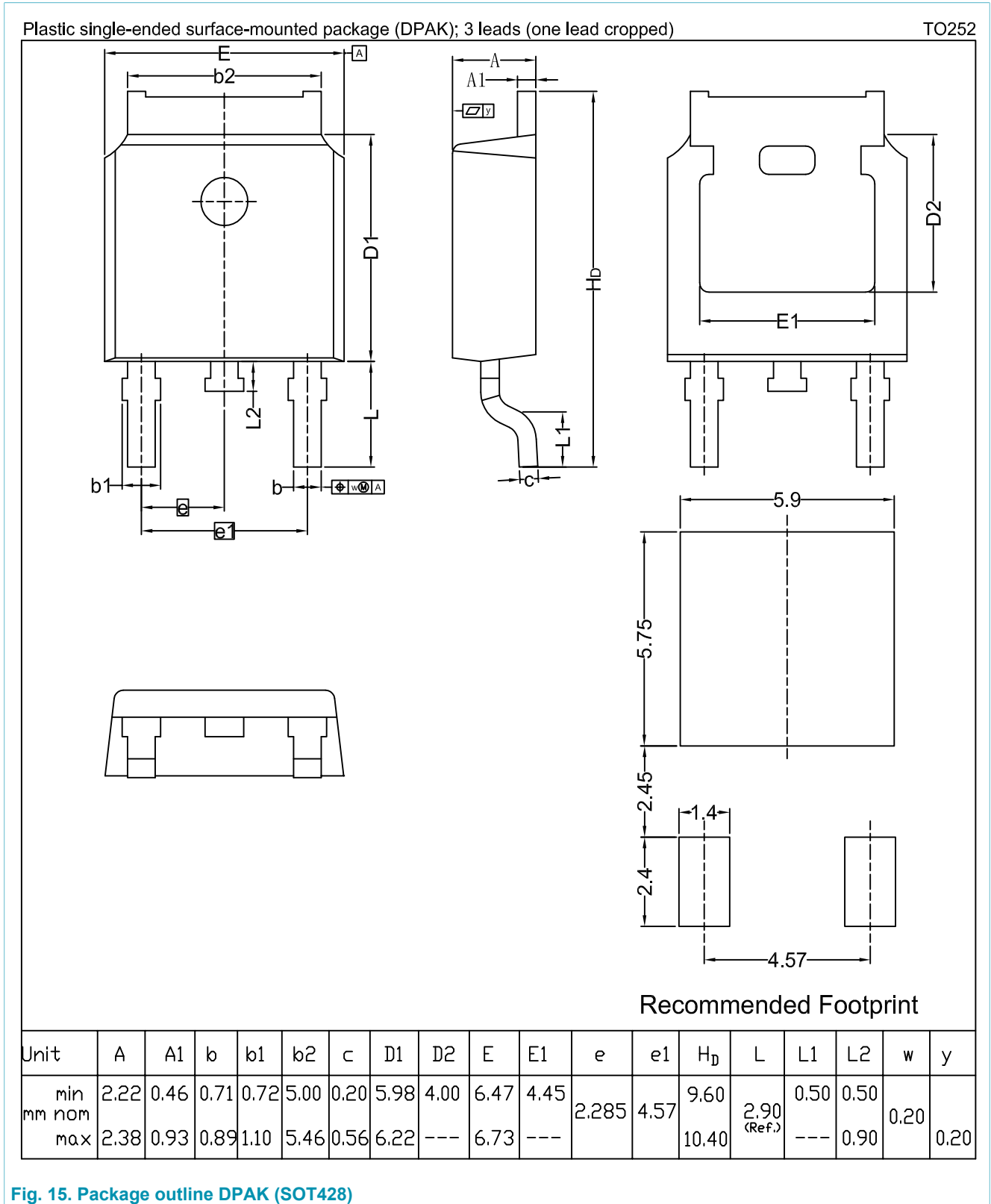


Fig. 15. Package outline DPAK (SOT428)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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