Freescale Semiconductor
Data Sheet: Technical Data

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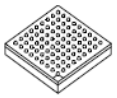
P2010

P2010 QorIQ Integrated Processor Hardware Specifications



WB-TePBGA–689
31 mm × 31 mm

The following list provides an overview of the P2010 feature set:

- Single high-performance Power Architecture® e500 cores.
- 36-bit physical addressing
  - Double-precision floating-point support
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache for each core
  - 800-MHz to 1.33-GHz clock frequency
- 512 Kbyte L2 cache with ECC. Also configurable as SRAM and stashing memory.
- Three 10/100/1000 Mbps enhanced three-speed Ethernet controllers (eTSECs)
  - TCP/IP acceleration, quality of service, and classification capabilities
  - IEEE Std 1588™ support
  - Lossless flow control
  - R/G/MII, R/TBI, SGMII
- High-speed interfaces supporting various multiplexing options:
  - Four SerDes to 3.125 GHz multiplexed across controllers
  - Three PCI Express interfaces
  - Two Serial RapidIO interfaces
  - Two SGMII interfaces
- High-Speed USB controller (USB 2.0)
  - Host and device support
  - Enhanced host controller interface (EHCI)
  - ULPI interface to PHY
- Enhanced secure digital host controller (SD/MMC)

Enhanced Serial peripheral interface (eSPI)

- Integrated security engine
  - Protocol support includes SNOW, ARC4, 3DES, AES, RSA/ECC, RNG, single-pass SSL/TLS, Kasumi
  - XOR acceleration
- 64-bit DDR2/DDR3 SDRAM memory controller with ECC support
- Programmable interrupt controller (PIC) compliant with OpenPIC standard
- Two four-channel DMA controllers
- Two I^2C controllers, DUART, timers
- Enhanced local bus controller (eLBC)
- 16 general-purpose I/O signals
- Operating junction temperature
- 31 × 31 mm 689-pin WB-TePBGA II (wire bond temperature-enhanced plastic BGA)

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Figure 1 shows the major functional units within the device.

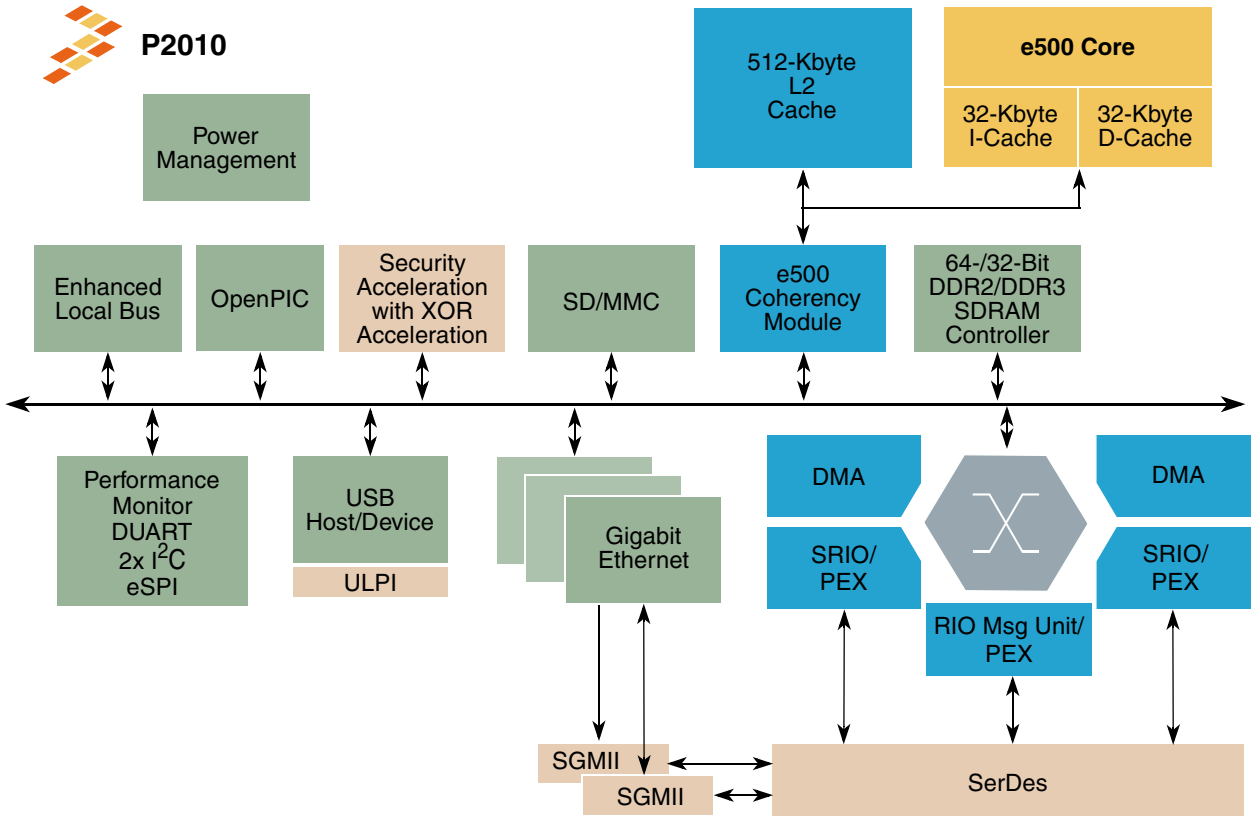


Figure 1. P2010 Block Diagram

1 Pinout Assignments and Reset States

1.1 Ball Layout Diagrams

Figure 2 shows the top view of the P2010 689-pin BGA ball map diagram.

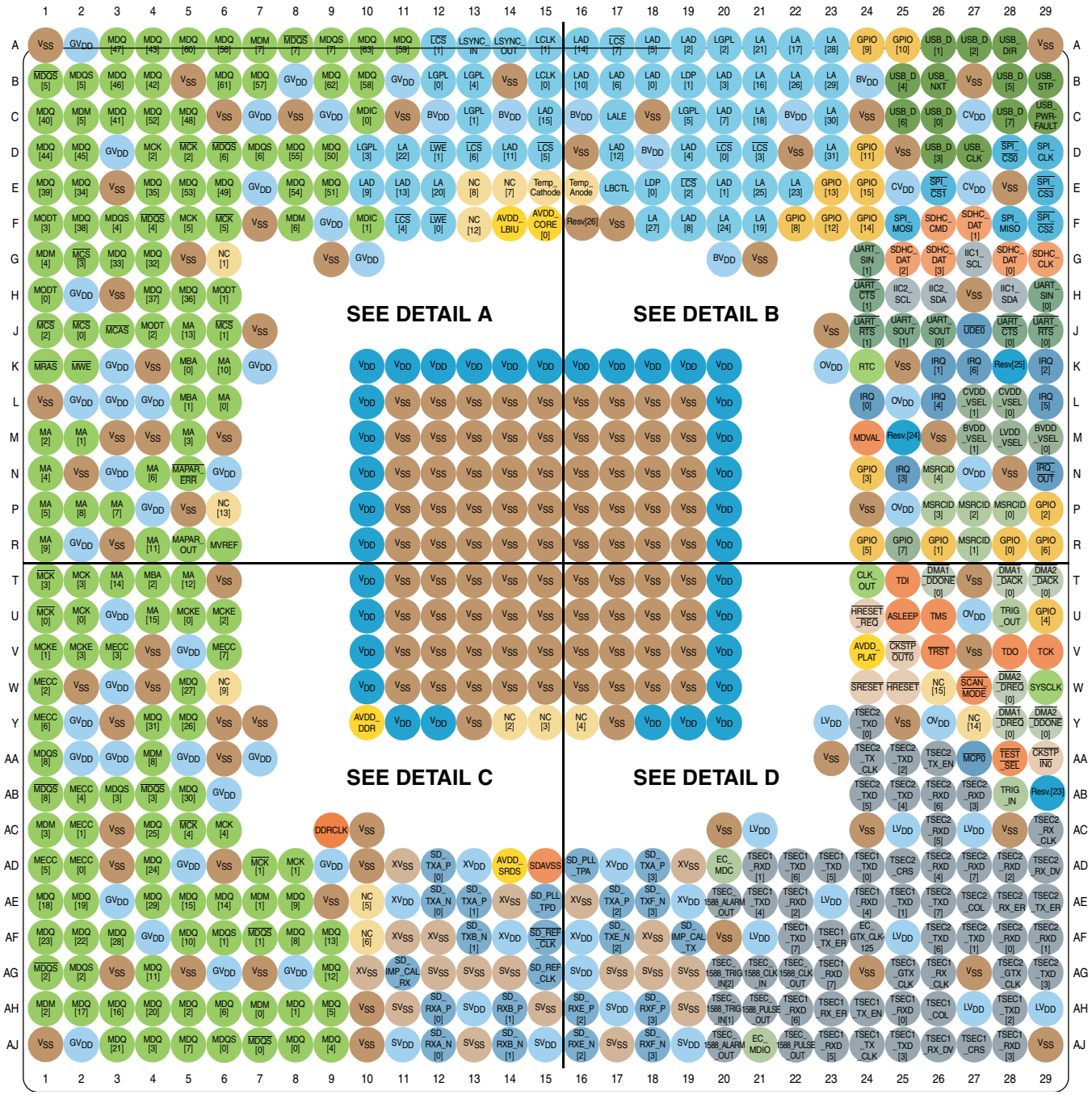
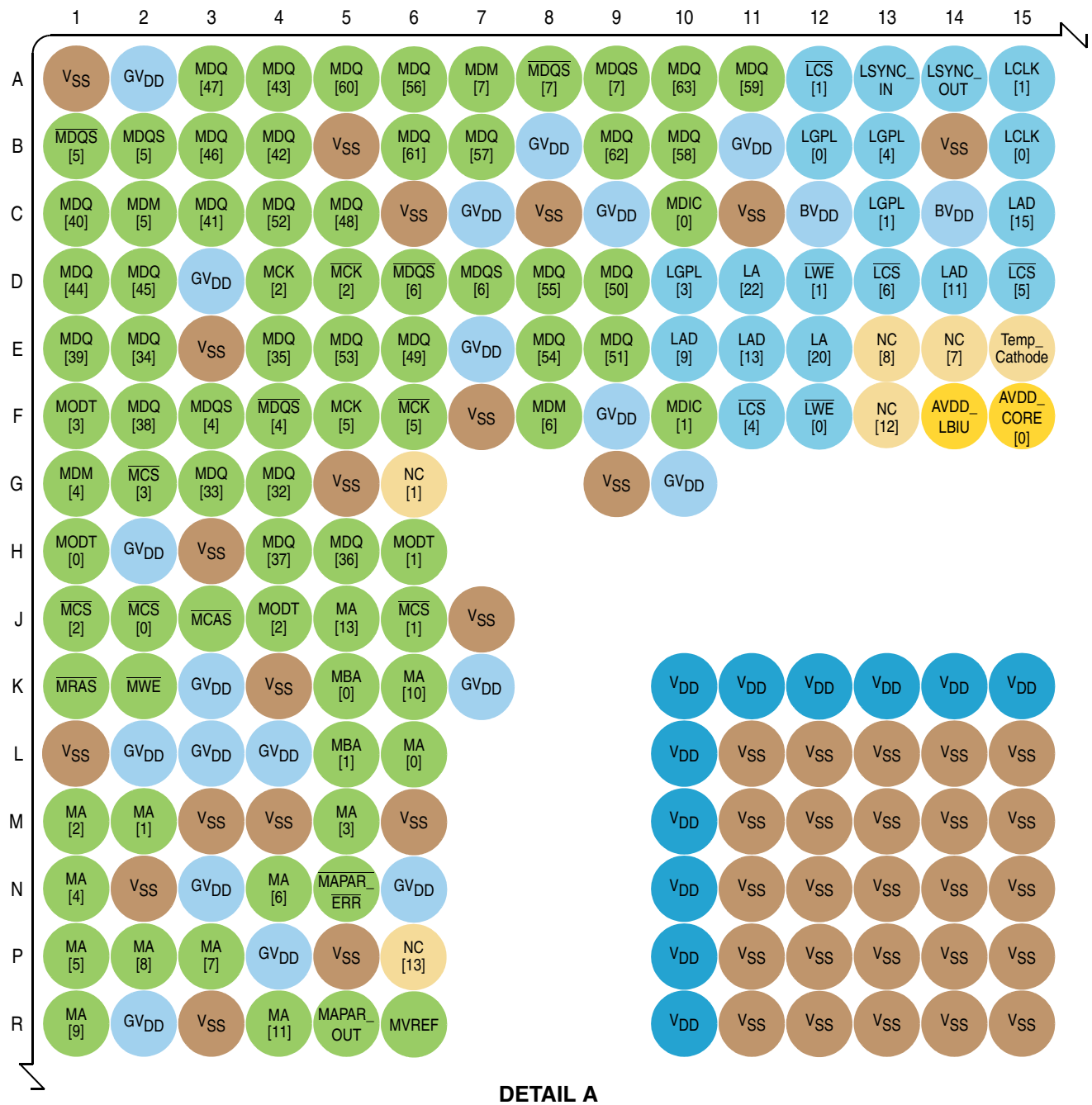
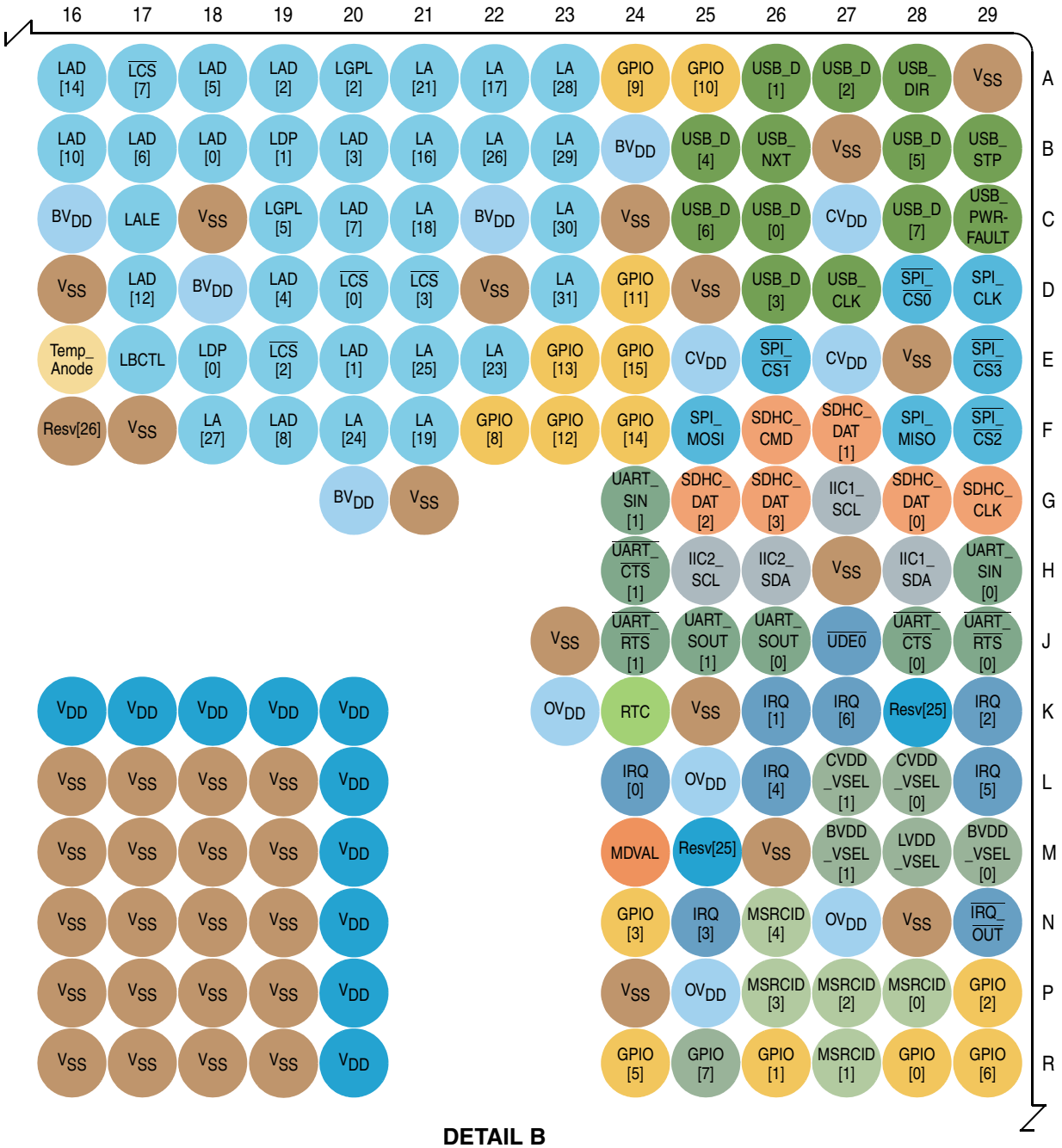


Figure 2. P2010 Top View Ballmap



DETAIL A

Figure 3. P2010 Ball Map—Detail A



DETAIL B

Figure 4. P2010 Ball Map—Detail B

DETAIL C

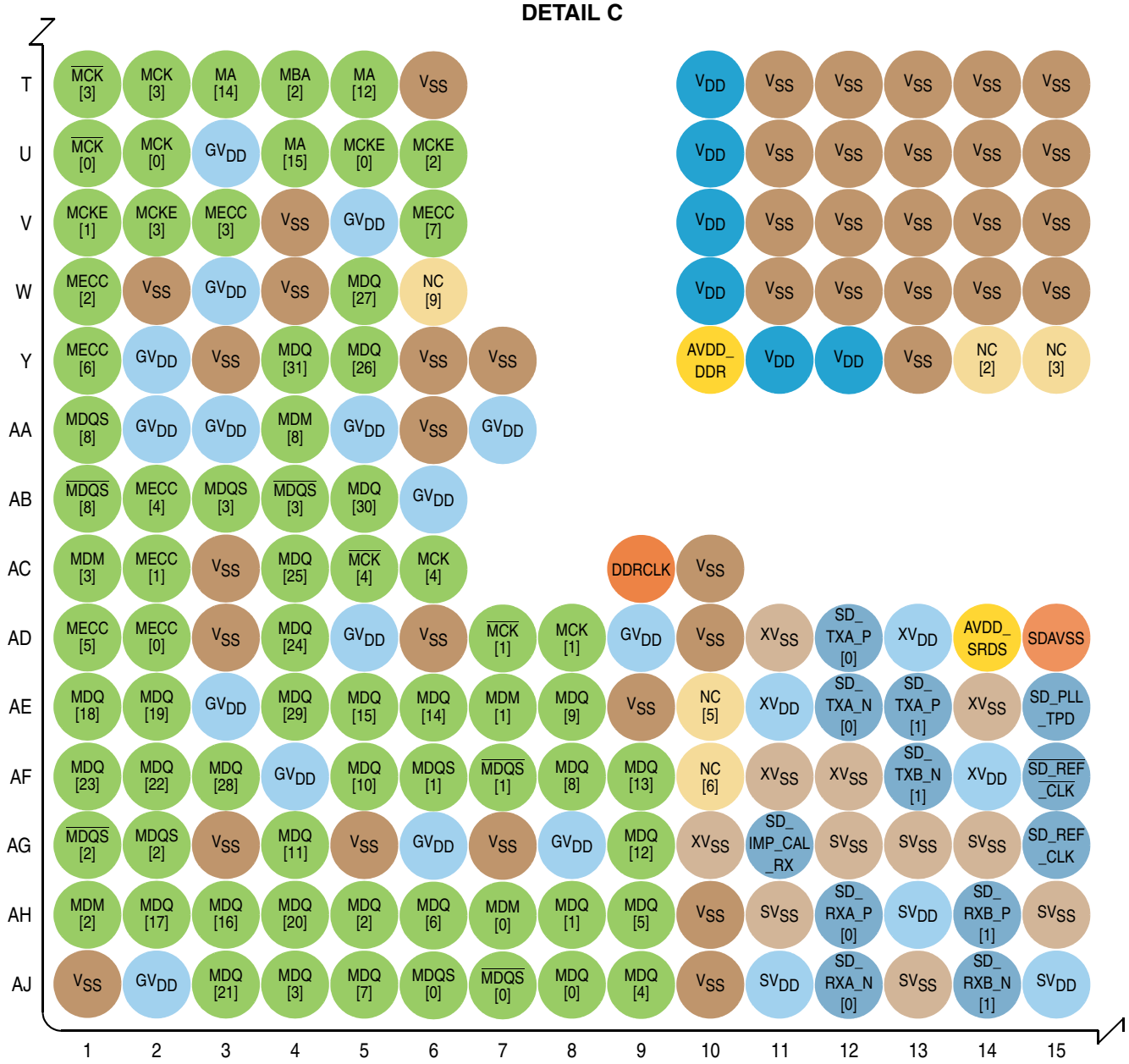


Figure 5. P2010 Ball Map—Detail C

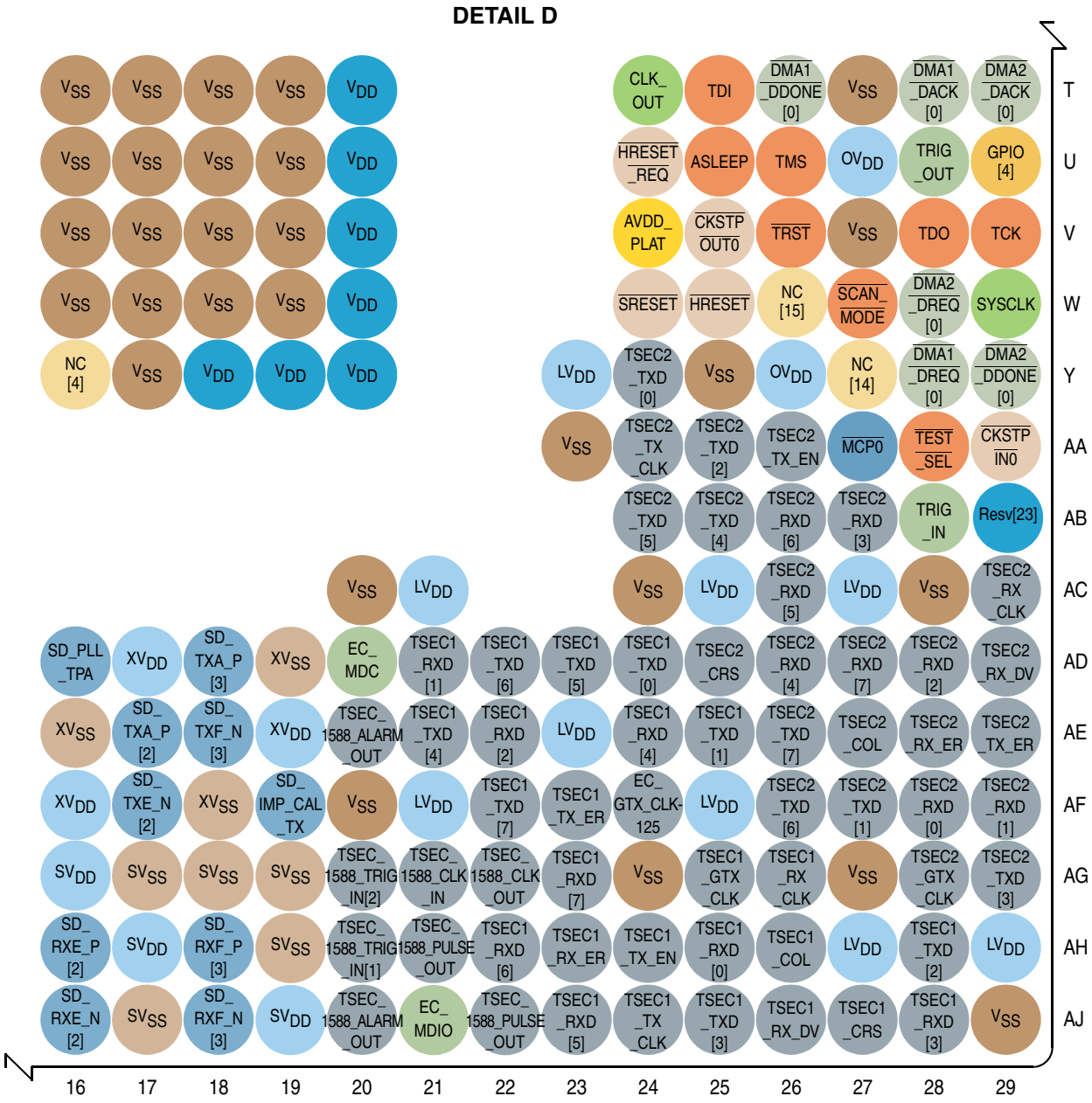


Figure 6. P2010 Ball Map—Detail D

1.2 Pinout List by Bus

Table 1 provides the pinout listing for the device.

Table 1. P2010 Pinout Listing [1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface					
MDQ00	Data	AJ8	IO	GV_{DD}	—
MDQ01	Data	AH8	IO	GV_{DD}	—
MDQ02	Data	AH5	IO	GV_{DD}	—
MDQ03	Data	AJ4	IO	GV_{DD}	—
MDQ04	Data	AJ9	IO	GV_{DD}	—
MDQ05	Data	AH9	IO	GV_{DD}	—
MDQ06	Data	AH6	IO	GV_{DD}	—
MDQ07	Data	AJ5	IO	GV_{DD}	—
MDQ08	Data	AF8	IO	GV_{DD}	—
MDQ09	Data	AE8	IO	GV_{DD}	—
MDQ10	Data	AF5	IO	GV_{DD}	—
MDQ11	Data	AG4	IO	GV_{DD}	—
MDQ12	Data	AG9	IO	GV_{DD}	—
MDQ13	Data	AF9	IO	GV_{DD}	—
MDQ14	Data	AE6	IO	GV_{DD}	—
MDQ15	Data	AE5	IO	GV_{DD}	—
MDQ16	Data	AH3	IO	GV_{DD}	—
MDQ17	Data	AH2	IO	GV_{DD}	—
MDQ18	Data	AE1	IO	GV_{DD}	—
MDQ19	Data	AE2	IO	GV_{DD}	—
MDQ20	Data	AH4	IO	GV_{DD}	—
MDQ21	Data	AJ3	IO	GV_{DD}	—
MDQ22	Data	AF2	IO	GV_{DD}	—
MDQ23	Data	AF1	IO	GV_{DD}	—
MDQ24	Data	AD4	IO	GV_{DD}	—
MDQ25	Data	AC4	IO	GV_{DD}	—
MDQ26	Data	Y5	IO	GV_{DD}	—
MDQ27	Data	W5	IO	GV_{DD}	—
MDQ28	Data	AF3	IO	GV_{DD}	—

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
MDQ29	Data	AE4	IO	GV_{DD}	—
MDQ30	Data	AB5	IO	GV_{DD}	—
MDQ31	Data	Y4	IO	GV_{DD}	—
MDQ32	Data	G4	IO	GV_{DD}	—
MDQ33	Data	G3	IO	GV_{DD}	—
MDQ34	Data	E2	IO	GV_{DD}	—
MDQ35	Data	E4	IO	GV_{DD}	—
MDQ36	Data	H5	IO	GV_{DD}	—
MDQ37	Data	H4	IO	GV_{DD}	—
MDQ38	Data	F2	IO	GV_{DD}	—
MDQ39	Data	E1	IO	GV_{DD}	—
MDQ40	Data	C1	IO	GV_{DD}	—
MDQ41	Data	C3	IO	GV_{DD}	—
MDQ42	Data	B4	IO	GV_{DD}	—
MDQ43	Data	A4	IO	GV_{DD}	—
MDQ44	Data	D1	IO	GV_{DD}	—
MDQ45	Data	D2	IO	GV_{DD}	—
MDQ46	Data	B3	IO	GV_{DD}	—
MDQ47	Data	A3	IO	GV_{DD}	—
MDQ48	Data	C5	IO	GV_{DD}	—
MDQ49	Data	E6	IO	GV_{DD}	—
MDQ50	Data	D9	IO	GV_{DD}	—
MDQ51	Data	E9	IO	GV_{DD}	—
MDQ52	Data	C4	IO	GV_{DD}	—
MDQ53	Data	E5	IO	GV_{DD}	—
MDQ54	Data	E8	IO	GV_{DD}	—
MDQ55	Data	D8	IO	GV_{DD}	—
MDQ56	Data	A6	IO	GV_{DD}	—
MDQ57	Data	B7	IO	GV_{DD}	—
MDQ58	Data	B10	IO	GV_{DD}	—
MDQ59	Data	A11	IO	GV_{DD}	—
MDQ60	Data	A5	IO	GV_{DD}	—

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
MDQ61	Data	B6	IO	GV_{DD}	—
MDQ62	Data	B9	IO	GV_{DD}	—
MDQ63	Data	A10	IO	GV_{DD}	—
MECC[00]	Error Correcting Code	AD2	IO	GV_{DD}	36
MECC[01]	Error Correcting Code	AC2	IO	GV_{DD}	36
MECC[02]	Error Correcting Code	W1	IO	GV_{DD}	36
MECC[03]	Error Correcting Code	V3	IO	GV_{DD}	36
MECC[04]	Error Correcting Code	AB2	IO	GV_{DD}	36
MECC[05]	Error Correcting Code	AD1	IO	GV_{DD}	36
MECC[06]	Error Correcting Code	Y1	IO	GV_{DD}	36
MECC[07]	Error Correcting Code	V6	IO	GV_{DD}	36
$\overline{\text{MAPAR\_ERR}}$	Address Parity Error	N5	I	GV_{DD}	37
MAPAR_OUT	Address Parity Error	R5	O	GV_{DD}	—
MDM[00]	Data Mask	AH7	O	GV_{DD}	—
MDM[01]	Data Mask	AE7	O	GV_{DD}	—
MDM[02]	Data Mask	AH1	O	GV_{DD}	—
MDM[03]	Data Mask	AC1	O	GV_{DD}	—
MDM[04]	Data Mask	G1	O	GV_{DD}	—
MDM[05]	Data Mask	C2	O	GV_{DD}	—
MDM[06]	Data Mask	F8	O	GV_{DD}	—
MDM[07]	Data Mask	A7	O	GV_{DD}	—
MDM[08]	Data Mask	AA4	O	GV_{DD}	—
MDQS[00]	Data Strobe	AJ6	IO	GV_{DD}	—
MDQS[01]	Data Strobe	AF6	IO	GV_{DD}	—
MDQS[02]	Data Strobe	AG2	IO	GV_{DD}	—
MDQS[03]	Data Strobe	AB3	IO	GV_{DD}	—
MDQS[04]	Data Strobe	F3	IO	GV_{DD}	—
MDQS[05]	Data Strobe	B2	IO	GV_{DD}	—
MDQS[06]	Data Strobe	D7	IO	GV_{DD}	—
MDQS[07]	Data Strobe	A9	IO	GV_{DD}	—
MDQS[08]	Data Strobe	AA1	IO	GV_{DD}	—
$\overline{\text{MDQS}}$[00]	Data Strobe	AJ7	IO	GV_{DD}	—

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MDQS}}$[01]	Data Strobe	AF7	IO	GV_{DD}	—
$\overline{\text{MDQS}}$[02]	Data Strobe	AG1	IO	GV_{DD}	—
$\overline{\text{MDQS}}$[03]	Data Strobe	AB4	IO	GV_{DD}	—
$\overline{\text{MDQS}}$[04]	Data Strobe	F4	IO	GV_{DD}	—
$\overline{\text{MDQS}}$[05]	Data Strobe	B1	IO	GV_{DD}	—
$\overline{\text{MDQS}}$[06]	Data Strobe	D6	IO	GV_{DD}	—
$\overline{\text{MDQS}}$[07]	Data Strobe	A8	IO	GV_{DD}	—
$\overline{\text{MDQS}}$[08]	Data Strobe	AB1	IO	GV_{DD}	—
MBA[00]	Bank Select	K5	O	GV_{DD}	—
MBA[01]	Bank Select	L5	O	GV_{DD}	—
MBA[02]	Bank Select	T4	O	GV_{DD}	—
MA[00]	Address	L6	O	GV_{DD}	—
MA[01]	Address	M2	O	GV_{DD}	—
MA[02]	Address	M1	O	GV_{DD}	—
MA[03]	Address	M5	O	GV_{DD}	—
MA[04]	Address	N1	O	GV_{DD}	—
MA[05]	Address	P1	O	GV_{DD}	—
MA[06]	Address	N4	O	GV_{DD}	—
MA[07]	Address	P3	O	GV_{DD}	—
MA[08]	Address	P2	O	GV_{DD}	—
MA[09]	Address	R1	O	GV_{DD}	—
MA[10]	Address	K6	O	GV_{DD}	—
MA[11]	Address	R4	O	GV_{DD}	—
MA[12]	Address	T5	O	GV_{DD}	—
MA[13]	Address	J5	O	GV_{DD}	—
MA[14]	Address	T3	O	GV_{DD}	—
MA[15]	Address	U4	O	GV_{DD}	—
$\overline{\text{MWE}}$	Write Enable	K2	O	GV_{DD}	—
$\overline{\text{MRAS}}$	Row Address Strobe	K1	O	GV_{DD}	—
$\overline{\text{MCAS}}$	Column Address Strobe	J3	O	GV_{DD}	—
$\overline{\text{MCS}}$[00]	Chip Select	J2	O	GV_{DD}	—
$\overline{\text{MCS}}$[01]	Chip Select	J6	O	GV_{DD}	—

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MCS}}$[02]	Chip Select	J1	O	GV_{DD}	—
$\overline{\text{MCS}}$[03]	Chip Select	G2	O	GV_{DD}	—
MCKE[00]	Clock Enable	U5	O	GV_{DD}	9
MCKE[01]	Clock Enable	V1	O	GV_{DD}	9
MCKE[02]	Clock Enable	U6	O	GV_{DD}	9
MCKE[03]	Clock Enable	V2	O	GV_{DD}	9
MCK[00]	Clock	U2	O	GV_{DD}	32
MCK[01]	Clock	AD8	O	GV_{DD}	32
MCK[02]	Clock	D4	O	GV_{DD}	32
MCK[03]	Clock	T2	O	GV_{DD}	32
MCK[04]	Clock	AC6	O	GV_{DD}	32
MCK[05]	Clock	F5	O	GV_{DD}	32
$\overline{\text{MCK}}$[00]	Clock Complements	U1	O	GV_{DD}	32
$\overline{\text{MCK}}$[01]	Clock Complements	AD7	O	GV_{DD}	32
$\overline{\text{MCK}}$[02]	Clock Complements	D5	O	GV_{DD}	32
$\overline{\text{MCK}}$[03]	Clock Complements	T1	O	GV_{DD}	32
$\overline{\text{MCK}}$[04]	Clock Complements	AC5	O	GV_{DD}	32
$\overline{\text{MCK}}$[05]	Clock Complements	F6	O	GV_{DD}	32
MODT[00]	On Die Termination	H1	O	GV_{DD}	—
MODT[01]	On Die Termination	H6	O	GV_{DD}	—
MODT[02]	On Die Termination	J4	O	GV_{DD}	—
MODT[03]	On Die Termination	F1	O	GV_{DD}	—
MDIC[00]	Driver Impedance Calibration	C10	IO	GV_{DD}	18
MDIC[01]	Driver Impedance Calibration	F10	IO	GV_{DD}	18
SerDes					
SD_TX[03]	Transmit Data (positive)	AD18	O	XV_{DD}	—
SD_TX[02]	Transmit Data (positive)	AE17	O	XV_{DD}	—
SD_TX[01]	Transmit Data (positive)	AE13	O	XV_{DD}	—
SD_TX[00]	Transmit Data (positive)	AD12	O	XV_{DD}	—
$\overline{\text{SD\_TX}}$[03]	Transmit Data (negative)	AE18	O	XV_{DD}	—
$\overline{\text{SD\_TX}}$[02]	Transmit Data (negative)	AF17	O	XV_{DD}	—

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{SD\_TX}}$[01]	Transmit Data (negative)	AF13	O	XV_{DD}	—
$\overline{\text{SD\_TX}}$[00]	Transmit Data (negative)	AE12	O	XV_{DD}	—
SD_RX[03]	Receive Data (positive)	AH18	I	XV_{DD}	—
SD_RX[02]	Receive Data (positive)	AH16	I	XV_{DD}	—
SD_RX[01]	Receive Data (positive)	AH14	I	XV_{DD}	—
SD_RX[00]	Receive Data (positive)	AH12	I	XV_{DD}	—
$\overline{\text{SD\_RX}}$[03]	Receive Data (negative)	AJ18	I	XV_{DD}	—
$\overline{\text{SD\_RX}}$[02]	Receive Data (negative)	AJ16	I	XV_{DD}	—
$\overline{\text{SD\_RX}}$[01]	Receive Data (negative)	AJ14	I	XV_{DD}	—
$\overline{\text{SD\_RX}}$[00]	Receive Data (negative)	AJ12	I	XV_{DD}	—
SD_REF_CLK	PLL Reference Clock	AG15	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK}}$	PLL Reference Clock Complement	AF15	I	XV_{DD}	—
Enhanced Local Bus Controller Interface					
LAD[00]	Muxed Data/Address	B18	IO	BV_{DD}	4, 23
LAD[01]	Muxed Data/Address	E20	IO	BV_{DD}	4, 23
LAD[02]	Muxed Data/Address	A19	IO	BV_{DD}	4, 23
LAD[03]	Muxed Data/Address	B20	IO	BV_{DD}	4, 23
LAD[04]	Muxed Data/Address	D19	IO	BV_{DD}	4, 23
LAD[05]	Muxed Data/Address	A18	IO	BV_{DD}	4, 23
LAD[06]	Muxed Data/Address	B17	IO	BV_{DD}	4, 23
LAD[07]	Muxed Data/Address	C20	IO	BV_{DD}	4, 23
LAD[08]	Muxed Data/Address	F19	IO	BV_{DD}	4, 23
LAD[09]	Muxed Data/Address	E10	IO	BV_{DD}	4, 23
LAD[10]	Muxed Data/Address	B16	IO	BV_{DD}	4, 23
LAD[11]	Muxed Data/Address	D14	IO	BV_{DD}	4, 23
LAD[12]	Muxed Data/Address	D17	IO	BV_{DD}	4, 23
LAD[13]	Muxed Data/Address	E11	IO	BV_{DD}	4, 23
LAD[14]	Muxed Data/Address	A16	IO	BV_{DD}	4, 23
LAD[15]	Muxed Data/Address	C15	IO	BV_{DD}	4, 23
LDP[00]	Data Parity	E18	IO	BV_{DD}	—
LDP[01]	Data Parity	B19	IO	BV_{DD}	—

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
LA[16]	Address	B21	O	BV_{DD}	7
LA[17]	Address	A22	O	BV_{DD}	15
LA[18]	Address	C21	O	BV_{DD}	4,7
LA[19]	Address	F21	O	BV_{DD}	4,7
LA[20]	Address	E12	O	BV_{DD}	4,7,21
LA[21]	Address	A21	O	BV_{DD}	4,7,21
LA[22]	Address	D11	O	BV_{DD}	4,7,21
LA[23]	Address	E22	O	BV_{DD}	4,7
LA[24]	Address	F20	O	BV_{DD}	4,7
LA[25]	Address	E21	O	BV_{DD}	7
LA[26]	Address	B22	O	BV_{DD}	4,7
LA[27]	Address	F18	O	BV_{DD}	7,25
LA[28]	Address	A23	O	BV_{DD}	4,7
LA[29]	Address	B23	O	BV_{DD}	5,7
LA[30]	Address	C23	O	BV_{DD}	5,7
LA[31]	Address	D23	O	BV_{DD}	5,7
$\overline{\text{LCS}}$[00]	Chip Selects	D20	O	BV_{DD}	8
$\overline{\text{LCS}}$[01]	Chip Selects	A12	O	BV_{DD}	8
$\overline{\text{LCS}}$[02]	Chip Selects	E19	O	BV_{DD}	8
$\overline{\text{LCS}}$[03]	Chip Selects	D21	O	BV_{DD}	8
$\overline{\text{LCS}}$[04]	Chip Selects	F11	O	BV_{DD}	8
$\overline{\text{LCS}}$[05]/$\overline{\text{DMA2\_DREQ}}$[01]	Chip Selects	D15	O	BV_{DD}	8
$\overline{\text{LCS}}$[06]/$\overline{\text{DMA2\_DACK}}$[01]	Chip Selects	D13	O	BV_{DD}	8
$\overline{\text{LCS}}$[07]/$\overline{\text{DMA2\_DDONE}}$[01]	Chip Selects	A17	O	BV_{DD}	8
$\overline{\text{LWE}}$[00]/$\overline{\text{LBS}}$[00]	Write Enable	F12	O	BV_{DD}	7
$\overline{\text{LWE}}$[01]/$\overline{\text{LBS}}$[01]	Write Enable	D12	O	BV_{DD}	4, 7
LBCTL	Buffer Control	E17	O	BV_{DD}	6
LALE	Address Latch Enable	C17	O	BV_{DD}	6
LGPL[00]/LFCLE	UPM General Purpose Line 0/Flash Command Latch Enable	B12	O	BV_{DD}	4
LGPL[01]/LFALE	UPM General Purpose Line 1/Flash Addr Latch Enable	C13	O	BV_{DD}	4

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
LGPL[02]/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM General Purpose Line 2/Output Enable/ Flash Read Enable	A20	O	BV_{DD}	6
LGPL[03]/$\overline{\text{LFWP}}$	UPM General Purpose Line 3/Flash Write Protect	D10	O	BV_{DD}	4
LGPL[04]/$\overline{\text{LGTA}}$/LFRB/ LUPWAIT/LPBSE	UPM General Purpose Line 4/Txn Termination/ Wait/Flash Ready-Busy	B13	O	BV_{DD}	34
LGPL[05]	UPM General Purpose Line 5/Addr mux	C19	O	BV_{DD}	4
LCLK[00]	Local Bus Clock	B15	O	BV_{DD}	—
LCLK[01]	Local Bus Clock	A15	O	BV_{DD}	—
LSYNC_IN	Local Bus DLL Synchronization	A13	I	BV_{DD}	—
LSYNC_OUT	Local Bus DLL Synchronization	A14	O	BV_{DD}	—
DMA					
$\overline{\text{DMA1\_DREQ}}$	DMA1 Channel 0 Request	Y28	I	OV_{DD}	—
$\overline{\text{DMA2\_DREQ}}$	DMA2 Channel 0 Request	W28	I	OV_{DD}	—
$\overline{\text{DMA1\_DACK}}$	DMA1 Channel 0 Acknowledge	T28	O	OV_{DD}	15
$\overline{\text{DMA2\_DACK}}$	DMA2 Channel 0 Acknowledge	T29	O	OV_{DD}	4, 7
$\overline{\text{DMA1\_DDONE}}$	DMA1 Channel 0 Done	T26	O	OV_{DD}	7,21
$\overline{\text{DMA2\_DDONE}}$	DMA2 Channel 0 Done	Y29	O	OV_{DD}	4, 7
Programmable Interrupt Controller					
$\overline{\text{UDE0}}$	Unconditional Debug Event Proc 0	J27	I	OV_{DD}	—
$\overline{\text{MCP0}}$	Machine Check Processor 0	AA27	I	OV_{DD}	—
IRQ[00]	External Interrupts	L24	I	OV_{DD}	—
IRQ[01]	External Interrupts	K26	I	OV_{DD}	—
IRQ[02]	External Interrupts	K29	I	OV_{DD}	—
IRQ[03]	External Interrupts	N25	I	OV_{DD}	—
IRQ[04]	External Interrupts	L26	I	OV_{DD}	—
IRQ[05]	External Interrupts	L29	I	OV_{DD}	—
IRQ[06]	External Interrupts	K27	I	OV_{DD}	—

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{IRQ\_OUT}}$	Interrupt Output	N29	O	OV_{DD}	2, 3
Voltage Select					
LVDD_VSEL	Voltage Select	M28	I	OV_{DD}	22
BVDD_VSEL[00]	Voltage Select	M29	I	OV_{DD}	22
BVDD_VSEL[01]	Voltage Select	M27	I	OV_{DD}	22
CVDD_VSEL[00]	Voltage Select	L28	I	OV_{DD}	22
CVDD_VSEL[01]	Voltage Select	L27	I	OV_{DD}	22
1588					
TSEC_1588_CLK_IN	Clock In	AG21	I	LV_{DD}	—
TSEC_1588_TRIG_IN1	Trigger In 1	AH20	I	LV_{DD}	—
TSEC_1588_TRIG_IN2	Trigger In 2	AG20	I	LV_{DD}	—
TSEC_1588_ALARM_OUT01	Trigger Out 1	AE20	O	LV_{DD}	4, 7
TSEC_1588_ALARM_OUT02	Trigger Out 2	AJ20	O	LV_{DD}	4, 7
TSEC_1588_CLK_OUT	Clock Out	AG22	O	LV_{DD}	24
TSEC_1588_PULSE_OUT[01]	Pulse Out 1	AH21	O	LV_{DD}	24
TSEC_1588_PULSE_OUT[02]	Pulse Out 2	AJ22	O	LV_{DD}	24
Ethernet Management Interface					
EC_MDC	Management Data Clock	AD20	O	LV_{DD}	4, 7
EC_MDIO	Management Data In/Out	AJ21	IO	LV_{DD}	—
Gigabit Ethernet Reference Clock					
EC_GTX_CLK125	Reference Clock	AF24	I	LV_{DD}	20
Three Speed Ethernet Controller 1					
TSEC1_TXD[07]/ TSEC3_TXD[03]	Transmit Data	AF22	O	LV_{DD}	4, 7
TSEC1_TXD[06]/ TSEC3_TXD[02]	Transmit Data	AD22	O	LV_{DD}	4, 7
TSEC1_TXD[05]/ TSEC3_TXD[01]	Transmit Data	AD23	O	LV_{DD}	4, 7
TSEC1_TXD[04]/ TSEC3_TXD[00]	Transmit Data	AE21	O	LV_{DD}	4, 7
TSEC1_TXD[03]	Transmit Data	AJ25	O	LV_{DD}	4, 7
TSEC1_TXD[02]	Transmit Data	AH28	O	LV_{DD}	4, 7
TSEC1_TXD[01]	Transmit Data	AE25	O	LV_{DD}	4, 7

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_TXD[00]	Transmit Data	AD24	O	LV_{DD}	4, 7
TSEC1_TX_EN	Transmit Enable	AH24	O	LV_{DD}	16
TSEC1_TX_ER	Transmit Error	AF23	O	LV_{DD}	4,7
TSEC1_TX_CLK	Transmit Clock	AJ24	I	LV_{DD}	—
TSEC1_GTX_CLK	Transmit Clock Out	AG25	O	LV_{DD}	—
TSEC1_CRS/TSEC3_RX_DV	Carrier Sense	AJ27	IO	LV_{DD}	—
TSEC1_COL/TSEC3_RX_CLK	Collision Detect	AH26	I	LV_{DD}	—
TSEC1_RXD[07]/ TSEC3_RXD[03]	Receive Data	AG23	I	LV_{DD}	—
TSEC1_RXD[06]/ TSEC3_RXD[02]	Receive Data	AH22	I	LV_{DD}	—
TSEC1_RXD[05]/ TSEC3_RXD[01]	Receive Data	AJ23	I	LV_{DD}	—
TSEC1_RXD[04]/ TSEC3_RXD[00]	Receive Data	AE24	I	LV_{DD}	—
TSEC1_RXD[03]	Receive Data	AJ28	I	LV_{DD}	—
TSEC1_RXD[02]	Receive Data	AE22	I	LV_{DD}	—
TSEC1_RXD[01]	Receive Data	AD21	I	LV_{DD}	—
TSEC1_RXD[00]	Receive Data	AH25	I	LV_{DD}	—
TSEC1_RX_DV	Receive Data Valid	AJ26	I	LV_{DD}	—
TSEC1_RX_ER	Receive Error	AH23	I	LV_{DD}	—
TSEC1_RX_CLK	Receive Clock	AG26	I	LV_{DD}	—
Three Speed Ethernet Controller 2					
TSEC2_TXD[07]	Transmit Data	AE26	O	LV_{DD}	4,7
TSEC2_TXD[06]	Transmit Data	AF26	O	LV_{DD}	15
TSEC2_TXD[05]/ TSEC3_TX_EN	Transmit Data	AB24	O	LV_{DD}	4,7, 16
TSEC2_TXD[04]/ TSEC3_GTX_CLK	Transmit Data	AB25	O	LV_{DD}	4,7
TSEC2_TXD[03]	Transmit Data	AG29	O	LV_{DD}	4,7
TSEC2_TXD[02]	Transmit Data	AA25	O	LV_{DD}	4,7
TSEC2_TXD[01]	Transmit Data	AF27	O	LV_{DD}	4,7 17
TSEC2_TXD[00]	Transmit Data	Y24	O	LV_{DD}	4,7
TSEC2_TX_EN	Transmit Enable	AA26	O	LV_{DD}	16

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TX_ER	Transmit Error	AE29	O	LV_{DD}	4,7
TSEC2_TX_CLK	Transmit Clock In	AA24	I	LV_{DD}	—
TSEC2_GTX_CLK	Transmit Clock Out	AG28	O	LV_{DD}	—
TSEC2_CRS/TSEC3_RX_ER	Carrier Sense	AD25	IO	LV_{DD}	—
TSEC2_COL/TSEC3_TX_CLK	Collision Detect	AE27	I	LV_{DD}	—
TSEC2_RXD[07]	Receive Data	AD27	I	LV_{DD}	—
TSEC2_RXD[06]	Receive Data	AB26	I	LV_{DD}	—
TSEC2_RXD[05]	Receive Data	AC26	I	LV_{DD}	—
TSEC2_RXD[04]	Receive Data	AD26	I	LV_{DD}	—
TSEC2_RXD[03]	Receive Data	AB27	I	LV_{DD}	—
TSEC2_RXD[02]	Receive Data	AD28	I	LV_{DD}	—
TSEC2_RXD[01]	Receive Data	AF29	I	LV_{DD}	—
TSEC2_RXD[00]	Receive Data	AF28	I	LV_{DD}	—
TSEC2_RX_DV	Receive Data Valid	AD29	I	LV_{DD}	—
TSEC2_RX_ER	Receive Error	AE28	I	LV_{DD}	—
TSEC2_RX_CLK	Transmit Clock In	AC29	I	LV_{DD}	—
DUART					
UART0_SOUT	Transmit Data	J26	O	OV_{DD}	21
UART1_SOUT	Transmit Data	J25	O	OV_{DD}	—
UART0_SIN	Receive Data	H29	I	OV_{DD}	—
UART1_SIN	Receive Data	G24	I	OV_{DD}	—
$\overline{\text{UART0\_CTS}}$	Clear to Send	J28	I	OV_{DD}	—
$\overline{\text{UART1\_CTS}}$	Clear to Send	H24	I	OV_{DD}	—
$\overline{\text{UART0\_RTS}}$	Ready to Send	J29	O	OV_{DD}	4
$\overline{\text{UART1\_RTS}}$	Ready to Send	J24	O	OV_{DD}	4
I2C					
IIC1_SDA	Serial Data	H28	IO	OV_{DD}	3,14
IIC1_SCL	Serial Clock	G27	IO	OV_{DD}	3,14
IIC2_SDA	Serial Data	H26	IO	OV_{DD}	3,14
IIC2_SCL	Serial Clock	H25	IO	OV_{DD}	3,14
eSDHC					

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SDHC_DATA[00]	Data	G28	IO	CV_{DD}	—
SDHC_DATA[01]	Data	F27	IO	CV_{DD}	—
SDHC_DATA[02]	Data	G25	IO	CV_{DD}	—
SDHC_DATA[03]	Data	G26	IO	CV_{DD}	—
SDHC_CMD	Command/Response	F26	IO	CV_{DD}	—
SDHC_CLK	Host to Card Clock	G29	IO	CV_{DD}	—
eSPI					
SPI_MISO	Master In Slave Out	F28	I	CV_{DD}	—
SPI_MOSI	Master Out Slave In	F25	IO	CV_{DD}	—
$\overline{\text{SPI\_CS}}$[00]/SDHC_DATA[04]	eSPI chip select	D28	IO	CV_{DD}	—
$\overline{\text{SPI\_CS}}$[01]/SDHC_DATA[05]	eSPI chip select	E26	IO	CV_{DD}	—
$\overline{\text{SPI\_CS}}$[02]/SDHC_DATA[06]	eSPI chip select	F29	IO	CV_{DD}	—
$\overline{\text{SPI\_CS}}$[03]/SDHC_DATA[07]	eSPI chip select	E29	IO	CV_{DD}	—
SPI_CLK	eSPI clock	D29	O	CV_{DD}	—
USB					
USB_NXT	USB Next data	B26	I	CV_{DD}	—
USB_DIR	USB Data Direction	A28	I	CV_{DD}	—
USB_STP	USB Stop	B29	O	CV_{DD}	15
USB_PWRFAULT	Power Fault	C29	I	CV_{DD}	—
USB_CLK	USB Bus Clock	D27	I	CV_{DD}	—
USB_D[07]	USB Data Bits	C28	I/O	CV_{DD}	—
USB_D[06]	USB Data Bits	C25	I/O	CV_{DD}	—
USB_D[05]	USB Data Bits	B28	I/O	CV_{DD}	—
USB_D[04]	USB Data Bits	B25	I/O	CV_{DD}	—
USB_D[03]	USB Data Bits	D26	I/O	CV_{DD}	—
USB_D[02]	USB Data Bits	A27	I/O	CV_{DD}	—
USB_D[01]	USB Data Bits	A26	I/O	CV_{DD}	—
USB_D[00]	USB Data Bits	C26	I/O	CV_{DD}	—
General-Purpose Input/Output					
GPIO[00]/IRQ[07]	General-Purpose Input/ Output	R28	IO	OV_{DD}	—

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
GPIO[01]/IRQ[08]	General-Purpose Input/ Output	R26	IO	OV_{DD}	—
GPIO[02]/IRQ[09]	General-Purpose Input/ Output	P29	IO	OV_{DD}	—
GPIO[03]/IRQ[10]	General-Purpose Input/ Output	N24	IO	OV_{DD}	—
GPIO[04]/IRQ[11]	General-Purpose Input/ Output	U29	IO	OV_{DD}	—
GPIO[05]	General-Purpose Input/ Output	R24	IO	OV_{DD}	—
GPIO[06]	General-Purpose Input/ Output	R29	IO	OV_{DD}	—
GPIO[07]	General-Purpose Input/ Output	R25	IO	OV_{DD}	—
GPIO[08]/$\overline{\text{SDHC\_CD}}$	General-Purpose Input/ Output	F22	IO	BV_{DD}	31
GPIO[09]/SDHC_WP	General-Purpose Input/ Output	A24	IO	BV_{DD}	—
GPIO[10]/USB_PCTL0	General-Purpose Input/ Output	A25	IO	BV_{DD}	—
GPIO[11]/USB_PCTL1	General-Purpose Input/ Output	D24	IO	BV_{DD}	—
GPIO[12]	General-Purpose Input/ Output	F23	IO	BV_{DD}	—
GPIO[13]	General-Purpose Input/ Output	E23	IO	BV_{DD}	—
GPIO[14]	General-Purpose Input/ Output	F24	IO	BV_{DD}	—
GPIO[15]	General-Purpose Input/ Output	E24	IO	BV_{DD}	—
System Control					
$\overline{\text{HRESET}}$	Hard Reset	W25	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	Reset Request	U24	O	OV_{DD}	15
$\overline{\text{SRESET}}$	Soft Reset	W24	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN0}}$	Checkstop In	AA29	I	OV_{DD}	2
$\overline{\text{CKSTP\_OUT[00]}}$	Checkstop Out	V25	O	OV_{DD}	2, 3
Debug					

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TRIG_IN	Trigger In	AB28	I	OV_{DD}	—
TRIG_OUT	Trigger Out	U28	O	OV_{DD}	7
MSRCID[00]	Debug Source ID 0	P28	O	OV_{DD}	4
MSRCID[01]	Debug Source ID 1	R27	O	OV_{DD}	21
MSRCID[02]	Debug Source ID 2	P27	O	OV_{DD}	15
MSRCID[03]	Debug Source ID 3	P26	O	OV_{DD}	15
MSRCID[04]	Debug Source ID 4	N26	O	OV_{DD}	21
MDVAL	Debug Data Valid	M24	O	OV_{DD}	15
Clocks					
CLK_OUT	Clock Out	T24	O	OV_{DD}	—
RTC	Real Time Clock	K24	I	OV_{DD}	—
DDRCLK	DDR Clock	AC9	I	OV_{DD}	19
SYSCLK	System Clock	W29	I	OV_{DD}	—
DFT					
$\overline{\text{SCAN\_MODE}}$	Scan Mode	W27	I	OV_{DD}	33
$\overline{\text{TEST\_SEL}}$	Test Select	AA28	I	OV_{DD}	30
JTAG					
TCK	Test Clock	V29	I	OV_{DD}	—
TDI	Test Data In	T25	I	OV_{DD}	10
TDO	Test Data Out	V28	O	OV_{DD}	9
TMS	Test Mode Select	U26	I	OV_{DD}	10
$\overline{\text{TRST}}$	Test Reset	V26	I	OV_{DD}	10
Power Management					
ASLEEP	Asleep	U25	O	OV_{DD}	7, 11, 15
No Connect					
NC1	No Connection	AE10	NC	OV_{DD}	—
NC2	No Connection	AF10	NC	OV_{DD}	—
NC3	No Connection	E13	NC	OV_{DD}	—
NC4	No Connection	E14	NC	OV_{DD}	—
NC5	No Connection	W6	NC	OV_{DD}	—

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
NC6	No Connection	Y14	NC	OV_{DD}	—
NC7	No Connection	Y15	NC	OV_{DD}	—
NC8	No Connection	Y16	NC	OV_{DD}	—
NC9	No Connection	G6	NC	OV_{DD}	—
NC12	No Connection	F13	NC	—	—
NC13	No Connection	P6	NC	—	—
NC14	No Connection	Y27	NC	—	—
NC15	No Connection	W26	NC	—	—
Reserve					
Reserve23	Reserved	AB29	Pull up 4.7K	OV_{DD}	—
Reserve24	Reserved	M25	Pull up 4.7K	OV_{DD}	—
Reserve25	Reserved	K28	Pull up 4.7K	OV_{DD}	—
Reserve26	Reserved	F16	Pull up 4.7K	V_{DD}	—
Power and Ground Signals					
AGND_SRDS	SerDes PLL GND	AD15	—	—	—
AVDD_CORE0	Core PLL0 Supply	F15	—	AV_{DD}_core0	13, 26
AVDD_DDR	DDR PLL Supply	Y10	—	AV_{DD}_DDR	13
AVDD_LBIU	Local Bus PLL Supply	F14	—	AV_{DD}_LBIU	13
AVDD_PLAT	Platform PLL Supply	V24	—	AV_{DD}_PLAT	13
AVDD_SRDS	SerDes PLL Supply	AD14	—	AV_{DD}_SRDS	13
BVDD	Local Bus, GPIO Supply	B24	—	BV_{DD}	—
BVDD	Local Bus, GPIO Supply	C12	—	BV_{DD}	—
BVDD	Local Bus, GPIO Supply	C14	—	BV_{DD}	—
BVDD	Local Bus, GPIO Supply	C16	—	BV_{DD}	—
BVDD	Local Bus, GPIO Supply	C22	—	BV_{DD}	—
BVDD	Local Bus, GPIO Supply	D18	—	BV_{DD}	—
BVDD	Local Bus, GPIO Supply	G20	—	BV_{DD}	—
CVDD	SPI, eSDHC, USB Supply	C27	—	CV_{DD}	—
CVDD	SPI, eSDHC, USB Supply	E25	—	CV_{DD}	—

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
CVDD	SPI, eSDHC, USB Supply	E27	—	CV_{DD}	—
GVDD	DDR Supply	A2	—	GV_{DD}	—
GVDD	DDR Supply	B8	—	GV_{DD}	—
GVDD	DDR Supply	B11	—	GV_{DD}	—
GVDD	DDR Supply	C7	—	GV_{DD}	—
GVDD	DDR Supply	C9	—	GV_{DD}	—
GVDD	DDR Supply	D3	—	GV_{DD}	—
GVDD	DDR Supply	E7	—	GV_{DD}	—
GVDD	DDR Supply	F9	—	GV_{DD}	—
GVDD	DDR Supply	G10	—	GV_{DD}	—
GVDD	DDR Supply	H2	—	GV_{DD}	—
GVDD	DDR Supply	K3	—	GV_{DD}	—
GVDD	DDR Supply	K7	—	GV_{DD}	—
GVDD	DDR Supply	L2	—	GV_{DD}	—
GVDD	DDR Supply	L3	—	GV_{DD}	—
GVDD	DDR Supply	L4	—	GV_{DD}	—
GVDD	DDR Supply	N3	—	GV_{DD}	—
GVDD	DDR Supply	N6	—	GV_{DD}	—
GVDD	DDR Supply	P4	—	GV_{DD}	—
GVDD	DDR Supply	R2	—	GV_{DD}	—
GVDD	DDR Supply	U3	—	GV_{DD}	—
GVDD	DDR Supply	V5	—	GV_{DD}	—
GVDD	DDR Supply	W3	—	GV_{DD}	—
GVDD	DDR Supply	Y2	—	GV_{DD}	—
GVDD	DDR Supply	AA2	—	GV_{DD}	—
GVDD	DDR Supply	AA3	—	GV_{DD}	—
GVDD	DDR Supply	AA5	—	GV_{DD}	—
GVDD	DDR Supply	AA7	—	GV_{DD}	—
GVDD	DDR Supply	AB6	—	GV_{DD}	—
GVDD	DDR Supply	AD5	—	GV_{DD}	—
GVDD	DDR Supply	AD9	—	GV_{DD}	—
GVDD	DDR Supply	AE3	—	GV_{DD}	—

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
GVDD	DDR Supply	AF4	—	GV_{DD}	—
GVDD	DDR Supply	AG6	—	GV_{DD}	—
GVDD	DDR Supply	AG8	—	GV_{DD}	—
GVDD	DDR Supply	AJ2	—	GV_{DD}	—
LVDD	TSEC I/O Supply	Y23	—	LV_{DD}	—
LVDD	TSEC I/O Supply	AC21	—	LV_{DD}	—
LVDD	TSEC I/O Supply	AC25	—	LV_{DD}	—
LVDD	TSEC I/O Supply	AC27	—	LV_{DD}	—
LVDD	TSEC I/O Supply	AE23	—	LV_{DD}	—
LVDD	TSEC I/O Supply	AF21	—	LV_{DD}	—
LVDD	TSEC I/O Supply	AF25	—	LV_{DD}	—
LVDD	TSEC I/O Supply	AH27	—	LV_{DD}	—
LVDD	TSEC I/O Supply	AH29	—	LV_{DD}	—
SVDD_SRDS	SerDes Core Logic Supply	AG16	—	SV_{DD_SRDS}	—
SVDD_SRDS	SerDes Core Logic Supply	AH13	—	SV_{DD_SRDS}	—
SVDD_SRDS	SerDes Core Logic Supply	AH17	—	SV_{DD_SRDS}	—
SVDD_SRDS	SerDes Core Logic Supply	AJ11	—	SV_{DD_SRDS}	—
SVDD_SRDS	SerDes Core Logic Supply	AJ15	—	SV_{DD_SRDS}	—
SVDD_SRDS	SerDes Core Logic Supply	AJ19	—	SV_{DD_SRDS}	—
SGND_SRDS	SerDes Core Logic GND	AG12	—	—	—
SGND_SRDS	SerDes Core Logic GND	AG13	—	—	—
SGND_SRDS	SerDes Core Logic GND	AG14	—	—	—
SGND_SRDS	SerDes Core Logic GND	AG17	—	—	—
SGND_SRDS	SerDes Core Logic GND	AG18	—	—	—
SGND_SRDS	SerDes Core Logic GND	AG19	—	—	—
SGND_SRDS	SerDes Core Logic GND	AH11	—	—	—
SGND_SRDS	SerDes Core Logic GND	AH15	—	—	—
SGND_SRDS	SerDes Core Logic GND	AH19	—	—	—
SGND_SRDS	SerDes Core Logic GND	AJ13	—	—	—
SGND_SRDS	SerDes Core Logic GND	AJ17	—	—	—
XVDD_SRDS	SerDes Transceiver Supply	AD13	—	XV_{DD_SRDS}	—
XVDD_SRDS	SerDes Transceiver Supply	AD17	—	XV_{DD_SRDS}	—

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
XVDD_SRDS	SerDes Transceiver Supply	AE11	—	XV_{DD_SRDS}	—
XVDD_SRDS	SerDes Transceiver Supply	AE19	—	XV_{DD_SRDS}	—
XVDD_SRDS	SerDes Transceiver Supply	AF14	—	XV_{DD_SRDS}	—
XVDD_SRDS	SerDes Transceiver Supply	AF16	—	XV_{DD_SRDS}	—
XGND_SRDS	SerDes Transceiver GND	AD11	—	—	—
XGND_SRDS	SerDes Transceiver GND	AD19	—	—	—
XGND_SRDS	SerDes Transceiver GND	AE14	—	—	—
XGND_SRDS	SerDes Transceiver GND	AE16	—	—	—
XGND_SRDS	SerDes Transceiver GND	AF11	—	—	—
XGND_SRDS	SerDes Transceiver GND	AF12	—	—	—
XGND_SRDS	SerDes Transceiver GND	AF18	—	—	—
XGND_SRDS	SerDes Transceiver GND	AG10	—	—	—
OVDD	General I/O Supply	K23	—	—	—
OVDD	General I/O Supply	L25	—	—	—
OVDD	General I/O Supply	N27	—	—	—
OVDD	General I/O Supply	P25	—	—	—
OVDD	General I/O Supply	U27	—	—	—
OVDD	General I/O Supply	Y26	—	—	—
VDD	Core Supply	K11, K13, K15, K17, K19, L10, K10, K12, K14, K16, L20, K18, K20, N10, N20, M10, M20, R10, R20, P10, P20, U10, U20, T10, T20, W10, V10, V20, W20, Y11,Y12, Y19, Y18, Y20	—	—	—

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
GND	Ground	A1, A29, B5, B14, B27, C6, C8, C11, C18, C24, D16, D22, D25, E3, E28, F7, G5, G9, G21, H3, H27, J7, J23, K4,F17, L12,L14, L16, L18, M11, K25, L1, L11, L13, L15, L17, L19, M3, M4, M6, M19, M12, M13, M14, M15, M16, M17, M18, P11, M26, N2, N11, N12, N13, N14, N15, N16, N17, N18, N19, N28, P5, P19, P12, P13, P14, P15, P16, P17, P18, T11, P24, R3, R11, R12, R13, R14, R15, R16, R17, R18, R19, T6, T19, T12, T13, T14, T15, T16, T17, T18, V11, T27, U11, U12, U13, U14, U15, U16, U17, U18, U19, V4, V19, V12, V13, V14, V15, V16, V17, V18, W12, V27, W2, W4, W11, W13, W14, W15, W16, W17, W19, Y3, Y6, Y7, W18, Y13, Y17, Y25, AA6, AA23, AC3, AC10, AC20, AC24, AC28, AD3, AD6, AE9, AF20, AG3, AG5, AG7, AG24, AG27, AJ1, AJ29, AH10, AJ10, AD10	—	—	—
Analog					
SD_IMP_CAL_RX	SerDes Rx Impedance Calibration	AG11	I	XV_{DD}	27
SD_IMP_CAL_TX	SerDes Tx Impedance Calibration	AF19	I	XV_{DD}	27
SD_PLL_TPA	SerDes PLL Test Point Analog	AD16	O	XV_{DD}	12
SD_PLL_TPD	SerDes PLL Test Point Digital	AE15	O	XV_{DD}	12
MVREF	SSTL_1.5/1.8 Reference Voltage	R6	—	$GV_{DD} \div 2$	—
Temp_Anode	Temp_Anode	E16	I	Internal Diode	35
Temp_Cathode	Temp_Cathode	E15	O	Internal Diode	35

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes

Note:

1. All multiplexed signals are listed only once and do not reoccur.
2. It is recommended that a weak pull-up resistor (2–10 KΩ) be placed on this pin to OV_{DD}.
3. Open drain signal. GPIO pins may be programmed to operate as open-drain outputs.
4. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. If the signal is intended to be high after reset and if there is any device on the net which might pull down the value of the net at reset, a pullup or active driver is needed.
5. The value of LA[29:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors.
6. The value of LALE, LGPL[02], LBCTL at reset set the e500 core0 clocks to CCB Clock PLL ratios. These pins require 4.7-kΩ pull-up or pull-down resistors.
7. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin is therefore described as an I/O for boundary scan.
8. If this pin is configured for local bus controller use, pull up with 2–10 KΩ resistor to BVDD to ensure there is no random chip select assertion due to possible noise or other causes.
9. This output is actively driven during reset rather than being three-stated during reset.
10. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
11. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a high state during reset.
12. Do not connect.
13. Independent supply derived from board VDD.
14. It is recommended that a pull-up resistor (~1 kΩ) be placed on this pin to OVDD.
15. The following pins must NOT be pulled down during power-on reset: $\overline{\text{DMA1\_DACK[00]}}$, LA[17], USB1_STP, TSEC2_TXD[06], $\overline{\text{HRESET\_REQ}}$, MSRCID[2:3], MDVAL, ASLEEP.
16. TSEC2_TXD[05] is a POR configuration pin for eSDHC card-detect (cfg_sdhc_cd_pol_sel), and it also has an alternate function of TSEC3_TX_EN. When eTSEC1 or eTSEC2 or eTSEC3 are used as parallel interfaces, the TSECx_TX_EN pins require an external 4.7-k pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven. However, the pull-down resistor on TSEC3_TX_EN causes the eSDHC card-detect (cfg_sdhc_cd_sel) to be inverted; the inversion should be overridden from the SDHCDCR[CD_INV] debug control register. If the device is configured to boot from the eSDHC interface, the SDHC_CD should be inverted on the board.
17. TSEC2_TXD[01] is used as cfg_dram_type. It must be valid at power up.
18. For DDR2 MDIC[00] is grounded through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor and MDIC[01] is connected to GVDD through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs. The calibration resistor value for DDR3 must be 20-Ω (full-strength mode), or 40.2-Ω (half-strength mode).

Table 1. P2010 Pinout Listing (continued)[1]

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes

19. DDRCLK input is only required when the P2010 DDR controller is running in asynchronous mode. See Section 4.2.2, “Clock Signals”, Section 4.4.3.2, “DDR PLL Ratio” and Table 4-10, “DDR Complex Clock PLL Ratio,” in the *P2020 QorIQ Integrated Communications Host Processor Family Reference Manual*
20. EC_GTX_CLK125 is a 125-MHz input clock shared among all eTSEC ports in the following modes: GMII, TBI, RGMII and RTBI. If none of the eTSEC ports is operating in these modes, the EC_GTX_CLK125 input can be tied off to GND. The EC_GTX_CLK125 signal high level is nominally LVDD.
21. These POR configuration inputs may be used in the future to control functionality. It is advised that boards are built with the ability to pulldown these pins.LA[20:22], UART_SOUT[00], MSRCID[01], MSRCID[04], and $\overline{\text{DMA1\_DDONE}}$[00] are reserved for future reset configuration.
22. Incorrect settings can lead to irreversible device damage.
23. The value of LAD[0:15] during reset sets the upper 16 bits of the GPPORCR as a user option setting.
24. Used to set the DDR clock PLL settings; requires a 4.7-kΩ pull-up or pull-down resistor.
25. Used to determine CPU boot configuration; requires a 4.7-kΩ pull-up or pull-down resistor.
26. Pin must be the same voltage as V_{DD}.
27. SD_IMP_CAL_RX is grounded through an 200-Ω precision ±1% resistor and SD_IMP_CAL_TX is grounded through an 100-Ω precision ±1% resistor.
30. Requires a pull down with 100~1K to GND
31. 100K pull down needed if this signal is used as a CD pin for SD cards. The pull down is not needed for MMC cards.
32. All unused MCK pins must be disabled via DDRCLKDR register.
33. This pin requires a 1 kΩ pull up to OV_{DD}.
34. For systems that boot from local bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pullup on LGPL4 is required.
35. These pins may be connected to a thermal diode monitoring device such as the ADT7461A. If a thermal diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.
36. This pin, if not used, must be pulled high or low via individual 2–10 kΩ resistor.
37. This pin must be pulled high or low via a 2–10 kΩ resistor.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the device. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the DC ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 2 provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Parameter		Symbol	Max Value	Unit	Notes
Core and platform supply voltage		V_{DD}	–0.3 to 1.1	V	—
PLL supply voltage		AV_{DD}_CORE0 AV_{DD}_DDR, AV_{DD}_LBIU, AV_{DD}_PLAT, AV_{DD}_SRDS	–0.3 to 1.1	V	2
Core power supply for SerDes transceivers		SV_{DD}_SRDS	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers		XV_{DD}_SRDS	–0.3 to 1.1	V	—
DDR2/3 DRAM I/O voltage		GV_{DD}	–0.3 to 1.98 –0.3 to 1.65	V	—
Three-speed Ethernet I/O, MII management voltage		LV_{DD}(eTSEC)	–0.3 to 3.63 –0.3 to 2.75	V	—
DUART, system control and power management, I^2C, GPIOx8, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	3
USB, eSPI, eSDHC		CV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	3
Enhanced local bus I/O voltage and GPIOx8 voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	3
Input voltage	DDR2/DDR3 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2/DDR3 DRAM reference	MV_{REF}	–0.3 to ($GV_{DD/2}$ + 0.3)	V	3
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	3, 4
	Enhanced local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	V	—
	DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
	SerDes	XV_{IN}	–0.3 to (XV_{DD} + 0.3)	V	—
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. AV_{DD} is measured at the input to the filter and not at the pin of the device.
3. **Caution:** (B,M,L,O,C, X)V_{IN} must not exceed (B,G,L,O, C,X)V_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

2.1.2 Recommended Operating Conditions

Table 3 provides the recommended operating conditions for this device. Note that the values in Table 3 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

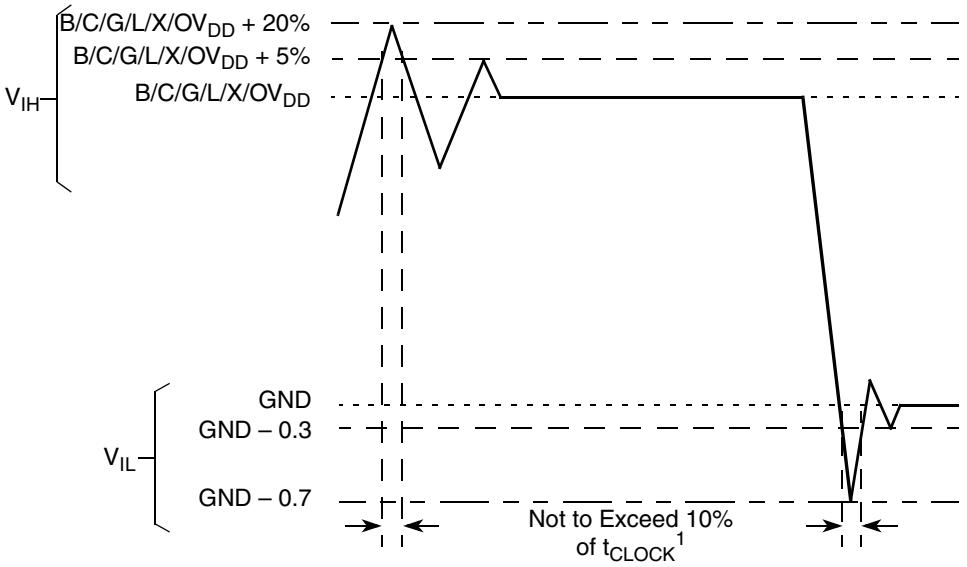
Parameter		Symbol	Recommended Value	Unit	Notes
Core and platform supply voltage		V_{DD}	1.05 ± 50 mV	V	1
PLL supply voltage		AV_{DD}_CORE0 AV_{DD}_CORE1 AV_{DD}_DDR, AV_{DD}_LBIU, AV_{DD}_PLAT, AV_{DD}_SRDS	1.05 ± 50 mV	V	—
Core power supply for SerDes transceivers		SV_{DD} _SRDS	1.05 ± 50 mV	V	—
Pad power supply for SerDes transceivers and PCI Express		XV_{DD}_SRDS	1.05 ± 50 mV	V	—
DDR2 DRAM I/O voltage		GV_{DD}	1.8 V ± 100 mV	V	—
DDR3 DRAM I/O voltage		GV_{DD}	1.5 V ± 75 mV	V	—
Three-speed Ethernet I/O voltage (eTSEC)		LV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
DUART, system control and power management, I^2C, GPIOx8, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
Enhanced local bus I/O and GPIOx8 voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
USB, eSPI, eSDHC I/O voltage		CV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	4
Input voltage	DDR2/3 DRAM signals	MV_{IN}	GND to GV_{DD}	V	—
	DDR2 DRAM reference	MV_{REF}	GV_{DD}/2	V	—
	DDR3 DRAM reference	MV_{REF}	GV_{DD}/2	V	—
	Three-speed Ethernet signals	LV_{IN}	GND to LV_{DD}	V	—
	Enhanced local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	—
	USB, eSPI, eSDHC	CV_{IN}	GND to CV_{DD}	V	—
	SerDes signals	XV_{IN}	GND to XV_{DD}	V	—

Table 3. Recommended Operating Conditions (continued)

Parameter		Symbol	Recommended Value	Unit	Notes
Operating Temperature range	Commercial	T_A T_J	T_A= 0 (min) to T_J= 125 (max)	°C	3
	Industrial	T_A T_J	T_A= –40 (min) to T_J= 125 (max)	°C	3

Notes:
1. **Caution:** (B,M,L,O,C, X)VIN must not exceed (B,G,L,O, C,X)VDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
2. **Caution:** Until V_{DD} reaches its recommended operating voltage, if L/C/B/G/OV_{DD} exceeds V_{DD} extra current may be drawn by the device.
3. Minimum temperature is specified with T_A; maximum temperature is specified with T_J.
4. CV_{DD} for eSDHC is limited for 3.3, 2.5, and 1.8 V

Figure 7 shows the undershoot and overshoot voltages at the interfaces of the device.



Note:
1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
   For eLBC, t_{CLOCK} references LCLK.
   For SerDes XV_{DD}, t_{CLOCK} references SD_REF_CLK.

Figure 7. Overshoot/Undershoot Voltage for BV_{DD}/CV_{DD}/GV_{DD}/LV_{DD}/XV_{DD}/OV_{DD}

The core voltage must always be provided at nominal 1.05 V (see Table 3 for actual recommended core voltage.) Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The SDRAM interface uses a differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD} \div 2$). The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.3 Output Driver Characteristics

Table 4 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage	Notes
Enhanced local bus interface, GPIO[0:7]	45 45 45	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	—
DDR2 signal (programmable)	18 (full-strength mode) 36 (half-strength mode)	GV_{DD} = 1.8 V	1
DDR 3 signal (programmable)	20 (full-strength mode) 40 (half-strength mode)	GV_{DD} = 1.5 V	1
eTSEC signals	45	LV_{DD} = 2.5/3.3 V	—
DUART, system control, JTAG	45	OV_{DD} = 3.3 V	—
I^2C	45	OV_{DD} = 3.3 V	—
USB, eSPI, eSDHC	45	CV_{DD} = 3.3 V CV_{DD} = 2.5 V CV_{DD} = 1.8 V	—

Note:
1. The drive strength of the DDR2/3 interface in half-strength mode is at T_J = 105 °C and at GV_{DD} (min).

2.2 Power Sequencing

The device. requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, AV_{DD}, BV_{DD}, LV_{DD}, CV_{DD}, OV_{DD}, SV_{DD_SRDS}, and XV_{DD_SRDS}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

NOTE

While V_{DD} is ramping, current may be supplied from V_{DD} through the device to GV_{DD}. Nevertheless, GV_{DD} from an external supply should follow the sequencing described above.

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power up, and extra current may be drawn by the device.

WARNING

Only 100,000 POR cycles are permitted per lifetime of a device.

2.3 Power Characteristics

The estimated typical core power consumption for the core complex bus (CCB) versus the core frequency for this family of QorIQ devices is shown in Table 5.

Table 5. P2010 Core Power Consumption

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V_{DD} (V)	Junction Temperature (°C)	Power (W)	Notes
Thermal	800	400	1.05	125	4.7	1, 2
Maximum					5.7	1, 3
Thermal	1000	500	1.05	125	4.9	1, 2
Maximum					6.0	1, 3
Thermal	1200	600	1.05	125	5.1	1, 2
Maximum					6.3	1, 3
Thermal	1333	667	1.05	125	5.4	1, 2
Maximum					6.7	1, 3

Notes:
1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Thermal power is the maximum power measured at nominal core voltage (V_{DD}_Core_*n*) and maximum operating junction temperature (see Table 3) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.
3. Maximum power is the maximum power measured at nominal core voltage (V_{DD}) and maximum operating junction temperature (see Table 3) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units busy at with one core at 100% efficiency and a typical workload on platform interfaces.
4. This table includes power numbers for the V_{DD} and AV_{DD}_*n* rails

2.3.1 I/O DC Power Supply Recommendation

Table 6 provides estimated I/O power numbers for each block: DDR, PCI Express, eLBC, eTSEC, serial RapidIO, SGMII, eSDHC, USB, eSPI, DUART, I^2C and GPIO.

Table 6. I/O Power Supply Estimated Values

Interface	Parameter	Symbol	Typical	Maximum	Unit	Notes
DDR2	400 MHz data rate	GV_{DD} (1.8 V)	0.7	1.0	W	1, 2, 3
	533 MHz data rate	GV_{DD} (1.8 V)	0.9	1.25	W	1, 2, 3
	667 MHz data rate	GV_{DD} (1.8 V)	1.1	1.6	W	1, 2, 3
DDR3	667 MHz data rate	GV_{DD} (1.5 V)	0.7	1.1	W	1, 2, 3
	800 MHz data rate	GV_{DD} (1.5 V)	0.8	1.2	W	1, 2, 3, 4
PCI Express	×1, 2.5 G-baud	XV_{DD} (1.05 V)	0.15	0.15	W	1, 2, 3
	×2, 2.5 G-baud	XV_{DD} (1.05 V)	0.21	0.21	W	1, 2, 3
	×4, 2.5 G-baud	XV_{DD} (1.05 V)	0.32	0.32	W	1, 2, 3

Table 6. I/O Power Supply Estimated Values (continued)

Interface	Parameter	Symbol	Typical	Maximum	Unit	Notes
Serial RapidIO	×1, 2.5 G-baud	XV_{DD} (1.05 V)	0.18	0.18	W	1, 2, 3
	×4, 2.5 G-baud	XV_{DD} (1.05 V)	0.39	0.39	W	1, 2, 3
SGMII	×1, 1.25G-baud	XV_{DD} (1.05 V)	0.1	0.2	W	1, 2, 3
eLBC	16-bit, 75 MHz	BV_{DD} (1.8 V)	0.05	0.09	W	1, 2, 3
		BV_{DD} (2.5 V)	0.08	0.13	W	1, 2, 3
		BV_{DD} (3.3 V)	0.11	0.20	W	1, 2, 3
eTSEC	MII, GMII, RGMII, RTBI, RMII, TBI, 1588	LV_{DD} (2.5 V)	0.07	0.15	W	1, 2, 3, 5
	MII, GMII, TBI, RMII, 1588	LV_{DD} (3.3 V)	0.11	0.20	W	1, 2, 3, 5
eSDHC	—	CV_{DD} (3.3 V)	0.03	0.04	W	1, 2, 3
		CV_{DD} (2.5 V)	0.02	0.03	W	1, 2, 3
		CV_{DD} (1.8 V)	0.01	0.02	W	1, 2, 3
USB	—	CV_{DD} (3.3 V)	0.05	0.06	W	1, 2, 3
		CV_{DD} (2.5 V)	0.04	0.05	W	1, 2, 3
		CV_{DD} (1.8 V)	0.02	0.03	W	1, 2, 3
eSPI	—	CV_{DD} (3.3 V)	0.03	0.04	W	1, 2, 3
		CV_{DD} (2.5 V)	0.02	0.03	W	1, 2, 3
		CV_{DD} (1.8 V)	0.01	0.02	W	1, 2, 3
I^2C	—	OV_{DD} (3.3 V)	0.01	0.02	W	1, 2, 3
DUART	—	OV_{DD} (3.3 V)	0.01	0.02	W	1, 2, 3
GPIO [0:7]	×8	OV_{DD} (3.3 V)	0.01	0.02	W	1, 2, 3, 6
GPIO [8:15]	×8	BV_{DD} (1.8 V)	0.01	0.02	W	1, 2, 3, 6
		BV_{DD} (2.5 V)	0.01	0.02	W	1, 2, 3, 6
		BV_{DD} (3.3 V)	0.01	0.02	W	1, 2, 3, 6

Notes:

1.The maximum value is dependent on actual use case such as what application, external components used, environmental conditions such as temperature voltage and frequency. This is not intended to be the maximum guaranteed current. Depending on use case different result is expected.

2. The typical value are estimates based on simulations at nominal recommended core voltage (V_{DD}) and assuming 65 C junction temperature.

3. The maximum value are estimates based on simulations at nominal recommended core voltage (V_{DD}) and assuming 105 C junction temperature.

4. 800 Mbps data rate only supported on DDR3.

5. The current values are per each eTSEC used.

6. GPIO ×8 support on OVDD and ×8 on BVDD rail supply.

2.4 Input Clocks

This section discusses the parameters for the input clocks.

2.4.1 System Clock Timing

Table 7 provides the system clock (SYSCLK) DC specifications for the device.

Table 7. SYSCLK DC Electrical Characteristics (OV_{DD} = 3.3 V ± 165 mV)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
High-level input voltage	V_{IH}	2.0	—	—	V	1
Low-level input voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DD})	I_{IN}	—	—	±50	μA	2

Note:

1. The max V_{IH}, and min V_{IL} values can be found in Table 3
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3

Table 8 provides the system clock (SYSCLK) AC timing specifications for the device.

Table 8. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	64.00	—	100	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	10	—	15.6	ns	1, 2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	±150	ps	—
SYSCLK jitter phase noise at –56 dBc	—	—	—	500	KHz	4
AC input swing limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Notes:

1. **Caution:** The CCB_clk to SYSCLK ratio and e500 core to CCB_clk ratio settings must be chosen such that the resulting SYSCLK frequency, e500 core frequency, and CCB_clk frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD} \div 2$.
3. Slew rate as measured from ±0.3 ΔV_{AC} at center of peak-to-peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.4.2 SYSCLK and Spread Spectrum Source Recommendations

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle

output jitter should meet the device input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the device is compatible with spread spectrum sources if the recommendations listed in Table 9 are observed.

Table 9. SYSCLK Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 3.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Note:

1. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device

CAUTION

The processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

2.4.3 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal must be greater than 2× the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

2.4.4 eTSEC Gigabit Reference Clock Timing

Table 10 provides the eTSEC gigabit reference clocks DC electrical characteristics.

Table 10. eTSEC Gigabit Reference Clock DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	—	V	1
Low-level input voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±40	μA	2

Note:

1. The max V_{IH}, and min V_{IL} values can be found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

Table 11 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the device.

Table 11. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—

Table 11. EC_GTX_CLK125 AC Timing Specifications (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2

Notes:
1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V, and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 2.10.2.5, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

2.4.5 DDR Clock Timing

Table 7 provides the system clock (DDRCLK) DC specifications for the device.

Table 12. DDRCLK DC Electrical Characteristics (OV_{DD} = 3.3 V ± 165 mV)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
High-level input voltage	V_{IH}	2.0	—	OV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	—	0.8	V	—
Input capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	—	±50	μA	1

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

Table 13 provides the DDR clock (DDRCLK) AC timing specifications for the device.

Table 13. DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	66.7	—	100	MHz	1, 2
DDRCLK cycle time	t_{DDRCLK}	10	—	15	ns	1, 2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	—	60	%	2
DDRCLK slew rate	—	1	—	4	V/ns	3
DDRCLK peak period jitter	—	—	—	±150	ps	—
DDRCLK jitter phase noise at –56 dBc	—	—	—	500	KHz	4

Table 13. DDRCLK AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Notes:

1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD} \div 2$.
3. Slew rate as measured from $\pm 0.3\ \Delta V_{AC}$ at center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes and eTSEC, see their specific sections in this document.

2.5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the device. Table 14 provides the RESET initialization AC timing specifications.

Table 14. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	μs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	μs	—
Input setup time for POR configurations (other than PLL configuration) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configurations (including PLL configuration) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1, 2

Note:

1. SYSCLK is the primary clock input for the device.
2. HRESET should have a rise time of no more than one SYSCLK cycle.

Table 15 provides the PLL lock times.

Table 15. PLL Lock Times

Parameter	Min	Max	Unit	Notes
Core PLL lock times	—	100	μs	—
Platform PLL lock time	—	100	μs	—
DDR PLL lock times	—	100	μs	—
Enhanced local bus PLL	—	100	μs	—

2.6 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum Power-On Ramp Rate is required to avoid falsely triggering the ESD circuitry. Table 16 provides the power supply ramp rate specifications.

Table 16. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OVDD/CVDD/ GVDD/BVDD/SVDD/LVDD, All VDD supplies, MVREF and all AVDD supplies.)	—	36000	Volts/Sec	1, 2

Note:
1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (e.g. exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range Table 3.

2.7 DDR2 and DDR3 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the device. DDR2 and DDR3 share the same AC timing specifications. Note that DDR2 SDRAM is GV_{DD}(typ) = 1.8 V and DDR3 SDRAM is GV_{DD}(typ) = 1.5 V.

2.7.1 DDR2 and DDR3 SDRAM Interface DC Electrical Characteristics

Table 17 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR2 SDRAM.

Table 17. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V[1]

Parameter	Symbol	Min	Max	Unit	Notes
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MV_{REF} + 0.125	—	V	5
Input low voltage	V_{IL}	—	MV_{REF} – 0.125	V	5
Output high current (V_{OUT} = 1.370 V)	I_{OH}	—	–13.4	mA	6
Output low current (V_{OUT} = 0.330 V)	I_{OL}	13.4	—	mA	6
Output leakage current	I_{OZ}	–50	50	μA	7

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed the MV_{REF} DC level by more than ±1% of GV_{DD} (for example, ±18 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. The voltage regulator for MVREFn must be able to supply up to 1500 μA.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Refer to the IBIS model for the complete output IV curve characteristics.
7. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 18 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 18. DDR3 SDRAM Interface DC Electrical Characteristics for GV_{DD}(typ) = 1.5 V[1]

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MV_{REF} + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MV_{REF} – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed the MV_{REF} DC level by more than ±1% of GV_{DD} (for example, ±15 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREFn with a min value of MVREFn – 0.04 and a max value of MVREFn + 0.04. V_{TT} should track variations in the DC level of MVREFn.
4. The voltage regulator for MVREFn must be able to supply up to125 μA current.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 19 provides the DDR Controller interface capacitance for DDR2 and DDR3.

Table 19. DDR2 DDR3 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V and 1.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1, 2

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.1 V (for DDR2), f = 1 MHz, T_A = 25 °C, V_{OUT} = GV_{DD} ÷ 2, V_{OUT} (peak-to-peak) = 0.2 V.
2. This parameter is sampled. GV_{DD} = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, T_A = 25 °C, V_{OUT} = GV_{DD} ÷ 2, V_{OUT} (peak-to-peak) = 0.150 V.

Table 20 provides the current draw characteristics for MV_{REF}.

Table 20. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for DDR2 SDRAM for MV_{REF}	MV_{REF}	—	1500	μA	1
Current draw for DDR3 SDRAM for MV_{REF}	MV_{REF}	—	1250	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 1500 μA current.

2.7.2 DDR2 and DDR3 SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that the required GV_{DD}(typ) voltage is 1.8 V or 1.5 V when interfacing to DDR2 or DDR3 SDRAM respectively.

2.7.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

Table 21, Table 22, and Table 23 provide the input AC timing specifications for the DDR controller.

Table 21. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions (see Table 3).

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	> 533 Mbps data rate	V_{ILAC}	—	MV_{REF} – 0.20	V	—
	≤ 533 Mbps data rate		—	MV_{REF} – 0.25		—
AC input high voltage	> 533 Mbps data rate	V_{IHAC}	MV_{REF} + 0.20	—	V	—
	≤ 533 Mbps data rate		MV_{REF} + 0.25	—		—

Table 22. DDR3 SDRAM Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions (see Table 3).

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.175	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.175	—	V	—

Table 23. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions (see Table 3).

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1, 2
800 Mbps data rate		–350	350	ps	1, 2
667 Mbps data rate		–390	390	ps	1, 2
533 Mbps data rate		–450	450	ps	1, 2
400 Mbps data rate		–515	515	ps	1, 2
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}	—	—	ps	1, 2
800 Mbps data rate		–275	275	ps	1, 2
667 Mbps data rate		–360	360	ps	1, 2
533 Mbps data rate		–488	488	ps	1, 2
400 Mbps data rate		–735	735	ps	1, 2

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[*n*] and any corresponding bit that is captured with MDQS[*n*]. This must be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm (T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

Figure 8 shows the DDR2 and DDR3 SDRAM interface input timing diagram.

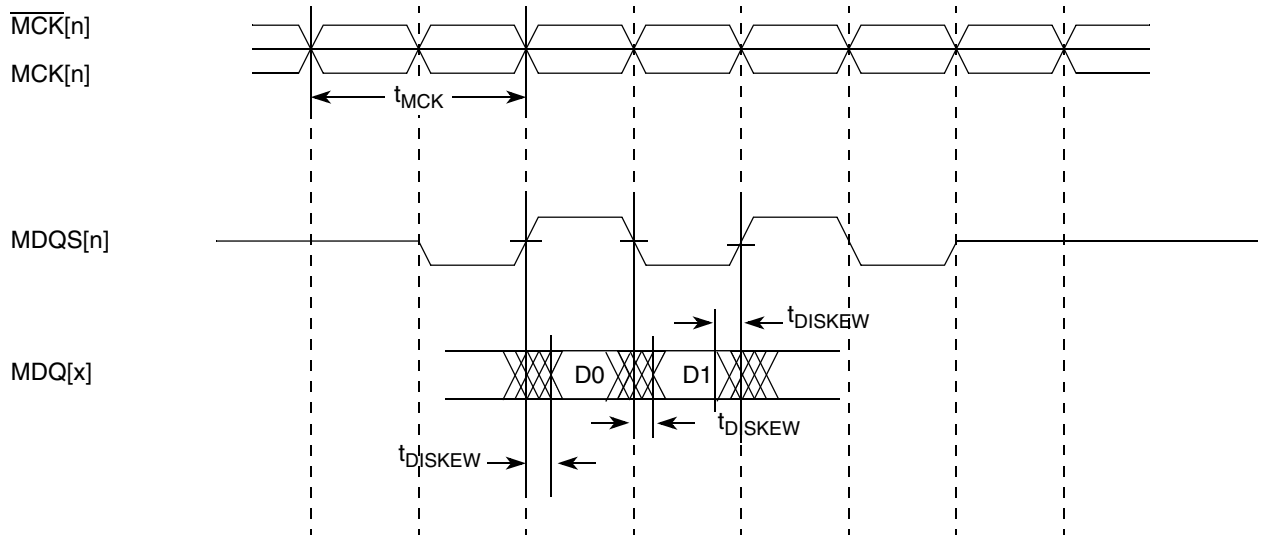


Figure 8. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

2.7.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

Table 24 contains the output AC timing targets for the DDR SDRAM interface.

Table 24. DDR2 and DDR3 SDRAM Output AC Timing Specifications

At recommended operating conditions (see Table 3).

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[*n*] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	
800 Mbps data rate		0.767	—		3, 7
667 Mbps data rate		.950	—		3
533 Mbps data rate		1.33	—		3, 4
400 Mbps data rate		1.8	—		3, 4
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	
800 Mbps data rate		0.767	—		3, 7
667 Mbps data rate		.950	—		3
533 Mbps data rate		1.33	—		3, 4
400 Mbps data rate		1.8	—		3, 4
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	
800 Mbps data rate		0.767	—		3, 7
667 Mbps data rate		.950	—		3
533 Mbps data rate		1.33	—		3, 4
400 Mbps data rate		1.8	—		3, 4

Table 24. DDR2 and DDR3 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol[1]	Min	Max	Unit	Notes
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	
800 Mbps data rate		0.767	—		3, 7
667 Mbps data rate		.950	—		3
533 Mbps data rate		1.33	—		3, 4
400 Mbps data rate		1.8	—		3, 4
MCK to MDQS Skew	t_{DDKHMH}			ns	
800 Mbps data rate		–0.525	0.525		5, 7
667 Mbps data rate		–0.600	0.600		5
533 Mbps data rate		–0.600	0.600		4, 5
400 Mbps data rate		–0.600	0.600		4, 5
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	
800 Mbps data rate		225	—		6, 7
667 Mbps data rate		300	—		6
533 Mbps data rate		388	—		4, 6
400 Mbps data rate		550	—		4, 6
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	
800 Mbps data rate		225	—		6, 7
667 Mbps data rate		300	—		6
533 Mbps data rate		388	—		4, 6
400 Mbps data rate		550	—		4,6
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ and MDQS/$\overline{\text{MDQS}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that minimum data rate for DDR3 is 667 MHz.
5. t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *P2010 QorIQ Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe must be centered inside of the data eye at the pins of the microprocessor.
7. DDR3 only.

NOTE

For the ADDR/CMD setup and hold specifications in Table 24, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

Figure 9 shows the DDR2 and DDR3 SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

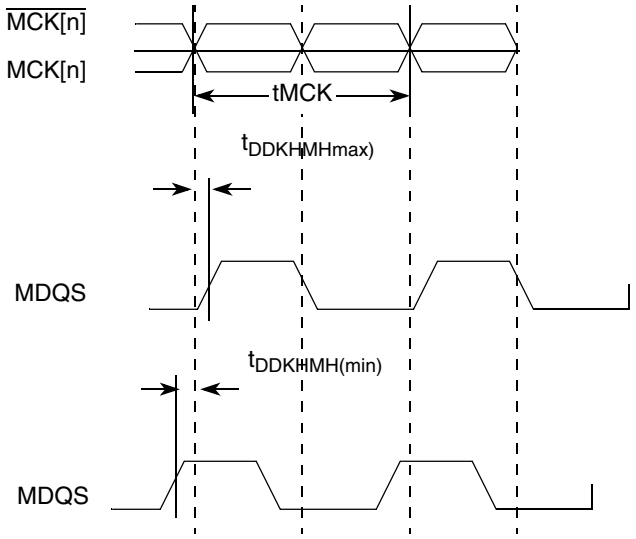


Figure 9. Timing Diagram for t_{DDKHMH}

Figure 10 shows the DDR SDRAM output timing diagram.

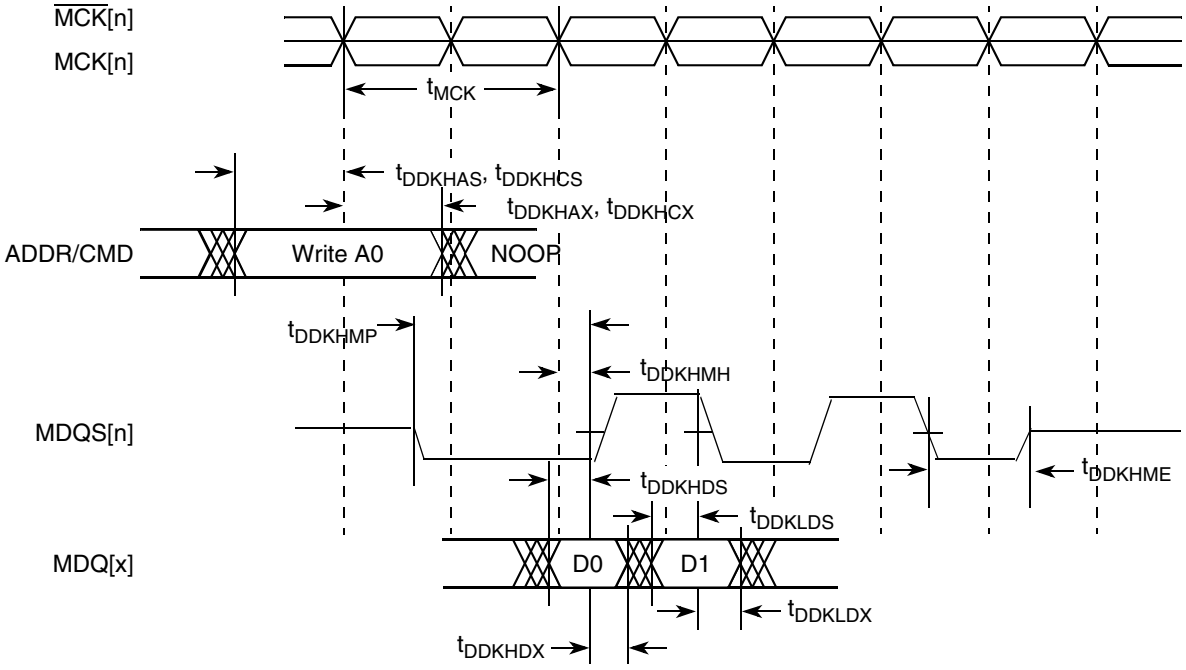


Figure 10. DDR2 and DD3 SDRAM Output Timing Diagram

Figure 11 provides the AC test load for the DDR bus.

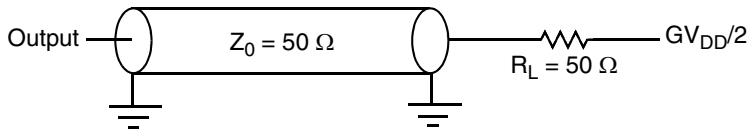


Figure 11. DDR AC Test Load

2.8 eSPI

This section describes the DC and AC electrical specifications for the eSPI.

2.8.1 eSPI DC Electrical Characteristics

Table 25 provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 3.3 V.

Table 25. SPI DC Electrical Characteristics (3.3 V)

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	2	—	V	1
Low-level input voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±70	μA	2
High-level output voltage (CV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (CV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

Table 26 provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 2.5 V.

Table 26. SPI DC Electrical Characteristics (2.5 V)

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	1.7	—	V	1
Low-level input voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±70	μA	2
High-level output voltage (CV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Low-level output voltage (CV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

Table 27 provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 1.8 V.

Table 27. SPI DC Electrical Characteristics (1.8 V)

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	1.25	—	V	1
Low-level input voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±70	μA	2
High-level output voltage (CV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Low-level output voltage (CV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions”

2.8.2 eSPI AC Timing Specifications

Table 28 provides the eSPI input and output AC timing specifications.

Table 28. eSPI AC Timing Specifications[1]

Characteristic	Symbol	Min	Max	Unit	Note
SPI_MOSI output—Master data (internal clock) hold time	t_{NIKHOX} t_{NIKHOX}	0.5 3.0	— —	ns	1, 2, 3
SPI_MOSI output—Master data (internal clock) delay	t_{NIKHOV} tNIKHOV	—	6.0 10	ns	1, 2, 3
SPI_CS outputs—Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	1, 2
SPI_CS outputs—Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	1, 2
SPI inputs—Master data (internal clock) input setup time	t_{NIIVKH}	5.75	—	ns	4
SPI inputs—Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	4

Notes:

1. Output specifications are measured from the 50% level of the CLK to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
3. The greater of the two output timings for t_{NIKHOX} and t_{NIKHOV} are used when the SPCOM[RxDelay] bit of eSPI Command Register is set. For example, the t_{NIKHOX} is 3.0ns and t_{NIKHOV} is 10ns if SPCOM[RxDelay] is set.
4. For Windbond Flash dual-output mode both SPI_MOSI and SPI_MISO are inputs.

Figure 12 provides the AC test load for the eSPI.

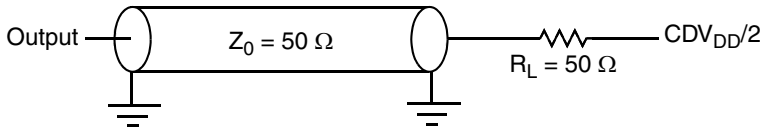
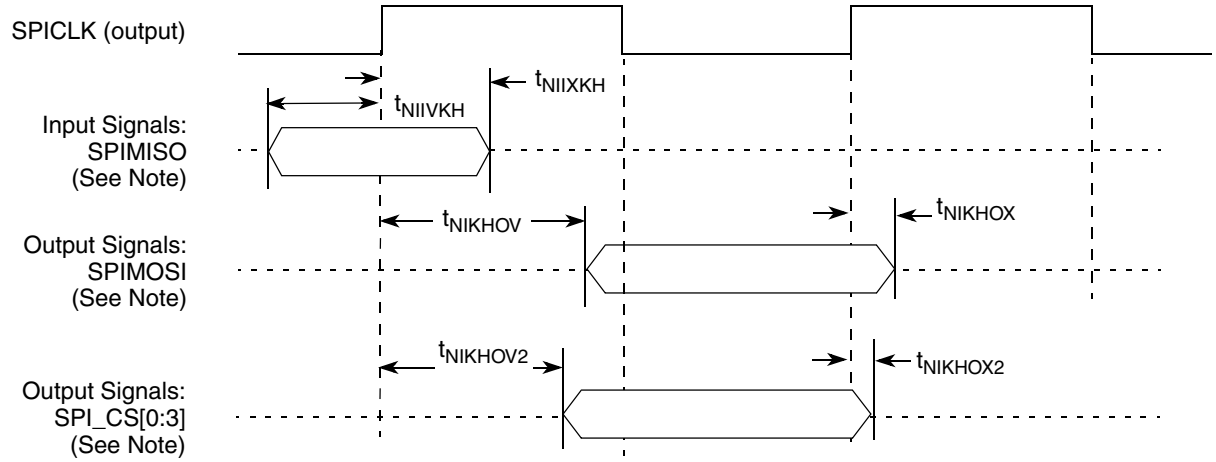


Figure 12. eSPI AC Test Load

Figure 13 represents the AC timing from Table 28. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 13 shows the eSPI timing in master mode (internal clock).



Note: The clock edge is selectable on eSPI.

Figure 13. eSPI AC Timing in Master Mode (Internal Clock) Diagram

2.9 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the device.

2.9.1 DUART DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the DUART interface.

Table 29. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	2	—	V	1
Low-level input voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = GND or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—

Table 29. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Low-level output voltage (OV_{DD} = min, I_{OL} = 2mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 2 and Table 3.

2.9.2 DUART AC Electrical Specifications

Table 30 provides the AC timing parameters for the DUART interface.

Table 30. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	CCB clock/1,048,576	baud	1
Maximum baud rate	CCB clock/16	baud	1, 2

Notes:
1. CCB clock refers to the platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.

2.10 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed Ethernet controller, and MII management.

2.10.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)— GMII/SGMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to the following interfaces:

- All gigabit media independent interface (GMII)
- Serial gigabit media independent interface (SGMII)
- Media independent interface (MII)
- Ten-bit interface (TBI)
- Reduced gigabit media independent interface (RGMII)
- Reduced ten-bit interface (RTBI)
- Reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC).

The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII, MII, RMII, and TBI interfaces can be operated at 3.3 or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with IEEE Std 802.3™.

The interfaces conform to specifications, as follows:

- SGMII interfaces conform (with exceptions) to the *Serial Gigabit Media-Independent Interface (SGMII) Specification, Version 1.8*.

- RGMII and RTBI interfaces conform to the *Reduced Gigabit Media-Independent Interface (RGMII) Specification, Version 1.3* (12/10/2000).
- The RMII interface conforms to the *RMII Consortium RMII Specification, Version 1.2* (3/20/1998).

The electrical characteristics for MDIO and MDC are specified in Section 2.10.7, "Ethernet Management Interface Electrical Characteristics."

2.10.1.1 IEEE 1588, GMII, MII, TBI, RGMII, RMII, and RTBI DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 31 and Table 32. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 31. IEEE 1588, GMII, MII, RMII, and TBI DC Electrical Characteristics at LV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (LV_{DD} = min, I_{OH} = –4.0 mA)	V_{OH}	2.40	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 4.0 mA)	V_{OL}	—	0.40	V	—
Input high voltage (IEEE 1588, MII, RMII and TBI)	V_{IH}	2.0	—	V	—
Input high voltage (GMII)	V_{IH}	1.90	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	40	μA	1
Input low current (V_{IN} = GND)	I_{IL}	–40	—	μA	1

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

Table 32. IEEE 1588, GMII, MII, RMII, RGMII, RTBI, and TBI DC Electrical Characteristics at LV_{DD} = 2.5 V

Parameters	Symbol	Min	Max	Unit	Notes
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD}= min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.70	V	—
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	40	μA	—
Input low current (V_{IN} = GND)	I_{IL}	–40	—	μA	1

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

2.10.2 GMII,MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

2.10.2.1 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

2.10.2.1.1 GMII Transmit AC Timing Specifications

Table 33 provides the GMII transmit AC timing specifications.

Table 33. GMII Transmit AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.5	ns	1
GTX_CLK data clock rise time (20%–80%)	t_{GTXR}	—	—	1.0	ns	—
GTX_CLK data clock fall time (80%–20%)	t_{GTXF}	—	—	1.0	ns	—

Note:
1. Data valid minimum setup time, t_{gtkhdv}, is a function of clock and maximum hold time (min setup = cycle time – max delay).

Figure 14 shows the GMII transmit AC timing diagram.

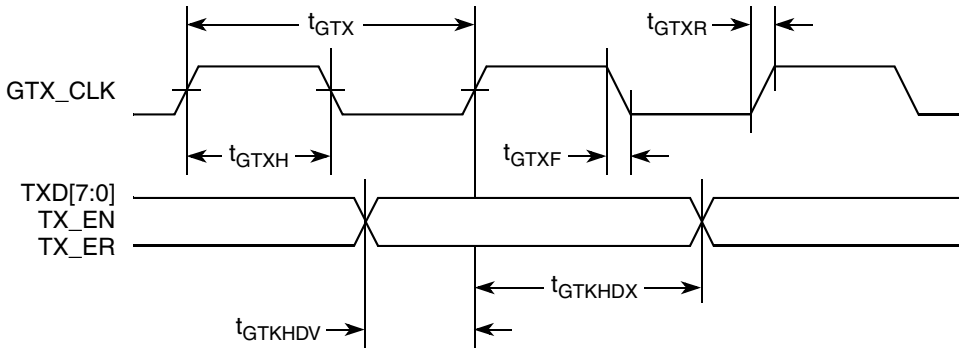


Figure 14. GMII Transmit AC Timing Diagram

2.10.2.1.2 GMII Receive AC Timing Specifications

Table 34 provides the GMII receive AC timing specifications.

Table 34. GMII Receive AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period	t_{GRX}	7.5	—	—	ns	1
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	65	%	2
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0	—	—	ns	—
RX_CLK clock rise (20%–80%)	t_{GRXR}	—	—	1.0	ns	2
RX_CLK clock fall time (80%–20%)	t_{GRXF}	—	—	1.0	ns	2

Note:
1. The frequency of RX_CLK should not exceed frequency of gigabit Ethernet reference clock by more than 300 ppm.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

Figure 15 provides the AC test load for eTSEC.

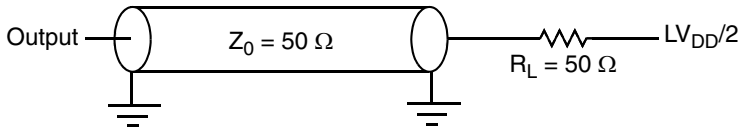


Figure 15. eTSEC AC Test Load

Figure 16 shows the GMII receive AC timing diagram.

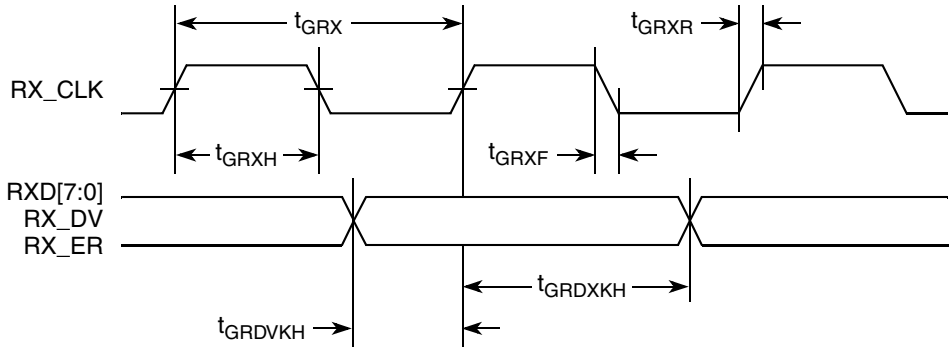


Figure 16. GMII Receive AC Timing Diagram

2.10.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

2.10.2.2.1 MII Transmit AC Timing Specifications

Table 35 provides the MII transmit AC timing specifications.

Table 35. MII Transmit AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns

Figure 17 shows the MII transmit AC timing diagram.

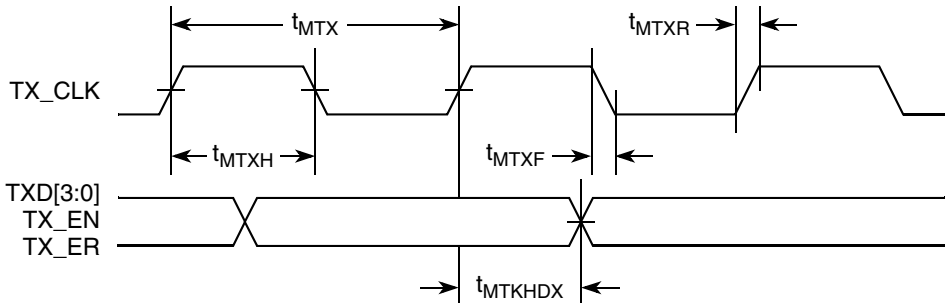


Figure 17. MII Transmit AC Timing Diagram

2.10.2.2.2 MII Receive AC Timing Specifications

Table 36 provides the MII receive AC timing specifications.

Table 36. MII Receive AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns	1
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns	1
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%	2
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns	—
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns	—
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns	2
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns	2

Note:

1. The frequency of RX_CLK should not exceed the frequency of TX_CLK by more than 300 ppm.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

Figure 18 provides the AC test load for eTSEC.

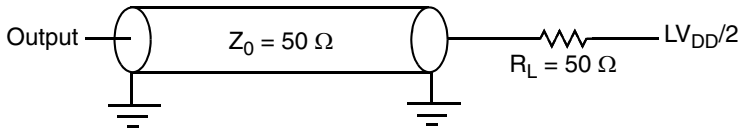


Figure 18. eTSEC AC Test Load

Figure 19 shows the MII receive AC timing diagram.

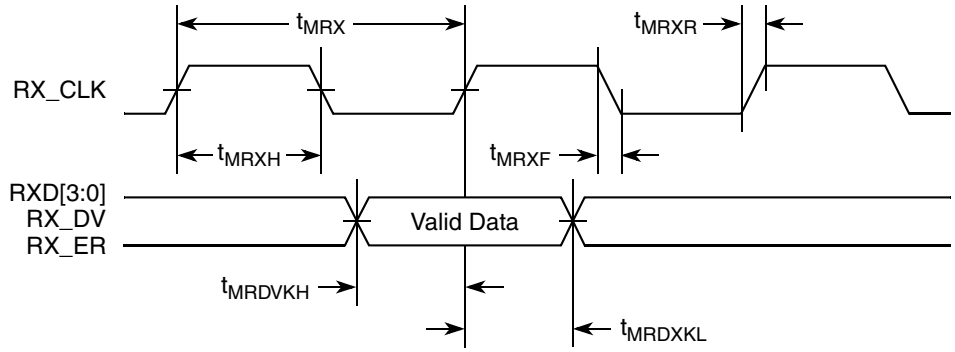


Figure 19. MII Receive AC Timing Diagram

2.10.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

2.10.2.3.1 TBI Transmit AC Timing Specifications

Table 37 provides the TBI transmit AC timing specifications.

Table 37. TBI Transmit AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns	—
GTX_CLK to TCG[9:0] delay time	t_{TTKHDX}	1.0	—	5.0	ns	1
GTX_CLK rise (20%–80%)	t_{TTXZ}	0.7	—	1.0	ns	—
GTX_CLK fall time (80%–20%)	t_{TTXF}	0.7	—	1.0	ns	—

Note:
1. Data valid t_{TTKHDV} to GTX_CLK minimum setup time is a function of clock and maximum hold time (min setup = cycle time – max delay).

Figure 20 shows the TBI transmit AC timing diagram.

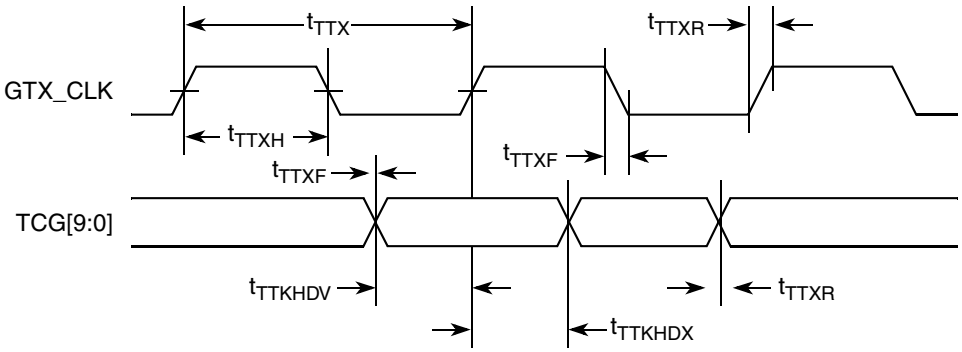


Figure 20. TBI Transmit AC Timing Diagram

2.10.2.3.2 TBI Receive AC Timing Specifications

Table 38 provides the TBI receive AC timing specifications.

Table 38. TBI Receive AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC*n*_RX_CLK[0:1] clock period	t_{TRX}	—	16.0	—	ns	1
TSEC*n*_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns	—
TSEC*n*_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%	2
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns	—
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.5	—	—	ns	—
TSEC*n*_RX_CLK[0:1] clock rise time (20%–80%)	t_{TRXR}	0.7	—	2.4	ns	2
TSEC*n*_RX_CLK[0:1] clock fall time (80%–20%)	t_{TRXF}	0.7	—	2.4	ns	2

Note:

1. The frequency of RX_CLK should not exceed the frequency of TX_CLK by more than 300 ppm.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

Figure 21 shows the TBI receive AC timing diagram.

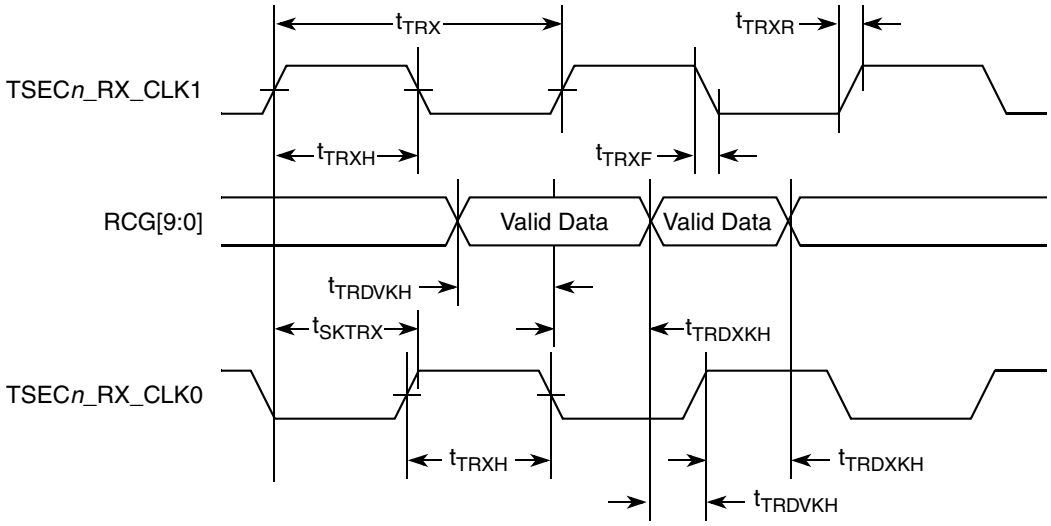


Figure 21. TBI Receive AC Timing Diagram

2.10.2.4 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on the TSEC*n* pin (no receive clock is used in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive is shown in Table 39.

Table 39. TBI Single-Clock Mode Receive AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period	t_{TRR}	7.5	8.0	8.5	ns	1
RX_CLK duty cycle	t_{TRRH}	40	50	60	%	2
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	1.0	ns	—
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	1.0	ns	—
RCG[9:0] setup time to RX_CLK rising edge	t_{TRRDV}	2.0	—	—	ns	2
RCG[9:0] hold time to RX_CLK rising edge	t_{TRRDX}	1.0	—	—	ns	2

Note:

1. The frequency of RX_CLK should not exceed the frequency of TX_CLK by more than 300 ppm.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

A timing diagram for TBI receive appears in Figure 22.

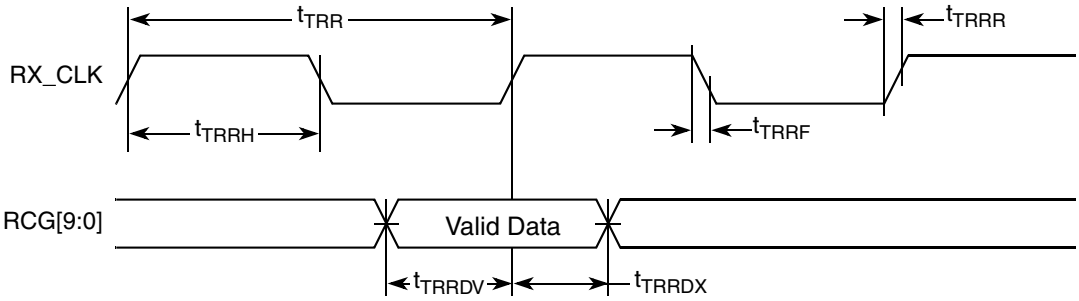


Figure 22. TBI Single-Clock Mode Receive AC Timing Diagram

2.10.2.5 RGMII and RTBI AC Timing Specifications

Table 40 presents the RGMII and RTBI AC timing specifications.

Table 40. RGMII and RTBI AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.8	ns	1
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	2
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	2, 3
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	4

Table 40. RGMII and RTBI AC Timing Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	4

Notes:
1. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
2. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
3. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
4. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
5. The frequency of RX_CLK should not exceed the frequency of gigabit Ethernet reference clock by more than 300 ppm.

Figure 23 shows the RGMII and RTBI AC timing and multiplexing diagrams.

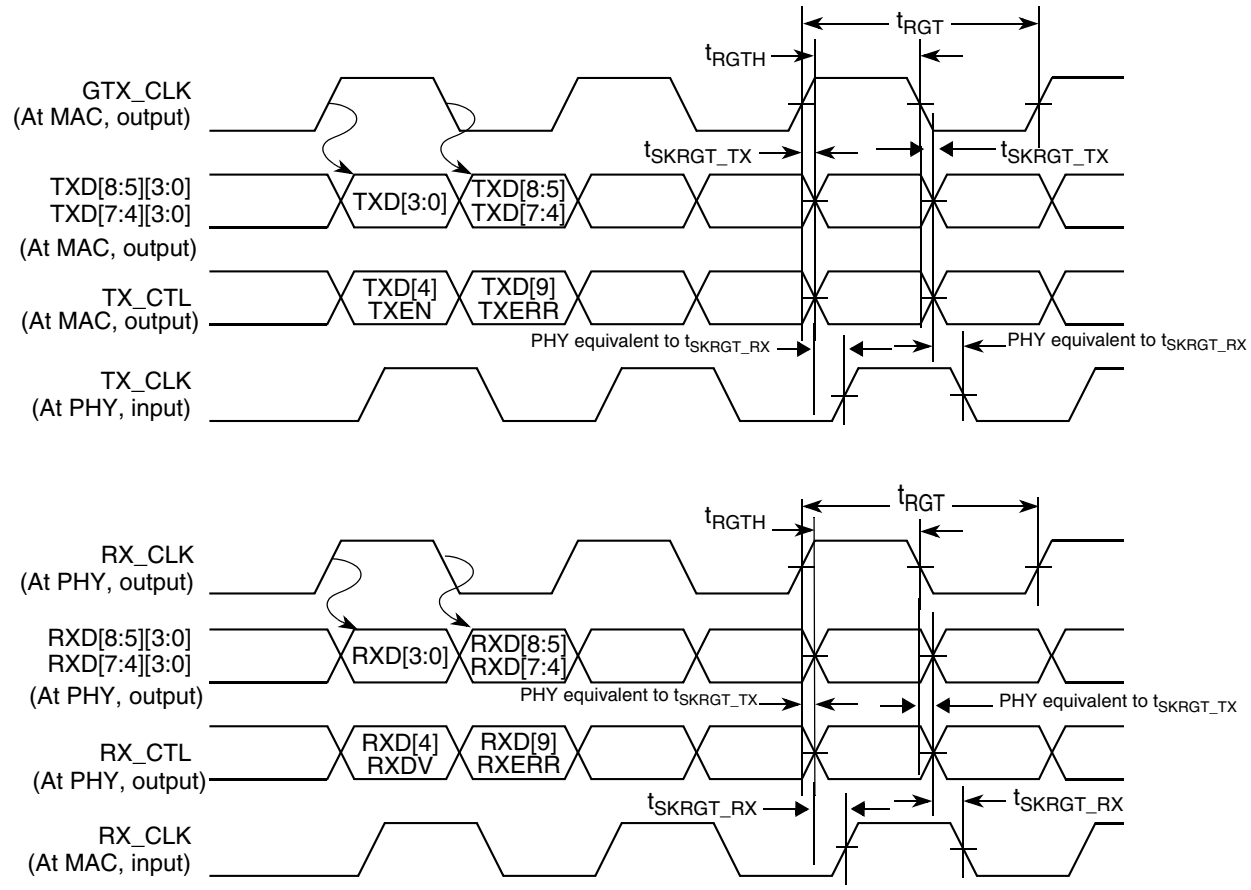


Figure 23. RGMII and RTBI AC Timing and Multiplexing Diagrams

2.10.2.6 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

2.10.2.6.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 41.

Table 41. RMII Transmit AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TSEC*n*_TX_CLK (reference clock) clock period	t_{RMT}	15.0	20.0	25.0	ns
TSEC*n*_TX_CLK duty cycle	t_{RMTH}	35	50	65	%
Rise time TSEC*n*_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time TSEC*n*_TX_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
TSEC*n*_TX_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Figure 24 shows the RMII transmit AC timing diagram.

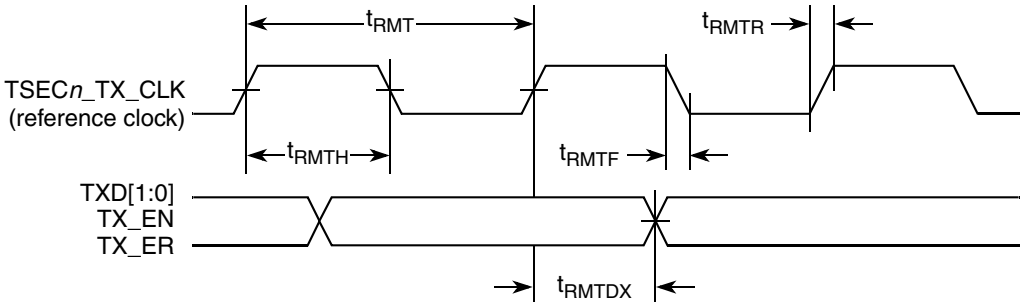


Figure 24. RMII Transmit AC Timing Diagram

2.10.2.6.2 RMII Receive AC Timing Specifications

Table 42 lists the RMII receive AC timing specifications.

Table 42. RMII Receive AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
TSEC*n*_TX_CLK (reference clock) clock period	t_{RMR}	15.0	20.0	25.0	ns	—
TSEC*n*_TX_CLK duty cycle	t_{RMRH}	35	50	65	%	1
Rise time TSEC*n*_TX_CLK (20%–80%)	t_{RMRR}	1.0	—	4.0	ns	1
Fall time TSEC*n*_TX_CLK (80%–20%)	t_{RMRF}	1.0	—	4.0	ns	1
RXD[1:0], CRS_DV, RX_ER setup time to TSEC*n*_TX_CLK rising edge	t_{RMRDV}	4.0	—	—	ns	—
RXD[1:0], CRS_DV, RX_ER hold time to TSEC*n*_TX_CLK rising edge	t_{RMRDX}	2.0	—	—	ns	—

Note:

1. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

Figure 25 provides the AC test load for eTSEC.

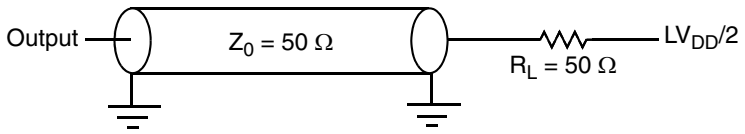


Figure 25. eTSEC AC Test Load

Figure 26 shows the RMII receive AC timing diagram.

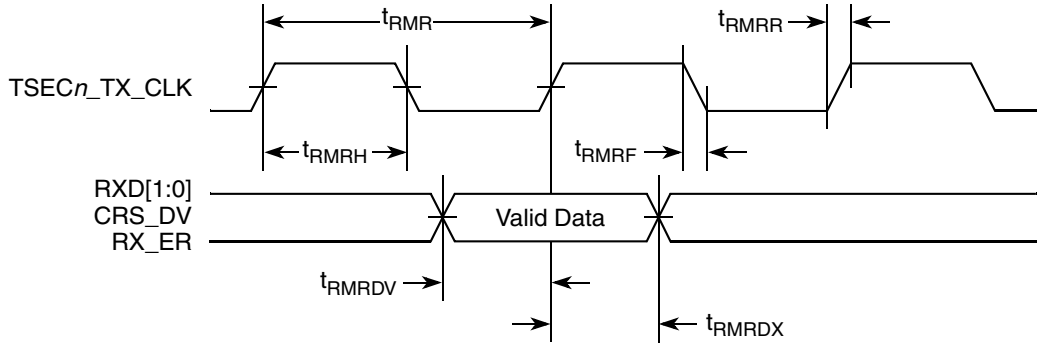


Figure 26. RMII Receive AC Timing Diagram

2.10.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the SerDes interface of device, as shown in Figure 27, where C_{TX} is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to SGND_SRDS2 (xcorevss). The reference circuit of the SerDes transmitter and receiver is shown in Figure 57.

2.10.3.1 DC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 2.18.2.3, "DC Level Requirement for SerDes Reference Clocks."

2.10.3.2 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

Note that the SGMII clock requirements for SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are intended to be used within the clocking guidelines specified by Section 2.18.3, "AC Requirements for PCI Express SerDes Reference Clocks."

2.10.4 SGMII Transmitter Electrical Characteristics

2.10.4.1 SGMII Transmit DC Timing Specifications

Table 43 and Table 44 describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX[n] and $\overline{\text{SD\_TX}}$[n]) as shown in Figure 28.

Table 43. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	$XV_{DD\_SRDS\text{-}Typ}/2 + \lvert V_{OD}\rvert_{-max}/2$	mV	1
Output low voltage	V_{OL}	$XV_{DD\_SRDS\text{-}Typ}/2 - \lvert V_{OD}\rvert_{-max}/2$	—	—	mV	1

Table 43. SGMII DC Transmitter Electrical Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage[2, 3, 4] (XV_{DD-Typ} at 1.05V)	$\|V_{OD}\|$	342	525	756	mV	Equalization setting: 1.0×
		313	481	693		Equalization setting: 1.09×
		285	437	630		Equalization setting: 1.2×
		257	394	568		Equalization setting: 1.33×
		228	350	504		Equalization setting: 1.5×
		200	307	442		Equalization setting: 1.71×
		171	262	378		Equalization setting: 2.0×
Output impedance (single-ended)	R_O	40	50	60	Ω	—

Note:

1. This does not align to DC-coupled SGMII. $XV_{DD\_SRDS2-Typ}$= 1.05 V.
2. $|V_{OD}| = |V_{SDn\_TXn} - V_{\overline{SDn\_TXn}}|$. $|V_{OD}|$ is also referred to as output differential peak voltage. $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.
3. The $|V_{OD}|$ value shown in the table assumes the following transmit equalization setting in the TXEQ0/1 (for SerDes lanes 0 and 1) or TXEQ2/3 (for SerDes lanes 2 and 3) bit field of device's SerDes Control Register:
   - The MSB (bit 0) of the above bit field is cleared (selecting the full $V_{DD-DIFF-p-p}$ amplitude – power up default).
   - The LSB (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. The $|V_{OD}|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS-Typ}$ = 1.05 V, no common mode offset variation (V_{OS} = 500 mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TX[*n*] and SD_TX[*n*].

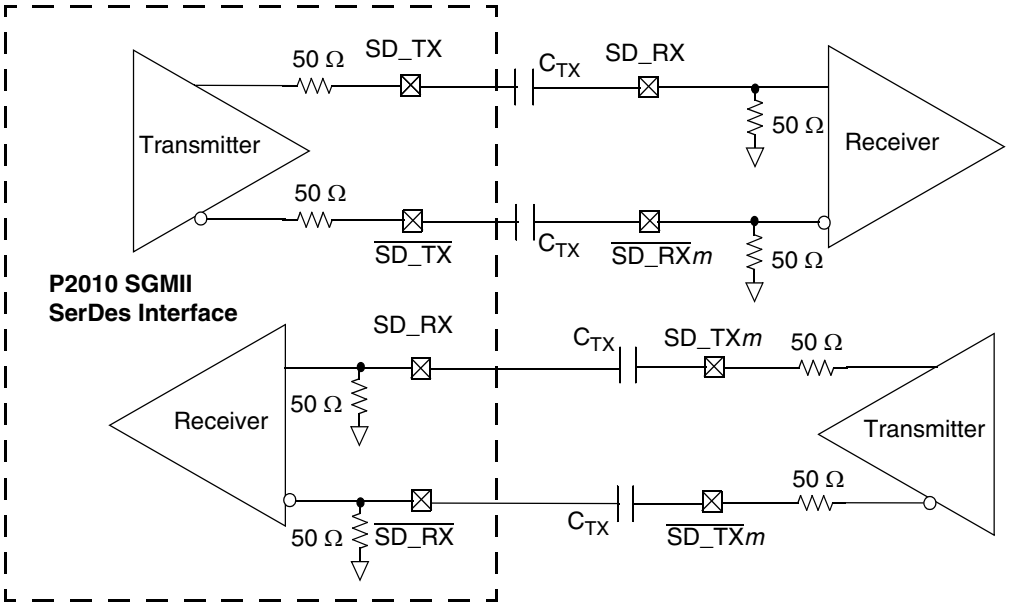


Figure 27. 4-Wire AC-Coupled SGMII Serial Link Connection Example

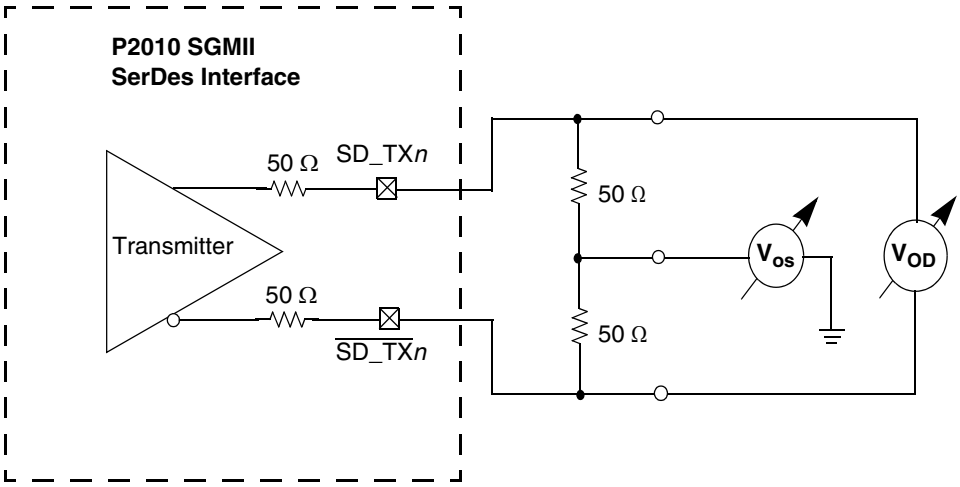


Figure 28. SGMII Transmitter DC Measurement Circuit

2.10.4.2 SGMII DC Receiver Timing Specification

Table 44 lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 44. SGMII DC Receiver Electrical Characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC Input voltage range		—	N/A			—	1
Input differential voltage	LSTS = 001	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 3
	LSTS = 100		175	—			
Loss of signal threshold	LSTS = 001	VLOS	30	—	100	mV	3, 4
	LSTS = 100		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	Ω	—

Note:

1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The LSTS shown in the table refers to the LSTS**2** or LSTS**3** bit field of device's SerDes Control Register SRDSCR4.
4. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. Refer to PCI Express Differential Receiver (Rx) Input Specifications section for further explanation.

2.10.5 SGMII AC Timing Specifications

This section discusses the AC timing specifications for the SGMII interface.

2.10.5.1 SGMII Transmit AC Timing Specifications

Table 45 provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 45. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD_SRDS2} = 1.1 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	1
Unit Interval	UI	799.92	800	800.08	ps	2
AC coupling capacitor	C_{TX}	10	100	200	nF	3

Notes:
1. See Figure 30 for single frequency sinusoidal jitter limits.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.10.6 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX[n] and $\overline{\text{SD\_TX}}$[n]) or at the receiver inputs (SD_RX[n] and $\overline{\text{SD\_RX}}$[n]) as depicted in Figure 29, respectively.

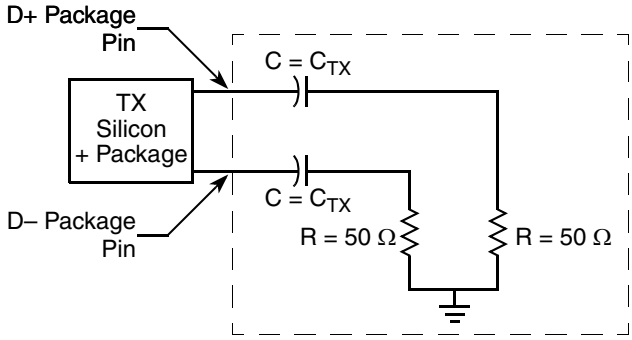


Figure 29. SGMII AC Test/Measurement Load

2.10.6.1 SGMII Receiver AC Timing Specification

Table 46 provides the SGMII receiver AC timing specifications. The AC timing specifications do not include RefClk jitter.

Table 46. SGMII Receive AC Timing Specifications

At recommended operating conditions with XV_{DD_SRDS2} = 1.1 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1, 2
Bit Error Ratio	BER	—	—	10^{-12}	—	—

Table 46. SGMII Receive AC Timing Specifications (continued)

At recommended operating conditions with XV_{DD_SRDS2} = 1.1 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	799.92	800.00	800.08	ps	3

Notes:
1. Measured at receiver.
3. Refer to RapidIO™ 1×/4× LP Serial Physical Layer Specification for interpretation of jitter specifications.
2. Each UI is 800 ps ± 100 ppm.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 30.

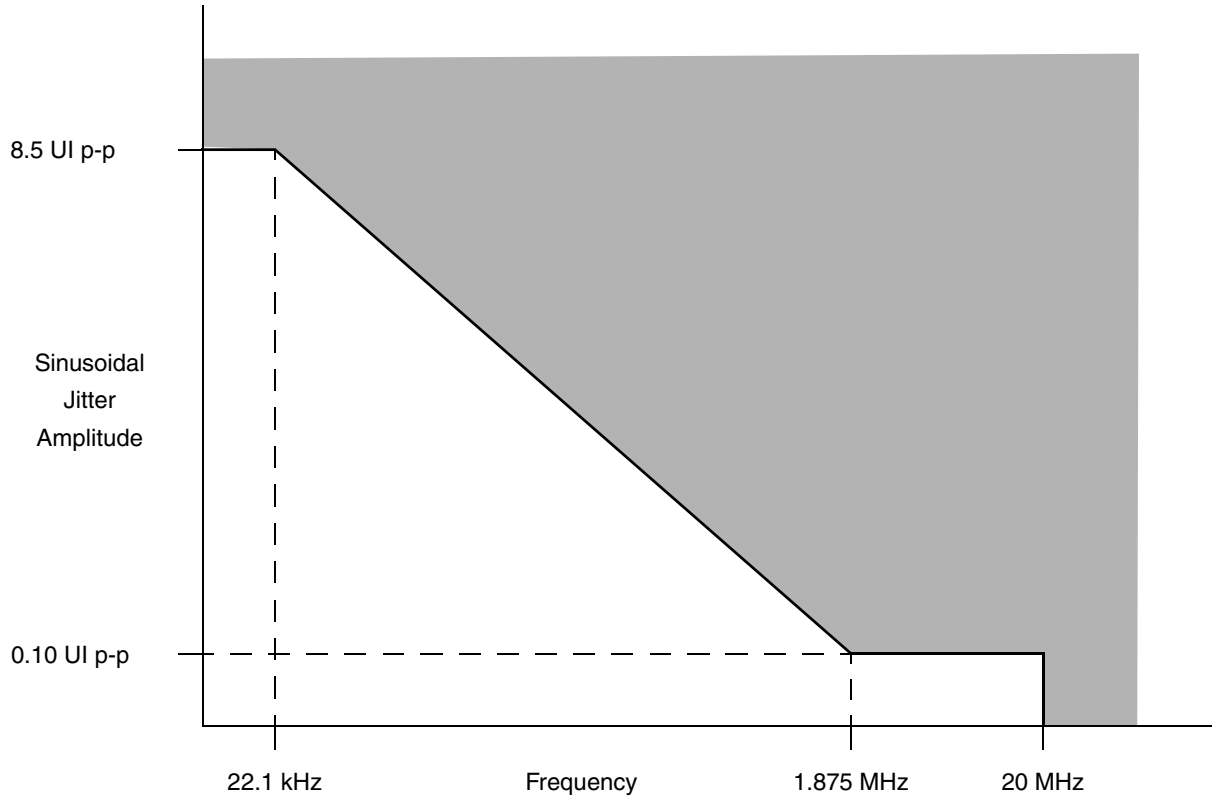


Figure 30. Single Frequency Sinusoidal Jitter Limits

2.10.7 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in "Section 2.10.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—GMII/SGMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics."

2.10.7.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V or 2.5 V. The DC electrical characteristics for MDIO and MDC are provided in Table 47 and Table 48. Table 47 provides the electrical characteristics at 3.3 V.

Table 47. MII Management DC Electrical Characteristics (LV_{DD} = 3.3 V)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.90	V	1
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	2
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–40	—	μA	—
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.50	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2.

Table 48 shows the electrical characteristics at 2.5 V.

Table 48. MII Management DC Electrical Characteristics (LV_{DD} = 2.5 V)

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.70	V	1
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	40	μA	2
Input low current (V_{IN} = GND)	I_{IL}	–40	—	μA	—
Output high voltage (LV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2.

2.10.7.2 MII Management AC Electrical Specifications

Table 49 provides the MII management AC timing specifications.

Table 49. MII Management AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	1
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO valid	t_{MDKHDV}	$2 \times (t_{plb\_clk} \times 8)$	—	—	ns	2
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{plb\_clk}) - 3$	—	$(16 \times t_{plb\_clk}) + 3$	ns	2, 3, 4

Table 49. MII Management AC Timing Specifications (continued)

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:
1. This parameter is dependent on the system clock speed. (The maximum frequency is the maximum platform frequency divided by 64.)
2. t_{plb_clk} is the platform (CCB) clock.
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns).
4. MDC to MDIO Data valid t_{MDKHDV} is a function of clock period and max delay time (t_{MDKHDX}). (Min setup = cycle time – max delay)

Figure 31 shows the MII management interface timing diagram.

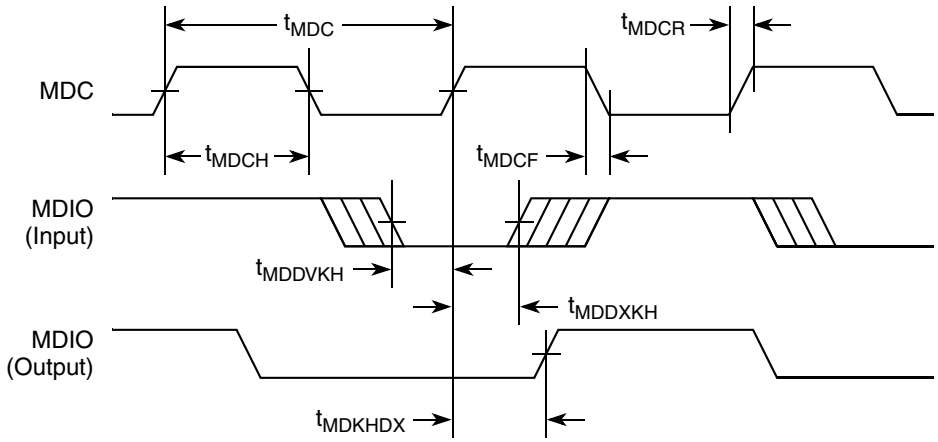


Figure 31. MII Management Interface Timing Diagram

2.10.8 eTSEC IEEE Std 1588 AC Specifications

Table 50 provides the IEEE 1588 AC timing specifications.

Table 50. eTSEC IEEE 1588 AC Timing Specifications

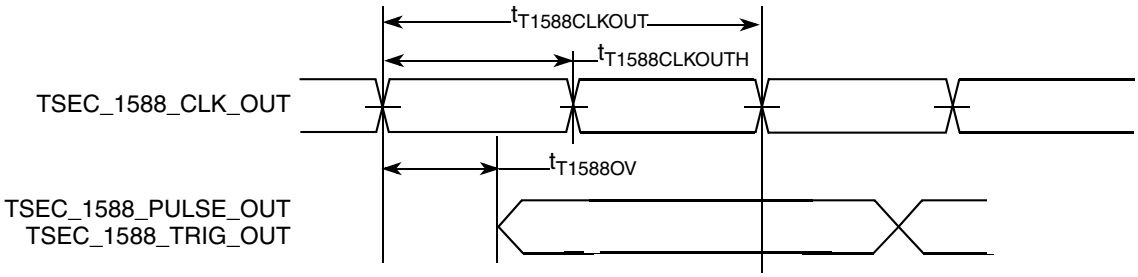
Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.3	—	$T_{RX\_CLK} \times 7$	ns	1, 2
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	3
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—

Table 50. eTSEC IEEE 1588 AC Timing Specifications (continued)

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$/ $t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	2

Notes:
1. T_{RX_CLK} is the maximum clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *P2010QorIQ Integrated Processor Reference Manual,* for a description of TMR_CTRL registers.
2. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns, respectively.
3. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *P2010 QorIQ Integrated Processor Reference Manual,* for a description of TMR_CTRL registers.

Figure 32 shows the data and command output AC timing diagram.



Note: eTSEC IEEE 1588 Output AC timing: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is noninverting. Otherwise, it is counted starting at the falling edge.

Figure 32. eTSEC IEEE 1588 Input AC Timing

Figure 33 shows the data and command input AC timing diagram.

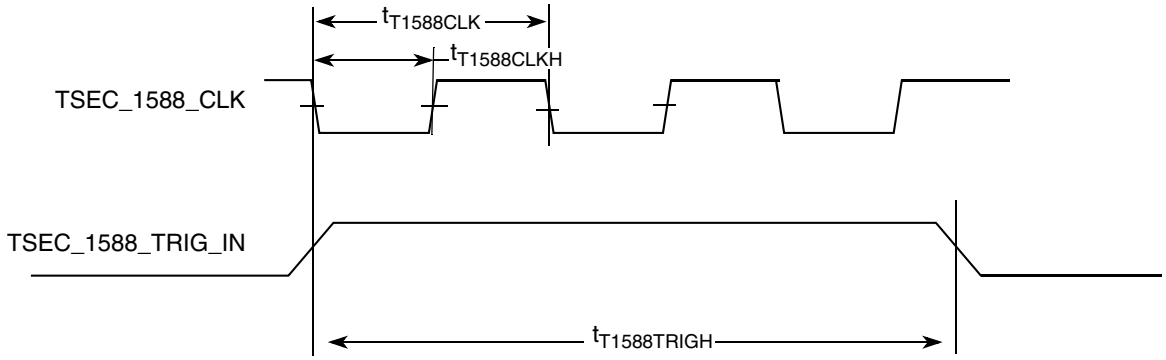


Figure 33. eTSEC IEEE 1588 Input AC Timing

2.11 USB

This section provides the AC and DC electrical specifications for the USB interface of the device.

2.11.1 USB DC Electrical Characteristics

Table 51, Table 52, and Table 53 provides the DC electrical characteristics for the USB interface.

Table 51. USB DC Electrical Characteristics (CV_{DD} = 3.3 V)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage[1]	V_{IH}	2.0	—	V	1
Low-level input voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±70	μA	2
High-level output voltage (CV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	3
Low-level output voltage (CV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Notes:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."
3. Not applicable for open drain signals

Table 52. USB DC Electrical Characteristics (CV_{DD} = 2.5 V)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage[1]	V_{IH}	1.7	—	V	1
Low-level input voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±70	μA	2
High-level output voltage (CV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	3
Low-level output voltage (CV_{DD} = min, I_{OL} = 1mA)	V_{OL}	—	0.4	V	—

Notes:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."
3. Not applicable for open drain signals

Table 53. USB DC Electrical Characteristics (CV_{DD} = 1.8V)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage[1]	V_{IH}	1.25	—	V	1
Low-level input voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±70	μA	2
High-level output voltage (CV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	3
Low-level output voltage (CV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."
3. Not applicable for open drain signals.

2.11.2 USB AC Electrical Specifications

Table 54 describes the general timing parameters of the USB interface of the device.

Table 54. USB General Timing Parameters[6] (ULPI Mode Only)

Parameter	Symbol[1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	2, 3, 4, 5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2, 3, 4, 5
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2, 3, 4, 5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2, 3, 4, 5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2, 3, 4, 5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $CV_{DD} \div 2$ of the rising edge of the USB clock to $0.4 \times CV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.
6. When switching the data pins from outputs to inputs using the USB_DIR pin, the output timings is violated on that cycle because the output buffers are tristated asynchronously. This should not be a problem, because the PHY should not be functionally looking at these signals on that cycle as per ULPI specifications.

Figure 34 and Figure 35 provide the AC test load and signals for the USB, respectively.

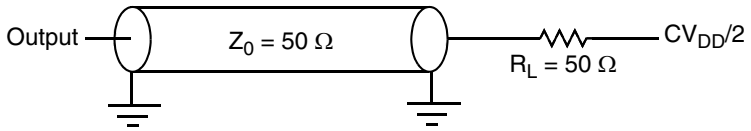


Figure 34. USB AC Test Load

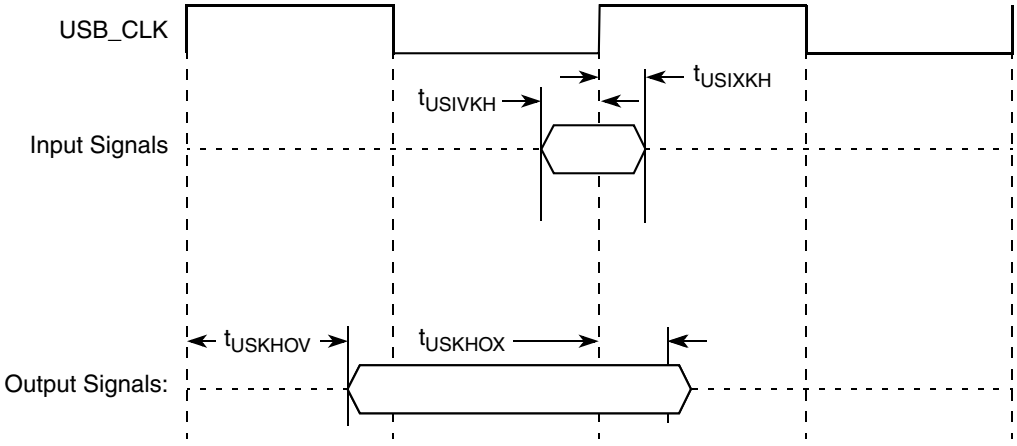


Figure 35. USB Signals

Table 55 provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 55. USB_CLK_IN AC Timing Specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Frequency range	Steady state	$f_{USB\_CLK\_IN}$	59.97	60	60.03	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.05	0	0.05	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second-order, high-pass filter of 500-kHz bandwidth	t_{CLK_PJ}	—	—	200	ps

2.12 Enhanced Local Bus

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

2.12.1 Enhanced Local Bus DC Electrical Characteristics

Table 56 provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 3.3 V DC.

Table 56. Enhanced Local Bus DC Electrical Characteristics (3.3 V DC)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	2	—	V	1
Low-level input voltage	V_{IL}	—	0.8	V	1

Table 56. Enhanced Local Bus DC Electrical Characteristics (3.3 V DC) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input current (V_{IN}[1] = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

Table 57 provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 2.5 V DC.

Table 57. Enhanced Local Bus DC Electrical Characteristics (2.5 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	1.70	—	V	1
Low-level input voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

Table 58 provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 1.8 V DC.

Table 58. Enhanced Local Bus DC Electrical Characteristics (1.8 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	1.25	—	V	1
Low-level input voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
High-level output voltage (BV_{DD} = min, IOH = –0.5 mA)	V_{OH}	1.35	—	V	—
Low-level output voltage (BV_{DD} = min, IOL = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

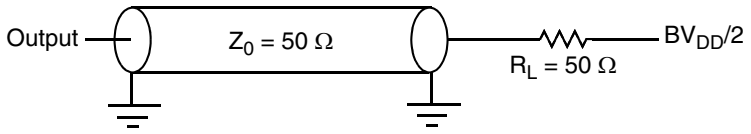
2.12.2 Enhanced Local Bus AC Electrical Specifications

This section describes the AC timing specifications for the enhanced local bus interface.

2.12.2.1 Test Condition

Figure 36 provides the AC test load for the enhanced local bus.

Figure 36. Enhanced Local Bus AC Test Load



2.12.2.2 Local Bus AC Timing Specifications for PLL Enable Mode

For PLL enable mode, all timings are relative to the rising edge of LSYNC_IN.

Table 59 describes the general timing parameters of the enhanced local bus interface.

Table 59. Enhanced Local Bus Timing Specifications (BV_{DD} = 3.3 V, 2.5 V, and 1.8 V)—PLL Enabled Mode[1]

Parameter	Symbol	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	6.67	12	ns	—
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	2
Input setup	t_{LBIVKH}	2	—	ns	—
Input hold	t_{LBIXKH}	0.55	—	ns	—
Output delay (Except LALE)	t_{LBKHOV}	—	3.8	ns	—
Output hold (Except LALE)	t_{LBKHOX}	0.7	—	ns	—
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	1 (LBCR[AHD] = 0) 1/2 (LBCR[AHD] = 1)	—	eLBC controller clock cycle (=1 platform clock cycles)	4

Note:

1. All signals are measured from $BV_{DD} \div 2$ of the rising edge of LSYNC_IN to $BV_{DD} \div 2$ of the signal in question.
2. Skew measured between different LCLK signals at $BV_{DD} \div 2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle. The eLBC controller clock refers to the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle × LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.

Figure 37 shows the AC timing diagram for PLL-enabled mode.

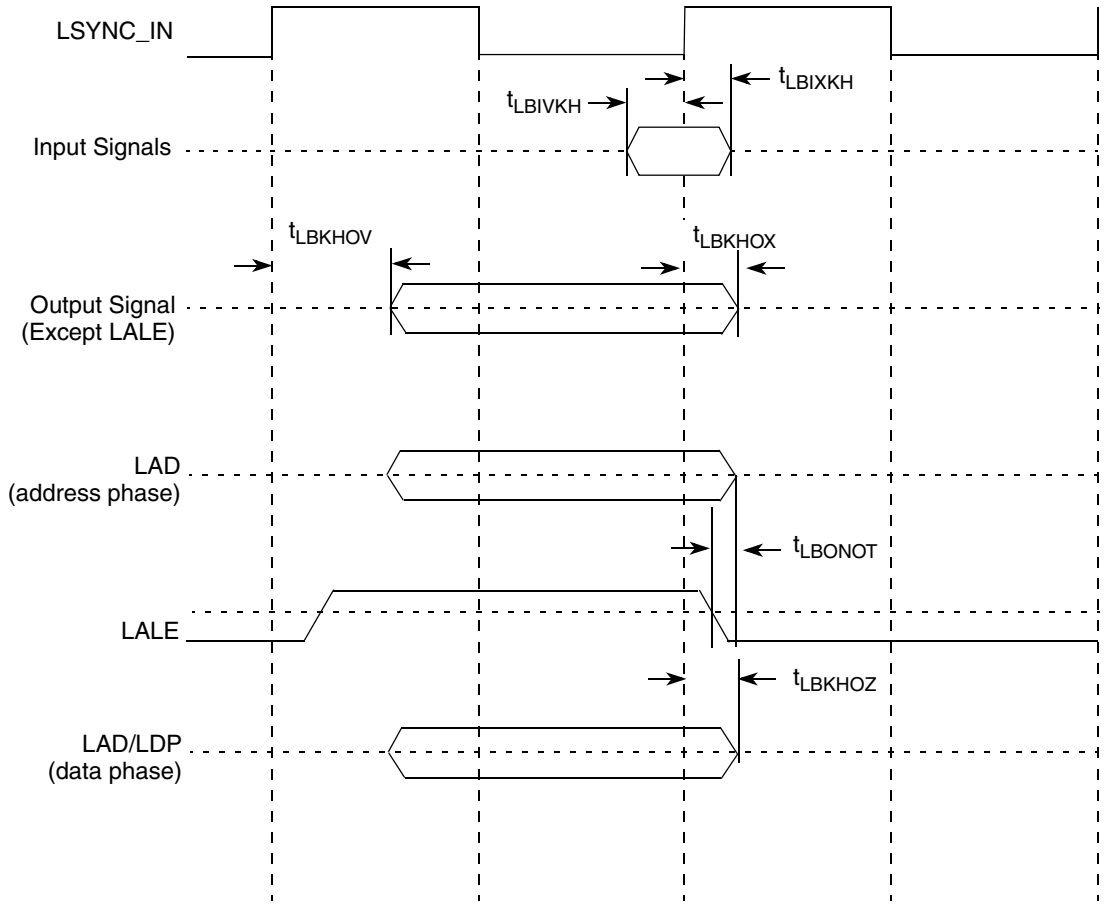


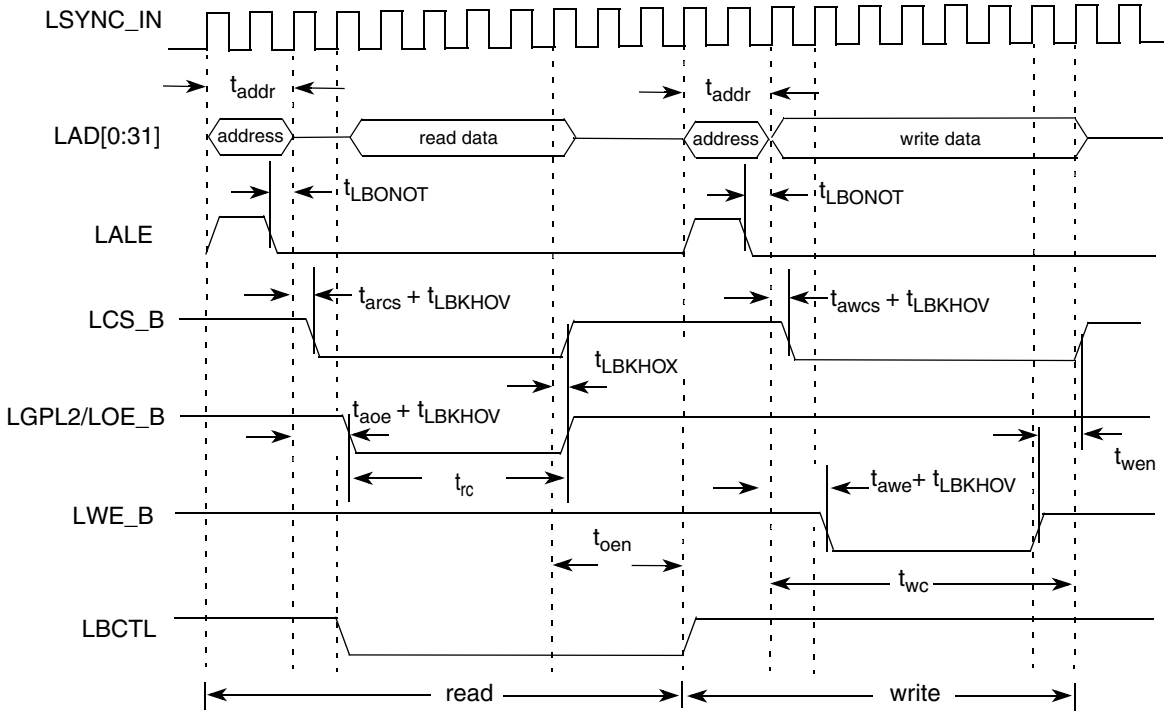
Figure 37. Local Bus AC Timing Diagram (PLL Enabled)

Figure 37 applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

Figure 38 shows how the AC timing diagram applies to GPCM. The same principle applies to UPM and FCM.



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. See the P2010reference manual.

Figure 38. GPCM Output Timing Diagram (PLL Enabled)

2.12.2.3 Local Bus AC Timing Specifications for PLL Bypass Mode

All output signal timings are relative to the falling edge of any LCLKs. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LGTA/LUPWAIT/LFRB are relative to the rising edge of LCLKs. LGTA/LUPWAIT/LFRB are relative to the falling edge of LCLKs.

Table 60 describes the timing specifications of the local bus interface.

Table 60. Enhanced Local Bus Timing Specifications (BV_{DD} = 3.3 V, 2.5 V, and 1.8 V)-PLL Bypassed

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	—
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m]	$t_{LBKSKEW}$	—	150	ps	2
Input setup (except LGTA/LUPWAIT/LFRB)	t_{LBIVKH}	6	—	ns	—

Table 60. Enhanced Local Bus Timing Specifications (BV_{DD} = 3.3 V, 2.5 V, and 1.8 V)-PLL Bypassed (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Input hold (except LGTA/LUPWAIT/LFRB)	t_{LBIXKH}	1	—	ns	—
Input setup (for LGTA/LUPWAIT/LFRB)	t_{LBIVKL}	6	—	ns	—
Input hold (for LGTA/LUPWAIT/LFRB)	t_{LBIXKL}	1	—	ns	—
Output delay (Except LALE)	t_{LBKLOV}	—	1.5	ns	—
Output hold (Except LALE)	t_{LBKLOX}	–3.5	—	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKLOZ}	—	2	ns	4
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	1 (LBCR[AHD] = 0) 1/2 (LBCR[AHD] = 1)	—	eLBC controller clock cycle (= 1 platform clock cycles)	5

Note:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLK signals at $BV_{DD}/2$.
3. Output hold is negative. This means that output transition happens earlier than the falling edge of LCLK.
4. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle, which is the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle × LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.

Figure 39 shows the enhanced local bus signals in PLL-bypass mode.

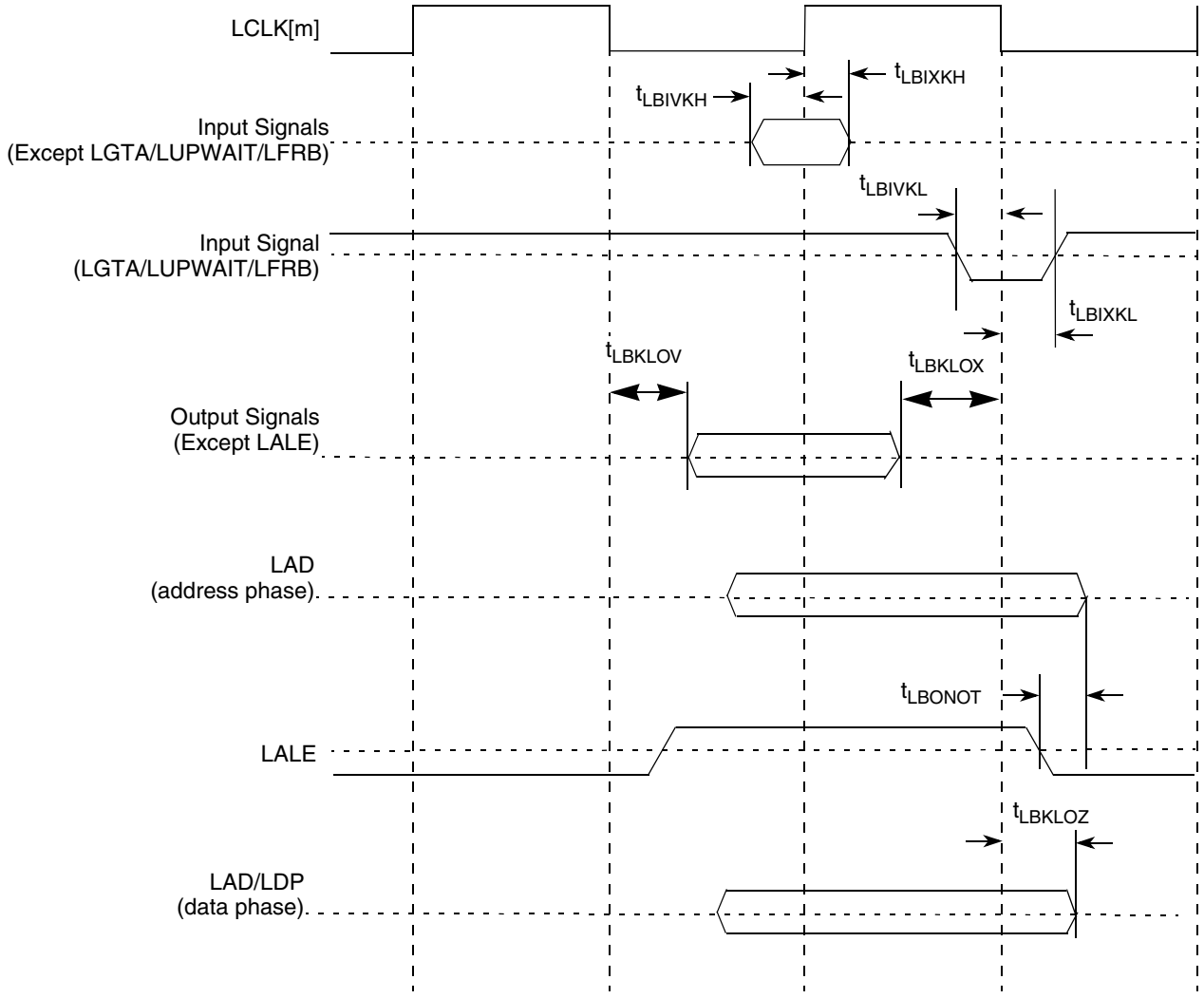


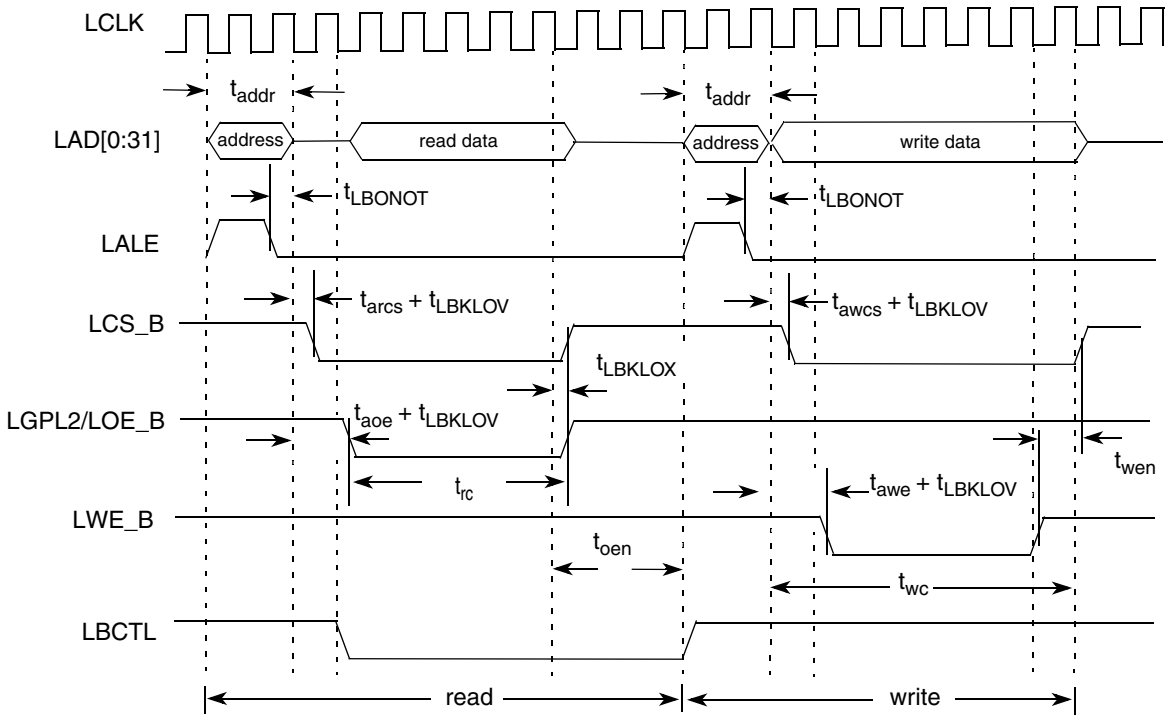
Figure 39. Enhanced Local Bus Signals (PLL Bypass Mode)

Figure 39 applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

Figure 40 shows how the AC timing diagram applies to GPCM. The same principle applies to UPM and FCM.



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. See the P2010reference manual.

Figure 40. GPCM Output Timing Diagram

2.13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC (SDIO) interface.

2.13.1 eSDHC DC Electrical Characteristics

Table 61 provides the DC electrical characteristics for the eSDHC (SDIO) interface.

Table 61. eSDHC Interface DC Electrical Characteristics (CV_{DD} = 3.3 V)

Parameter	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	0.625 × CV_{DD}	—	V	1
Input low voltage	V_{IL}	—	—	0.25 × CV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = –100 uA at OV_{DD}min	0.75 × CV_{DD}	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100uA at OV_{DD}min	—	0.125 × CV_{DD}	V	—
Output high voltage	V_{OH}	I_{OH} = –100 uA	CV_{DD}-0.2	—	V	2

Table 61. eSDHC Interface DC Electrical Characteristics (continued)(CV_{DD} = 3.3 V)

Parameter	Symbol	Condition	Min	Max	Unit	Note
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	2
Input leakage current	I_{IN}	—	–70	70	uA	—

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3
2. Open drain mode for MMC cards only.

2.13.2 eSDHC AC Timing Specifications

This section describes the AC electrical specifications for the eSDHC (SDIO) interface. Table 62 provides the eSDHC AC timing specifications for full speed mode as defined in Figure 41 and Figure 42.

Table 62. eSDHC AC Timing Specifications

Parameter	Symbol[1]	Min	Max	Unit	Notes
SD_CLK clock frequency SD Full-speed/High-speed mode MMC Full-speed/High-speed mode	f_{SHSCK}	0	 25/50 20/52	MHz	2, 3
SD_CLK clock low time—Full-speed mode/High-speed mode	t_{SHSCKL}	10/7	—	ns	3
SD_CLK clock high time—Full-speed mode/High-speed mode	t_{SHSCKH}	10/7	—	ns	3
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	3
Input setup times: SD_CMD, SD_DATX, SD_CD to SD_CLK	$t_{SHSIVKH}$	3.7	—	ns	3, 4, 5
Input hold times: SD_CMD, SD_DATX, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	3
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	–3	3	ns	3, 5

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full speed mode, clock frequency value can be 0–25 MHz for a SD/SDIO card and 0–20 MHz for a MMC card. In high speed mode, clock frequency value can be 0–50 MHz for a SD/SDIO card and 0–52 MHz for a MMC card.
3. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF
4. To satisfy setup timing, one way board routing delay between Host and Card, on SD_CLK, SD_CMD, and SD_DATx should not exceed 0.65ns.
5. The parameter values apply to both full speed and high speed modes.

This figure provides the eSDHC clock input timing diagram.

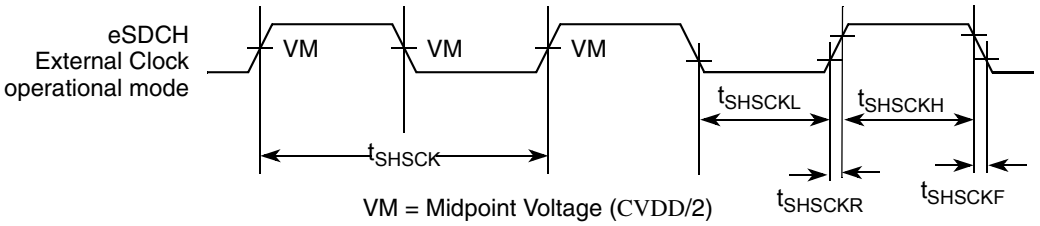


Figure 41. eSDHC Clock Input Timing Diagram

This figure provides the data and command input/output timing diagram.

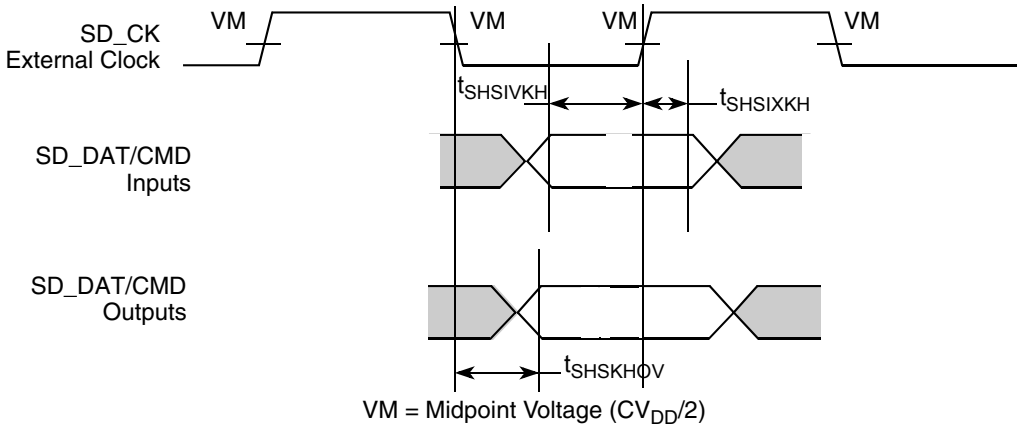


Figure 42. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.14 Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at least 3 system clocks (SYSCLK periods).

2.14.1 PIC DC Electrical Characteristics

Table 65 provides the DC electrical characteristics for the PIC interface.

Table 63. PIC DC Electrical Characteristics

Parameter	Symbol [1]	Min	Max	Unit	Note
High-level input voltage	V_{IH}	2	—	V	1
Low-level input voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Note that the symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.14.2 PIC AC Electrical Characteristics

Table 64 shows the PIC AC timing specifications.

Table 64. PIC Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Notes
PIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLK	1

Note:

1. PIC inputs and outputs are asynchronous to any visible clock. PIC outputs must be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge-triggered mode.

2.15 JTAG

This section discusses the JTAG interface.

2.15.1 JTAG DC Electrical Characteristics

Table 65 provides the DC electrical characteristics for the JTAG interface.

Table 65. JTAG DC Electrical Characteristics

Parameter	Symbol [1]	Min	Max	Unit	Note
High-level input voltage	V_{IH}	2	—	V	1
Low-level input voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN}[1] = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol found in Table 3.

2.15.2 JTAG AC Electrical Specifications

This section describes the AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface of the device.

This table provides the JTAG AC timing specifications as defined in Figure 44 through Figure 46.

Table 66. JTAG AC Timing Specifications (Independent of SYSCLK)

At recommended operating conditions (see Table 3).

Parameter	Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at OV_{DD}/2	t_{JTKHKL}	15	—	ns	—

Table 66. JTAG AC Timing Specifications (Independent of SYSCLK) (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol[1]	Min	Max	Unit	Notes
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}	4	—	ns	—
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times	t_{JTKLDV}	0	10	ns	3
Output hold times	t_{JTKLDX}	0	—	ns	3

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

Figure 43 provides the AC test load for TDO and the boundary-scan outputs.

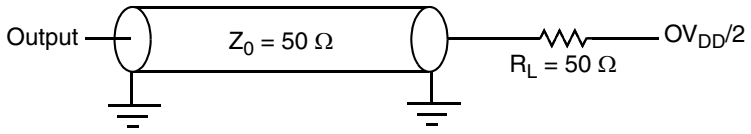


Figure 43. AC Test Load for the JTAG Interface

Figure 44 provides the JTAG clock input timing diagram.

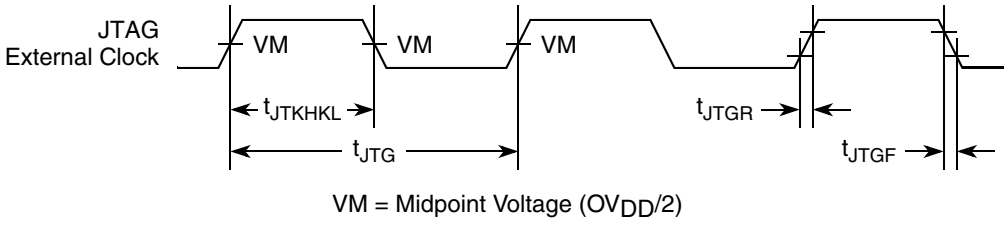


Figure 44. JTAG Clock Input Timing Diagram

Figure 45 provides the $\overline{\text{TRST}}$ timing diagram.

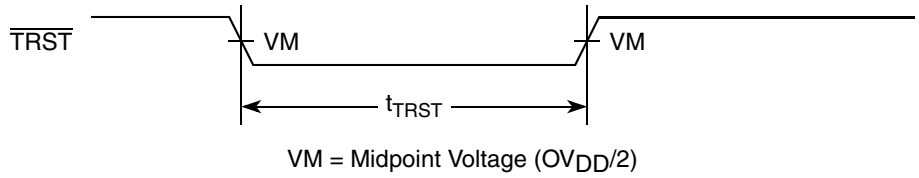


Figure 45. $\overline{\text{TRST}}$ Timing Diagram

Figure 46 provides the boundary-scan timing diagram.

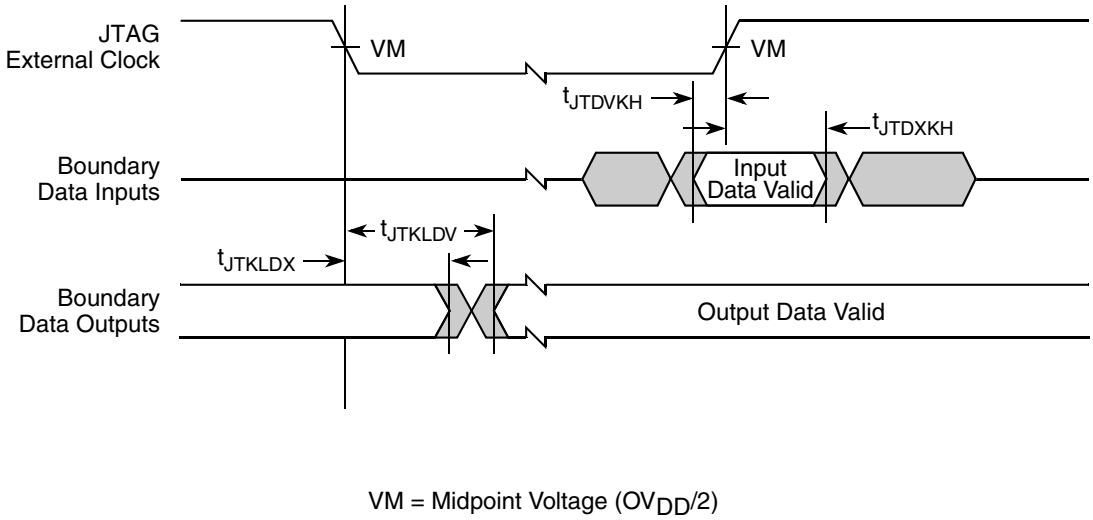


Figure 46. Boundary-Scan Timing Diagram

2.16 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the device.

2.16.1 I²C DC Electrical Characteristics

Table 67 provides the DC electrical characteristics for the I²C interfaces.

Table 67. I²C DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	2	—	V	1
Input low voltage level	V_{IL}	—	0.8	V	1
Output Low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	0	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD}(max)	I_I	–40	40	μA	4

Table 67. I²C DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the *P2020 QorIQ Integrated Communications Host Processor Family Reference Manual* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.16.2 I²C AC Electrical Specifications

Table 68 provides the AC timing parameters for the I²C interfaces.

Table 68. I²C AC Electrical Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 67).

Parameter	Symbol[1]	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz[4]	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—

Table 68. I²C AC Electrical Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 67).

Parameter	Symbol[1]	Min	Max	Unit	Note
Capacitive load for each bus line	Cb	—	400	pF	—

Note:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the device acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the device as transmitter, application note AN2919, referred to in note 2 above, is recommended.
4. The maximum t_{I2OVKL} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

Figure 47 provides the AC test load for the I²C.

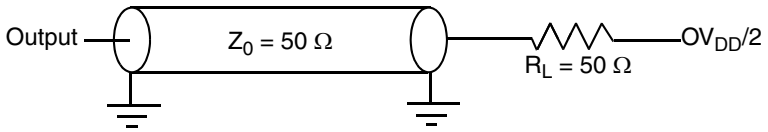


Figure 47. I²C AC Test Load

Figure 48 shows the AC timing diagram for the I²C bus.

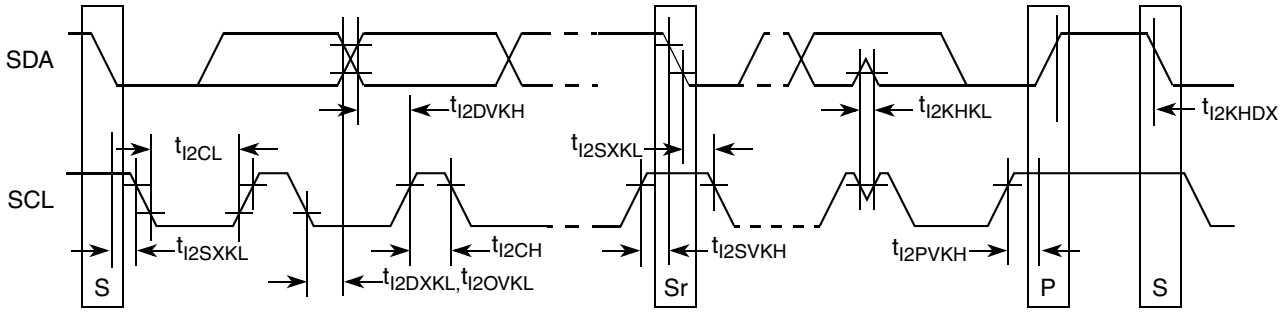


Figure 48. I²C Bus AC Timing Diagram

2.17 GPIO

This section describes the DC and AC electrical specifications for the GPOUT and GPIN interface of the device.

2.17.1 GPIO DC Electrical Characteristics

Table 69 provides the DC electrical characteristics for the GPIO interface.

Table 69. PIO[0:7] DC Electrical Characteristics (3.3 V)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	—	V	1, 2
Low-level input voltage	V_{IL}	—	0.8	V	1, 2
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±40	μA	—
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 2.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 2.

Table 70. GPIO[8:15] DC Electrical Characteristics (3.3 V)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	—	V	1, 2
Low-level input voltage	V_{IL}	—	0.8	V	1, 2
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±40	μA	—
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 2.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 2.

Table 71. GPIO[8:15] DC Electrical Characteristics (2.5 V)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	1.7	—	V	1, 2
Low-level input voltage	V_{IL}	—	0.7	V	1, 2
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±40	μA	—
High-level output voltage (BV_{DD} = mn, I_{OH} = –1 mA)	V_{OH}	1.7	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.7	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 2.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 2.

Table 72. GPIO[8:15] DC Electrical Characteristics (1.8 V)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	1.2	—	V	1, 2
Low-level input voltage	V_{IL}	—	0.6	V	1, 2
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±40	μA	—
High-level output voltage (BV_{DD} = mn, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:
1.The min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 2.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 2.

2.17.2 GPIO AC Electrical Specifications

Table 73 provides the GPIO input and output AC timing specifications.

Table 73. GPIO Input and Output AC Timing Specifications[1]

Characteristic	Symbol [2]	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	1.5 × plat ÷ 2	ns	1

Notes:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 49 provides the AC test load for the GPIO.

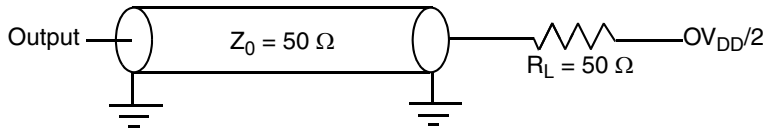


Figure 49. GPIO AC Test Load

2.18 High-Speed Serial Interfaces (HSSI)

The device features one Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express SGMII and/or Serial RapidIO data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

2.18.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 50 shows how the signals are defined. For illustration purposes, only one SerDes lane is used for description. Figure 50 shows the waveform for either a transmitter output (SD_TX and $\overline{\text{SD\_TX}}$) or a receiver input (SD_RX and $\overline{\text{SD\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

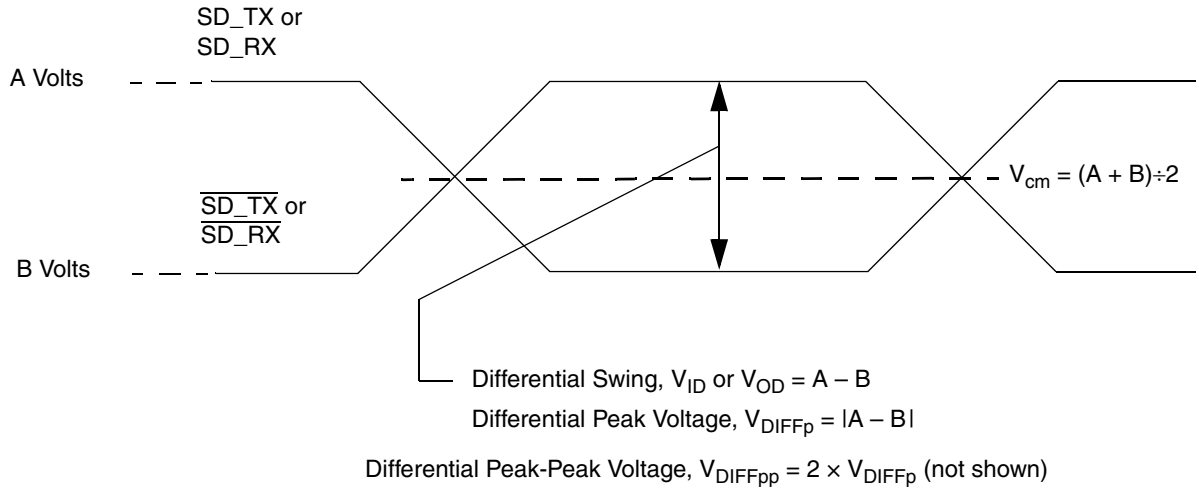


Figure 50. Differential Voltage Definitions for Transmitter or Receiver

Using this waveform, the definitions are as follows. To simplify the illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing

The transmitter output signals and the receiver input signals SD_TX, $\overline{\text{SD\_TX}}$, SD_RX and $\overline{\text{SD\_RX}}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's Single-Ended Swing.

Differential Output Voltage, V_{OD} (or **Differential Output Swing**)

The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX} - V_{\overline{SDn\_TX}}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or **Differential Input Swing**)

The Differential Input Voltage (or Swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SDn\_RX} - V_{\overline{SDn\_RX}}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, V_{DIFFp} = |A – B| Volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD\_TX}}$, for example) from the non-inverting signal (SD_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 50 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SDn\_TX} + V_{\overline{SDn\_TX}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the case of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred to as the single-ended swing for each signal. In this example, because the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.18.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK and $\overline{SD\_REF\_CLK}$ for PCI Express and Serial RapidIO, or SD_REF_CLK and $\overline{SD\_REF\_CLK}$ for the SGMII interface respectively.

The following sections describe the SerDes reference clock requirements and some application information.

2.18.2.1 SerDes Spread Spectrum Clock Source Recommendations

SD_REF_CLK/$\overline{SD\_REF\_CLK}$ are designed to work with spread spectrum clock for PCI Express protocol only with the spreading specification defined in Table 74. When using spread spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation should be used.

The spread spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread spectrum supported protocols. For example, if the spread spectrum clocking is desired on a SerDes reference clock for PCI Express and the same reference clock is used for any other protocol such as SGMII/SRIO due to the SerDes lane usage mapping option, spread spectrum clocking cannot be used at all.

Table 74. SerDes Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 3.

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	—
Frequency spread	+0	–0.5	%	1

Note:

1. Only down spreading is allowed.

2.18.2.2 SerDes Reference Clock Receiver Characteristics

Figure 51 shows a receiver reference diagram of the SerDes reference clocks.

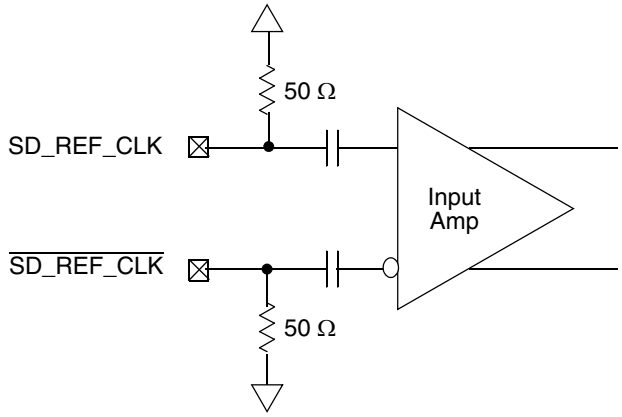


Figure 51. Receiver of SerDes Reference Clocks

The characteristics are as follows:

- The supply voltage requirements for XV_{DD_SRDS2} are specified in Table 2 and Table 3.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 51. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has on-chip 50-Ω termination to SGND_SRDS*n* (xcorevss) followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range is the following:
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement is as follows:
  - This requirement is described in detail in the following sections.

2.18.2.3 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the device SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below:

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have

a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

— For **external DC-coupled** connection, as described in Section 2.18.2.2, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 52 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

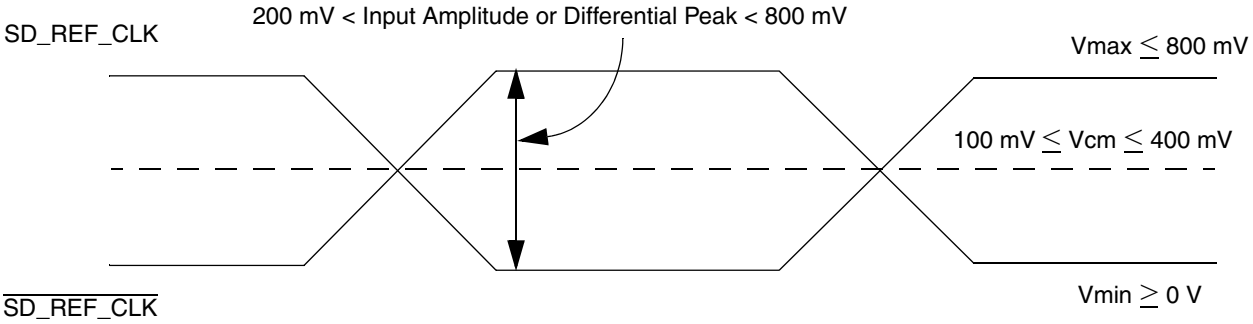


Figure 52. Differential Reference Clock Input DC Requirements (External DC-Coupled)

— For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS*n*. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS*n*). Figure 53 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

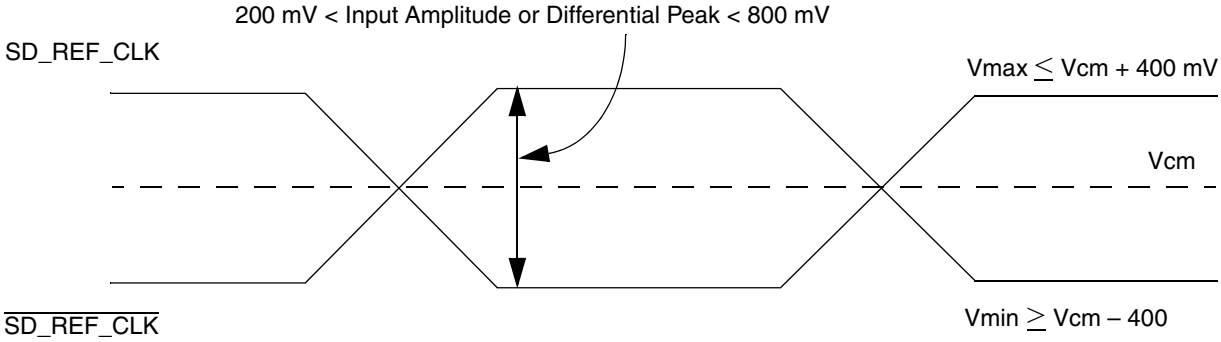


Figure 53. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- **Single-ended Mode**
  — The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  — The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 54 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

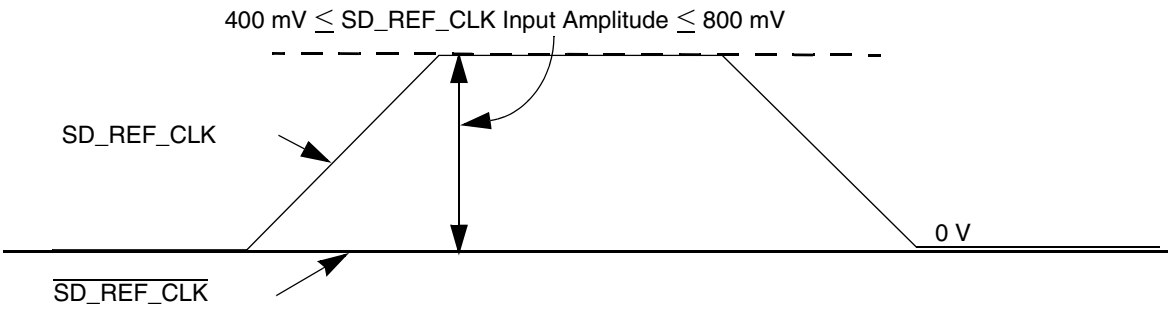


Figure 54. Single-Ended Reference Clock Input DC Requirements

2.18.3 AC Requirements for PCI Express SerDes Reference Clocks

Table 75 lists AC requirements for the PCI Express, SGMII, and SRIO SerDes reference clocks to be guaranteed by the customer's application design.

Table 75. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ Input Clock Requirements

Parameter	Symbol	Min	Typical	Max	Unit	Notes
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	+350	ppm	—
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	7
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak Jitter @ 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	6
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter @ 10^{-6} BER (Peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2, 6
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3, 6
Differential input high voltage	V_{IH}	200	—	—	mV	3
Differential input low voltage	V_{IL}	—	—	–200	mV	3

Table 75. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ Input Clock Requirements (continued)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Rising edge rate (SD_REF_CLK) to falling edge rate (SD_REF_CLK) matching	Rise-Fall Matching	—	—	20	%	4, 5, 6

Notes:

1. **Caution:** Only 100 and 125 have been tested. In-between values do not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK minus $\overline{\text{SD\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 55.
4. Measurement taken from single-ended waveform.
5. Matching applies to rising edge for SD_REF_CLK and falling edge rate for $\overline{\text{SD\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK rising meets $\overline{\text{SD\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK must be compared to the fall edge rate of $\overline{\text{SD\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 56.
6. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
7. Measurement taken from the differential waveform.

Figure 55 shows the differential measurement points for rise and fall time.

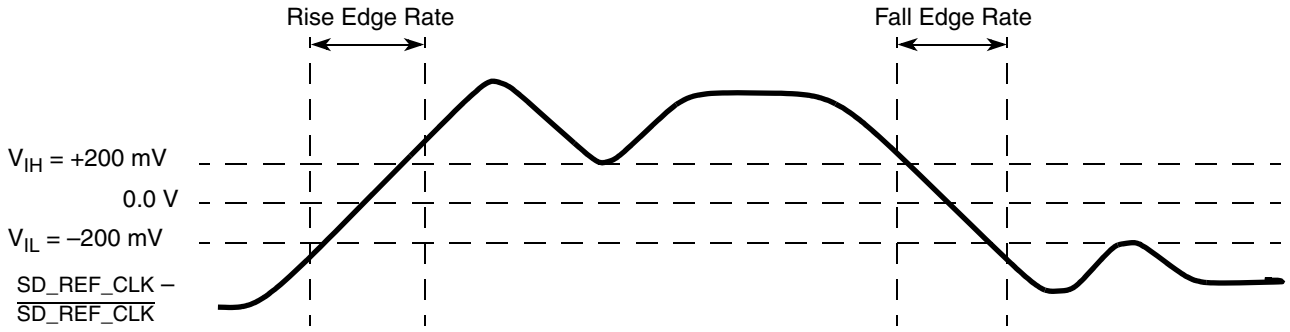


Figure 55. Differential Measurement Points for Rise and Fall Time

Figure 56 shows the single-ended measurement points for rise and fall time matching.

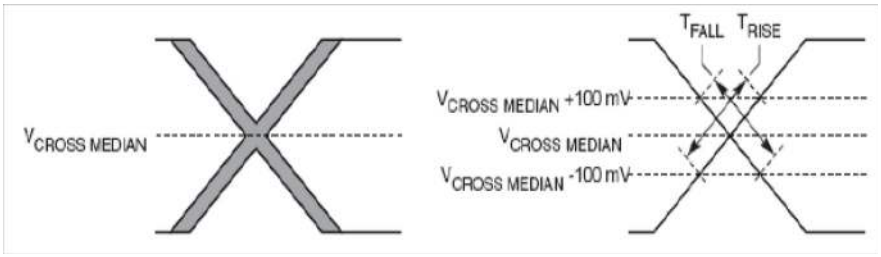


Figure 56. Single-Ended Measurement Points for Rise and Fall Time Matching

2.18.4 SerDes Transmitter and Receiver Reference Circuits

Figure 57 shows the reference circuits for SerDes data lane's transmitter and receiver.

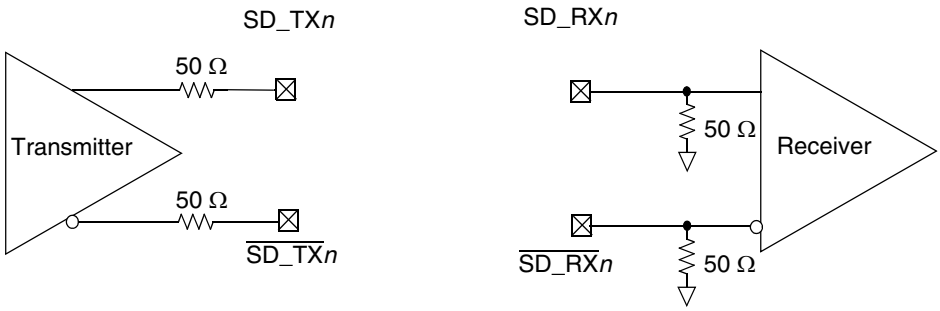


Figure 57. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO or SGMII) in this document based on the application usage:

- Section 2.10.3, "SGMII Interface Electrical Characteristics"
- Section 2.19, "PCI Express"
- Section 2.20, "Serial RapidIO (SRIO)"

Note that external AC Coupling capacitor is required for the above three serial transmission protocols per the protocol's standard requirements.

2.18.5 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ± 300 ppm tolerance.

2.19 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the P2010.

2.19.1 PCI Express DC Requirements for SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

For more information, see Section 2.18.2.3, "DC Level Requirement for SerDes Reference Clocks."

2.19.2 PCI Express DC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.19.2.1 PCI Express DC Physical Layer Transmitter Specifications

Table 76 defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 76. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Comments
Differential Peak-to-Peak Output Voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \div \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$ See Note 1.
De-emphasized Differential Output Voltage (Ratio)	$V_{TX\text{-}DE\text{-}RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 1.
DC Differential TX Impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	TX DC Differential mode low impedance
Transmitter DC Impedance	$Z_{TX\text{-}DC}$	40	50	60	Ω	Required TX D+ as well as D– DC impedance during all states

Note:

1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 58 and measured over any 250 consecutive Tx UIs.

Table 78 defines the PCI Express (2.5 Gb/s) AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

2.19.2.2 PCI Express DC Physical Layer Receiver Specifications

Table 77 defines the DC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 77. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Comments
Differential Input Peak-to-Peak Voltage	$V_{RX\text{-}DIFFp\text{-}p}$	175	—	1200	mV	$V_{RX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$ See Note 1.
DC Differential Input Impedance	$Z_{RX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	RX DC Differential mode impedance. See Note 2
DC Input Impedance	$Z_{RX\text{-}DC}$	40	50	60	Ω	Required RX D+ as well as D– DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered Down DC Input Impedance	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	50	—	—	kΩ	Required RX D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 3.

Table 77. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications (continued)

Parameter	Symbol	Min	Typical	Max	Units	Comments
Electrical Idle Detect Threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the Receiver

Notes:
1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 58 must be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

2.19.3 PCI Express AC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.19.3.1 PCI Express AC Physical Layer Transmitter Specifications

This section discusses the PCI Express AC physical layer transmitter specification for 2.5 Gb/s.

Table 78 defines the PCI Express (2.5 Gb/s) AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 78. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Comments
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum TX Eye Width	T_{TX-EYE}	0.70	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.

Table 78. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications (continued)

Parameter	Symbol	Min	Typical	Max	Units	Comments
AC Coupling Capacitor	C_{TX}	75	—	200	nF	All transmitters are AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 58 and measured over any 250 consecutive Tx UIs.
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. P2010 SerDes transmitter does not have CTX built-in. An external AC Coupling capacitor is required

2.19.3.2 Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in Figure 58.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

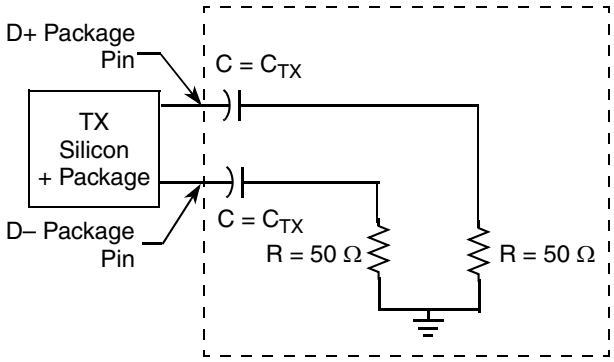


Figure 58. Test/Measurement Load

2.19.3.3 PCI Express AC Physical Layer Receiver Specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 Gb/s.

Table 79 defines the AC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 79. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Comments
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum Receiver Eye Width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 58 must be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.20 Serial RapidIO (SRIO)

This section describes the DC and AC electrical specifications for the RapidIO interface for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter must be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ±100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

2.20.1 Signal Definitions

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 59 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A Volts and B Volts where A > B.

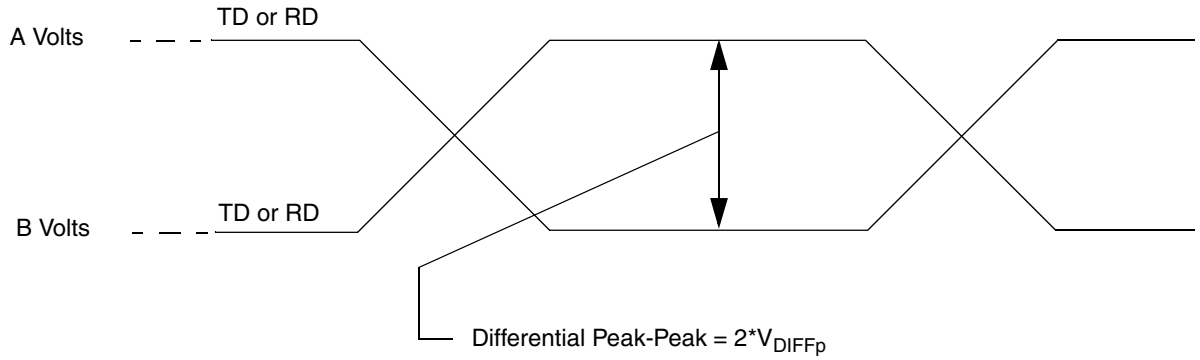


Figure 59. Differential Peak-Peak Voltage of Transmitter or Receiver

Using these waveforms, the definitions are as follows:

- The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD and $\overline{\text{RD}}$ each have a peak-to-peak swing of A – B Volts.
- The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{\overline{TD}}$
- The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{\overline{RD}}$
- The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts
- The peak value of the differential transmitter output signal and the differential receiver input signal is A –B Volts.
- The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 × (A – B) Volts.

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

2.20.2 Equalization

With the use of high speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- Pre-emphasis on the transmitter
- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

2.20.3 DC Requirements for Serial RapidIO

This section explains the DC requirements for the Serial RapidIO interface.

2.20.3.1 DC Requirements for Serial RapidIO SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clocks of the Serial RapidIO interface are described in Section 2.18.2.3, "DC Level Requirement for SerDes Reference Clocks."

2.20.4 DC Serial RapidIO Timing Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case is better than

- –10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100-Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, have a minimum value 60 ps in each case.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GBaud, 20 ps at 2.50 GBaud and 15 ps at 3.125 GBaud.

Table 80 defines the Transmitter DC specifications for the Serial RapidIO interface.

Table 80. SRIO Transmitter DC Timing Specifications—1.25 GBaud, 2.5 GBaud, 3.125 GBaud

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output Voltage,	V_O	–0.40	—	2.30	V	1
Long Run Differential Output Voltage	V_{DIFFPP}	800	—	1600	mV p-p	—
Short Run Differential Output Voltage	V_{DIFFPP}	500	—	1000	mV p-p	—

Note:

1. Voltage relative to COMMON of either signal comprising a differential pair.

2.20.5 DC Serial RapidIO Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance results in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

Table 81 defines the Receiver DC specifications for the Serial RapidIO interface.

Table 81. SRIO Receiver DC Timing Specifications—1.25 GBaud, 2.5 GBaud, 3.125 GBaud

Characteristic	Symbol	Min	Typical	Max	Unit	Notes
Differential Input Voltage	V_{IN}	200	—	1600	mV p-p	Measured at receiver

2.20.6 AC Requirements for Serial RapidIO

This section explains the AC requirements for the Serial RapidIO interface.

2.20.6.1 AC Requirements for Serial RapidIO SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

Please note that the Serial RapidIO clock requirements for SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are intended to be used within the clocking guidelines specified by Section 2.18.3, "AC Requirements for PCI Express SerDes Reference Clocks."

2.20.6.2 AC Requirements for Serial RapidIO Transmitter and Receiver

Table 82 defines the transmitter AC specifications for the Serial RapidIO interface. The AC timing specifications do not include RefClk jitter.

Table 82. SRIO Transmitter AC Timing Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic Jitter	J_D	—	—	0.17	UI p-p
Total Jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 1.25 GBaud	UI	800–100ppm	800	800+100ppm	ps
Unit Interval: 2.5 GBaud	UI	400–100ppm	400	400+100ppm	ps
Unit Interval: 3.125 GBaud	UI	320–100ppm	320	320+100ppm	ps

Table 83 defines the receiver AC specifications for the Serial RapidIO interface. The AC timing specifications do not include RefClk jitter.

Table 83. SRIO Receiver AC Timing Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic Jitter Tolerance	J_D	0.37	—	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	—	UI p-p	Measured at receiver
Bit Error Rate	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800–100ppm	800	800+100ppm	ps	—
Unit Interval: 2.5 GBaud	UI	400–100ppm	400	400+100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320–100ppm	320	320+100ppm	ps	—

Note:

1. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 60. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Figure 60 shows the single frequency sinusoidal jitter limits.

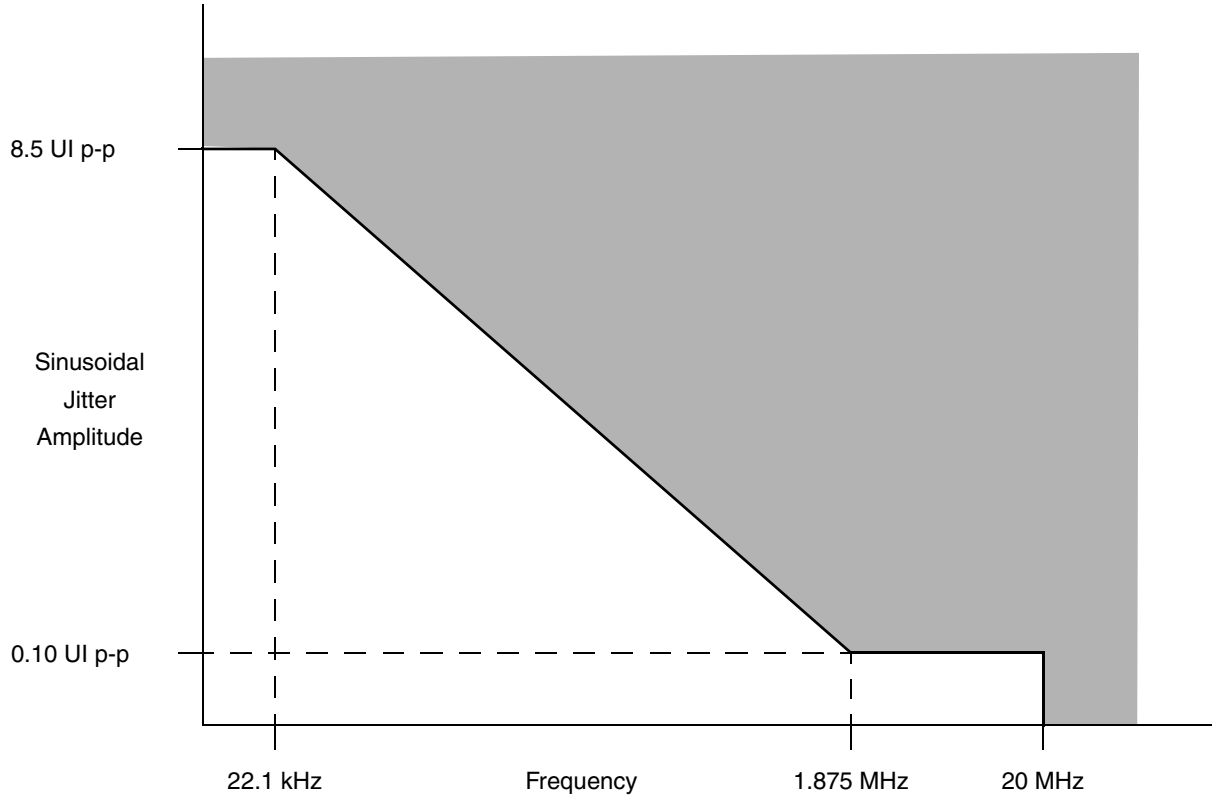


Figure 60. Single Frequency Sinusoidal Jitter Limits

3 Thermal

This section describes the thermal specifications of the device.

3.1 Thermal Characteristics

Table 84 provides the package thermal characteristics.

Table 84. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	21	°C/W	1, 2
Junction-to-ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	14	°C/W	1, 2
Junction-to-ambient (at 200 ft/min)	Single layer board (1s)	$R_{\theta JA}$	16	°C/W	1, 2
Junction-to-ambient (at 200 ft/min)	Four layer board (2s2p)	$R_{\theta JA}$	12	°C/W	1, 2
Junction-to-board thermal	—	$R_{\theta JB}$	7	°C/W	3

Table 84. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-case thermal (Top)	—	$R_{\theta JC}$	5	°C/W	4

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

3.2 Temperature Diode

The device has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices. These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the P2010 on-board temperature diode:

Operating range: 10 – 230 μA

Ideality factor over 13.5 – 220 μA; n = 1.011 +/- 0.008

4 Package Information

This section provides the package parameters and ordering information.

4.1 Package Parameters for the P2010 WB-TePBGA

The package parameters are provided in the following list. The package type is 31 mm × 31 mm, 689 plastic ball grid array (WB-TePBGA).

Package outline	31 mm × 31 mm
Interconnects	689
Pitch	1.00 mm
Module height (typical)	2.0 mm to 2.46 mm (Maximum)
Solder Balls	3.5% Ag, 96.5% Sn
Ball diameter (typical)	0.60 mm

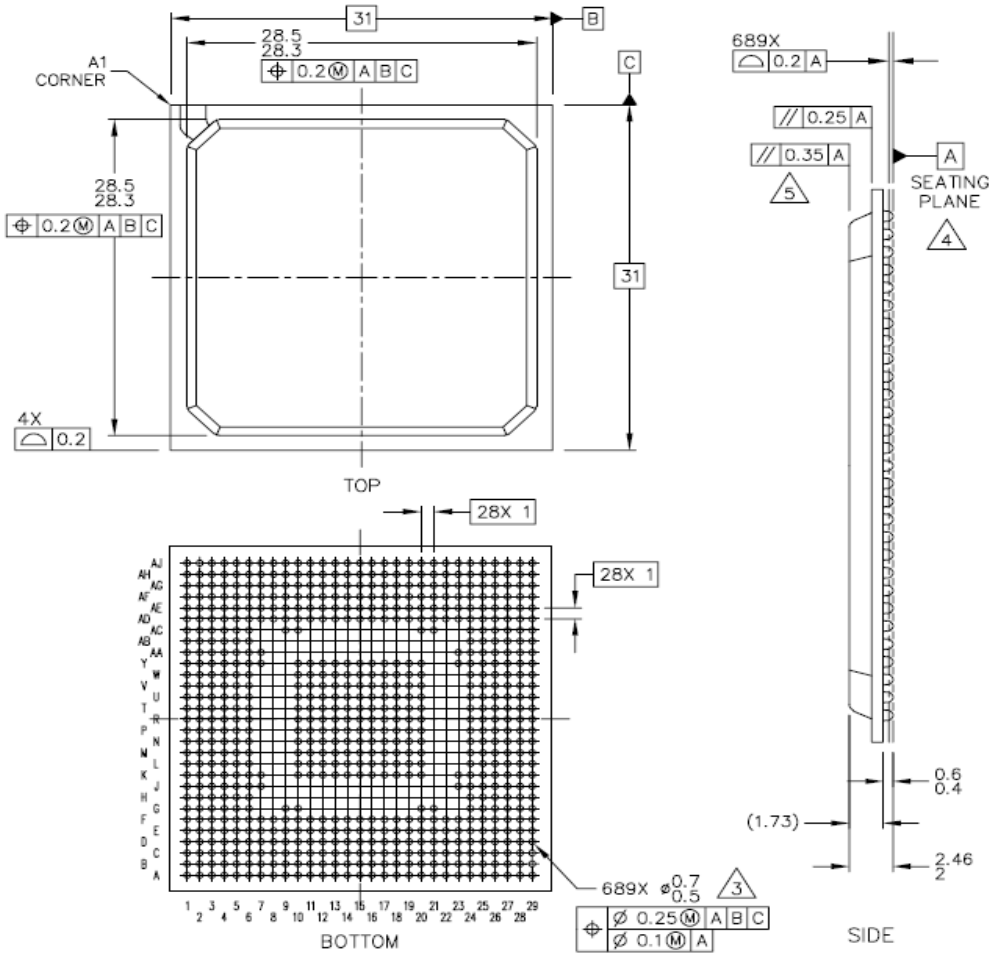


Figure 61. P2010 Package

NOTES for Figure 61:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14. 5M-1994.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement excludes any effect of mark on top surface of package.

4.2 Ordering Information

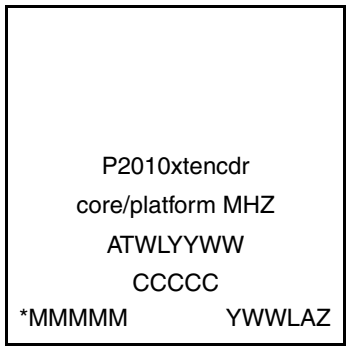
Table 85 provides the Freescale part numbering nomenclature for the device. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. Each part number also contains a revision code which refers to the die mask revision number.

Table 85. Part Numbering Nomenclature

p	*2*	*02 or 01*	*0*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
Generation	**Platform**	**Number of Cores**	**Derivative**	**Qual Status**	**Temperature Range**	**Encryption**	**Package Type**	**CPU Frequency**	**DDR Speed**	**Die Revision**
P = 45nm	1–5	01 = Single core 02 = Dual core	0–9	P = Prototype N = Qual'd to Industrial Tier	S = Std Temp X = Ext. Temp	E = SEC Present N = SEC Not Present	2 = TEPBGA2 Pb free	H = 800 MHz K = 1000 MHz M = 1200 MHz N = 1333 MHz	F = 667 MHz H = 800 MHz	A = Rev 1.0 B = Rev 2.0 C = Rev 2.1

4.2.1 Part Marking

Parts are marked as in the example shown in Figure 62.



TePBGA II

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.
P2010xtencdr is the orderable part number. See Table 85 for details.

Figure 62. Part Marking for WB-TePBGA Device

5 Product Documentation

The following documents are required for a complete description of the device and are needed to design properly with the part:

- *P2020 QorIQ Integrated Processor Reference Manual* (document number P2020RM)
- *e500 PowerPC Core Reference Manual* (E500CORERM)

6 Revision History

Table 86 provides a revision history for the this hardware specification.

Table 86. Document Revision History

Rev. Number	Date	Substantive Change(s)
2	08/2013	• In the features list, removed "(T_j) range: 0-125 °C and -40 °C-125 °C (industrial standard)" from the "Operating junction temperature" bullet point. • In the features list, changed the 36-bit physical addressing clock frequency from 1.2 GHz to 1.33 GHz. • In Table 1, added overbar to the signal TEST_SEL. • In Table 3, modified the recommended value for DDR2 and DDR3 DRAM reference input voltages. • In Table 5, added rows for core frequency = 1333. • In Table 17 and Table 18, updated footnote 2. • In Table 85, added CPU frequency N = 1333.

Table 86. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
1	03/2012	• In Table 1, "P2010 Pinout Listing [1]," updated the text corresponding to footnote 16 from: "When eTSEC1 and eTSEC2 are used as parallel interfaces, pins TSEC1_TX_EN and TSEC2_TX_EN require an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven. TSEC2_TXD[05] is a POR configuration pin for eSDHC card-detect (cfg_sdhc_cd_pol_sel) and also has an alternate function as TSEC3_TX_EN. When using eTSEC3 as a parallel interface, the TSEC3_TX_EN requires a pull down. However, because the pull-down resistor on TSEC2_TXD[05]/TSEC3_TX_EN signal causes the eSDHC card-detect (cfg_sdhc_cd_pol_sel) to be inverted, the inversion must be overridden from the SDHCDCR [CD_INV] debug control register." to: "TSEC2_TXD[05] is a POR configuration pin for eSDHC card-detect (cfg_sdhc_cd_pol_sel), and it also has an alternate function of TSEC3_TX_EN. When eTSEC1 or eTSEC2 or eTSEC3 are used as parallel interfaces, the TSECx_TX_EN pins require an external 4.7-k pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven. However, the pull-down resistor on TSEC3_TX_EN causes the eSDHC card-detect (cfg_sdhc_cd_sel) to be inverted; the inversion should be overridden from the SDHCDCR[CD_INV] debug control register. If the device is configured to boot from the eSDHC interface, the SDHC_CD should be inverted on the board." • In Table 2, "Absolute Maximum Ratings[1]," for DDR2/DDR3 DRAM signals and reference rows, updated the value in the "Maximum" column from "–0.3 to (GV_{DD} + 0.3)" to "–0.3 to (GV_{DD} + 0.3)" and "–0.3 to (GV_{DD}/2 + 0.3)," respectively. • In Table 2, "Absolute Maximum Ratings[1]," for the SerDes row, updated the value in the "Maximum" column from "–0.3 to (OV_{DD} + 0.3)" to "–0.3 to (XV_{DD} + 0.3)." • In Table 6, I/O Power Supply Estimated Values," added "RMII" to the "Parameters" column for the eTSEC row that corresponds to LVDD (2.5 V), and added "MII, GMII, TBI, RMII, and 1588" to the "Parameters" column for the eTSEC row that corresponds to LVDD (3.3 V). • In Section 2.10.1.1, "IEEE 1588, GMII, MII, TBI, RGMII, RMII, and RTBI DC Electrical Characteristics," Table 31, IEEE 1588, GMII, MII, RMII, and TBI DC Electrical Characteristics at LV_{DD} = 3.3 V," and Table 32, "IEEE 1588, GMII, MII, RMII, RGMII, RTBI, and TBI DC Electrical Characteristics at LV_{DD} = 2.5 V," added "IEEE 1588" to the title. • In Table 31, IEEE 1588, GMII, MII, RMII, and TBI DC Electrical Characteristics at LV_{DD} = 3.3 V," added "IEEE 1588" to the cell containing the "Input high voltage" parameter. • In Table 42, "RMII Receive AC Timing Specifications," updated the parameter "RXD[1:0], CRS_DV, RX_ER setup time to TSEC*n*_RX_CLK rising edge" to "RXD[1:0], CRS_DV, RX_ER setup time to TSEC*n*_TX_CLK rising edge," and the parameter "RXD[1:0], CRS_DV, RX_ER hold time to TSEC*n*_RX_CLK rising edge" to "RXD[1:0], CRS_DV, RX_ER hold time to TSEC*n*_TX_CLK rising edge." • In Figure 26, "RMII Receive AC Timing Diagram," changed "TSECn_RX_CLK" to "TSECn_TX_CLK." • In Table 58, "Enhanced Local Bus DC Electrical Characteristics (1.8 V DC)," in the "Parameters" column, changed "Low-level output voltage (BV_{DD} = min, IOH = –0.5 mA)" to "Low-level output voltage (BV_{DD} = min, IOH = 0.5 mA)." • In Table 61, "eSDHC Interface DC Electrical Characteristics (CVDD = 3.3 V)," changed the minimum value of parameter "Input leakage current" from "–40" to "–70." • In Figure 42, "eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock," changed "t_{HSIVKH}" to "$t_{SHSIVKH}$" and changed "t_{HSIXKH}" to "$t_{SHSIXKH}$." • In Table 66, "JTAG AC Timing Specifications (Independent of SYSCLK)," changed parameter "JTAG external clock pulse width measured at 1.4 V" to "JTAG external clock pulse width measured at OV_{DD}/2."

Table 86. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
1 continued	03/2012	• In Table 75, "SD_REF_CLK and SD_REF_CLK Input Clock Requirements," added the following footnote to the table and added it to the "Notes" column of row "SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle": "7. Measurement taken from the differential waveform." • In Table 75, "SD_REF_CLK and SD_REF_CLK Input Clock Requirements," removed "(Measure at 1.6 V)" from parameter "SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle." • In Figure 59, "Differential Peak-Peak Voltage of Transmitter or Receiver," changed "Differential Peak-Peak = 2 ℜ× (A,Ä" to "Differential Peak-Peak = 2*V_{DIFFp}." • In Section 2.2, "Power Sequencing," added the following warning: "Only 100,000 POR cycles are permitted per lifetime of a device." • In Table 45, "SGMII Transmit AC Timing Specifications," updated the minimum value for the AC coupling capacitor parameter from 5 to 10. • In Table 42, "RMII Receive AC Timing Specifications," removed note from "TSECn_TX_CLK (reference clock) clock period" row. • In Table 58, "Enhanced Local Bus DC Electrical Characteristics (1.8 V DC)," changed parameter from "Low-level output voltage (BV_{DD} = min, IOH = 0.5 mA)" to "Low-level output voltage (BV_{DD} = min, IOL = 0.5 mA)." • In Figure 42, "eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock," updated text from "VM = Midpoint Voltage (OV_{DD}/2)" to "VM = Midpoint Voltage (CV_{DD}/2)." • In Figure 41, "eSDHC Clock Input Timing Diagram," updated the text from "VM = Midpoint Voltage (OVDD/2)" to "VM = Midpoint Voltage (CVDD/2)."
0	04/2011	Initial public release

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08/2013