

## MC34063A / MC33063A SMPS Controller

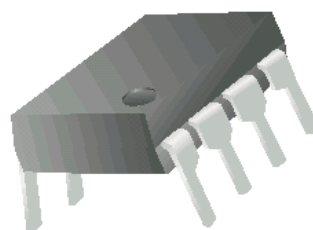
### Features

- Operation from 3.0 to 40V Input
- Short Circuit Current Limiting
- Low Standby Current
- Output Switch Current of 1.5A Without External Transistors
- Adjustable Output Voltage
- Frequency of Operation from 100Hz to 100KHz
- Step-up, Step Down, or Inverting Switching Regulators

### Description

The MC34063A/MC33063A is a monolithic regulator subsystem intended for a DC to DC converter. The device contains a temperature-compensated bandgap reference, a duty cycle control oscillator, driver, and high-current output switch. It can be used for step-down, step-up, or inverting switching and series pass regulators.


8-DIP




8-SOP



### Ordering Information

Part Number	Operating Temperature Range	 Eco Status	Package
MC34063AP	0 ~ +70°C	RoHS	8-DIP
MC34063AD	0 ~ +70°C	RoHS	8-SOP
MC33063AP	-40 ~ +85°C	RoHS	8-DIP
MC33063AD	-40 ~ +85°C	RoHS	8-SOP

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### Block Diagram

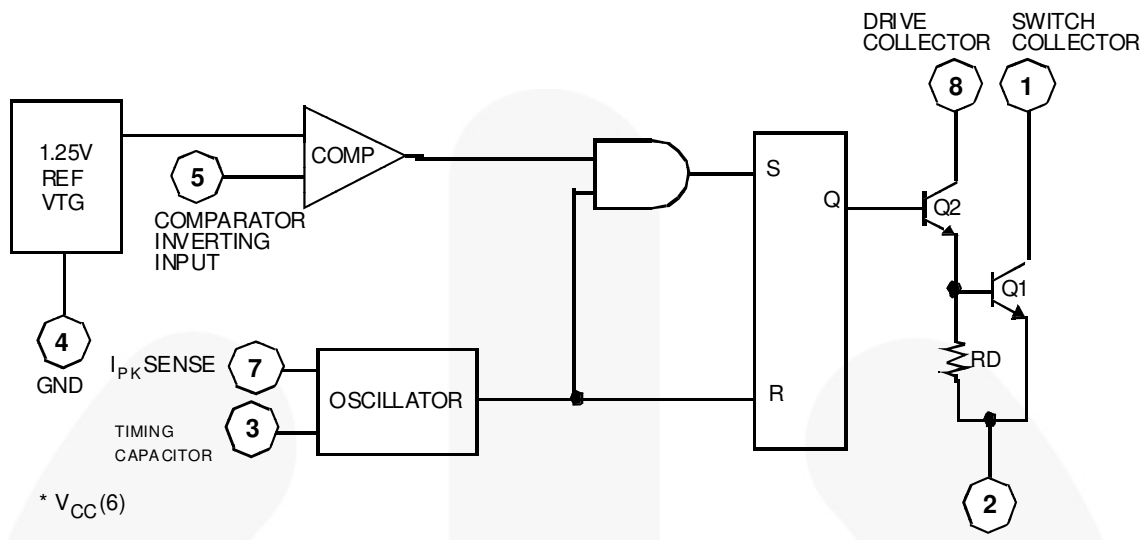


Figure 1. Block Diagram



## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply Voltage		40	V
$V_{I(Comp)}$	Comparator Input Voltage Range	-0.3	+40	V
$V_{C(SW)}$	Switch Collector Voltage		40	V
$V_{E(SW)}$	Switch Emitter Voltage		40	V
$V_{CE(SW)}$	Switch Collector to Emitter Voltage		40	V
$V_{C(DR)}$	Driver Collector Voltage		40	V
$I_{SW}$	Switch Current		1.5	A
$T_{STG}$	Storage Temperature Range	-65	+150	°C
$P_D$	Power Dissipation	SOP	0.8	W
		DIP	1	

## Electrical Characteristics

$V_{CC} = 5.0V$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$  for MC34063,  $T_A = -40^\circ C$  to  $+85^\circ C$  for MC33063, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
<b>Oscillator</b>							
$I_{CHG}$	Charging Current	$V_{CC}=5$ to $40V$ , $T_A=25^\circ C$	22	31	42	$\mu A$	
$I_{DISCHG}$	Discharging Current	$V_{CC}=5$ to $40V$ , $T_A=25^\circ C$	140	190	260	$\mu A$	
$V_{(OSC)}$	Oscillator Amplitude	$T_A=25^\circ C$		0.5		V	
K	Discharge-to-Charge Current Ratio	$V_7=V_{CC}$ , $T_A=25^\circ C$	5.2	6.1	7.5		
$V_{SENSE(CL)}$	Current Limit Sense Voltage	$I_{CHG}=I_{DISCHG}$ , $T_A=25^\circ C$	250	300	350	mV	
<b>Output Switch</b>							
$V_{CE(SAT)1}$	Saturation Voltage 1 <sup>(1)</sup>	$I_{SW}=1.0A$ , $V_{C(driver)}=V_{C(SW)}$		0.95	1.30	V	
$V_{CE(SAT)2}$	Saturation Voltage 2 <sup>(1)</sup>	$I_{SW}=1.0A$ , $V_{C(driver)}=50mA$		0.45	0.70	V	
$G_{I(DC)}$	DC Current Gain <sup>(1)</sup>	$I_{SW}=1.0A$ , $V_{CE}=5.0V$ , $T_A=25^\circ C$	50	180			
$I_{C(OFF)}$	Collector Off-State Current <sup>(1)</sup>	$V_{CE}=40V$ , $T_A=25^\circ C$		0.01	100.00	$\mu A$	
<b>Comparator</b>							
$V_{TH}$	Threshold Voltage		1.21	1.24	1.29	V	
$\Delta V_{TH}$	Threshold Voltage Line Regulation	$V_{CC}=3$ to $40V$		2	5	mV	
$I_{BIAS}$	Input Bias Current	$V_I=0V$		50	400	nA	
<b>Total Device</b>							
$I_{CC}$	Supply Current	MC34063	$V_{CC}=5$ to $40V$ , $C_T=0.001\mu F$ , $V_7=V_{CC}$ , $V_5>V_{TH}$ , pin 2=GND			4	mA
		MC33063				5	

### Note:

- Output switch tests are performed under pulsed conditions to minimize power dissipation.

### Typical Performance Characteristics

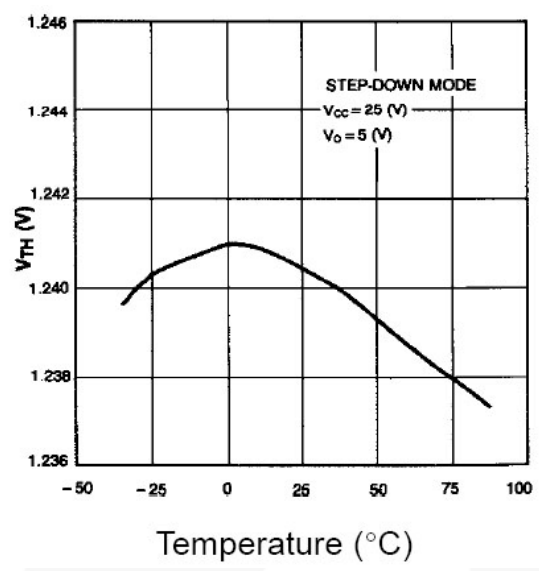


Figure 2. Temperature Drift ( $V_{TH}$ )

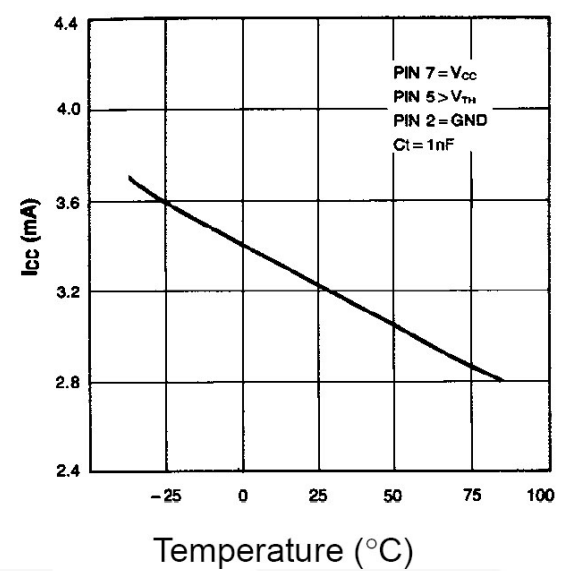
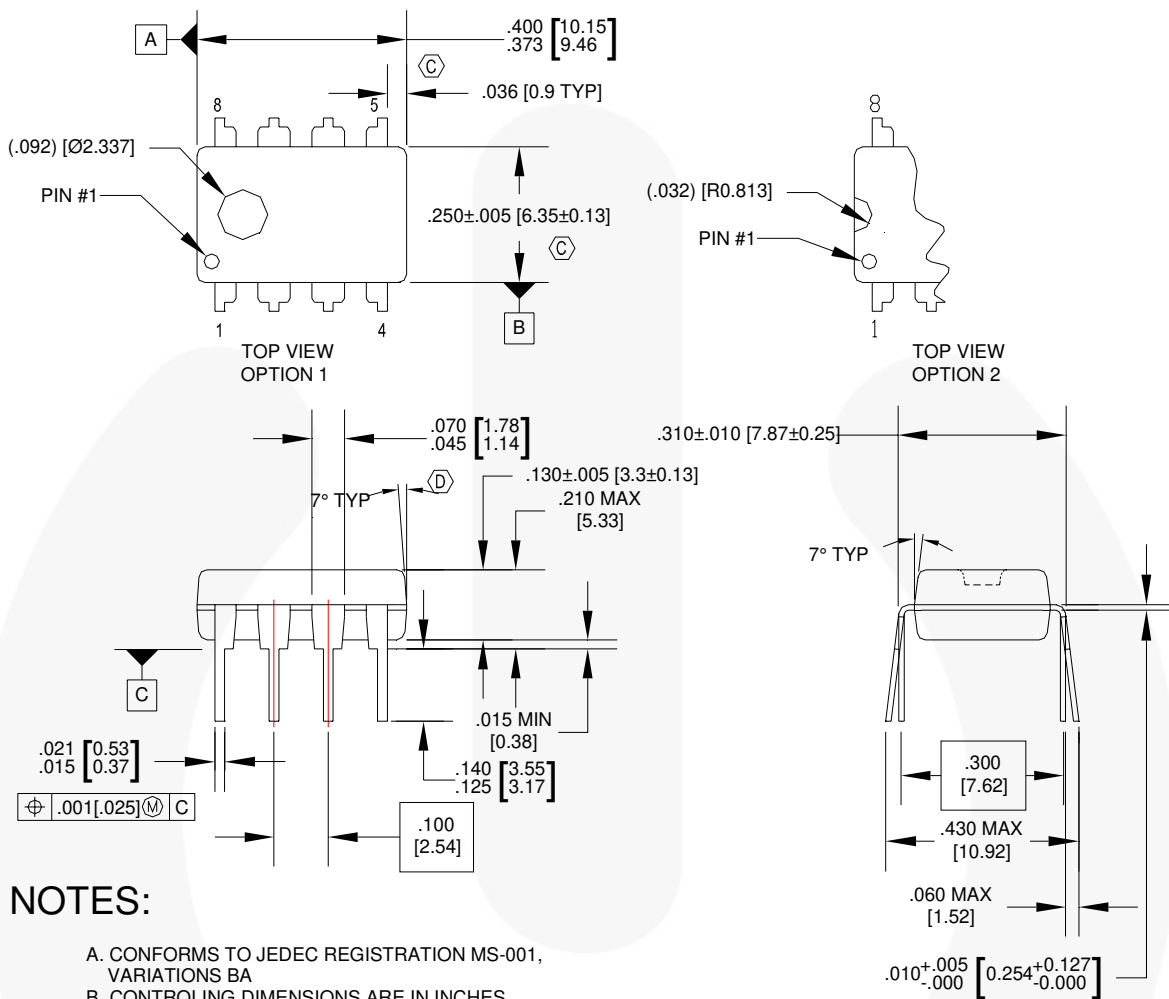


Figure 3. Temperature Drift ( $I_{CC}$ )

## Physical Dimensions



### NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS BA
- B. CONTROLLING DIMENSIONS ARE IN INCHES  
REFERENCE DIMENSIONS ARE IN MILLIMETERS
- C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED  
.010 INCHES OR 0.25MM.
- D. DOES NOT INCLUDE DAMBAR PROTRUSIONS.  
DAMBAR PROTRUSIONS SHALL NOT EXCEED  
.010 INCHES OR 0.25MM.
- E. DIMENSIONING AND TOLERANCING  
PER ASME Y14.5M-1994.

N08EREVG

Figure 4. 8-Lead PDIP, JEDEC MS-001

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

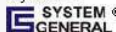
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