STEVAL-IPE005V1

Demonstration programmer board based on the STPM01

Data Brief

Features

- Full compatible with the STPM01 energy meter and with the appropriate manager software
- Integrated system designed to provide a complete, ready-to-use energy meter
- High-end solution for power metering based on the STR710 Microcontroller with embedded RTC
- External memory interface (EMI) ready to drive 1 Mbyte of on-board SRAM.
- On-board optical insulated serial line
- On-board charge pump
- Access to the STPM01 device registers, using a dedicated SPI bus interface

Applications

- Demonstration purposes:
  - connecting the demonstration board to an AC power source and changing all the settings parameters through the GUI interface and the hardware programmer/ reader board
- To evaluate and develop a custom application

Description

The STEVAL-IPE005V1 demonstration board works in conjunction with the STPM01 energy meter ASSP device and with the STPM01 manager software. It is an integrated system designed to provide the user with a complete, ready-to-use energy meter application. This board is a high-end solution for power metering based on the STR710 microcontroller with an embedded RTC and an external memory interface (EMI) ready to drive 1Mbyte of on-board SRAM. The demonstration board also integrates an on-board optical insulated serial line allowing isolation of the board ground reference in order to avoid propagation of over-voltage on the PC side.

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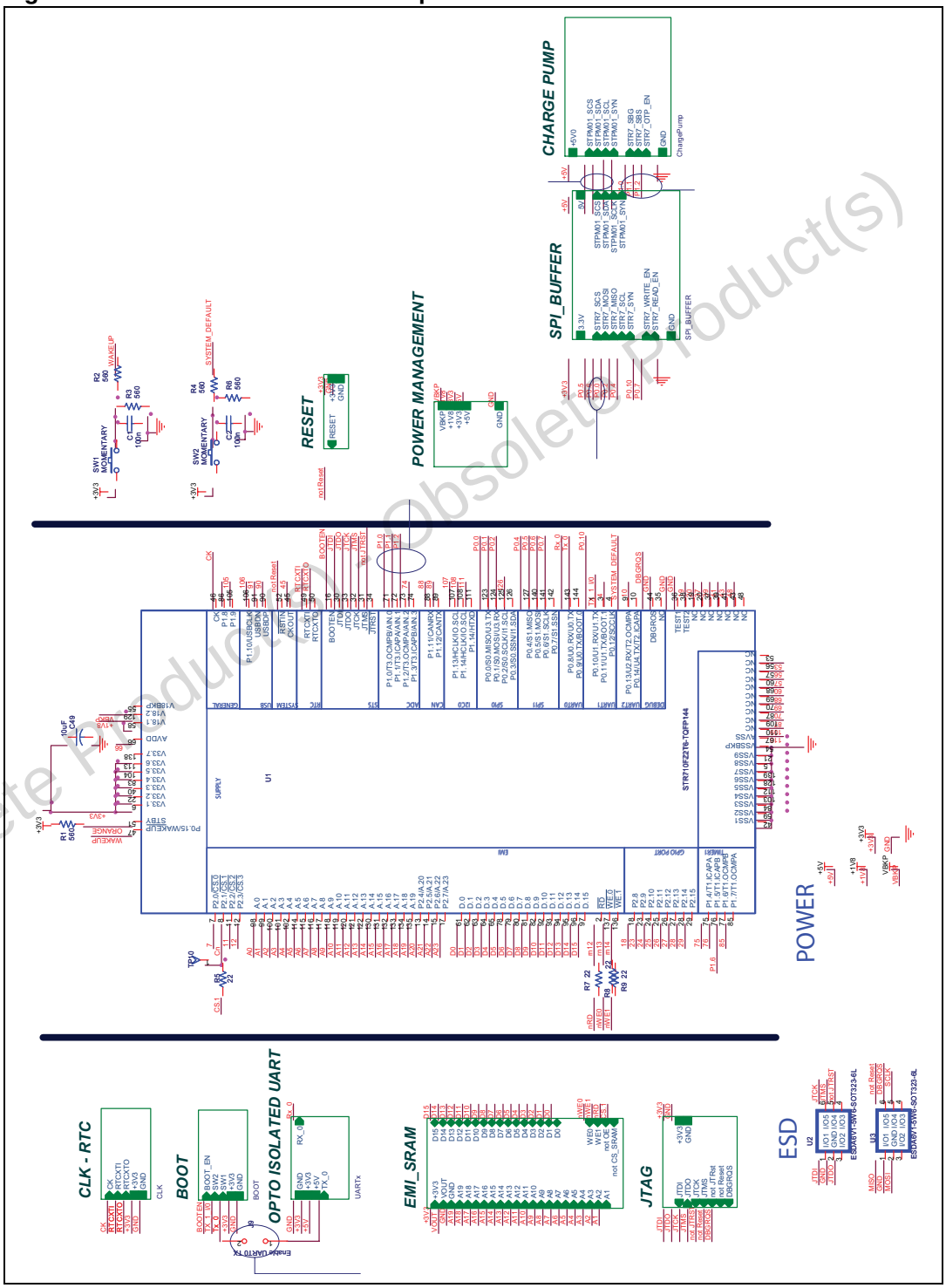
Moreover, the on-board charge pump allows burning the STPM01 energy meter ASSP device registers.

Access to the STPM01 device registers is ensured using a dedicated SPI bus interface. The STPM01 programmer kit demonstrates how effectively the STPM01 can be used in real-world energy meter applications and it helps the user to develop his own application.

1 Demonstration board schematics

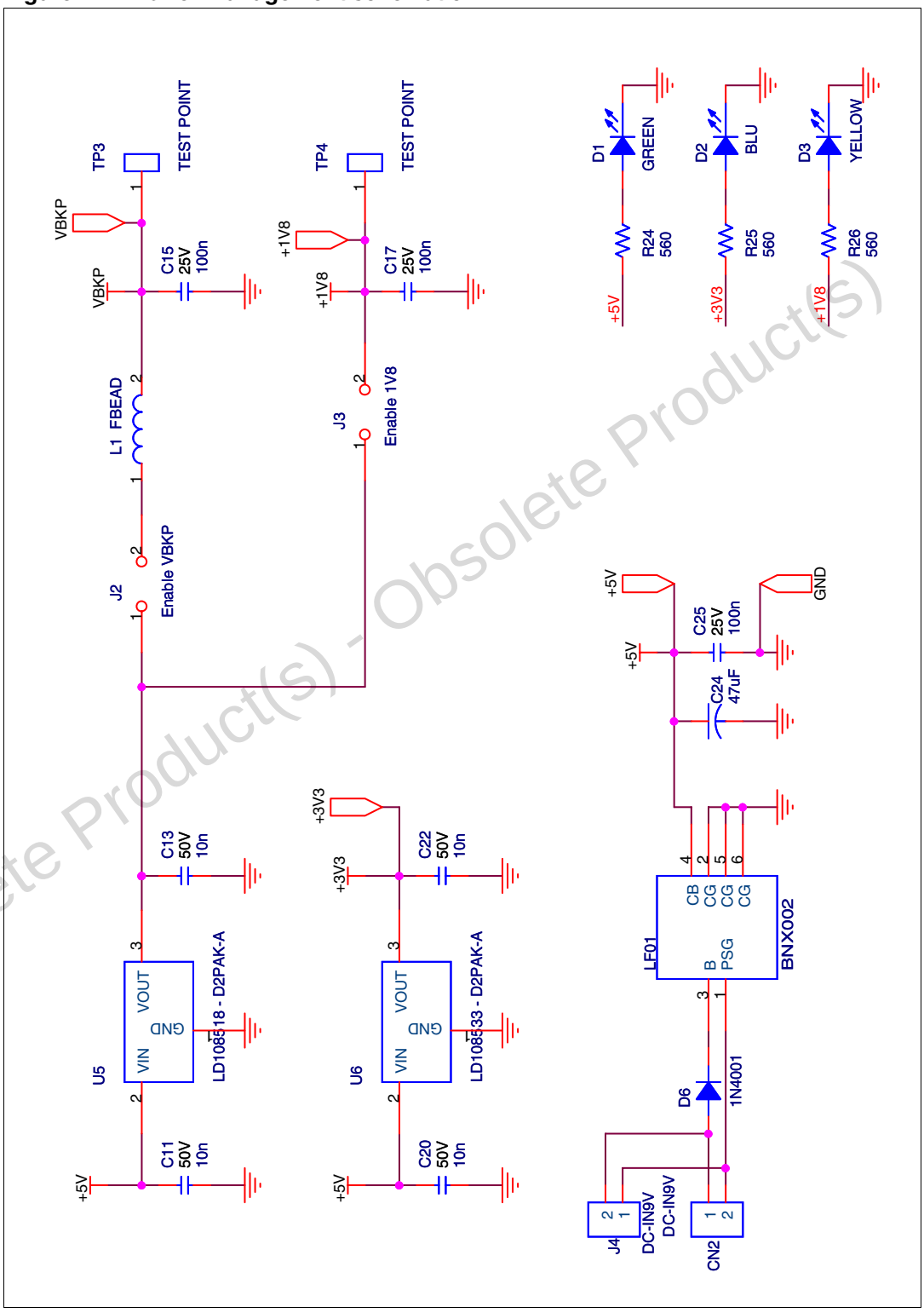
1.1 Microcontroller and main parts schematic

Figure 1. Microcontroller and main parts schematic



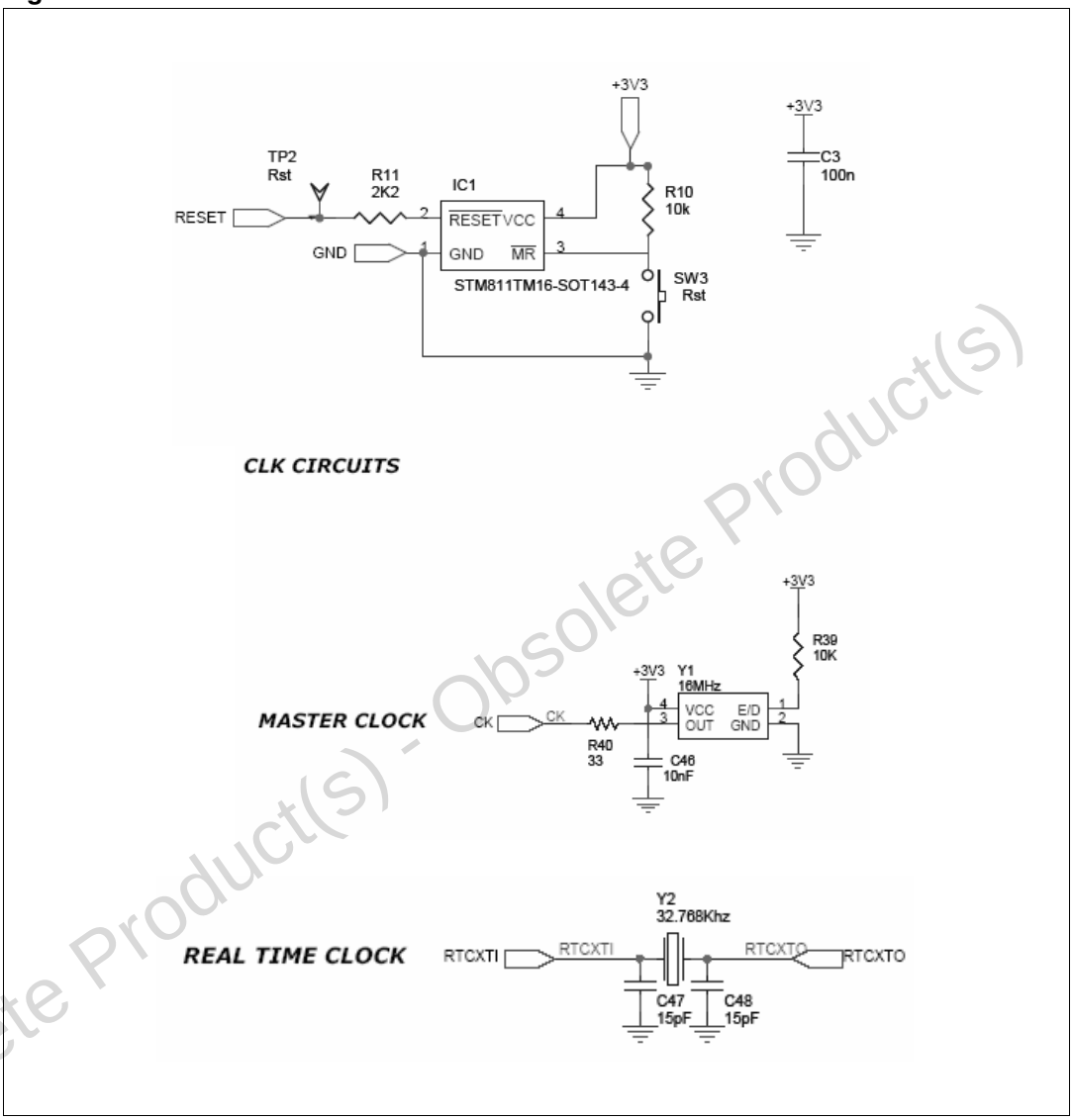
1.2 Power management

Figure 2. Power management schematic



1.3 Reset and clock circuits

Figure 3. Reset and clock circuits



1.4 Boot management and Jtag circuit

Figure 4. Boot management and Jtag circuits

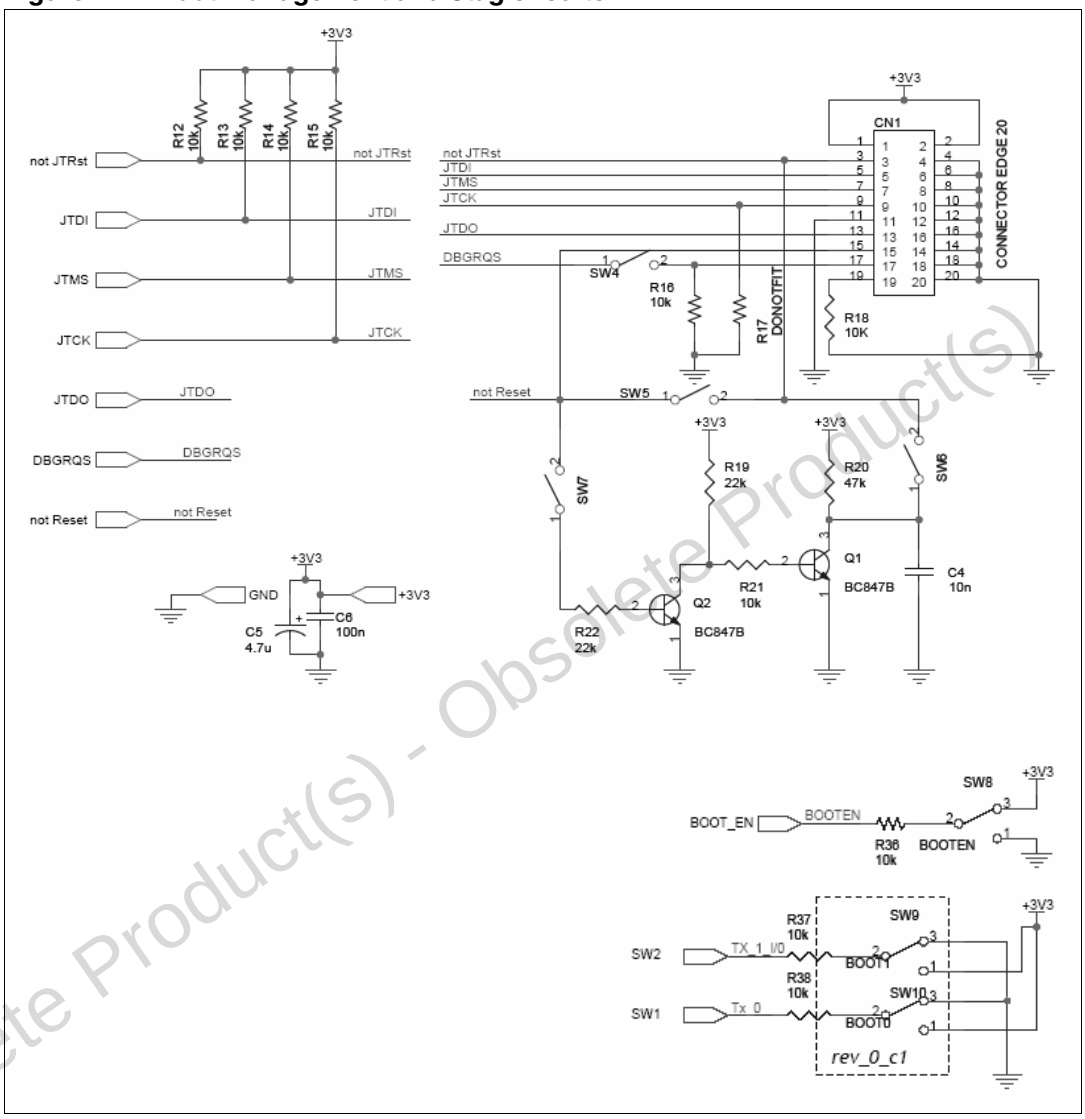
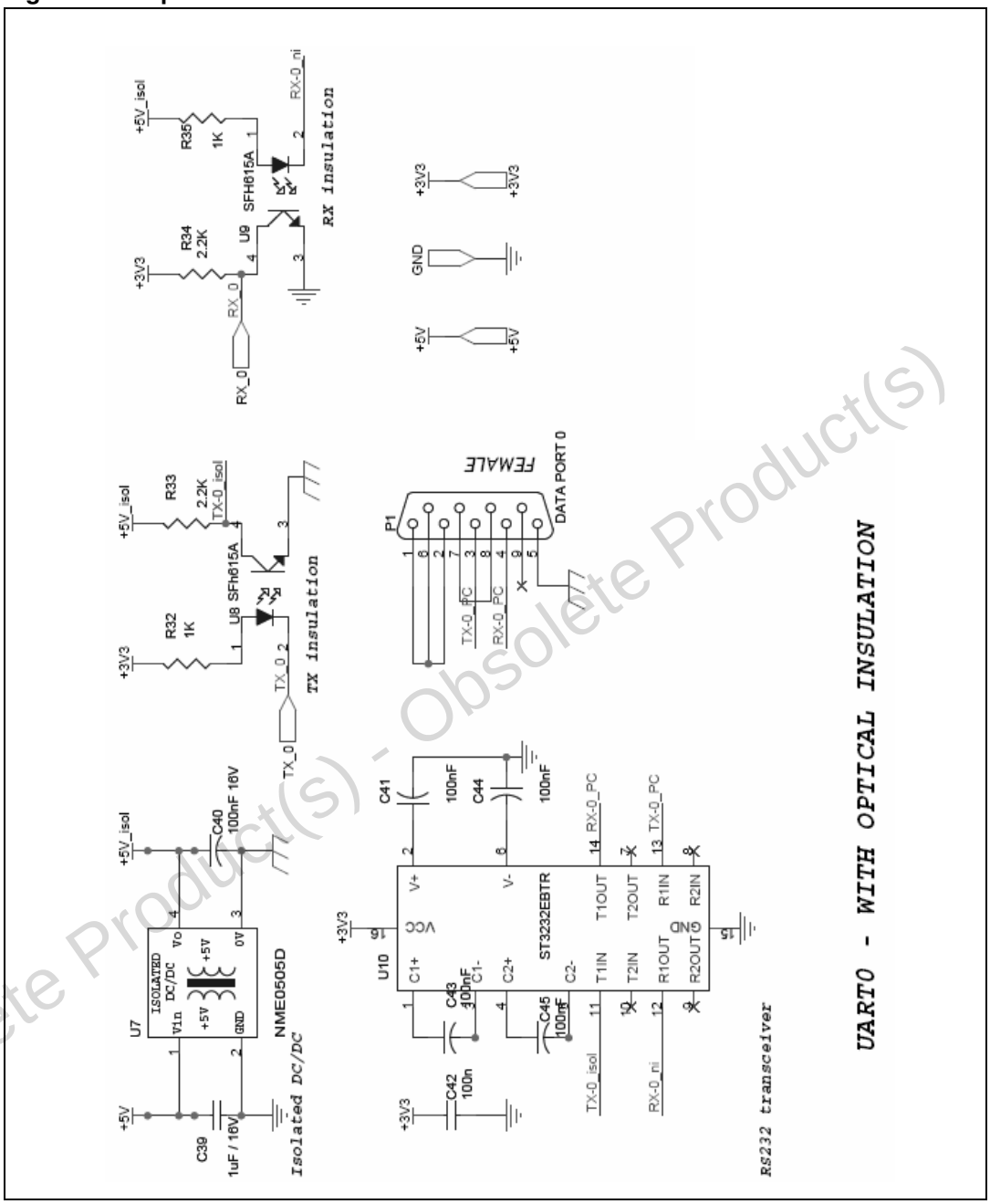
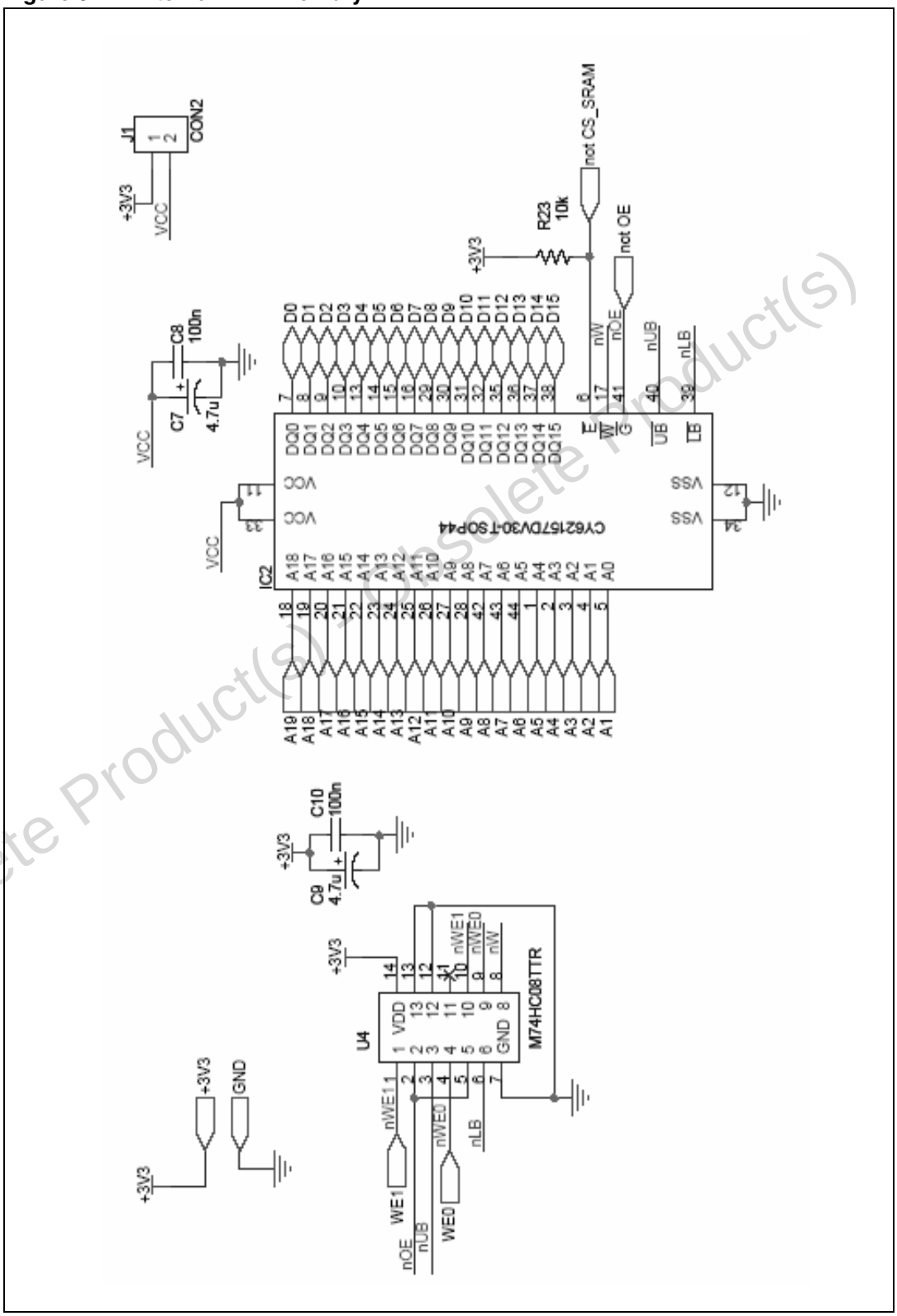


Figure 5. Opto-isolated UART



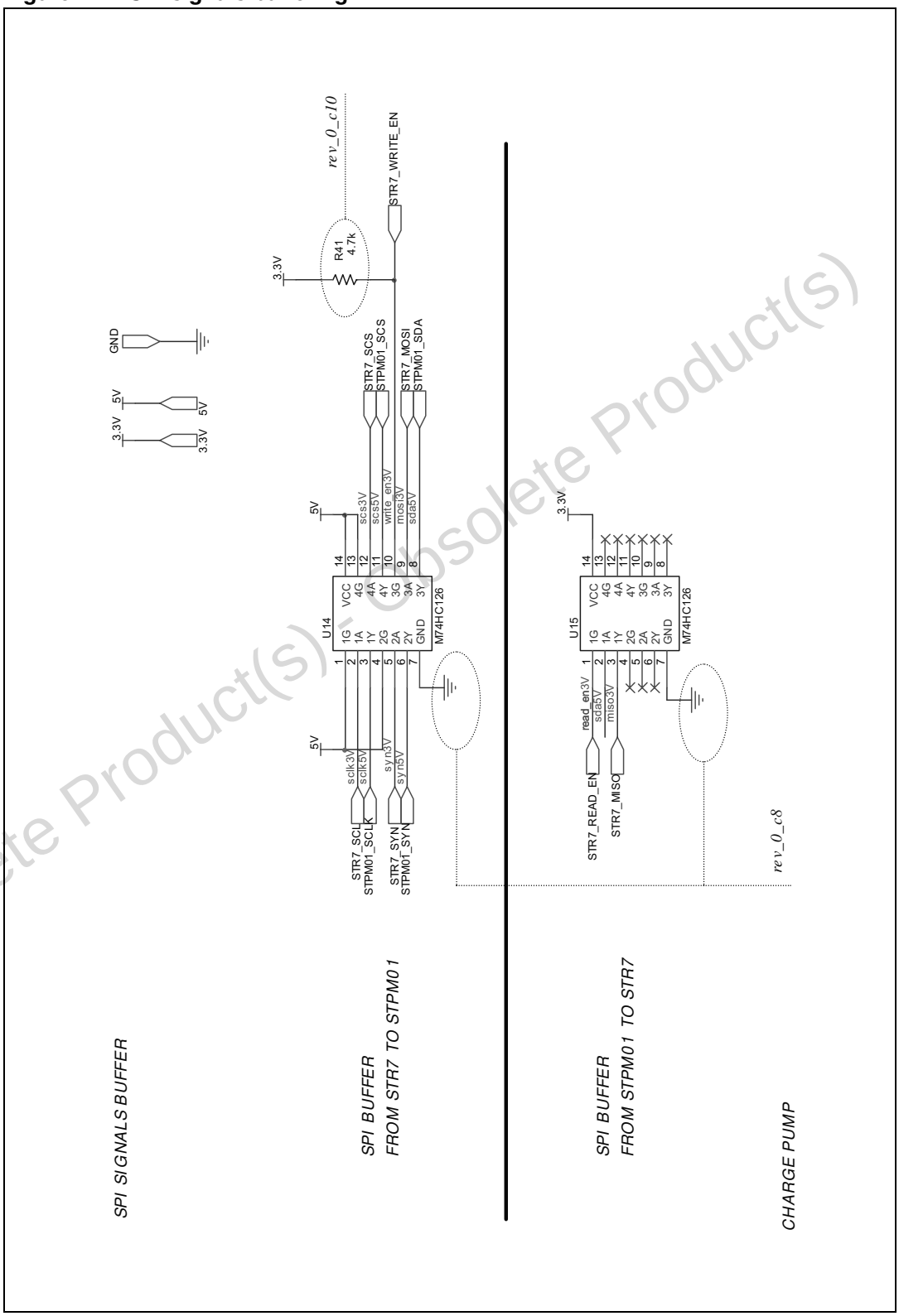
1.5 External RAM memory

Figure 6. External RAM memory



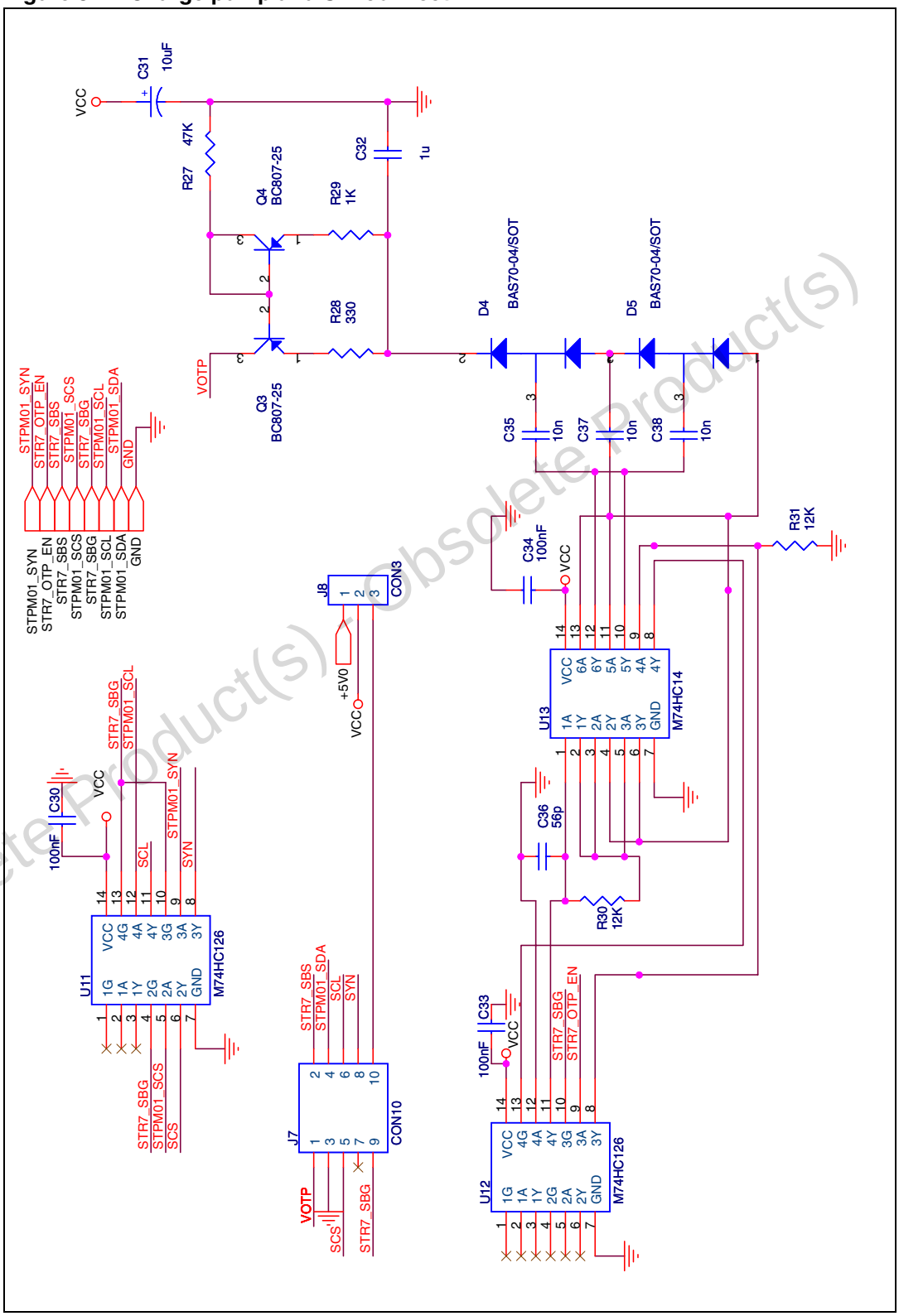
1.6 SPI signals buffering

Figure 7. SPI signals buffering



1.7 Charge pump and SPI connector

Figure 8. Charge pump and SPI connect



2 Revision history

Table 1. Document revision history

Date	Revision	Changes
24-Nov-2008	1	Initial release.

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