

FEATURES

- Low offset voltage: 2.5 μV maximum
- Low offset voltage drift: 0.015 $\mu\text{V}/^\circ\text{C}$ maximum
- Low noise
 - 5.6 nV/ $\sqrt{\text{Hz}}$ at $f = 1 \text{ kHz}$, $A_V = +100$
 - 97 nV p-p at $f = 0.1 \text{ Hz}$ to 10 Hz , $A_V = +100$
- Open-loop gain: 130 dB minimum
- CMRR: 135 dB minimum
- PSRR: 130 dB minimum
- Unity-gain crossover: 4 MHz
- Gain bandwidth product: 3 MHz at $A_V = +100$
- 3 dB closed-loop bandwidth: 6.2 MHz
- Single-supply operation: 2.2 V to 5.5 V
- Dual-supply operation: $\pm 1.1 \text{ V}$ to $\pm 2.75 \text{ V}$
- Rail-to-rail input and output (RRIO)
- Unity-gain stable

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Extended industrial temperature range: -55°C to $+125^\circ\text{C}$
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available upon request

APPLICATIONS

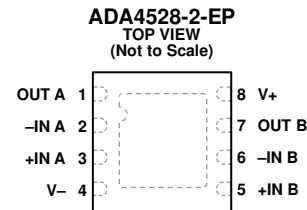
- Thermocouples/thermopiles
- Load cell and bridge transducers
- Precision instrumentation
- Electronic scales
- Medical instrumentation
- Handheld test equipment

GENERAL DESCRIPTION

The [ADA4528-2-EP](#) is an ultralow noise, zero-drift operational amplifier featuring rail-to-rail input and output swing. With an offset voltage of 2.5 μV , offset voltage drift of 0.015 $\mu\text{V}/^\circ\text{C}$, and typical noise of 97 nV p-p (0.1 Hz to 10 Hz, $A_V = +100$), the [ADA4528-2-EP](#) is well suited for applications in which error sources cannot be tolerated.

The [ADA4528-2-EP](#) has a wide operating supply range of 2.2 V to 5.5 V, high gain, and excellent CMRR and PSRR specifications,

PIN CONNECTION DIAGRAM



NOTES
1. CONNECT THE EXPOSED PAD TO V- OR LEAVE IT UNCONNECTED.

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Figure 1.

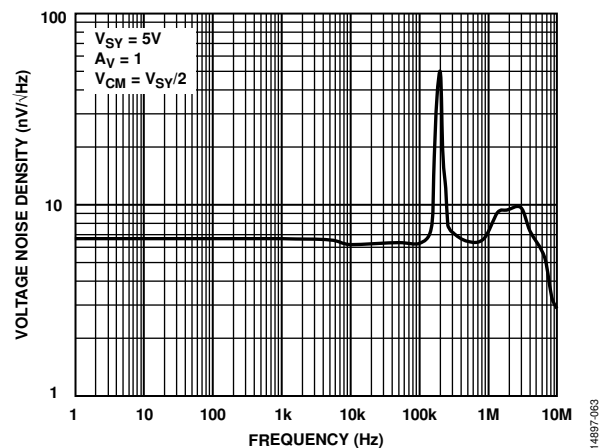


Figure 2. Voltage Noise Density vs. Frequency

which make it ideal for applications that require precision amplification of low level signals, such as position and pressure sensors, strain gages, and medical instrumentation.

The [ADA4528-2-EP](#) is specified over the extended industrial temperature range (-55°C to $+125^\circ\text{C}$) and is available in an 8-lead LFCSP package.

Additional application and technical information can be found in the [ADA4528-2](#) datasheet.

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REVISION HISTORY

8/2016—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

$V_{SY} = 2.5\text{ V}$, $V_{CM} = V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = 0\text{ V to }2.5\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.3	2.5	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.002	0.018	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		220	400	pA
Input Offset Current	I_{OS}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		440	800	pA
Input Voltage Range			0		2.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }2.5\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	135	158		dB
Open-Loop Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $V_O = 0.1\text{ V to }2.4\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	116	140		dB
		$R_L = 2\text{ k}\Omega$, $V_O = 0.1\text{ V to }2.4\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	126	132		dB
Input Resistance						
Differential Mode	R_{INDM}			225		k Ω
Common Mode	R_{INCM}			1		G Ω
Input Capacitance						
Differential Mode	C_{INDM}			15		pF
Common Mode	C_{INCM}			30		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 10\text{ k}\Omega$ to V_{CM} $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.49	2.495		V
			2.485			V
		$R_L = 2\text{ k}\Omega$ to V_{CM} $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.46	2.48		V
			2.44			V
Output Voltage Low	V_{OL}	$R_L = 10\text{ k}\Omega$ to V_{CM} $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	10	mV
					15	mV
		$R_L = 2\text{ k}\Omega$ to V_{CM} $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	40	mV
					60	mV
Short-Circuit Current	I_{SC}			± 30		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1\text{ kHz}$, $A_V = +10$		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.2\text{ V to }5.5\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	130	150		dB
			127			dB
Supply Current per Amplifier	I_{SY}	$I_O = 0\text{ mA}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.4	1.7	mA
					2.1	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1$		0.45		V/ μs
Settling Time to 0.1%	t_s	$V_{IN} = 1.5\text{ V step}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = -1$		7		μs
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1$		4		MHz
Phase Margin	Φ_M	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1$		57		Degrees
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +100$		3		MHz
-3 dB Closed-Loop Bandwidth	f_{-3dB}	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1$		6.2		MHz
Overload Recovery Time		$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = -10$		50		μs

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	$f = 0.1 \text{ Hz to } 10 \text{ Hz}, A_v = +100$		97		nV p-p
Voltage Noise Density	e_n	$f = 1 \text{ kHz}, A_v = +100$		5.6		nV/ $\sqrt{\text{Hz}}$
		$f = 1 \text{ kHz}, A_v = +100, V_{CM} = 2.0 \text{ V}$		5.5		nV/ $\sqrt{\text{Hz}}$
Current Noise	i_n p-p	$f = 0.1 \text{ Hz to } 10 \text{ Hz}, A_v = +100$		10		pA p-p
Current Noise Density	i_n	$f = 1 \text{ kHz}, A_v = +100$		0.7		pA/ $\sqrt{\text{Hz}}$

ELECTRICAL CHARACTERISTICS—5 V OPERATION

$V_{SY} = 5\text{ V}$, $V_{CM} = V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = 0\text{ V to }5\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.3	2.5	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.002	0.015	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		125	250	pA
Input Offset Current	I_{OS}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		250	500	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }5\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	137	160		dB
Open-Loop Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $V_O = 0.1\text{ V to }4.9\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	127	139		dB
		$R_L = 2\text{ k}\Omega$, $V_O = 0.1\text{ V to }4.9\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	121	131		dB
			120			dB
Input Resistance				190		$\text{k}\Omega$
Differential Mode	R_{INDM}					
Common Mode	R_{INCM}			1		$\text{G}\Omega$
Input Capacitance						
Differential Mode	C_{INDM}			16.5		pF
Common Mode	C_{INCM}			33		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 10\text{ k}\Omega$ to V_{CM} $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.99	4.995		V
		$R_L = 2\text{ k}\Omega$ to V_{CM} $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.98			V
			4.96	4.98		V
			4.94			V
Output Voltage Low	V_{OL}	$R_L = 10\text{ k}\Omega$ to V_{CM} $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	10	mV
		$R_L = 2\text{ k}\Omega$ to V_{CM} $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	40	mV
					60	mV
Short-Circuit Current	I_{SC}			± 40		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1\text{ kHz}$, $A_V = +10$		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.2\text{ V to }5.5\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	130	150		dB
			127			dB
Supply Current per Amplifier	I_{SY}	$I_O = 0\text{ mA}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.5	1.8	mA
					2.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1$		0.5		$\text{V}/\mu\text{s}$
Settling Time to 0.1%	t_s	$V_{IN} = 4\text{ V step}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = -1$		10		μs
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1$		4		MHz
Phase Margin	Φ_M	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1$		57		Degrees
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +100$		3.4		MHz
-3 dB Closed-Loop Bandwidth	f_{-3dB}	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1$		6.5		MHz
Overload Recovery Time		$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = -10$		50		μs
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	$f = 0.1\text{ Hz to }10\text{ Hz}$, $A_V = +100$		99		nV p-p
Voltage Noise Density	e_n	$f = 1\text{ kHz}$, $A_V = +100$		5.9		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$, $A_V = +100$, $V_{CM} = 4.5\text{ V}$		5.3		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise	i_n p-p	$f = 0.1\text{ Hz to }10\text{ Hz}$, $A_V = +100$		10		pA p-p
Current Noise Density	i_n	$f = 1\text{ kHz}$, $A_V = +100$		0.5		$\text{pA}/\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	$\pm V_{SY} \pm 0.3$ V
Input Current ¹	± 10 mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

¹ The input pins have clamp diodes to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment.

Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure (still air).

θ_{JC} is the junction to case thermal resistance, measured on the exposed pad of the package.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-8-19 ¹	52	3.9	°C/W

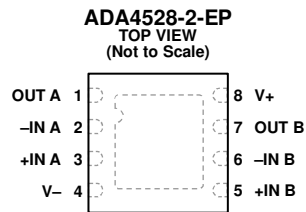
¹ Thermal reporting per JEDEC JESD51-12.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. CONNECT THE EXPOSED PAD TO V- OR LEAVE IT UNCONNECTED.

14887-207

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A.
2	-IN A	Inverting Input, Channel A.
3	+IN A	Noninverting Input, Channel A.
4	V-	Negative Supply Voltage.
5	+IN B	Noninverting Input, Channel B.
6	-IN B	Inverting Input, Channel B.
7	OUT B	Output, Channel B.
8	V+	Positive Supply Voltage.
	EPAD	Exposed Pad. Connect the exposed pad to V- or leave it unconnected.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

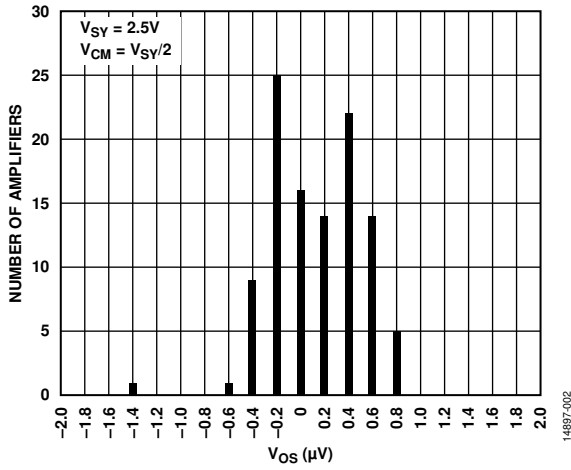


Figure 4. Input Offset Voltage (V_{OS}) Distribution

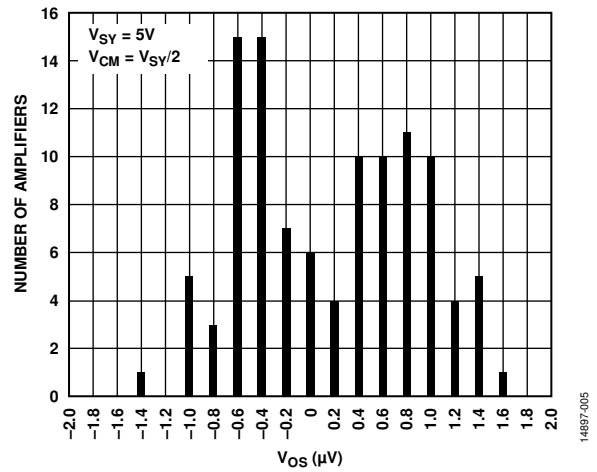


Figure 7. Input Offset Voltage (V_{OS}) Distribution

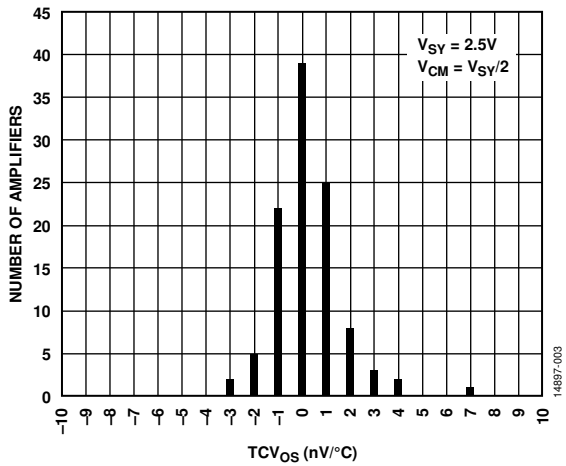


Figure 5. Input Offset Voltage Temperature Coefficient ($TC_{V_{OS}}$) Drift Distribution

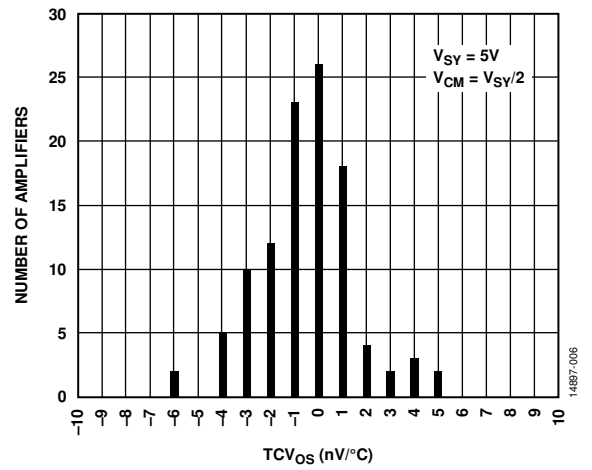


Figure 8. Input Offset Voltage Temperature Coefficient ($TC_{V_{OS}}$) Drift Distribution

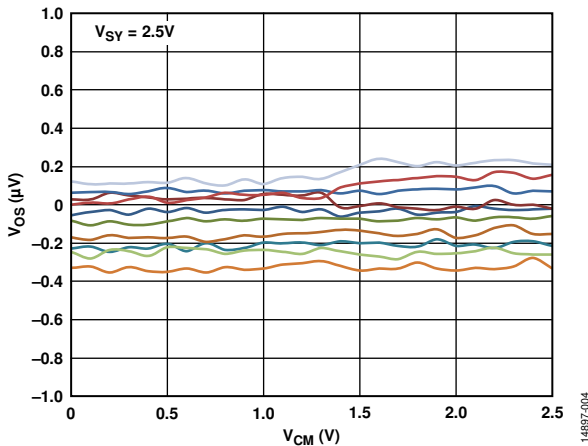


Figure 6. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM})

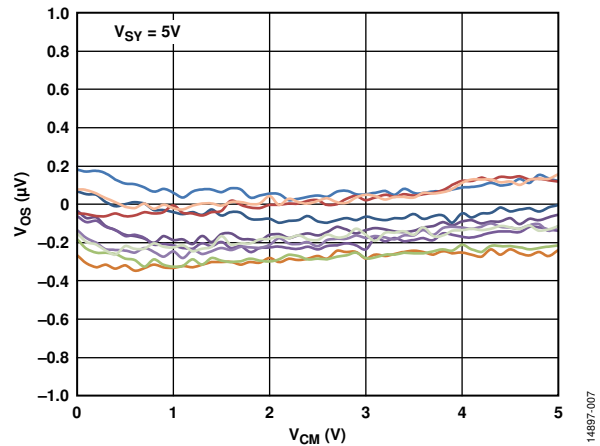


Figure 9. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM})

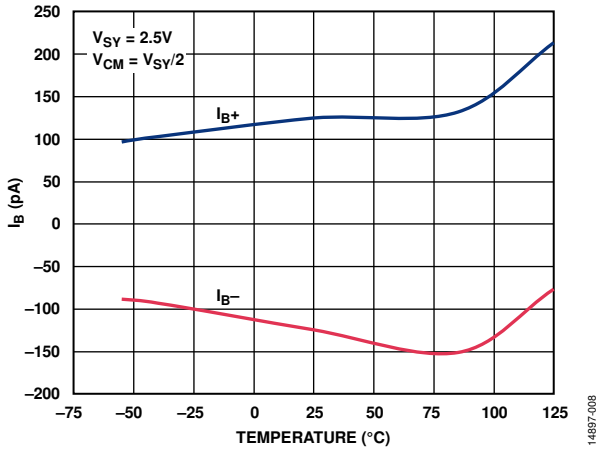


Figure 10. Input Bias Current (I_B) vs. Temperature

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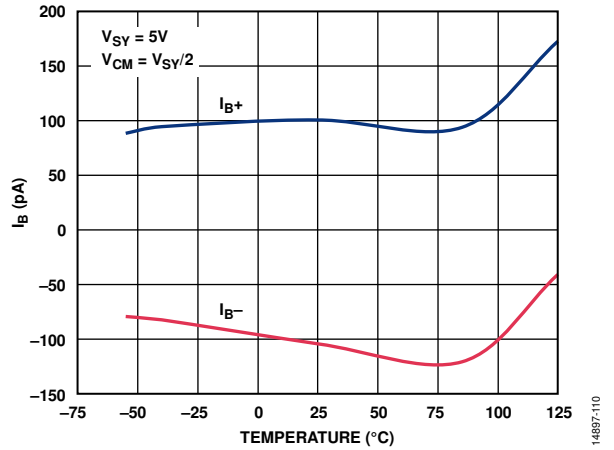


Figure 13. Input Bias Current (I_B) vs. Temperature

14897-110

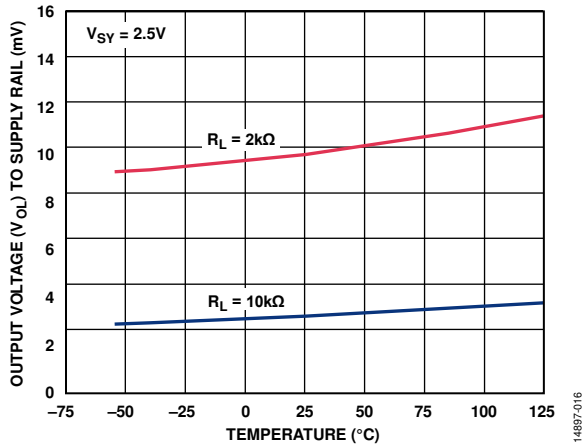


Figure 11. Output Voltage (V_{OU}) to Supply Rail vs. Temperature

14897-016

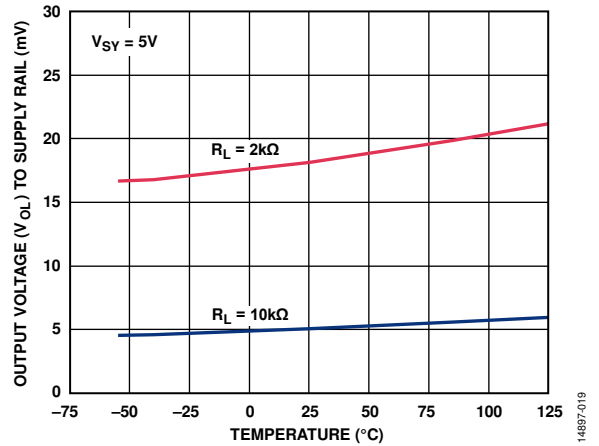


Figure 14. Output Voltage (V_{OU}) to Supply Rail vs. Temperature

14897-019

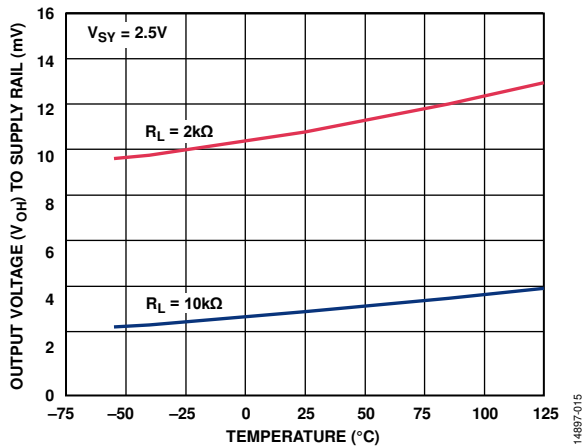


Figure 12. Output Voltage (V_{OH}) to Supply Rail vs. Temperature

14897-015

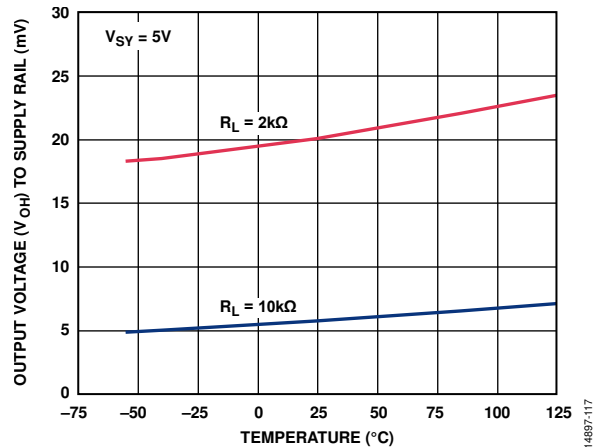


Figure 15. Output Voltage (V_{OH}) to Supply Rail vs. Temperature

14897-117

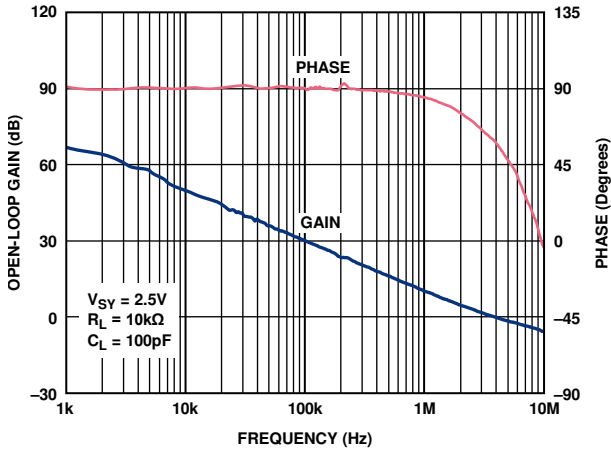


Figure 16. Open-Loop Gain and Phase vs. Frequency

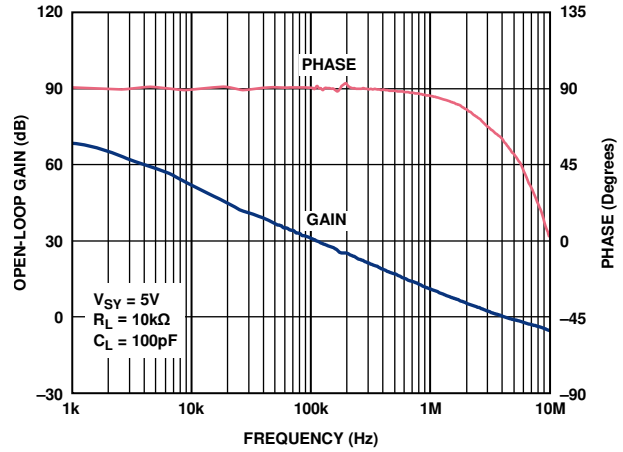


Figure 19. Open-Loop Gain and Phase vs. Frequency

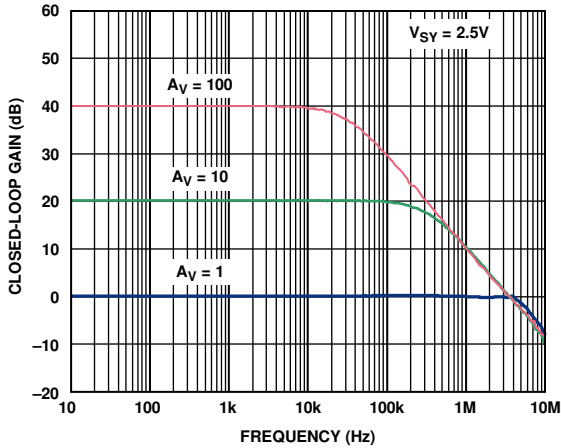


Figure 17. Closed-Loop Gain vs. Frequency

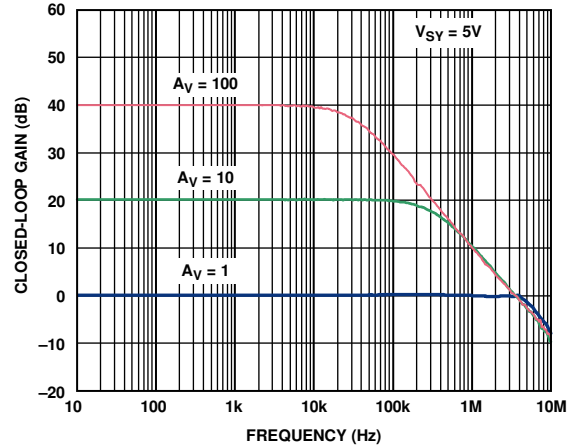


Figure 20. Closed-Loop Gain vs. Frequency

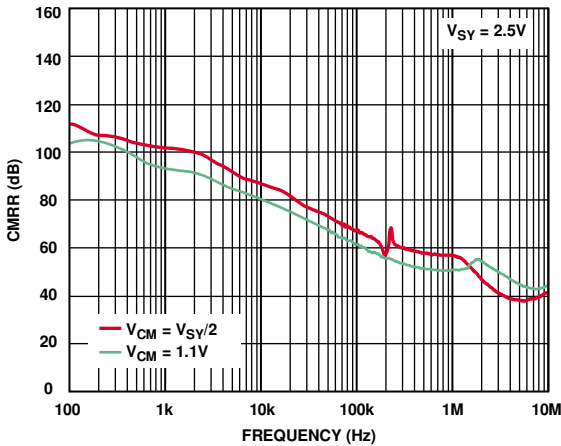


Figure 18. CMRR vs. Frequency

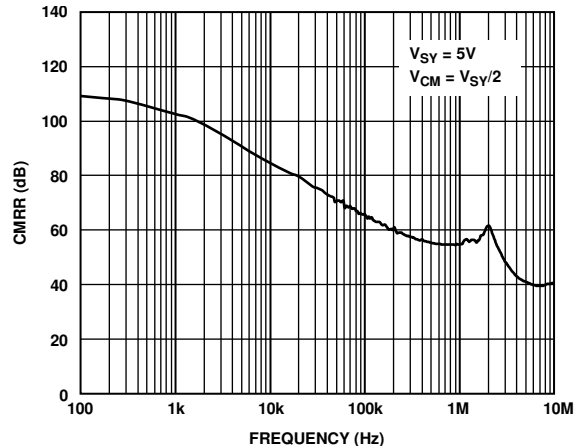


Figure 21. CMRR vs. Frequency

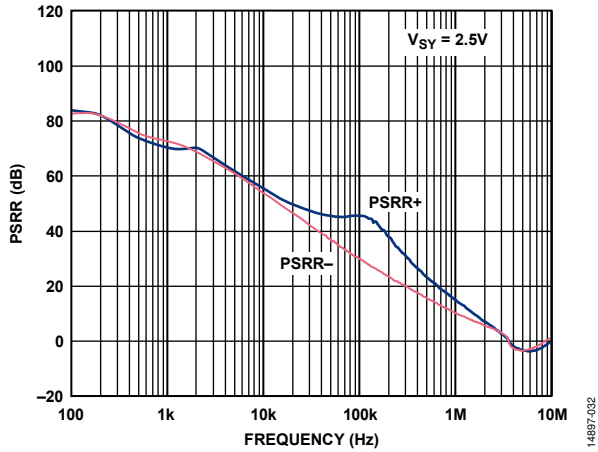


Figure 22. PSRR vs. Frequency

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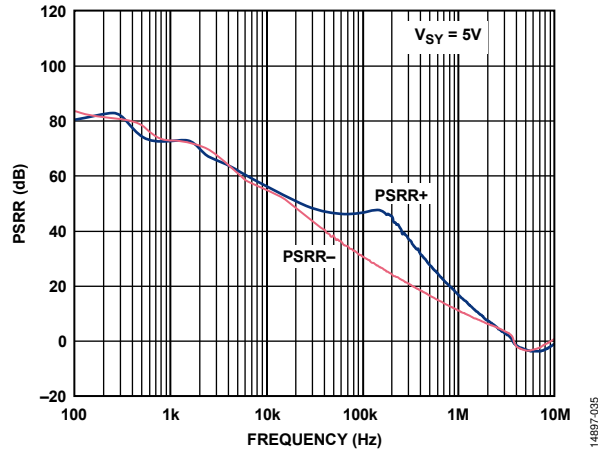


Figure 25. PSRR vs. Frequency

14897-035

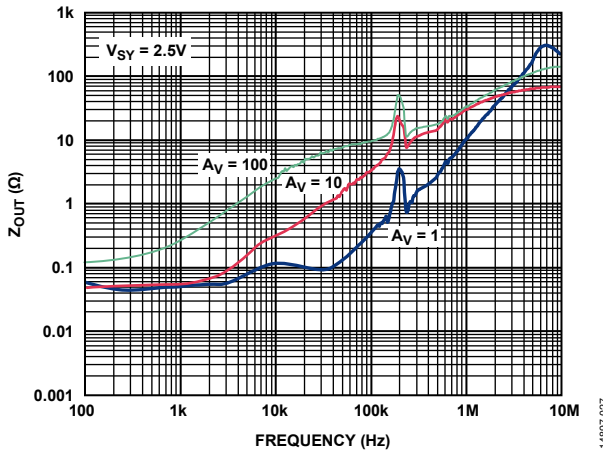


Figure 23. Closed-Loop Output Impedance (Z_{OUT}) vs. Frequency

14897-027

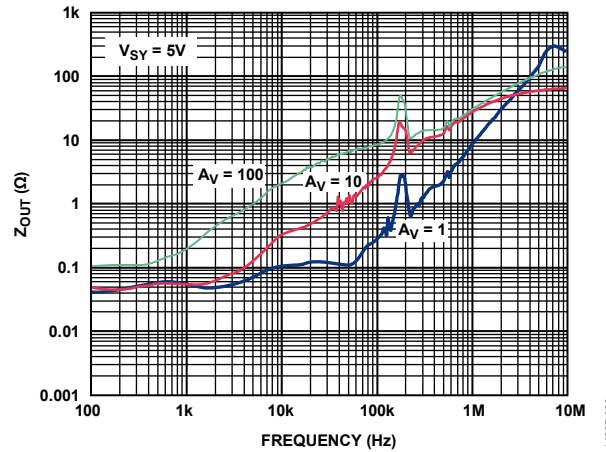


Figure 26. Closed-Loop Output Impedance (Z_{OUT}) vs. Frequency

14897-030

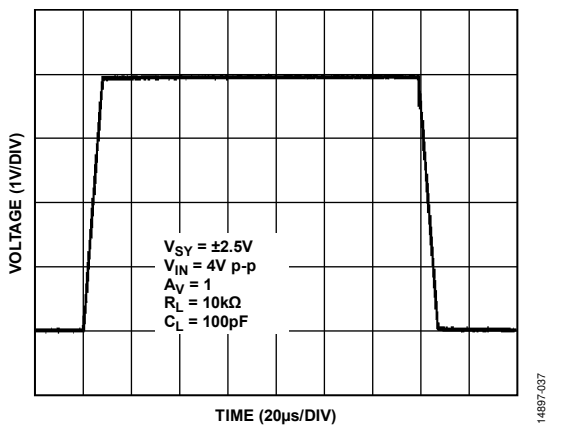


Figure 24. Large Signal Transient Response

14897-037

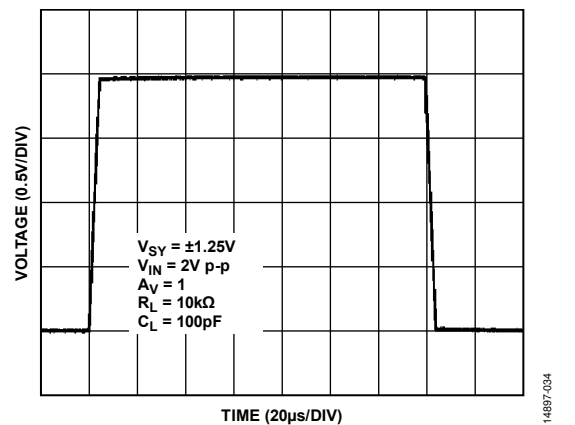


Figure 27. Large Signal Transient Response

14897-034

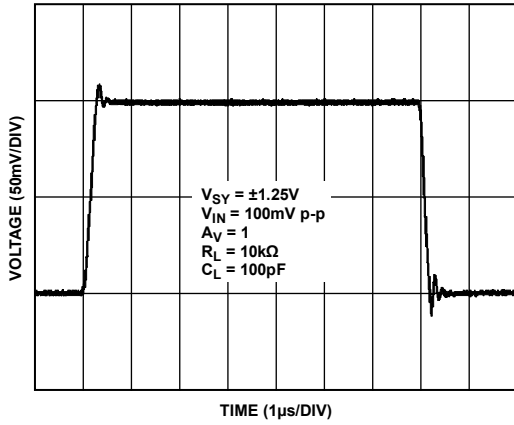


Figure 28. Small Signal Transient Response

14897-038

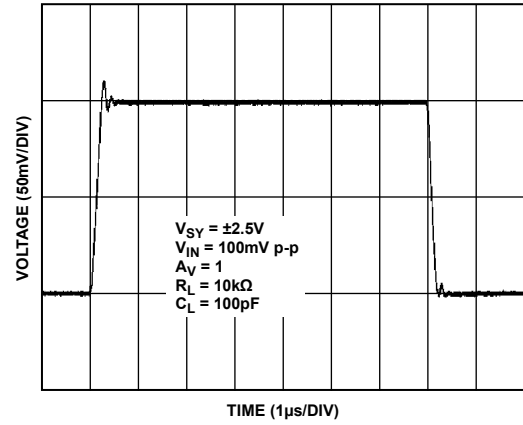


Figure 31. Small Signal Transient Response

14897-041

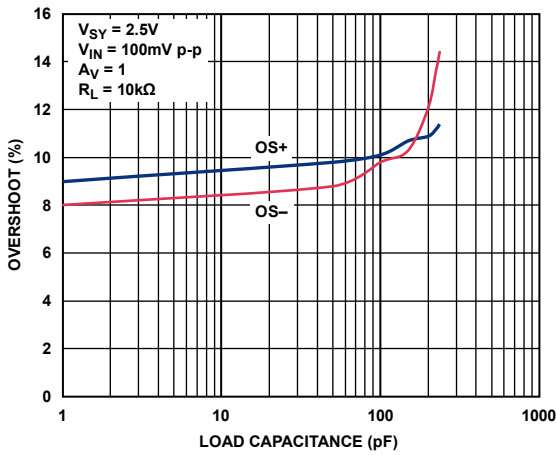


Figure 29. Small Signal Overshoot vs. Load Capacitance

14897-033

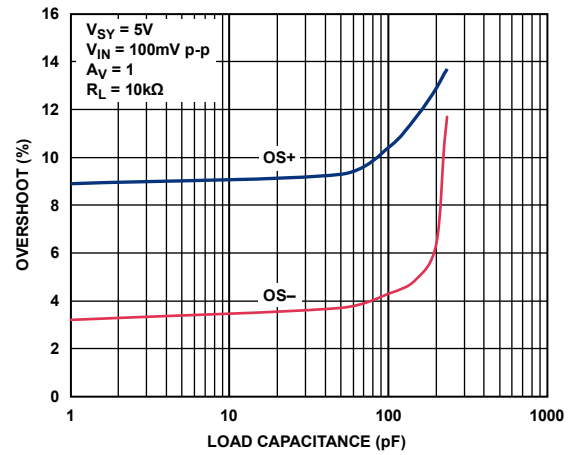


Figure 32. Small Signal Overshoot vs. Load Capacitance

14897-036

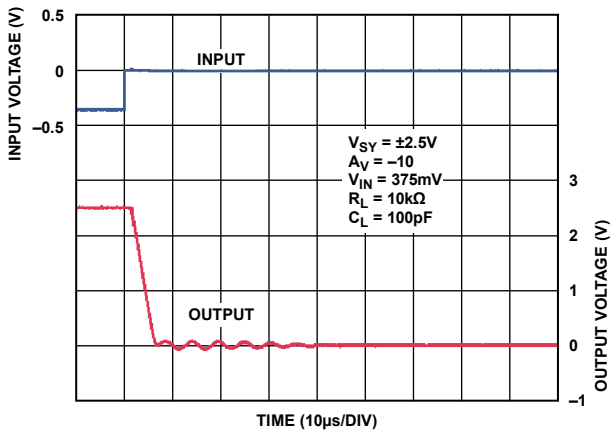


Figure 30. Positive Overload Recovery

14897-043

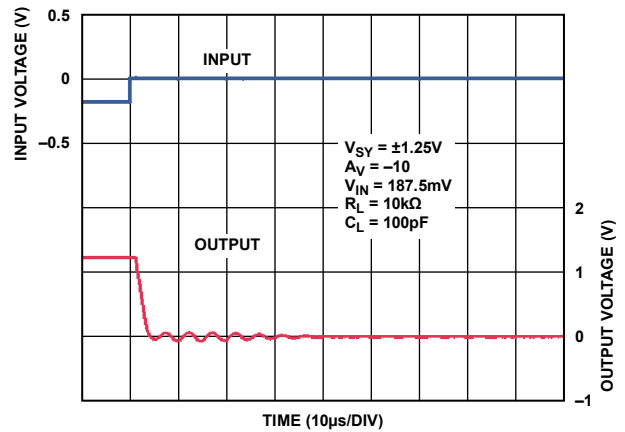


Figure 33. Positive Overload Recovery

14897-040

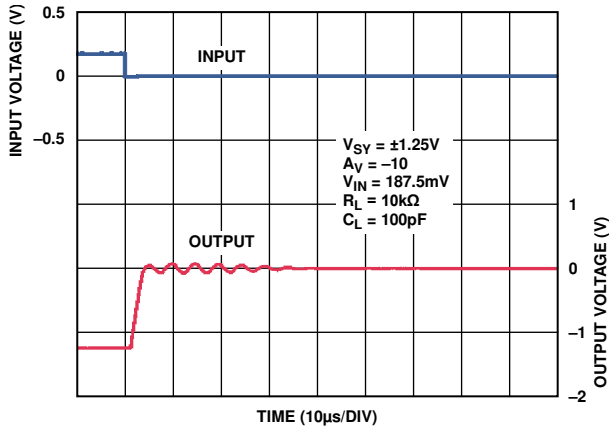


Figure 34. Negative Overload Recovery

14897-039

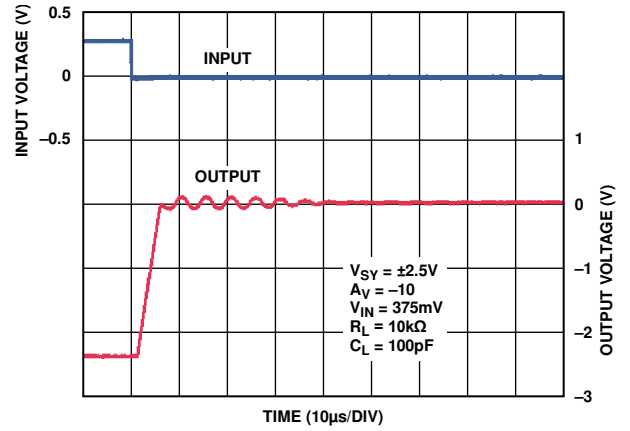


Figure 37. Negative Overload Recovery

14897-042

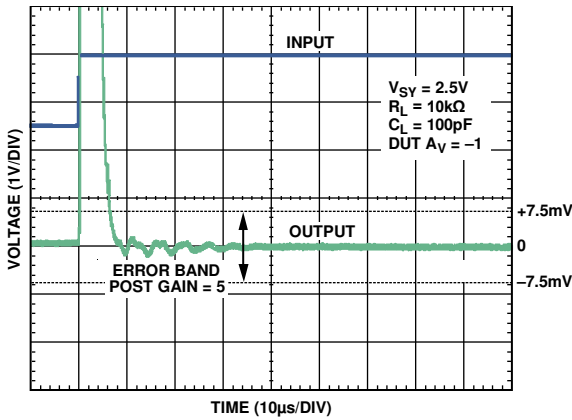


Figure 35. Positive Settling Time to 0.1%

14897-044

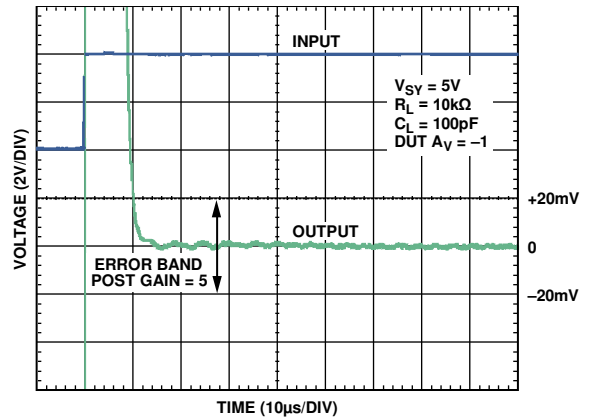


Figure 38. Positive Settling Time to 0.1%

14897-047

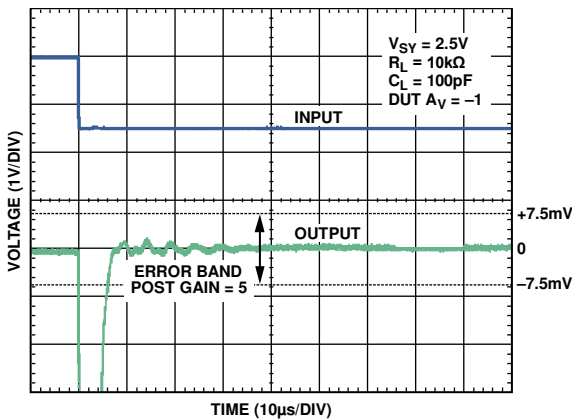


Figure 36. Negative Settling Time to 0.1%

14897-045

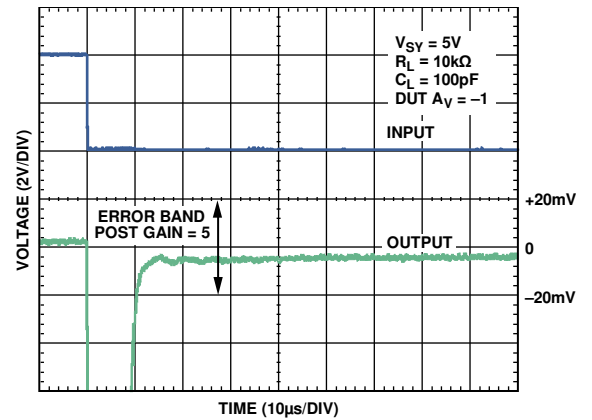


Figure 39. Negative Settling Time to 0.1%

14897-048

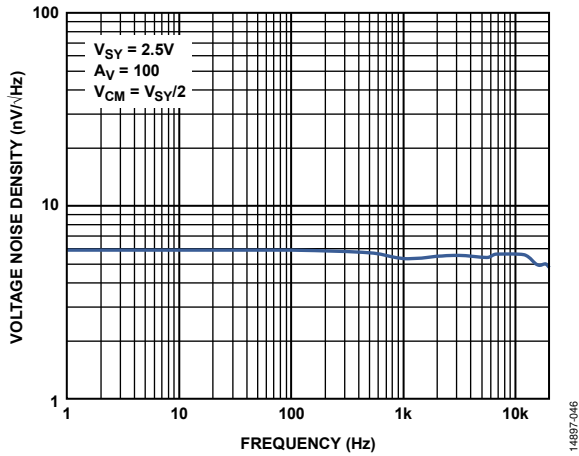


Figure 40. Voltage Noise Density vs. Frequency

14897-046

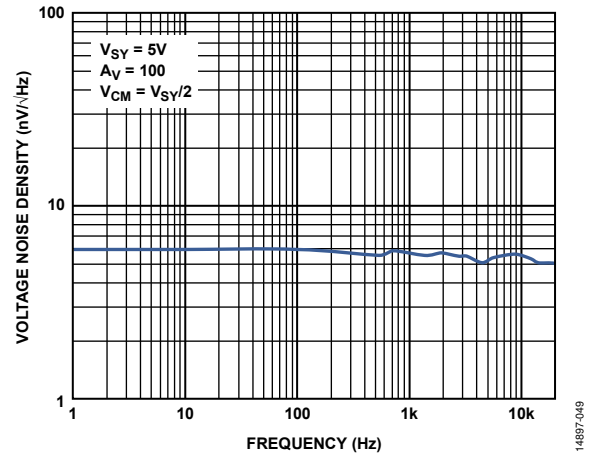


Figure 43. Voltage Noise Density vs. Frequency

14897-049

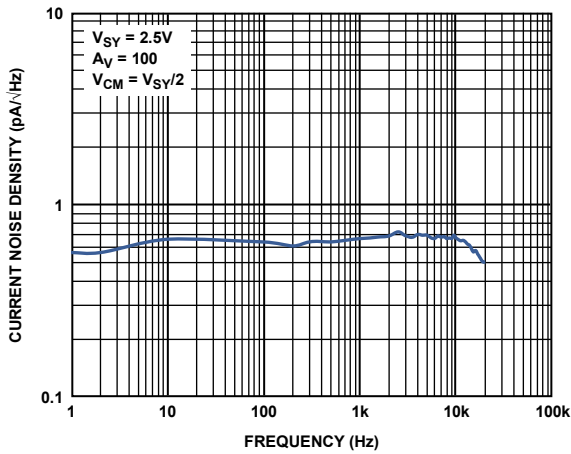


Figure 41. Current Noise Density vs. Frequency

14897-150

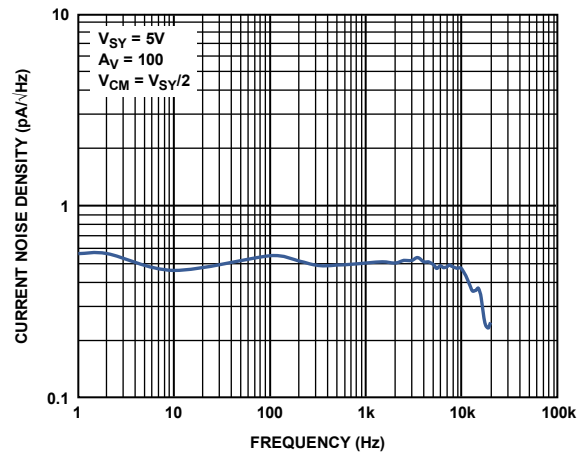


Figure 44. Current Noise Density vs. Frequency

14897-153

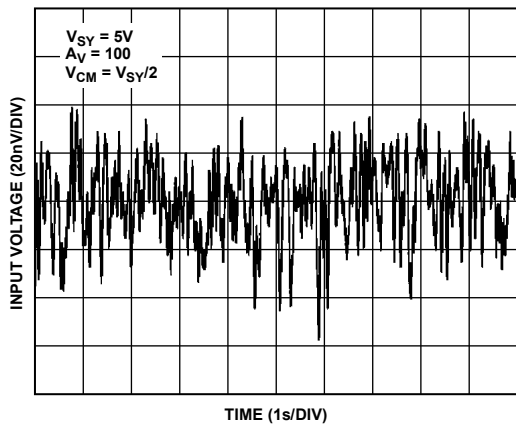


Figure 42. 0.1 Hz to 10 Hz Noise

14897-053

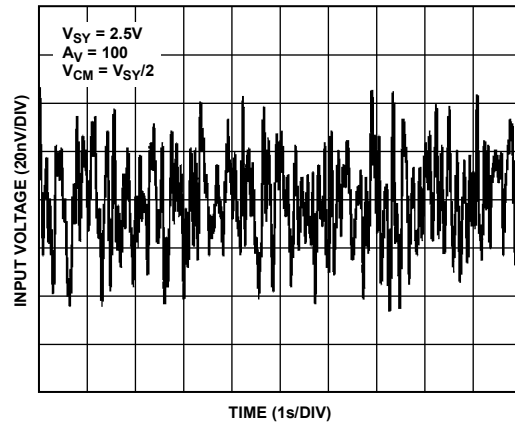


Figure 45. 0.1 Hz to 10 Hz Noise

14897-050

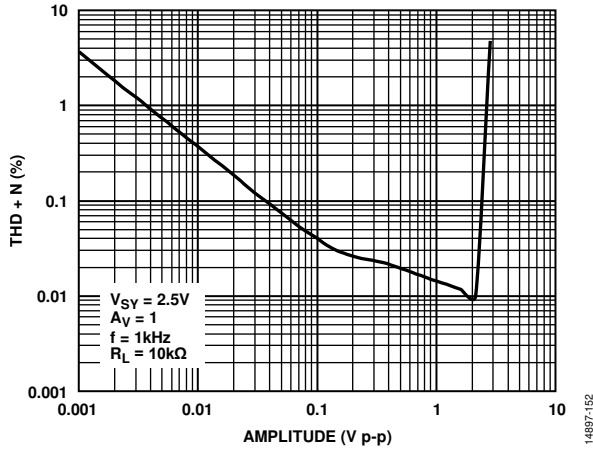


Figure 46. THD + N vs. Amplitude

14897-152

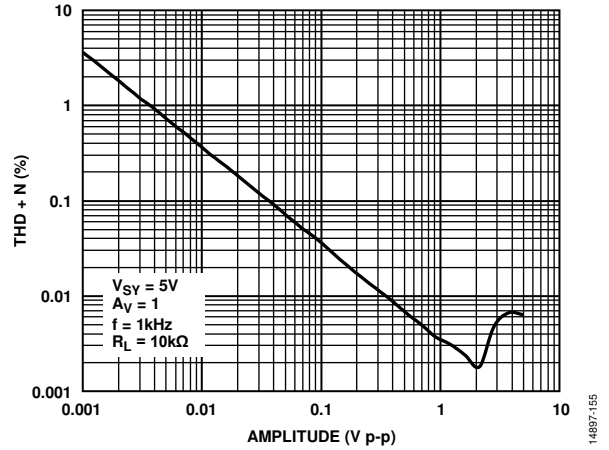


Figure 49. THD + N vs. Amplitude

14897-155

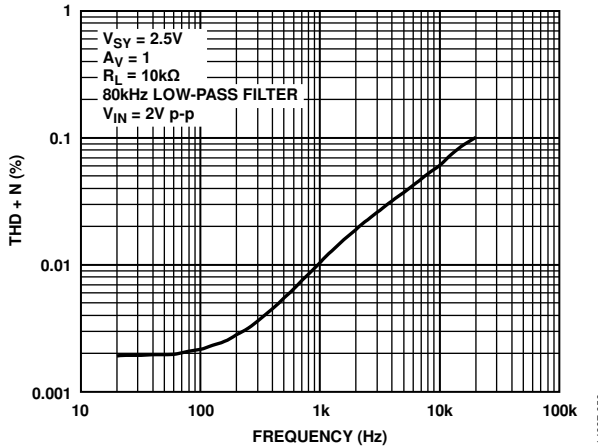


Figure 47. THD + N vs. Frequency

14897-056

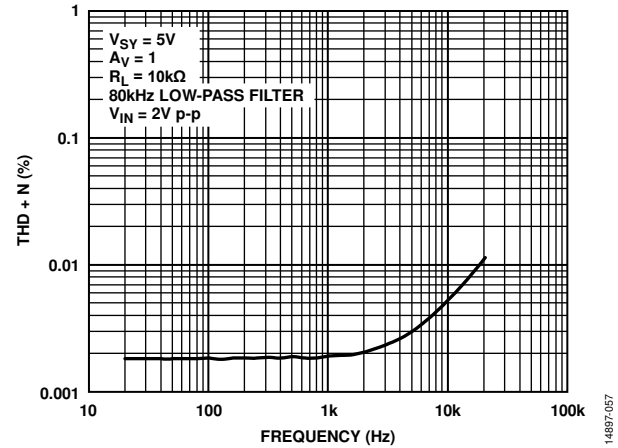


Figure 50. THD + N vs. Frequency

14897-057

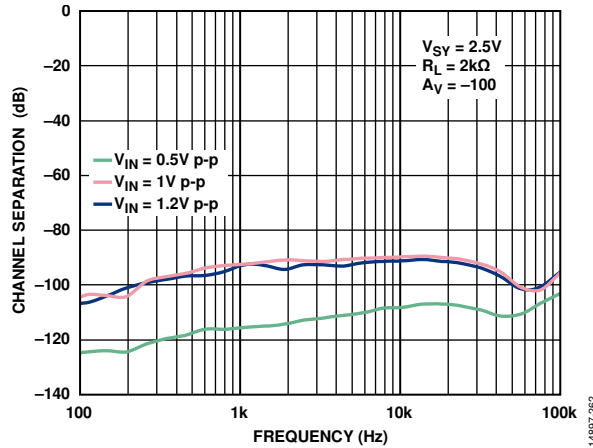


Figure 48. Channel Separation vs. Frequency

14897-262

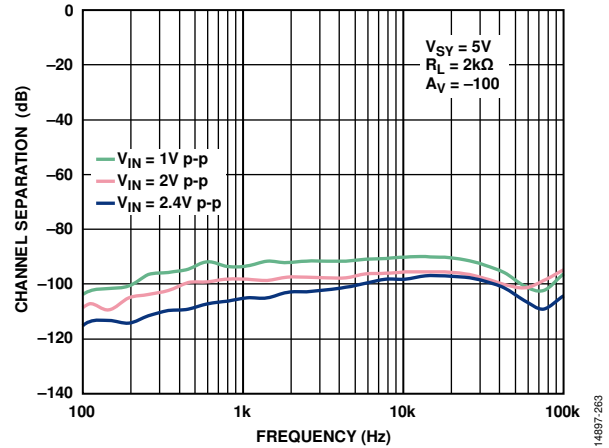


Figure 51. Channel Separation vs. Frequency

14897-263

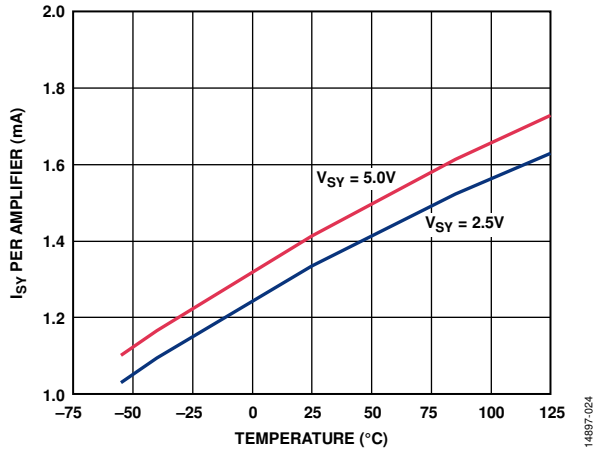


Figure 52. Supply Current (I_{SY}) per Amplifier vs. Temperature

14897-024

OUTLINE DIMENSIONS

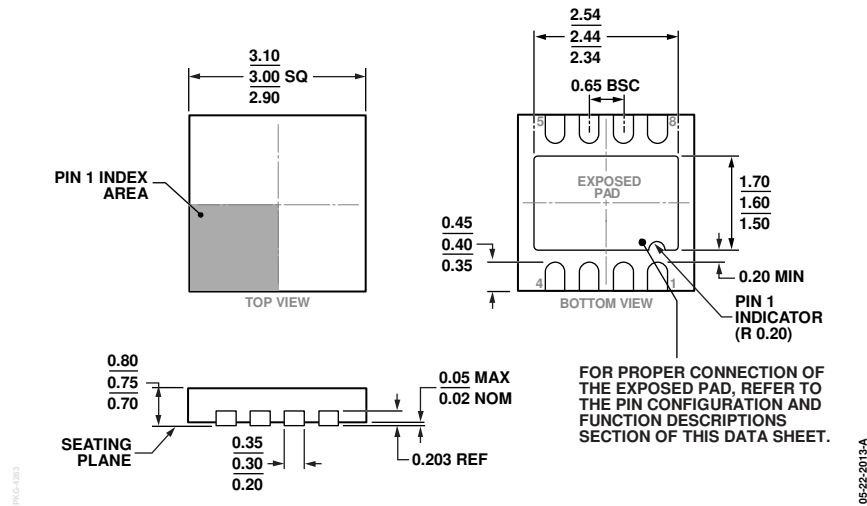


Figure 53. 8-Lead Lead Frame Chip Scale Package [LFCSP]
 3 mm × 3 mm Body and 0.75 mm Package Height
 (CP-8-19)
 Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADA4528-2TCPZ-EP	-55°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-19	A3H
ADA4528-2TCPZ-EPR7	-55°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-19	A3H

¹ Z = RoHS Compliant Part.