

## 100304 Low Power Quint AND/NAND Gate

### General Description

The 100304 is monolithic quint AND/NAND gate. The Function output is the wire-NOR of all five AND gate outputs. All inputs have 50 kΩ pull-down resistors.

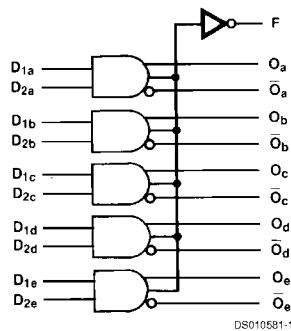
- 2000V ESD protection
- Pin/function compatible with 100104
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

### Features

- Low Power Operation

### Ordering Code:

### Logic Symbol



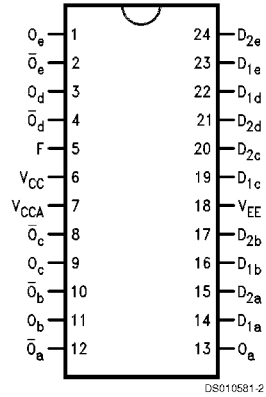
### Logic Equation

$$F = \overline{D_{1a}} \cdot \overline{D_{2a}} + \overline{D_{1b}} \cdot \overline{D_{2b}} + \overline{D_{1c}} \cdot \overline{D_{2c}} + \overline{D_{1d}} \cdot \overline{D_{2d}} + \overline{D_{1e}} \cdot \overline{D_{2e}}$$

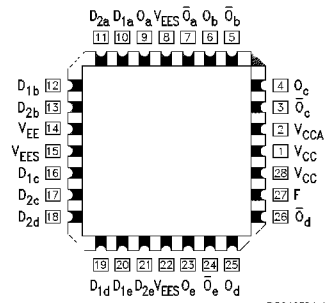
Pin Names	Description
$D_{na}$ – $D_{ne}$	Data Inputs
F	Function Output
$O_a$ – $O_e$	Data Outputs
$\overline{O_a}$ – $\overline{O_e}$	Complementary Data Outputs

## Connection Diagrams

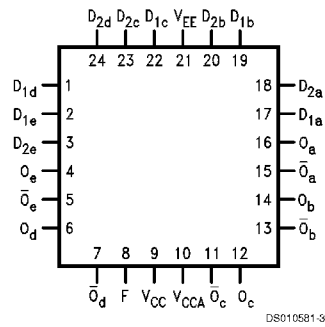
24-Pin DIP



28-Pin PCC



24-Pin Quad Cerpak



## Absolute Maximum Ratings (Note 1)

Above which the useful life may be impaired

Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	
Ceramic	+175°C
Plastic	+150°C
$V_{EE}$ Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	$V_{EE}$ to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	$\geq 2000V$

## Recommended Operating Conditions

Case Temperature ( $T_C$ )	
Commercial	0°C to +85°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Supply Voltage ( $V_{EE}$ )	-5.7V to -4.2V

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

## Commercial Version DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$  (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH(Max)}$ Loading with $50\Omega$ to $-2.0V$
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1620	mV	or $V_{IL(Min)}$
$V_{OHC}$	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH(Min)}$ Loading with
$V_{OLC}$	Output LOW Voltage			-1610	mV	or $V_{IL(Max)}$ $50\Omega$ to $-2.0V$
$V_{IH}$	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs
$V_{IL}$	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs
$I_{IL}$	Input LOW Current	0.50			$\mu A$	$V_{IN} = V_{IL(Min)}$
$I_{IH}$	Input High Current $D_{2a}-D_{2e}$ $D_{1a}-D_{1e}$			250 350	$\mu A$	$V_{IN} = V_{IH(Max)}$
$I_{EE}$	Power Supply Current	-69	-43	-30	mA	Inputs open

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## DIP AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	0.40	1.75	0.40	1.65	0.40	1.75	ns	Figures 1, 2
$t_{PHL}$	$D_{na}-D_{ne}$ to $O, \bar{O}$								
$t_{PLH}$	Propagation Delay	1.00	2.60	1.00	2.60	1.15	3.20	ns	
$t_{PHL}$	Data to F								
$t_{TLH}$	Transition Time	0.35	1.20	0.35	1.20	0.35	1.20	ns	
$t_{THL}$	20% to 80%, 80% to 20%								

## PCC and Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	0.40	1.55	0.40	1.45	0.40	1.55	ns	Figures 1, 2
$t_{PHL}$	$D_{na}-D_{ne}$ to O, $\bar{O}$								
$t_{PLH}$	Propagation Delay	1.00	2.40	1.00	2.40	1.15	3.00	ns	
$t_{PHL}$	Data to F								
$t_{TLH}$	Transition Time	0.35	1.10	0.35	1.15	0.35	1.10	ns	
$t_{THL}$	20% to 80%, 80% to 20%								

## Industrial Version PCC DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -40^\circ C$  to  $+85^\circ C$  (Note 4)

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions	
		Min	Max	Min	Max			
$V_{OH}$	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH (Max)}$ or $V_{IL (Min)}$	Loading with 50Ω to -2.0V
$V_{OL}$	Output LOW Voltage	-1830	-1575	-1830	-1620			
$V_{OHC}$	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH (Min)}$ or $V_{IL (Max)}$	Loading with 50Ω to -2.0V
$V_{OLC}$	Output LOW Voltage		-1565		-1610			
$V_{IH}$	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs	
$V_{IL}$	Input LOW Voltage	-1830	-1480	-1830	-1475		Guaranteed LOW Signal for All Inputs	
$I_{IL}$	Input LOW Current	0.50		0.50		μA	$V_{IN} = V_{IL (Min)}$	
$I_{IH}$	Input HIGH Current		250		250		$V_{IN} = V_{IH (Max)}$	
	$D_{2a}-D_{2e}$				350			
	$D_{1a}-D_{1e}$				350			
$I_{EE}$	Power Supply Current	-69	-30	-69	-30	mA	Inputs Open	

**Note 4:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## PCC AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	0.35	1.55	0.40	1.45	0.40	1.55	ns	Figures 1, 2
$t_{PHL}$	$D_{na}-D_{ne}$ to O, $\bar{O}$								
$t_{PLH}$	Propagation Delay	1.00	2.40	1.00	2.40	1.15	3.00	ns	
$t_{PHL}$	Data to F								
$t_{TLH}$	Transition Time	0.35	1.10	0.35	1.15	0.35	1.10	ns	
$t_{THL}$	20% to 80%, 80% to 20%								

## Military Version DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -55^\circ C$  to  $+125^\circ C$

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes	
$V_{OH}$	Output HIGH Voltage	-1025	-870	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$	Loading with $50\Omega$ to $-2.0V$	(Notes 5, 6, 7)
		-1085	-870	mV	$-55^\circ C$			
$V_{OL}$	Output LOW Voltage	-1830	-1620	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with $50\Omega$ to $-2.0V$	(Notes 5, 6, 7)
		-1830	-1555	mV	$-55^\circ C$			
$V_{OHC}$	Output HIGH Voltage	-1035		mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with $50\Omega$ to $-2.0V$	(Notes 5, 6, 7)
		-1085		mV	$-55^\circ C$			
$V_{OLC}$	Output LOW Voltage		-1610	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with $50\Omega$ to $-2.0V$	(Notes 5, 6, 7)
			-1555	mV	$-55^\circ C$			
$V_{IH}$	Input HIGH Voltage	-1165	-870	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed HIGH Signal for All Inputs	(Notes 5, 6, 7, 8)	
$V_{IL}$	Input LOW Voltage	-1830	-1475	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed LOW Signal for All Inputs	(Notes 5, 6, 7, 8)	
$I_{IL}$	Input LOW Current	0.50		$\mu A$	$-55^\circ C$ to $+125^\circ C$	$V_{EE} = -4.2V$ $V_{IN} = V_{IL} (Min)$	(Notes 5, 6, 7)	
$I_{IH}$	Input High Current $D_{2a}-D_{2e}$ $D_{1a}-D_{1e}$		250 350	$\mu A$	$0^\circ C$ to $+125^\circ C$	$V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$	(Notes 5, 6, 7)	
	$D_{2a}-D_{2e}$ $D_{1a}-D_{1e}$		350 500	$\mu A$	$-55^\circ C$			
$I_{EE}$	Power Supply Current	-75	-25	mA	$-55^\circ C$ to $+125^\circ C$	Inputs Open	(Notes 5, 6, 7)	

**Note 5:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 6:** Screen tested 100% on each device at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups, 1, 2, 3, 7, and 8.

**Note 7:** Sample tested (Method 5005, Table I) on each manufactured lot at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups A1, 2, 3, 7, and 8.

**Note 8:** Guaranteed by applying specified input condition and testing  $V_{OH}/V_{OL}$ .

## AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$	Propagation Delay	0.30	1.90	0.40	1.80	0.30	2.30	ns	Figures 1, 2	(Notes 9, 10, 11)
$t_{PHL}$	$D_{na} - D_{ne}$ to O, $\bar{O}$									
$t_{PLH}$	Propagation Delay	0.80	2.90	0.90	2.80	0.90	3.40	ns		
$t_{PHL}$	Data to F							ns		(Note 12)
$t_{TLH}$	Transition Time	0.20	1.80	0.30	1.60	0.20	2.00			
$t_{THL}$	20% to 80%, 80% to 20%									

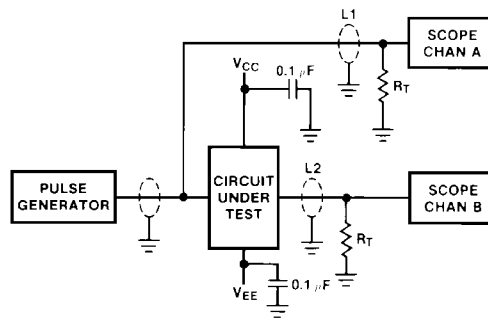
**Note 9:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 10:** Screen tested 100% on each device at  $+25^\circ C$  temperature only, Subgroup A9.

**Note 11:** Sample tested (Method 5005, Table I) on each mfg. lot at  $+25^\circ C$ , Subgroup A9, and at  $+125^\circ C$  and  $-55^\circ C$  temperatures, Subgroups A10 and A11.

**Note 12:** Not tested at  $+25^\circ C$ ,  $+125^\circ C$ , and  $-55^\circ C$  temperature (design characterization data).

## Test Circuitry



DS010581-5

### Notes:

$V_{CC}, V_{CCA} = +2V$ ,  $V_{EE} = -2.5V$

$L_1$  and  $L_2 =$  equal length  $50\Omega$  impedance lines

$R_T = 50\Omega$  terminator internal to scope

Decoupling  $0.1 \mu F$  from GND to  $V_{CC}$  and  $V_{EE}$

All unused outputs are loaded with  $50\Omega$  to GND

$C_L =$  Fixture and stray capacitance  $\leq 3 pF$

FIGURE 1. AC Test Circuit

## Switching Waveforms

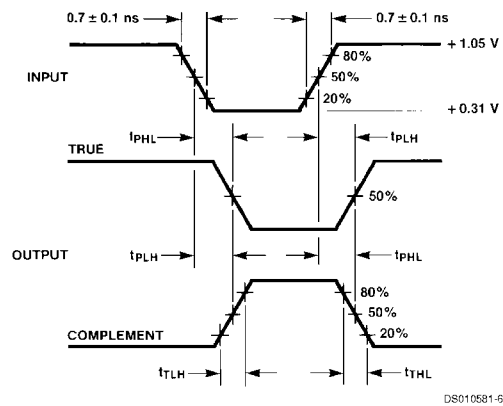
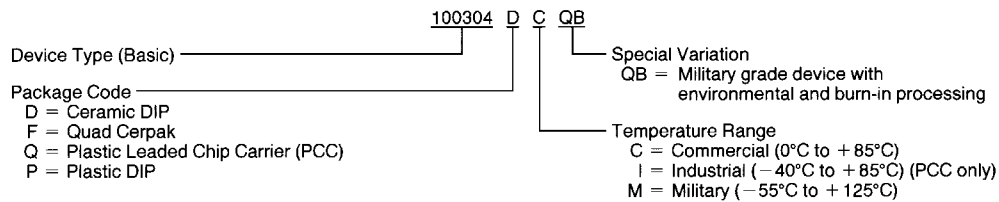


FIGURE 2. Propagation Delay and Transition Times

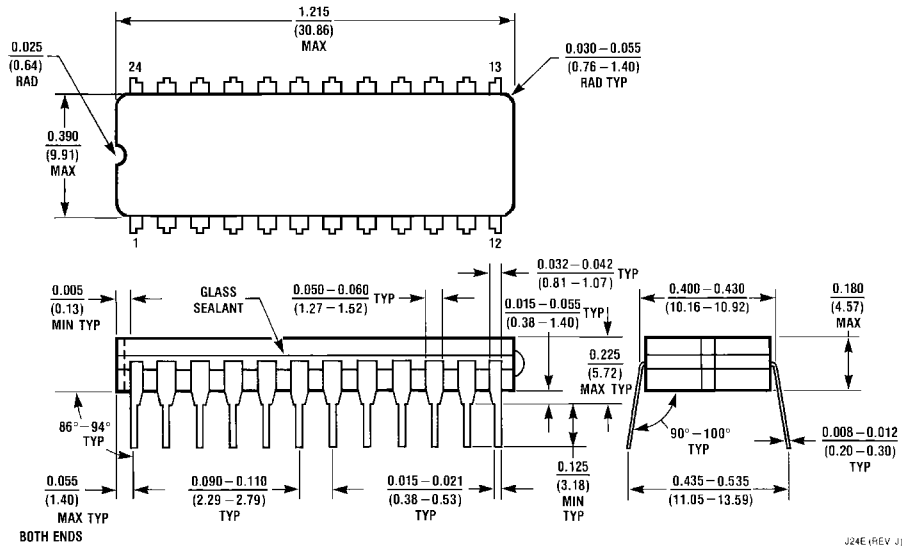
## Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

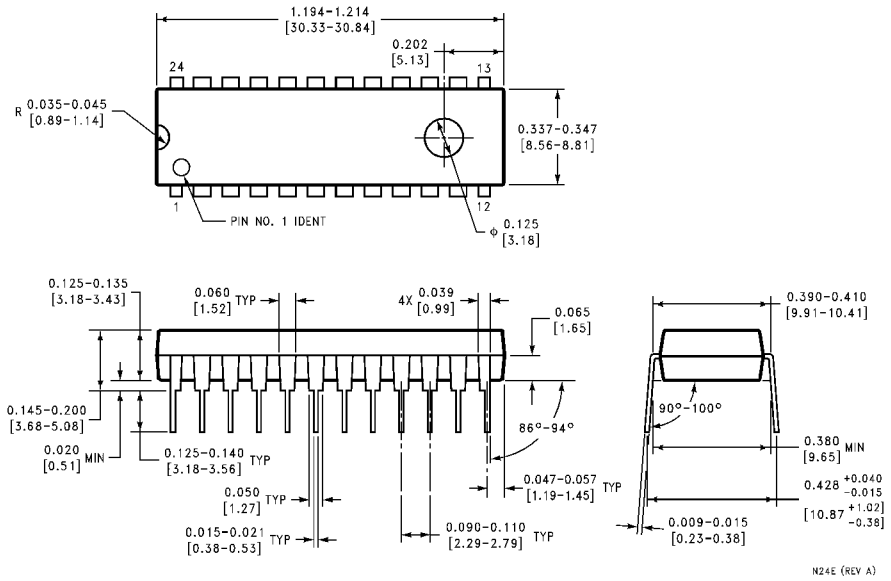


DS010581-7

**Physical Dimensions** inches (millimeters) unless otherwise noted



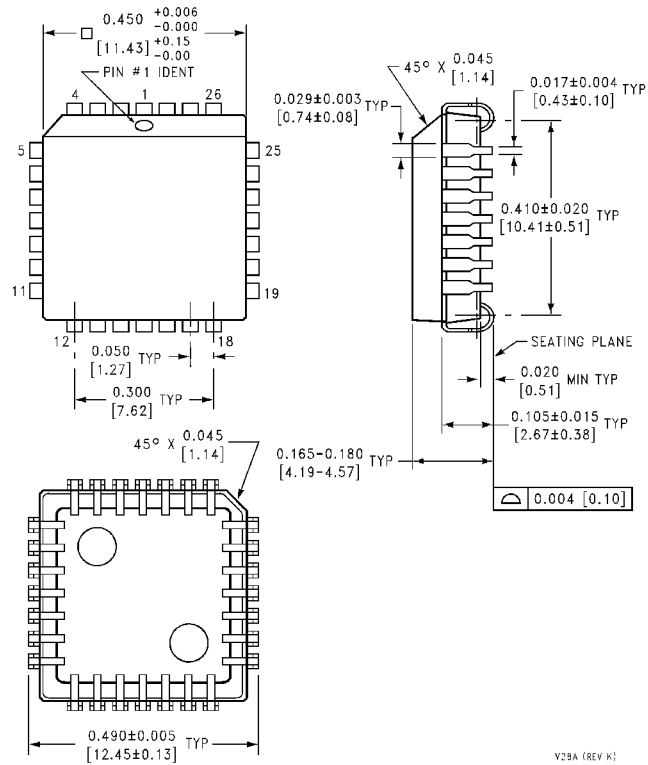
**24-Pin Ceramic Dual-In-Line Package (D)**  
Package Number J24E



**24-Pin Plastic Dual-In-Line Package (P)**  
Package Number N24E



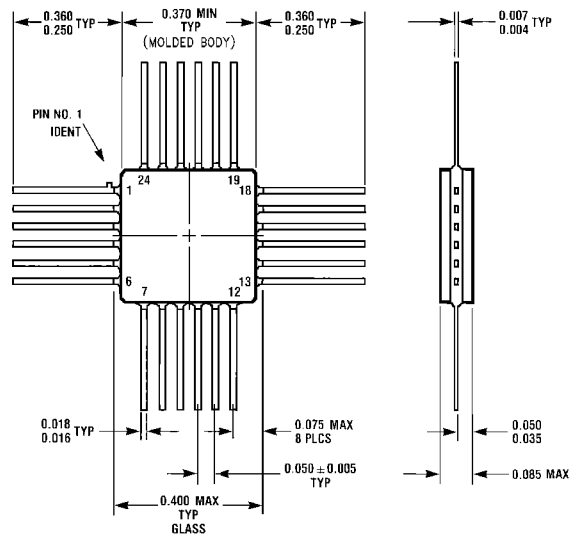
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**28-Pin Plastic Leaded Chip Carrier (Q)  
Package Number V28A**

V28A (REV K)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



W24B (REV B)

**24-Pin Quad Cerpak (F)  
Package Number W24B**

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