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BCM8724 PRODUCT Brief

DUAL 10-GIGABIT ETHERNET XFI TO XAUI™ TRANSCEIVER

FEATURES

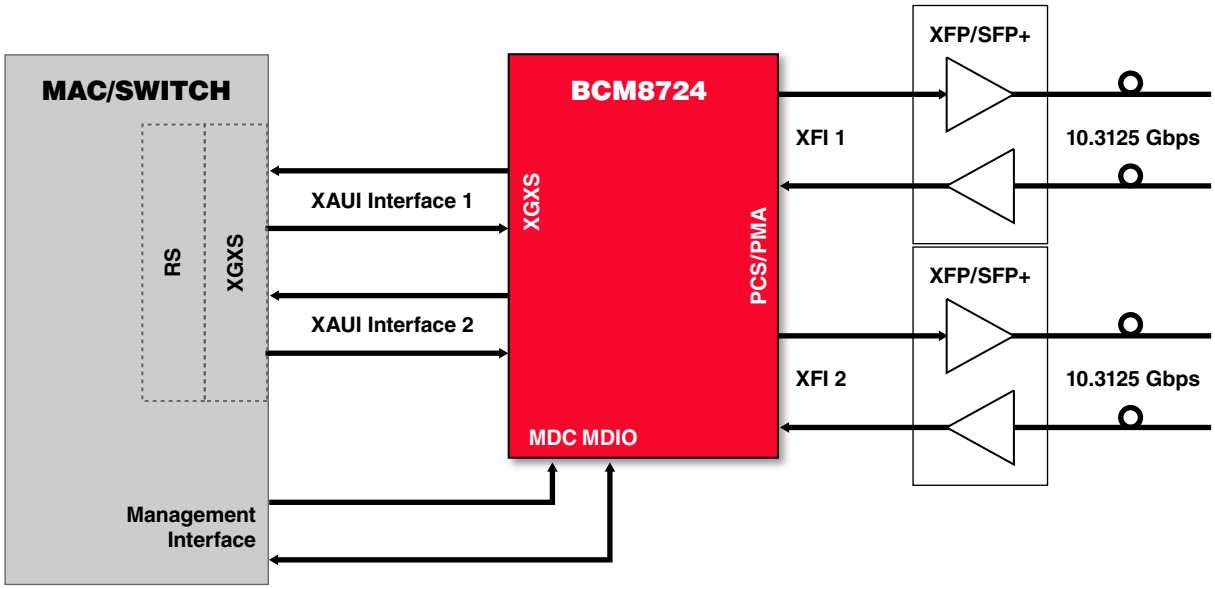
- **Dual XFI to XAUI™ 10-GbE transceiver**
- **Fully integrated CMU, CDR, SerDes, limiting amplifier, and EyeOpener™**
- **Dual 10-GbE PMD interfaces with phase adjust**
  - PMD interface: serial 10.3125-Gbps CML
- **Dual four-lane XAUI interfaces (3.125 Gbps)**
  - XAUI link synchronization/deskew
  - XAUI transmit pre-emphasis for transmission over backplanes
- **PCS 64B/66B scrambler/descrambler**
- **XGXS 8B/10B error detection ENDEC**
- **Adjustable receive equalization on 10-GbE serial interfaces (EyeOpener™)**
- **Loopback modes supporting IEEE standard modes**
- **802.3 Clause 45 management interface with extended indirect address register access**
- **Built-In Self-Test (BIST) on the 10-GbE serial and XAUI interfaces**
- **Power dissipation: 1.8W**
- **Core Supply : 1.2V, I/O – 3.3V**
- **Packaged in a 19 mm x 19 mm Plastic BGA**

SUMMARY OF BENEFITS

- **Meets or exceeds IEEE 802.3ae**
- **Supports XFP/XFI and SFP+ interfaces**
- **Simplifies designing and routing high-density linecard applications with multiple 10-GbE optical interfaces with either XFP or SFP+**
- **Reduces space and power in multiport 10-GbE linecard applications**
- **Based on a proven design that is compliant with 10-GbE interface standards**

APPLICATIONS

- **High-density 10-GbE linecards using either SFP+ or XFP optical modules**
- **LAN/MAN switch/routers**
- **Hubs and repeaters**
- **Network interface cards (NICs)**



BCM8724 Block Diagram

The BCM8724 Ethernet LAN-PHY is a fully integrated dual-serialization/deserialization (10.3125 Gbps) interface device performing the extension functions for a 10-gigabit serial Ethernet reconciliation sublayer (RS) interface. The XGXS, PCS, and PMA functions include 8B/10B coding, 64B/66B coding, SerDes, clock multiplication unit (CMU), and clock and data recovery (CDR).

On-chip clock synthesis is performed by the high-frequency low-jitter phase-locked loops for the PMD and XAUI output retimers. Individual PMD and XAUI clock recovery is performed on the device by synchronizing directly to their respective incoming data streams. Elastic buffers are provided to allow the XAUI and PMD interfaces to operate in asynchronous configuration. Only an external 156.25-MHz oscillator is required for the reference clock input.

The serial 10-GbE receiver includes an adjustable equalizer/EyeOpener that allows for compensation for long trace lengths in multichannel linecard applications.

The BCM8724 is available in a 19 mm x 19 mm, 324-pin FBGA with a 1.0-mm ball pitch RoHS compliant package.

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