

**REVISIONS**

| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
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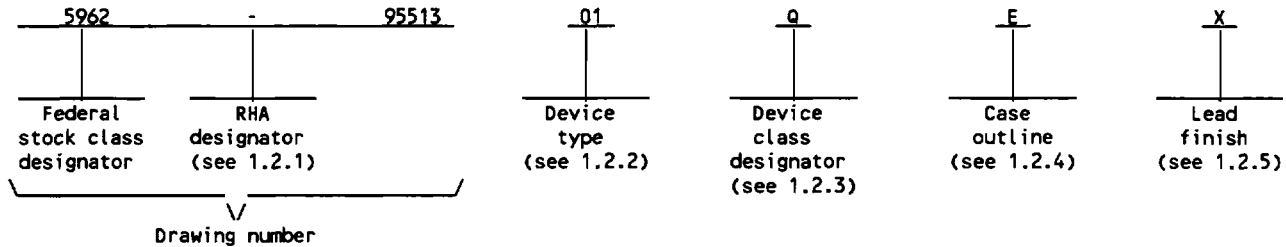
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| REV STATUS OF SHEETS | REV   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |  |  |  |  |
|                      | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |  |  |  |  |

|   |                                   |   |                           |  |
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| PMIC N/A  | PREPARED BY<br>Marcia Kelleher    | DEFENSE ELECTRONICS SUPPLY CENTER<br>DAYTON, OHIO 45444 |                           |  |
| <p align="center"><b>STANDARD<br/>MICROCIRCUIT<br/>DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p> | CHECKED BY<br>Rajesh Pithadia     |   |                           | MICROCIRCUIT, DIGITAL-LINEAR, QUAD, 8-BIT<br>ANALOG DATA ACQUISITION AND MONITORING<br>SYSTEMS, MONOLITHIC SILICON |
|   | APPROVED BY<br>Michael A Frye     |   |                           |  |
|   | DRAWING APPROVAL DATE<br>95-12-04 | SIZE<br><b>A</b>  | CAGE CODE<br><b>67268</b> |  |
|   | REVISION LEVEL                    | SHEET 1 OF 14   |                           |  |

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

| <u>Device type</u> | <u>Generic number</u> | <u>Circuit function</u>                              |
|--------------------|-----------------------|--|
| 01                 | ADC0851               | 8-bit analog data acquisition and monitoring systems |
| 02                 | ADC0858               | 8-bit analog data acquisition and monitoring systems |

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

| <u>Device class</u> | <u>Device requirements documentation</u>  |
|---------------------|---|
| M                   | Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883 |
| Q or V              | Certification and qualification to MIL-I-38535  |

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

| <u>Outline letter</u> | <u>Descriptive designator</u> | <u>Terminals</u> | <u>Package style</u> |
|-----------------------|-------------------------------|------------------|----------------------|
| E                     | GDIP1-T16 or CDIP2-T16        | 16               | dual-in-line         |
| R                     | GDIP1-T20 or CDIP2-T20        | 20               | dual-in-line         |

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

|   |                   |                       |                    |
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1.3 Absolute maximum ratings. 1/

|  |                            |
|--|----------------------------|
| Supply voltage ( $V_{CC}$ ) . . . . .                            | 6.5 V                      |
| Voltage at logic and analog inputs . . . . .                     | -0.3 V to $V_{CC} + 0.3$ V |
| Input current per pin . . . . .                                  | $\pm 5$ mA                 |
| Input current per package . . . . .                              | $\pm 20$ mA                |
| Storage temperature range . . . . .                              | -65°C to +150°C            |
| Junction temperature ( $T_J$ ) . . . . .                         | +150°C                     |
| Lead temperature (soldering, 10 seconds) . . . . .               | 260°C                      |
| Power dissipation ( $P_D$ ):                                     |                            |
| Device type 01 . . . . .   | 160 mW                     |
| Device type 02 . . . . .   | 160 mW                     |
| Thermal resistance, junction-to-case ( $\theta_{JC}$ ) . . . . . | See MIL-STD-1835           |
| Thermal resistance, junction-to-ambient ( $\theta_{JA}$ ):       |                            |
| Device type 01 . . . . .   | 73°C/W                     |
| Device type 02 . . . . .   | 68°C/W                     |

1.4 Recommended operating conditions.

|   |                                 |
|---|---------------------------------|
| Supply voltage range ( $V+$ ) . . . . .                 | 3.0 V $\leq$ $V+$ $\leq$ 15.5 V |
| Ambient operating temperature range ( $T_A$ ) . . . . . | -55°C to +125°C                 |

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.  
 MIL-STD-973 - Configuration Management.  
 MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standard Microcircuit Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.  
 2/ When the input voltage ( $V_{IN}$ ) at any pin exceeds the power supply rails ( $V_{IN} < GND$  or  $V_{IN} > V+$ ) the absolute value of the current at that pin should be limited to 5 mA or less.

|  |                            |                |                   |
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### 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Mode selection tables. The mode selection tables shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 57 (see MIL-I-38535, appendix A).

### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

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TABLE I. Electrical performance characteristics.

| Test   | Symbol           | Conditions <sup>1/</sup><br>-55°C ≤ T <sub>A</sub> ≤ +125°C<br>unless otherwise specified | Group A<br>subgroups | Device<br>types | Limits        |                           | Unit |
|--|------------------|---|----------------------|-----------------|---------------|---------------------------|------|
|  |                  |   |                      |                 | Min           | Max                       |      |
| <b>CONVERTER AND MULTIPLEXER CHARACTERISTICS</b> |                  |   |                      |                 |               |                           |      |
| Total unadjusted error                           | ETU              |   | 1, 2, 3              | All             |               | ±1                        | LSB  |
| Comparator offset                                | V <sub>CO</sub>  |   | 1, 2, 3              | All             |               | ±20                       | mV   |
| V <sub>REF</sub> input resistance                | R <sub>IV</sub>  |   | 1, 2, 3              | All             | 3.5           | 10                        | kΩ   |
| Common mode input voltage                        | V <sub>ICM</sub> | All MUX inputs and COM input  | 1, 2, 3              | All             | GND<br>- 0.05 | V <sub>CC</sub><br>+ 0.05 | V    |
| DC common mode error                             | E <sub>CC</sub>  | ΔV <sub>CM</sub> = -0.05 V to +0.05 V   | 1, 2, 3              | All             |               | ±1/4                      | LSB  |
| Power supply sensitivity                         | V <sub>SEN</sub> | V <sub>REF</sub> = 4.75 V, V <sub>CC</sub> = 5 V ±5 %                                     | 1, 2, 3              | All             |               | ±1/4                      | LSB  |
|  |                  | V <sub>REF</sub> = 4.5 V, V <sub>CC</sub> = 5 V ±10 %                                     | 1, 2, 3              | All             |               | ±1/2                      | LSB  |
| Off channel leakage current                      | I <sub>OFF</sub> | On channel = 5 V, <sup>2/</sup><br>Off channel = 0 V                                      | 1, 2, 3              | All             | -3.0          |                           | μA   |
|  |                  | On channel = 0 V, <sup>2/</sup><br>Off channel = 5 V                                      | 1, 2, 3              | All             |               | +3.0                      | μA   |
| On channel leakage current                       | I <sub>ON</sub>  | On channel = 5 V, <sup>2/</sup><br>Off channel = 0 V                                      | 1, 2, 3              | All             |               | +3.0                      | μA   |
|  |                  | On channel = 0 V, <sup>2/</sup><br>Off channel = 5 V                                      | 1, 2, 3              | All             | -3.0          |                           | μA   |
| <b>DIGITAL CHARACTERISTICS</b>                   |                  |   |                      |                 |               |                           |      |
| Logical "1" input voltage                        | V <sub>INH</sub> | V <sub>CC</sub> = 5.5 V   | 1, 2, 3              | All             | 2.2           |                           | V    |
| Logical "0" input voltage                        | V <sub>INL</sub> | V <sub>CC</sub> = 4.5 V   | 1, 2, 3              | All             |               | 0.8                       | V    |
| Logical "1" input current                        | I <sub>IH</sub>  | V <sub>IN</sub> = V <sub>CC</sub>   | 1, 2, 3              | All             |               | 3.0                       | μA   |
| Logical "0" input current                        | I <sub>IL</sub>  | V <sub>IN</sub> = 0 V   | 1, 2, 3              | All             | -3.0          |                           | μA   |
| Logical "1" output voltage<br>except INT         | V <sub>OH</sub>  | V <sub>CC</sub> = 4.5 V, I <sub>OUT</sub> = -360 μA                                       | 1, 2, 3              | All             | 2.4           |                           | V    |
|  |                  | V <sub>CC</sub> = 4.5 V, I <sub>OUT</sub> = -10 μA  | 1, 2, 3              | All             | 4.2           |                           | V    |
| Logical "0" output voltage                       | V <sub>OL</sub>  | V <sub>CC</sub> = 4.5 V, I <sub>OUT</sub> = 1.6 mA  | 1, 2, 3              | All             |               | 0.4                       | V    |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

| Test   | Symbol                               | Conditions 1/<br>-55°C ≤ T <sub>A</sub> ≤ +125°C<br>unless otherwise specified | Group A<br>subgroups | Device<br>type | Limits |      | Unit               |
|--|--------------------------------------|--|----------------------|----------------|--------|------|--------------------|
|  |                                      |  |                      |                | Min    | Max  |                    |
| Three state output current<br>(DO)                           | I <sub>OTH</sub>                     | V <sub>OUT</sub> = 0.4 V,<br>CS = logic "1" = 5 V                              | 1, 2, 3              | All            | -3.0   |      | μA                 |
|  |                                      | V <sub>OUT</sub> = 5 V,<br>CS = logic "1" = 5 V                                | 1, 2, 3              | All            |        | +3.0 | μA                 |
| I <sub>SOURCE</sub> , except INT                             | I <sub>SOURCE</sub>                  | V <sub>OUT</sub> shorted to GND  | 1, 2, 3              | All            | 6.5    |      | mA                 |
| I <sub>SINK</sub>  | I <sub>SINK</sub>                    | V <sub>OUT</sub> shorted to I <sub>CC</sub>                                    | 1, 2, 3              | All            | 8      |      | mA                 |
| Supply current   | I <sub>CC</sub>                      | f <sub>CLK</sub> = 1 MHz   | 1, 2, 3              | All            |        | 10   | mA                 |
| Data clock frequency   | f <sub>CLK</sub>                     | 3/   | 9, 10, 11            | 02             |        | 2    | MHz                |
| Clock duty time  | DT                                   | 3/   | 9, 10, 11            | All            | 40     | 60   | %                  |
| CS falling edge or data<br>input valid to CLK rising<br>edge | t <sub>s</sub>                       | 3/   | 9, 10, 11            | All            | 70     |      | ns                 |
| Data input valid after<br>CLK rising edge                    | t <sub>h</sub>                       | 3/   | 9, 10, 11            | All            | 30     |      | ns                 |
| CLK rising edge to output<br>data valid                      | t <sub>PD1</sub><br>t <sub>PDO</sub> | C <sub>L</sub> = 100 pF 3/   | 9, 10, 11            | All            |        | 200  | ns                 |
| Rising edge of CS to data<br>output Hi-Z                     | t <sub>1H</sub><br>t <sub>0H</sub>   | C <sub>L</sub> = 100 pF, R = 2 kΩ 3/   | 9, 10, 11            | All            |        | 200  | ns                 |
| Oscillator clock frequency<br>(analog timing)                | f <sub>OSC</sub>                     | R <sub>EXT</sub> = 3.16 kΩ,<br>C <sub>EXT</sub> = 170 pF 3/                    | 9, 10, 11            | All            | .6     | 1.4  | MHz                |
| CS to end of conversion<br>delay                             | f <sub>EOC</sub>                     | 3/   | 9, 10, 11            | All            | 1      | 2    | OSC CLK<br>periods |
| Conversion time  | f <sub>CONV</sub>                    | 3/   | 9, 10, 11            | All            | 17     | 18   | OSC CLK<br>periods |
| CS to interrupt delay  | t <sub>CS-INT</sub>                  | 3/   | 9, 10, 11            | All            |        | 120  | ns                 |

1/ V<sub>CC</sub> = +5 V, V<sub>REF</sub> = 4.5 V, A<sub>GND</sub> = D<sub>GND</sub> = 0 V, f<sub>OSC</sub> = 1 MHz (R<sub>EXT</sub> = 3.16 kΩ, C<sub>EXT</sub> = 170 pF).

2/ Leakage current is measured with the oscillator clock disabled.

3/ V<sub>CC</sub> = +5 V, V<sub>REF</sub> = 4.5 V, A<sub>GND</sub> = D<sub>GND</sub> = 0 V, f<sub>CLK</sub> = 1 MHz, t<sub>r</sub> = t<sub>f</sub> = 5 ns. See figure 3.

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| Device type     | 01               | 02               |
|-----------------|------------------|------------------|
| Case outline    | E                | R                |
| Terminal number | Terminal symbol  |                  |
| 1               | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 2               | OSC              | OSC              |
| 3               | $\overline{CS}$  | $\overline{CS}$  |
| 4               | CLK              | CLK              |
| 5               | DI               | DI               |
| 6               | DO               | DO               |
| 7               | $\overline{INT}$ | $\overline{INT}$ |
| 8               | EOC              | EOC              |
| 9               | V <sub>REF</sub> | D <sub>GND</sub> |
| 10              | A <sub>GND</sub> | V <sub>REF</sub> |
| 11              | COM              | A <sub>GND</sub> |
| 12              | CH1              | COM              |
| 13              | CH0              | CH7              |
| 14              | COMPL            | CH6              |
| 15              | COMPH            | CH5              |
| 16              | D <sub>GND</sub> | CH4              |
| 17              | ---              | CH3              |
| 18              | ---              | CH2              |
| 19              | ---              | CH1              |
| 20              | ---              | CH0              |

FIGURE 1. Terminal connections.

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| MODE ADDRESS |    |    |    | MODE                        |
|--------------|----|----|----|-----------------------------|
| M3           | M2 | M1 | M0 |                             |
| 1            | 0  | 0  | 0  | Watchdog                    |
| 1            | 0  | 0  | 1  | Write one limit             |
| 1            | 0  | 1  | 0  | One A/D conversion          |
| 1            | 0  | 1  | 1  | Read one limit              |
| 1            | 1  | 0  | 0  | Test (for factory use only) |
| 1            | 1  | 0  | 1  | Write all limits            |
| 1            | 1  | 1  | 0  | Auto A/D conversion         |
| 1            | 1  | 1  | 1  | Read all limits             |

FIGURE 2. Mode selection table.

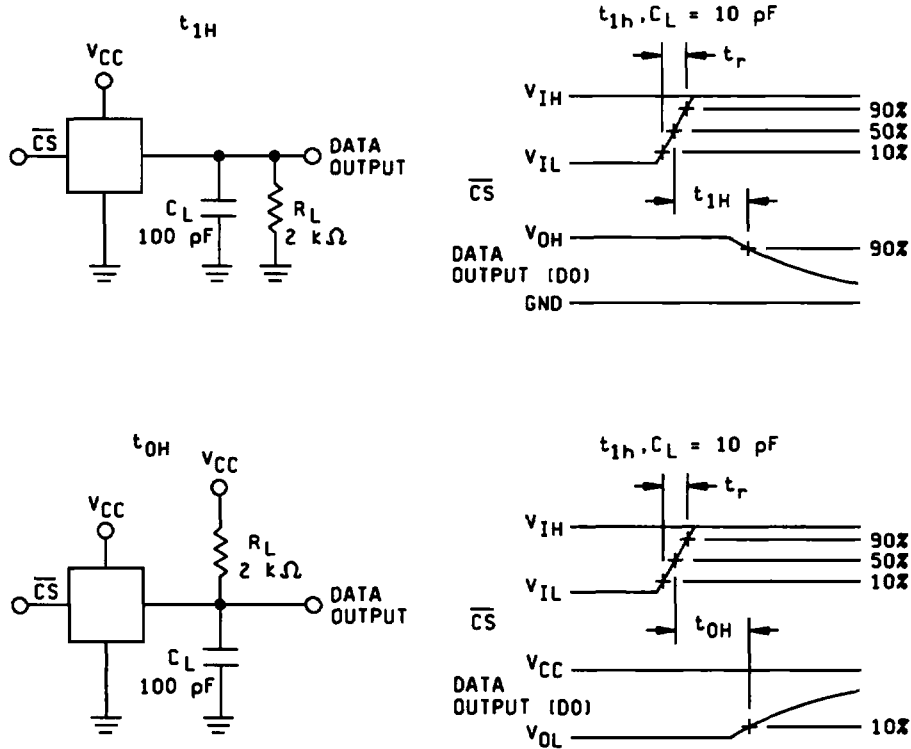


FIGURE 3. Test circuit and timing diagrams.

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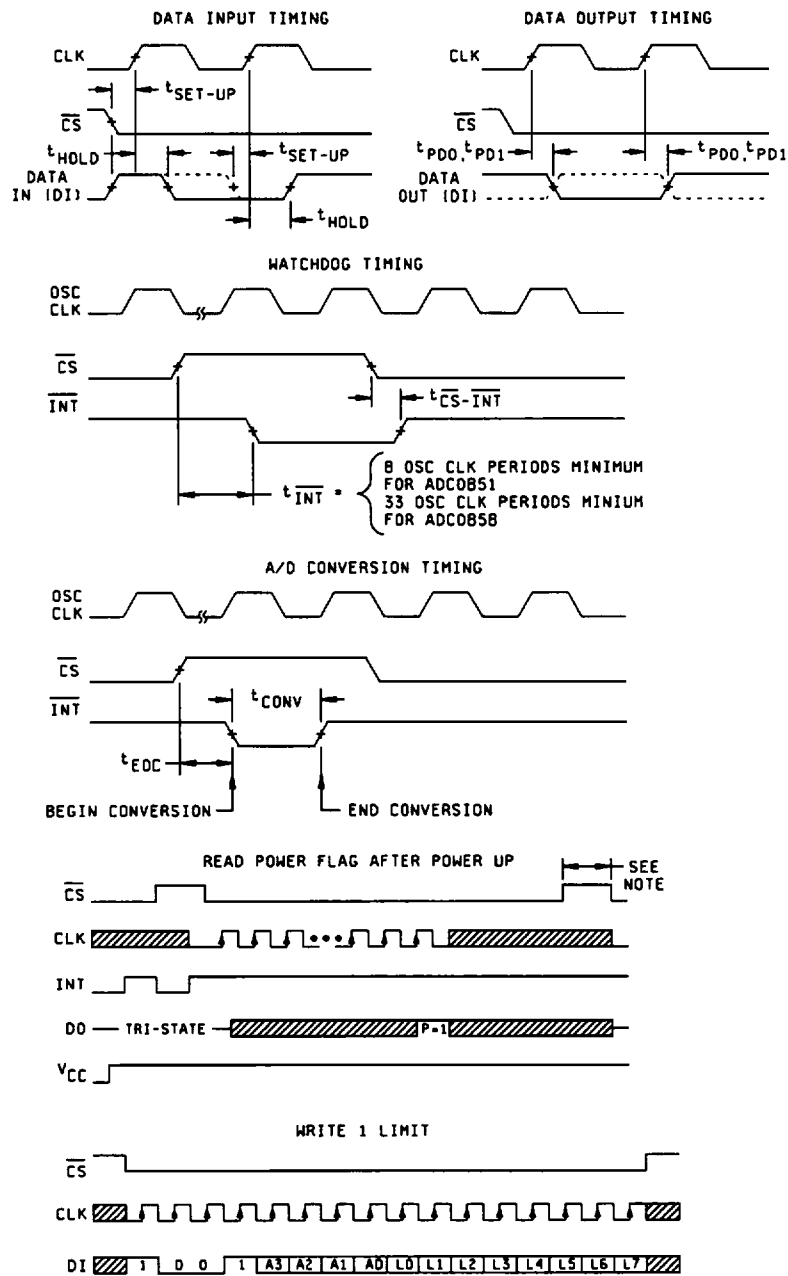
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NOTE: To change to a new mode of operation, this time must be shorter than 8 OSC clock periods for device type 01 and shorter than 32 OSC clock periods for device type 02.

FIGURE 3. Test circuit and timing diagrams - Continued.

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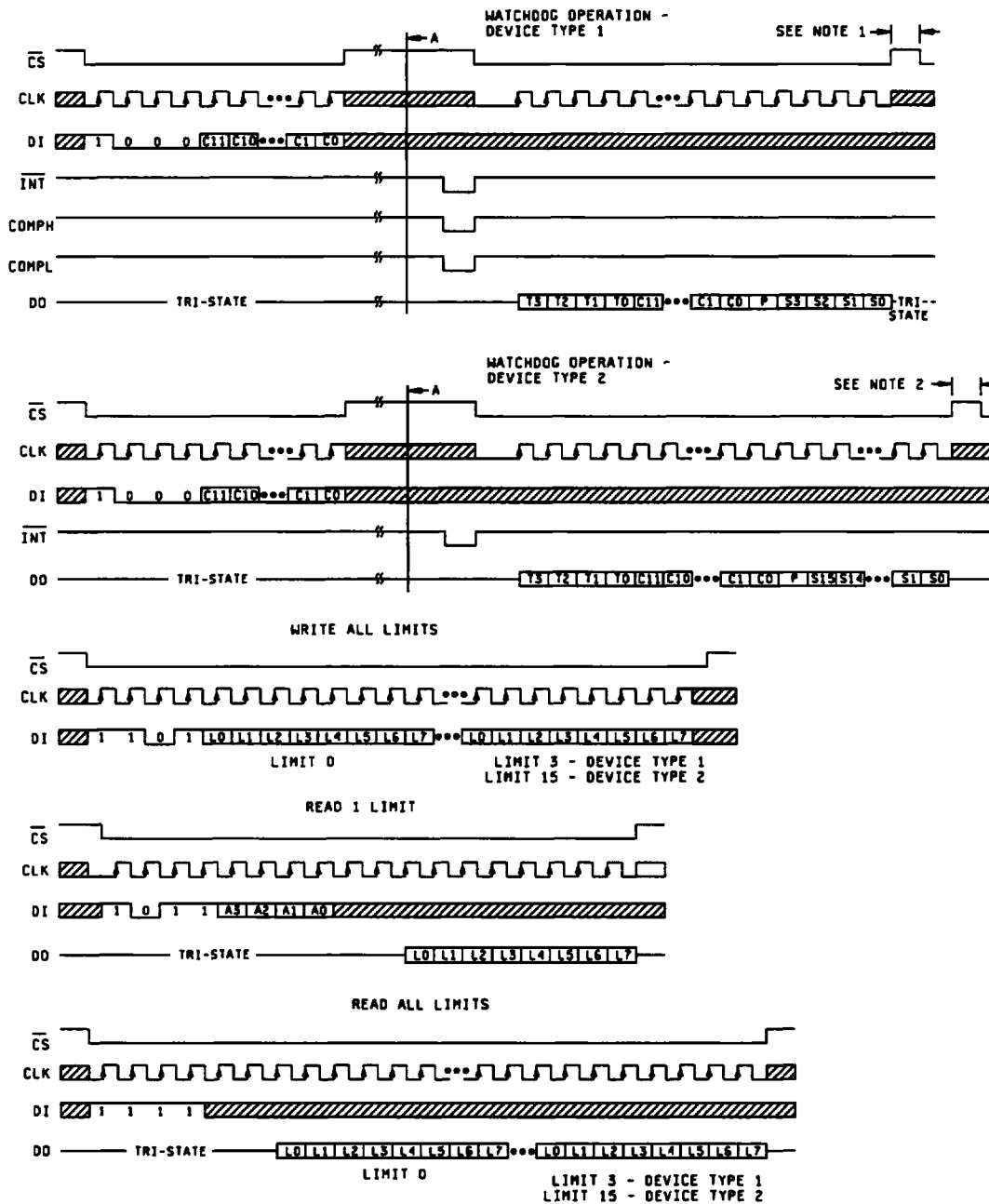
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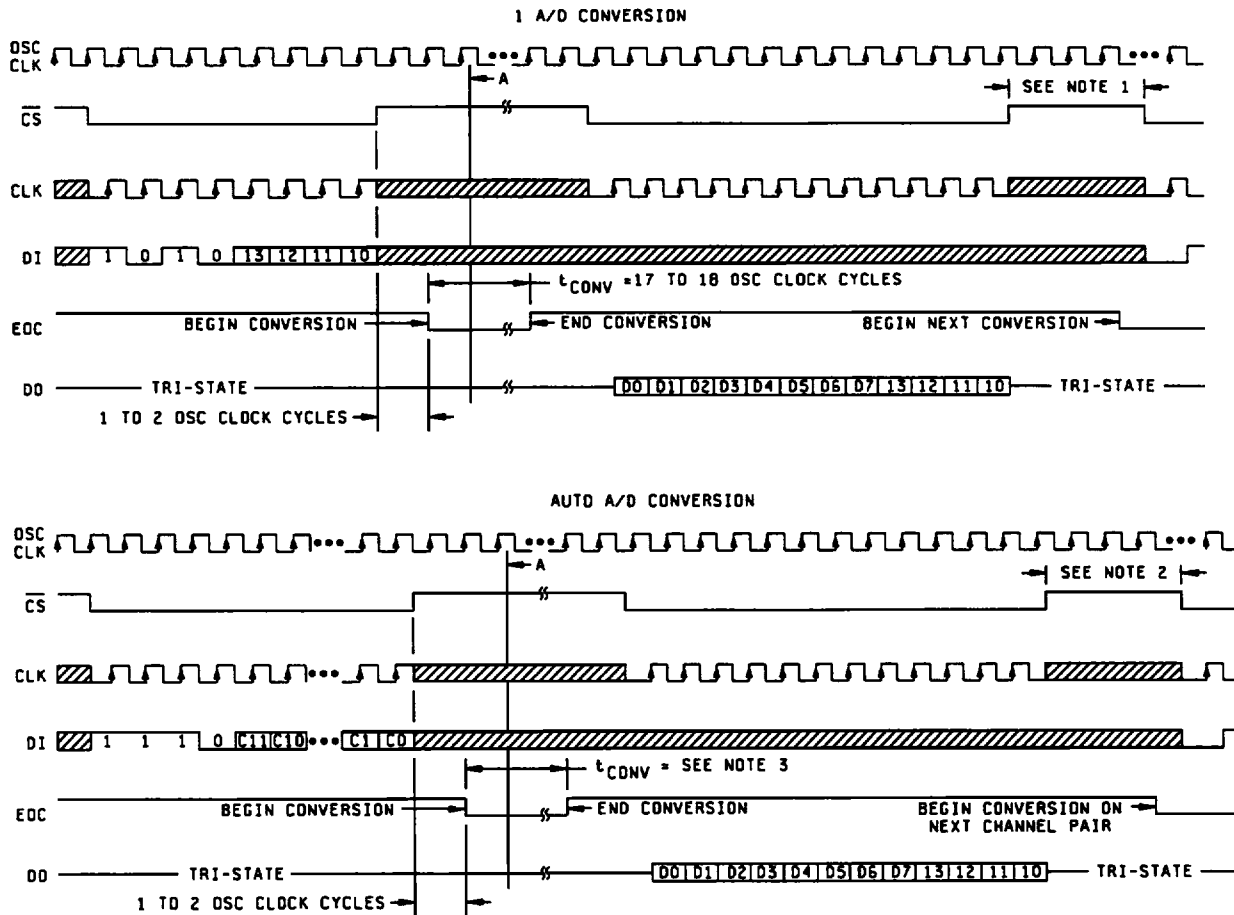


**NOTES:**

1. This time must be shorter than 8 OSC clock periods in order to change to a new mode. Otherwise, watchdog operation repeats from point "A" on the timing diagram.
2. This time must be shorter than 32 OSC clock periods in order to change to a new mode. Otherwise, watchdog operation repeats from point "A" on the timing diagram.

FIGURE 3. Test circuit and timing diagrams - Continued.

|   |                   |                |                   |
|---|-------------------|----------------|-------------------|
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- NOTES:
1. In order to change to a new mode, this time should be shorter than 17 OSC clock periods. A new A/D conversion on the same input repeats from point "A" on the timing diagram if this time is 18 or more OSC clock periods.
  2. In order to change to a new mode, this time should be shorter than 17 OSC clock periods.
  3. There are two A/D conversion modes that produce 8-bit conversion data. During either type of A/D conversion, a single-ended analog input or a differential analog input pair is digitized to produce this conversion data.

FIGURE 3. Test circuit and timing diagrams - Continued.

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4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
- b.  $T_A = +125^{\circ}\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

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TABLE II. Electrical test requirements.

| Test requirements                                 | Subgroups<br>(in accordance with MIL-STD-883, TM 5005, table I) |                       | Subgroups<br>(in accordance with MIL-I-38535, table III) |                       |
|---|---|-----------------------|--|-----------------------|
|   | Device class M  |                       | Device class Q   | Device class V        |
| Interim electrical parameters (see 4.2)           | ---   |                       | ---  | ---                   |
| Final electrical parameters (see 4.2)             | 1/ 1, 2, 3, 9, 10, 11   | 1/ 1, 2, 3, 9, 10, 11 | 1/ 1, 2, 3, 9, 10, 11                                    | 1/ 1, 2, 3, 9, 10, 11 |
| Group A test requirements (see 4.4)               | 1, 2, 3, 9, 10, 11  | 1, 2, 3, 9, 10, 11    | 1, 2, 3, 9, 10, 11                                       | 1, 2, 3, 9, 10, 11    |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 3   | 1, 2, 3               | 1, 2, 3  | 1, 2, 3               |
| Group D end-point electrical parameters (see 4.4) | 1   | 1                     | 1  | 1                     |
| Group E end-point electrical parameters (see 4.4) | ---   |                       | ---  | ---                   |

1/ PDA applies to subgroup 1.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ , after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

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6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

| <u>Military documentation format</u>                    | <u>Example PIN under new system</u> | <u>Manufacturing source listing</u> | <u>Document listing</u> |
|---|-------------------------------------|-------------------------------------|-------------------------|
| New MIL-H-38534 Standard Microcircuit Drawings          | 5962-XXXXXZZ(H or K)YY              | QML-38534                           | MIL-BUL-103             |
| New MIL-I-38535 Standard Microcircuit Drawings          | 5962-XXXXXZZ(Q or V)YY              | QML-38535                           | MIL-BUL-103             |
| New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings | 5962-XXXXXZZ(M)YY                   | MIL-BUL-103                         | MIL-BUL-103             |

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 95-11-27

Approved sources of supply for SMD 5962-95512 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

| Standard microcircuit drawing PIN | Vendor CAGE number | Vendor similar PIN <sup>1/</sup> |
|-----------------------------------|--------------------|----------------------------------|
| 5962-9551301QEX                   | 27014              | ADC0851CMJ/883                   |
| 5962-9551302QRX                   | 27014              | ADC0858CMJ/883                   |

<sup>1/</sup> Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

27014

Vendor name and address

National Semiconductor Corporation  
PO Box 58090  
Santa Clara, CA 95052

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.