Panasonic

NN30501A

http://www.semicon.panasonic.co.jp/en/

V_{IN} = 4.5V to 24V, 6A
Charge & Dump Storage System with 1 CH Buck Converter

FEATURES

- Built in Buck & Boost converter, to charge and dump the storage capacitor.
  - User programmable charge and dump voltage threshold.
  - External soft start capacitor with inductor peak current control for charging storage capacitor.
  - Dumping Status indicator.
- 1-Channel high-speed response DC-DC step down regulator circuit that employs hysteretic control system.
  - Output Voltage Range : 0.75V to 5.5V
  - Optimized frequency for efficiency :600 kHz
  - Internal Soft Start for component reduction
  - Power Good Indication for Output Over/Under voltage
  - Over/Under Voltage Detection (OVD/UVD)
  - Over Current Protection (OCP)
  - Short Circuit Protection (SCP)
- Built-in Under Voltage Lockout (UVLO) at typical 3.8V
- Thermal Shut Down (TSD)
- Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)
  (Size : 4 mm X 5 mm, 0.5 mm pitch)

DESCRIPTION

This IC provides the necessary charge and dump function for backup power management. The storage capacitor is charged through an internal Boost converter with user programmable soft start period. After charging is completed, the voltage is maintained through trickle charge at very low frequency. This charging voltage level is user-programmable.

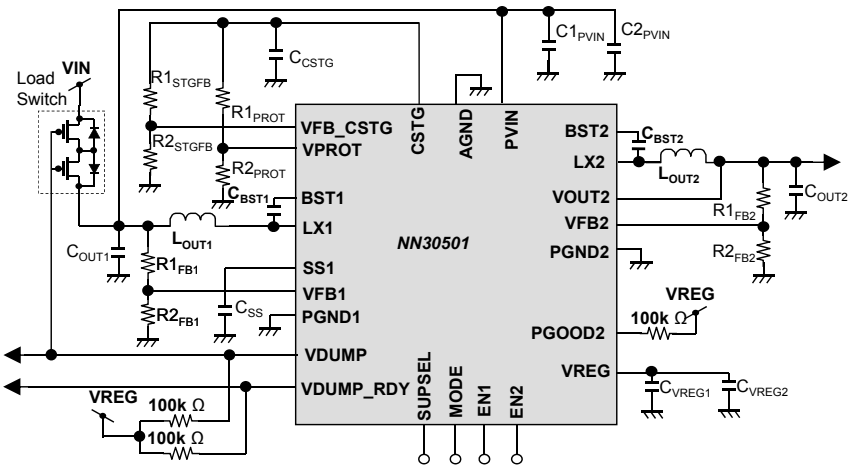
When the input voltage of the system drops below the user-programmable threshold, the energy from the storage capacitor will be dumped through an internal BUCK converter. A dumping status indicator is also provided.

This IC also provide a wide input range, high efficiency BUCK converter that can supply maximum 6A load current.

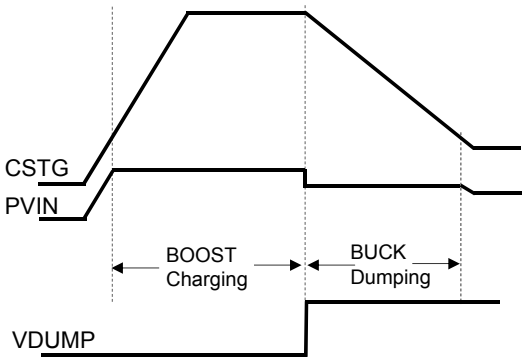
APPLICATIONS

- SSDs (Solid State Drives)
- Servers

TYPICAL APPLICATION



Charge and Dump Operation



Note:
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

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ORDERING INFORMATION

Order Number	Feature	Package	Packing Form
NN30501A-VB	Maximum Output Current : 6A	32 pin HQFN	Emboss taping

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	PV_{IN}	30	V	*1
Operating free-air temperature	T_{opr}	– 40 to + 85	°C	*2
Operating junction temperature	T_j	– 40 to + 150	°C	*2
Storage temperature	T_{stg}	– 55 to + 150	°C	*2
Input voltage range	V_{FB1_CSTG}, V_{FB1}, V_{OUT2}, V_{FB2}, V_{PROT}	– 0.3 to (V_{REG} + 0.3)	V	*1 *3
	V_{EN1}, V_{EN2}, V_{SS1}, V_{MODE}, V_{SUPSEL}	– 0.3 to 6.0	V	*1
Output voltage range	V_{PGOOD2}, V_{VDUMP_RDY}, V_{VDUMP}	– 0.3 to (V_{REG} + 0.3)	V	*1 *3
	V_{CSTG}, V_{LX1}	30	V	*1
	V_{LX2}	– 0.3 to (PV_{IN} + 0.3)	V	*1 *4
ESD	HBM	2	kV	—

Note: Do not apply external currents and voltages to any pin not specifically mentioned.
This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected. V_{IN} is voltage for PVIN. $V_{IN} = PV_{IN}$.
*1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25 °C.
*3: (V_{REG} + 0.3)V must not exceed 6V.
*4: (PV_{IN} + 0.3)V must not exceed 30V.

POWER DISSIPATION RATING

Package	θ_{j-a}	θ_{j-c}	P_D (T_a = 25 °C)	P_D (T_a = 85 °C)	Note
32 pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)	34.2 °C /W	5.4 °C /W	2.50 W	1.30 W	*1
	34.2 °C /W	5.4 °C /W	3.65 W	1.90 W	*2

Note: For the actual usage, please refer to the P_D-T_a characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.
*1: Glass Epoxy Substrate (4 Layers) [50 X 50 X 0.8 t (mm)]
*2: Glass Epoxy Substrate (4 Layers) [50 X 50 X 1.57 t (mm)] + Thermal vias

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Min	Typ	Max	Unit	Note
Supply voltage range	PV_{IN}	4.5	12	24	V	—
Input voltage range	V_{EN1}	– 0.3	—	5.0	V	*1
	V_{EN2}	– 0.3	—	5.0	V	*1
	V_{MODE}	– 0.3	—	5.0	V	*1
	V_{SUPSEL}	– 0.3	—	V_{REG} + 0.3	V	*1
Output voltage range	V_{DUMP_RDY}	– 0.3	—	V_{REG} + 0.3	V	*1
	V_{DUMP}	– 0.3	—	V_{REG} + 0.3	V	*1
	V_{PGOOD2}	– 0.3	—	V_{REG} + 0.3	V	*1
	V_{CSTG}	– 0.3	—	28	V	—
	V_{LX1}	– 0.3	—	V_{CSTG} + 0.6	V	—
	V_{LX2}	– 0.3	—	V_{IN} + 0.3	V	*2

Note: Voltage values, unless otherwise specified, are with respect to GND.

GND is voltage for AGND, PGND. AGND = PGND

V_{IN} is voltage for PVIN. V_{IN} = PV_{IN}.

Do not apply external currents or voltages to any pin not specifically mentioned.

*1: must not exceed 6V.

*2: (V_{IN} + 0.3)V must not exceed 24V.

ELECTRICAL CHARACTERISTICS

***5V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 15V, PV_{IN} = 5V, V_{OUT1} Setting = 4.5V, SUPSEL = 0V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

***12V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 28V, PV_{IN} = 12V, V_{OUT1} Setting = 10.2V, SUPSEL = 5V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current Consumption (12V System)							
Consumption current at active	I_{OPR2}	V_{EN1} = V_{EN2} = V_{MODE} = 1.8V, I_{OUT1} = I_{OUT2} = 0A, $R1_{STGFB}$ = 150kΩ, $R2_{STGFB}$ = 3.3kΩ, $R1_{FB1}$ = 32kΩ, $R2_{FB1}$ = 2kΩ, $R1_{FB2}$ = 15kΩ, $R2_{FB2}$ = 18kΩ DCDC No switching	—	1.70	3.40	mA	—
Consumption current at standby	I_{STB2}	V_{EN1} = V_{EN2} = 0V, $R1_{STGFB}$ = 150kΩ, $R2_{STGFB}$ = 3.3kΩ, $R1_{FB1}$ = 32kΩ, $R2_{FB1}$ = 2kΩ, $R1_{FB2}$ = 15kΩ, $R2_{FB2}$ = 18kΩ	—	500	1000	µA	—

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ELECTRICAL CHARACTERISTICS (Continued)

***5V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 15V, PV_{IN} = 5V, V_{OUT1} Setting = 4.5V, SUPSEL = 0V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

***12V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 28V, PV_{IN} = 12V, V_{OUT1} Setting = 10.2V, SUPSEL = 5V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Logic Pin Characteristics							
EN1 pin Low-level input voltage	V_{EN1L}	PV_{IN} = 12V	—	—	0.3	V	—
EN1 pin High-level input voltage	V_{EN1H}	PV_{IN} = 12V	1.5	—	5.0	V	—
EN1 pin leak current	$I_{leakEN1}$	PV_{IN} = 12V, V_{EN1} = 5V	—	6.25	12.5	µA	—
EN2 pin Low-level input voltage	V_{EN2L}	PV_{IN} = 12V	—	—	0.3	V	—
EN2 pin High-level input voltage	V_{EN2H}	PV_{IN} = 12V	1.5	—	5.0	V	—
EN2 pin leak current	$I_{leakEN2}$	PV_{IN} = 12V, V_{EN2} = 5V	—	6.25	12.5	µA	—
MODE pin Low level input voltage	V_{MDL}	PV_{IN} = 12V	—	—	0.3	V	—
MODE pin High level input voltage	V_{MDH}	PV_{IN} = 12V	1.5	—	5.0	V	—
MODE pin leak current	I_{leakMD}	PV_{IN} = 12V, V_{MODE} = 5V	—	10.0	20.0	µA	—
SUPSEL pin Low level input voltage	$V_{SUPSELL}$	PV_{IN} = 12V	—	—	0.3	V	—
SUPSEL pin High level input voltage	$V_{SUPSELH}$	PV_{IN} = 12V	1.5	—	5.0	V	—
SUPSEL pin leak current	$I_{leakSUPSEL}$	PV_{IN} = 12V, V_{SUPSEL} = 5V	—	6.25	12.5	µA	—
VREG Characteristics							
Output voltage	V_{REG}	PV_{IN} = 12V, I_{VREG} = 10mA	5.30	5.50	5.70	V	—
Line regulation	$V_{REGLINE}$	PV_{IN} = 12V, I_{VREG} = 10mA $V_{REGLIN} = V_{REG}$ (V_{IN} = 12V) − V_{REG} (V_{IN} = 6V) I_{VREG} = 10mA	—	—	200	mV	—
Drop out voltage	V_{REGDO}	PV_{IN} = 4.5V I_{VREG} = 10mA	4.1	—	—	V	—

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ELECTRICAL CHARACTERISTICS (Continued)

***5V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 15V, PV_{IN} = 5V, V_{OUT1} Setting = 4.5V, SUPSEL = 0V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

***12V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 28V, PV_{IN} = 12V, V_{OUT1} Setting = 10.2V, SUPSEL = 5V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
VFB Characteristics							
VFB1 comparator threshold	V_{FB1TH}	PV_{IN} = 12V	0.594	0.600	0.606	V	—
VFB1 pin leak current 1	$I_{leakF11}$	PV_{IN} = 12V, V_{FB1} = 0V	– 1	—	1	µA	—
VFB1 pin leak current 2	$I_{leakF12}$	PV_{IN} = 12V, V_{FB1} = 6V	– 1	—	1	µA	—
VFB2 comparator threshold	V_{FB2TH}	PV_{IN} = 12V	0.594	0.600	0.606	V	—
VFB2 pin leak current 1	$I_{leakF21}$	PV_{IN} = 12V, V_{FB2} = 0V	– 1	—	1	µA	—
VFB2 pin leak current 2	$I_{leakF22}$	PV_{IN} = 12V, V_{FB2} = 6V	– 1	—	1	µA	—
VFB_CSTG comparator threshold	$V_{FBCSTGTH}$	PV_{IN} = 12V	0.594	0.600	0.606	V	—
VFB_CSTG pin leak current 1	$I_{leakFCSTG1}$	PV_{IN} = 12V, V_{FB2} = 0V	– 1	—	1	µA	—
VFB_CSTG pin leak current 2	$I_{leakFCSTG2}$	PV_{IN} = 12V, V_{FB2} = 6V	– 1	—	1	µA	—
Under Voltage Lockout (UVLO)							
UVLO detection voltage	$V_{UVLODET}$	PV_{IN} = 5V to 0V	3.6	3.8	4.0	V	—
UVLO recover voltage	$V_{UVLORST}$	PV_{IN} = 0V to 5V	4.0	4.2	4.4	V	—
SS1 Characteristics							
SS1 Internal Resistance	R_{SS_INT}	PV_{IN} =12V	2.5	5.0	7.5	MΩ	*1
DCDC2 Soft Start Timing							
Soft start time DCDC2	$DD2_{SS}$	PV_{IN} =12V, Δt = 90% V_{OUT2} -10% V_{OUT2}	—	0.8	—	ms	*1

*1: Typical Design Value

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ELECTRICAL CHARACTERISTICS (Continued)

***5V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 15V, PV_{IN} = 5V, V_{OUT1} Setting = 4.5V, SUPSEL = 0V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

***12V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 28V, PV_{IN} = 12V, V_{OUT1} Setting = 10.2V, SUPSEL = 5V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DC-DC1 Characteristics (BOOST – 5V System)							
Line regulation	$DD1_{LINE1}$	V_{IN1} = 4.5V to 5.5V I_{OUT1} = 0mA	—	0.25	0.75	%/V	—
Output ripple voltage	$DD1_{RPL11}$	I_{OUT1} = 0mA, CSTG = 40uF	—	30	—	mV [p-p]	*1
DC-DC1 Characteristics (BOOST – 12V System)							
Line regulation	$DD1_{LINE1}$	V_{IN1} = 10V to 14V I_{OUT1} = 0mA	—	0.25	0.75	%/V	—
Output ripple voltage	$DD1_{RPL11}$	I_{OUT1} = 0mA, CSTG = 40uF	—	60	—	mV [p-p]	*1

*1: Typical Design Value

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ELECTRICAL CHARACTERISTICS (Continued)

***5V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 15V, PV_{IN} = 5V, V_{OUT1} Setting = 4.5V, SUPSEL = 0V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

***12V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 28V, PV_{IN} = 12V, V_{OUT1} Setting = 10.2V, SUPSEL = 5V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DC-DC1 Characteristics (BUCK – 5V System)							
Line regulation	$DD1_{LINE1}$	V_{CSTG} = 7V to 15V I_{OUT1} = 0.5A, V_{OUT1} = 4.5V	—	0.25	0.75	%/V	—
Load regulation	$DD1_{LOAD1}$	I_{OUT1} = 10mA to 6A, V_{CSTG} = 12V, V_{OUT1} = 4.5V	—	3.5	—	%	*1
Output ripple voltage 1	$DD1_{RPL11}$	I_{OUT1} = 10mA, V_{CSTG} = 15V, V_{OUT1} = 4.5V	—	30	—	mV [p-p]	*1
Output ripple voltage 2	$DD1_{RPL21}$	I_{OUT1} = 3A V_{CSTG} = 15V, V_{OUT1} = 4.5V	—	30	—	mV [p-p]	*1
Switching Frequency DCDC1	$DD1_{FREQ1}$	I_{OUT1} = 3A V_{CSTG} = 15V, V_{OUT1} = 4.5V	—	330	—	kHz	*1
DC-DC1 Characteristics (BUCK – 12V System)							
Line regulation	$DD1_{LINE2}$	V_{IN1} = 15V to 21V I_{OUT1} = 0.5A, V_{OUT1}= 10.2V	—	0.25	0.75	%/V	—
Load regulation	$DD1_{LOAD2}$	I_{OUT1} = 10mA to 6A, V_{CSTG} = 20V, V_{OUT1}= 10.2V	—	3.5	—	%	*1
Output ripple voltage 1	$DD1_{RPL12}$	I_{OUT1} = 10mA, V_{CSTG} = 28V, V_{OUT1}= 10.2V	—	25	—	mV [p-p]	*1
Output ripple voltage 2	$DD1_{RPL22}$	I_{OUT1} = 3A V_{CSTG} = 28V, V_{OUT1}= 10.2V	—	25	—	mV [p-p]	*1
Switching Frequency DCDC1	$DD1_{FREQ1}$	I_{OUT1} = 3A V_{CSTG} = 28V, V_{OUT1}= 10.2V	—	800	—	kHz	*1

*1: Typical Design Value

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ELECTRICAL CHARACTERISTICS (Continued)

***5V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 15V, PV_{IN} = 5V, V_{OUT1} Setting = 4.5V, SUPSEL = 0V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

***12V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 28V, PV_{IN} = 12V, V_{OUT1} Setting = 10.2V, SUPSEL = 5V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DC-DC2 Characteristics							
DCDC2 Line regulation	$DD2_{LINE1}$	PV_{IN} = 6V to 24V I_{OUT2} = 0.5A, V_{OUT2} = 1.1V	—	0.25	0.75	%/V	—
DCDC2 Load regulation	$DD2_{LOAD1}$	I_{OUT2} = 10mA to 6A, PV_{IN} = 12V, V_{OUT2} = 1.1V	—	3.5	—	%	*1
DCDC2 Output ripple voltage 1	$DD2_{RPL11}$	I_{OUT2} = 10mA , PV_{IN} = 12V, V_{OUT2} = 1.1V	—	20	—	mV [p-p]	*1
DCDC2 Output ripple voltage 2	$DD2_{RPL21}$	I_{OUT2} = 3A PV_{IN} = 12V, V_{OUT2} = 1.1V	—	20	—	mV [p-p]	*1
DCDC2 Load transient response 1	$DD2_{TR11}$	I_{OUT2} = 100mA to 3A Δt = 0.5A/µs, PV_{IN} = 12V, V_{OUT2} = 1.1V	—	20	—	mV	*1
DCDC2 Load transient response 2	$DD2_{TR21}$	I_{OUT2} = 3A to 100mA Δt = 0.5A/µs, PV_{IN} = 12V, V_{OUT2} = 1.1V	—	20	—	mV	*1
Switching Frequency DCDC2	$DD2_{FREQ1}$	I_{OUT2} = 3A PV_{IN} = 12V, V_{OUT2} = 1.1V	—	600	—	kHz	*1

*1: Typical Design Value

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ELECTRICAL CHARACTERISTICS (Continued)

***5V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 15V, PV_{IN} = 5V, V_{OUT1} Setting = 4.5V, SUPSEL = 0V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

***12V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 28V, PV_{IN} = 12V, V_{OUT1} Setting = 10.2V, SUPSEL = 5V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DC-DC1 Output Power MOS On Resistance							
DCDC1 High Side Power MOSFET ON resistance	$DD1R_{ONH}$	PV_{IN} = 12V, V_{GS} = 5.0V	—	20	40	mΩ	—
DCDC1 Low Side Power MOSFET ON resistance	$DD1R_{ONL}$	PV_{IN} = 12V, V_{GS} = 5.0V	—	20	40	mΩ	—
DCDC1 MIN input and output voltage difference	$DD1V_{diff}$	$V_{diff} = V_{IN1} - V_{OUT1}$	—	2.5	—	V	*1
DC-DC2 Output Power MOS On Resistance							
DCDC2 High Side Power MOSFET ON resistance	$DD2R_{ONH}$	PV_{IN} = 12V, V_{GS} = 5.0V	—	20	40	mΩ	—
DCDC2 Low Side Power MOSFET ON resistance	$DD2R_{ONL}$	PV_{IN} = 12V, V_{GS} = 5.0V	—	20	40	mΩ	—
DCDC2 MIN input and output voltage difference	$DD2V_{diff}$	$V_{diff} = V_{IN2} - V_{OUT2}$	—	1.5	—	V	*1

*1: Typical Design Value

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ELECTRICAL CHARACTERISTICS (Continued)

***5V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 15V, PV_{IN} = 5V, V_{OUT1} Setting = 4.5V, SUPSEL = 0V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

***12V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 28V, PV_{IN} = 12V, V_{OUT1} Setting = 10.2V, SUPSEL = 5V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
VDUMP							
VDUMP Threshold (V_{FB1} for Dumping Threshold setting)	V_{DUMP_VTH}	PV_{IN} = 12V, V_{DUMP} : Low to High	0.56	0.600	0.64	V	—
VDUMP ON Resistance	RV_{DUMP}	PV_{IN} = 12V, I_{DUMP} = +20mA	—	10	15	Ω	—
VDUMP_RDY							
VDUMP_RDY Threshold 1 (V_{FB_CSTG} ratio for UVD release)	V_{RDY1}	PV_{IN} = 12V, V_{FB_CSTG} ratio for V_{DUMP_RDY} Low to High	82	90	98	%	—
VDUMP_RDY Threshold 2 (V_{FB_CSTG} ratio for UVD detect)	V_{RDY2}	PV_{IN} = 12V, V_{FB_CSTG} ratio for V_{DUMP_RDY} High to Low	72	80	88	%	—
VDUMP_RDY ON Resistance	RV_{RDY1}	PV_{IN} = 12V, I_{DUMP_RDY} = +20mA	—	10	15	Ω	—
PGOOD2 Characteristics							
PGOOD2 Threshold 1 (V_{FB} ratio for UVD detect)	V_{PGUVD}	PV_{IN} = 12V, V_{PGOOD2} : High to Low	77	85	93	%	—
PGOOD2 Hysteresis 1 (V_{FB} ratio for UVD release)	ΔV_{PGUVD}	PV_{IN} = 12V, V_{PGOOD2} : Low to High	3.5	5.0	6.5	%	—
PGOOD2 Threshold 2 (V_{FB} ratio for OVD detect)	V_{PGOVD}	PV_{IN} = 12V, V_{PGOOD2} : High to Low	107	115	123	%	—
PGOOD2 Hysteresis 2 (V_{FB} ratio for OVD release)	ΔV_{PGOVD}	PV_{IN} = 12V, V_{PGOOD2} : Low to High	3.5	5.0	6.5	%	—
PGOOD2 On Resistance	RON_{PG}	PV_{IN} = 12V, I_{PGOOD2} = +20mA	—	10	15	Ω	—

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ELECTRICAL CHARACTERISTICS (Continued)

***5V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 15V, PV_{IN} = 5V, V_{OUT1} Setting = 4.5V, SUPSEL = 0V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

***12V System**

DCDC1: C_{OUT1} = 22µF × 4, L_{OUT1} = 3.3µH, V_{CSTG} Setting = 28V, PV_{IN} = 12V, V_{OUT1} Setting = 10.2V, SUPSEL = 5V
DCDC2: C_{OUT2} = 22µF × 4, L_{OUT2} = 1.0µH, V_{OUT2} Setting = 1.1V, Switching Frequency = 600kHz, MODE = 0V, EN1 = EN2 = 1.8V, T_a = 25°C ± 2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DCDC1 Boost mode Protection							
VPROT OVP Detect	VPR_{OVP1}	PV_{IN} = 12V	—	1.16	—	V	*1
VPROT OVP Release	VPR_{OVP2}	PV_{IN} = 12V	—	1	—	V	*1
VPROT OVP Hysteresis	VPR_{OHYS}	VPR_{OVP1c} - VPR_{OVP2}	—	160	—	mV	*1
DCDC1 Buck mode Protection							
DC-DC1 Over Current Protection Limit	$DD1_{OCP}$	PV_{IN} = 12V	—	8	—	A	*1 *2
DCDC2 Protection							
DC-DC2 Over Current Protection Limit	$DD2_{OCP}$	PV_{IN} = 12V	—	8	—	A	*1 *2
DC-DC2 Short Circuit Protection Threshold	$DD2_{VSCP}$	PV_{IN} = 12V, V_{FB2} = 0.6V to 0.0V	50	60	70	%	—
Thermal Shutdown							
Thermal Shut Down (TSD) Threshold	TSD	PV_{IN} = 12V	—	130	—	°C	*1
Thermal Shut Down (TSD) Hysteresis	TSD_{HYS}	PV_{IN} = 12V	—	30	—	°C	*1

*1: Typical Design Value
*2: In addition to the built-in over current protection, ensure the IC operates normally within the safe operating region. The IC power dissipation or thermal performance varies with the PCB size, layout and materials.

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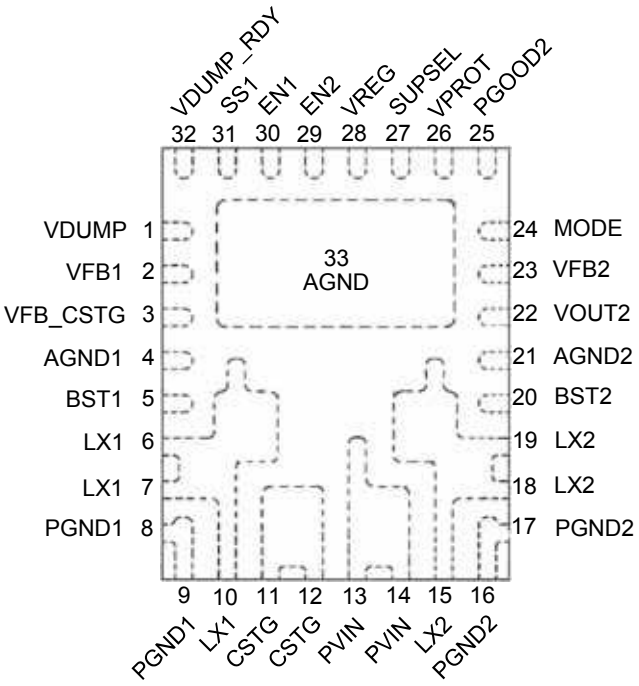
PIN CONFIGURATION

TOP VIEW



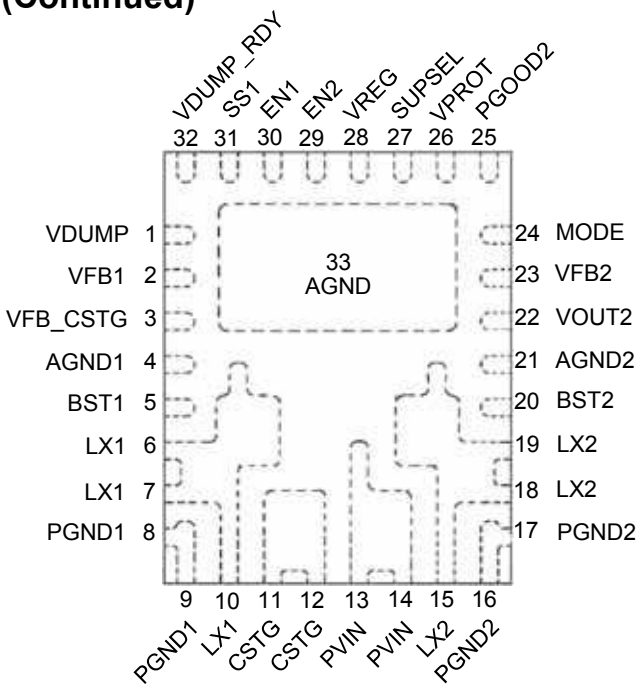
PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	VDUMP	Output	VDUMP open drain output
2	VFB1	Input	Comparator negative input pin for channel 1 BUCK Mode DC-DC
3	VFB_CSTG	Input	Comparator negative input pin for channel 1 BOOST Mode DC-DC
4	AGND1	Ground	Ground pin
5	BST1	Output	Supply input pin for high side FET gate driver for channel 1
6	LX1	Output	Power MOSFET output pin & for radiation of heat for channel 1
7			
10			
8	PGND1	Ground	Ground pin for Power MOSFET for channel 1
9			
11	CSTG	Input/ Output	Output pin during BOOST mode & Input pin during BUCK mode for channel 1
12			
13	PVIN	Power supply	Power supply pin for Power MOSFET & for radiation of heat for channel 2
14			
16	PGND2	Ground	Ground pin for Power MOSFET for channel 2
17			

Note: For the details on pin description, please refer to the OPERATION and APPLICATION INFORMATION section.

PIN CONFIGURATION (Continued)

TOP VIEW



PIN FUNCTIONS (continued)

Pin No.	Pin name	Type	Description
15	LX2	Output	Power MOSFET output pin & for radiation of heat for channel 2
18			
19			
20	BST2	Output	Supply input pin for high side FET gate driver for channel 2
21	AGND2	Ground	Ground pin
22	VOUT2	Input	Output voltage sense pin for channel 2
23	VFB2	Input	Comparator negative input pin for channel 2
24	MODE	Input	Control pin to change DCDC operation mode (Skip/FCCM)
25	PGOOD2	Output	Power good open drain pin for channel 2
26	VPROT	Input	Protection Pin for DCDC1 Boost Mode
27	SUPSEL	Input	5V/12V system selector
28	VREG	Output	Internal regulator
29	EN2	Input	ON/OFF control pin for channel 2
30	EN1	Input	ON/OFF control pin for channel 1
31	SS1	Input	Soft start pin for channel 1 DC-DC
32	VDUMP_RDY	Output	VDUMP ready open drain output
33	AGND	Ground	Ground pin for heat radiation

Note: For the details on pin description, please refer to the OPERATION and APPLICATION INFORMATION section.

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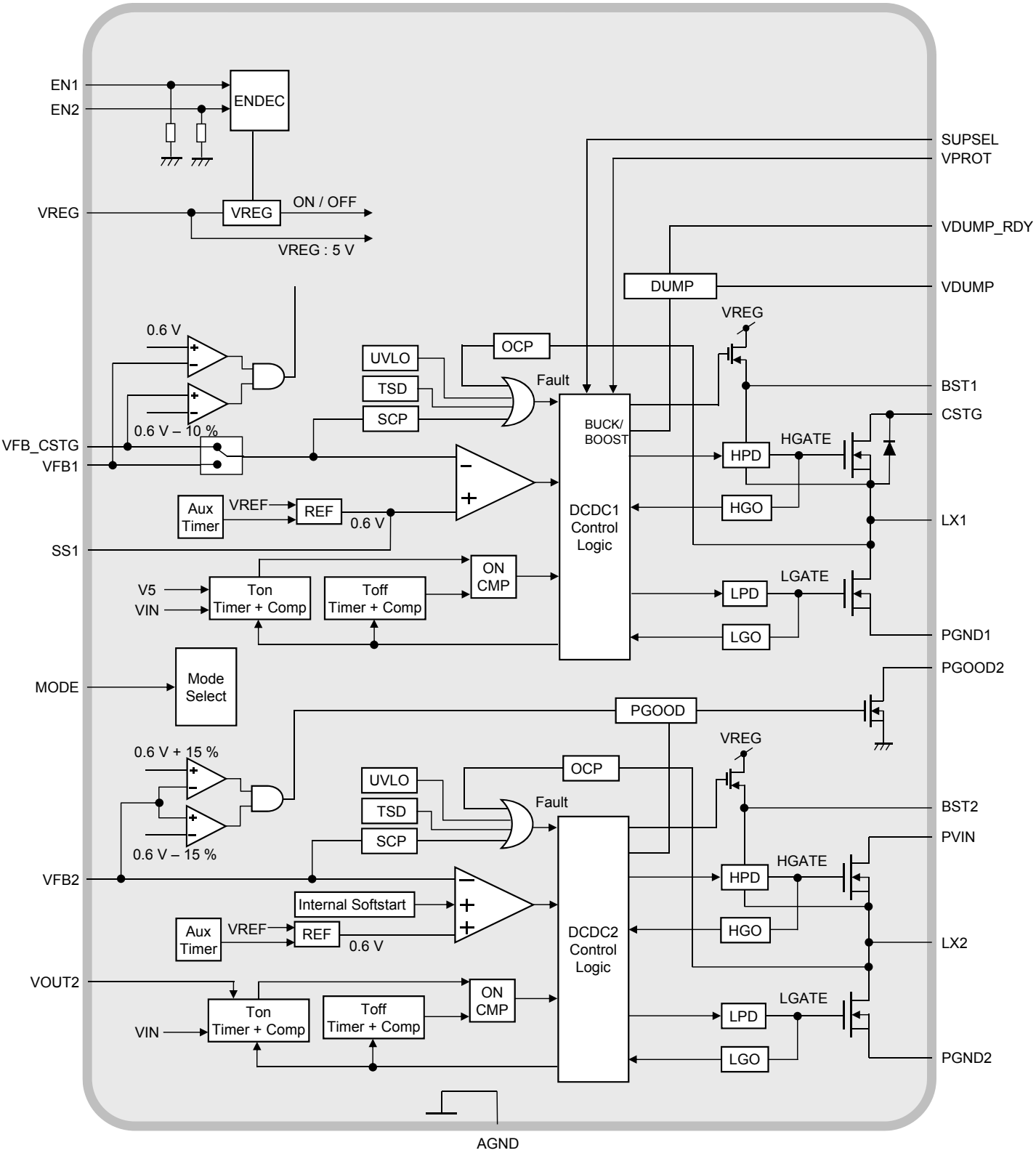
FUNCTIONAL BLOCK DIAGRAM



Note : This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

OPERATION

1. CH1 Storage Capacitor Charging & Dumping

(A) Storage Capacitor Charging

When EN1 is high and PVIN rises above the Under Voltage Lock Out (UVLO), the inbuilt BOOST converter start to operate and charges the storage capacitor at CSTG pin. The CSTG soft start period or the average charging current is determined by the external capacitor connected at the SS1 pin.

The final charging voltage level is user programmable through external resistor ratio across VFB_CSTG and CTSG pins.

At steady state, the BOOST converter will continue to trickle charge the storage capacitor to maintain its threshold.

(B) Storage Capacitor Dumping

When voltage level at CSTG reaches 90% of its final value, the system is ready for dumping. The dumping threshold level is user programmable through resistor ratio across PVIN & VFB1.

When PVIN drop below the dumping threshold, the built-in BOOST converter stops charging. The built-in BUCK converter starts to operate and dumps its charge from the storage capacitor to PVIN.

At the same time, the DUMP status pin flags high to indicate system in dumping mode. This status flag can be used by the system to initiate the dumping process. The storage dumping process is latched type event, it can only be reset by EN1 is low or system Under Voltage Lock Out (UVLO)

Please note that VDUMP_RDY will change to LOW when CSTG voltage drops to 80%.

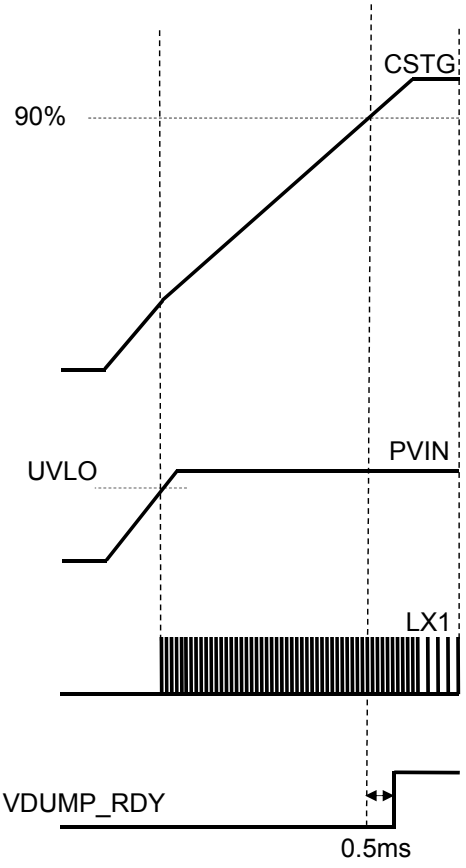


Figure 1A : Storage capacitor charging

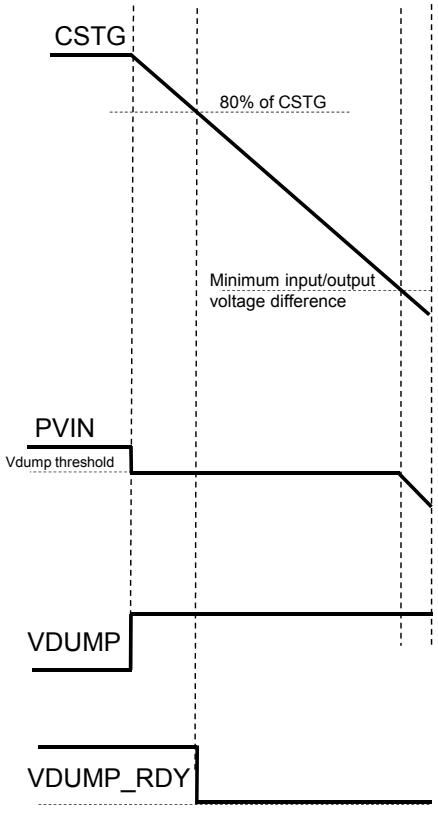


Figure 1B : Storage capacitor dumping

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OPERATION (Continued)

1. CH1 Storage Capacitor Charging & Dumping (Continued)

(C) Storage Capacitor Charging Voltage Setting

The Output Voltage can be set by external resistance of FB_CSTG pin, and its calculation is as follows.

$$V_{CSTG} = (1 + \frac{R1_{STGFB}}{R2_{STGFB}}) \times 0.6$$

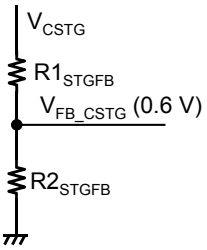

Figure 1C : Charging voltage setting

Below resistors are recommended for following popular output voltages.

V_{CSTG} [V]	$R1_{STGFB}$ [Ω]	$R2_{STGFB}$ [Ω]
27.87	150k	3.3k
22.5	56k	1.5k
17.4	56k	2k
14.7	47k	2k

V_{FB_CSTG} comparator threshold is adjusted to ±1%, but the actual output voltage accuracy becomes more than ±1% due to the influence from the circuits other than V_{FB_CSTG} comparator.

(D) Storage Capacitor Charging Soft Start

The soft start during BOOST charging is programmable through SS1 pin. The soft start time constant T_{SS}, can be computed as follows:

$$Tss = Css \times 5M\Omega$$

(E) Storage Capacitor Dumping Voltage Setting

The IC will trigger dumping mode when input supply voltage decreases to the programmed dumping threshold voltage. The dumping threshold voltage can be set by external resistance connected to V_{OUT1} and V_{FB1} pin, and its calculation is as follows.

$$V_{OUT1} = (1 + \frac{R1_{FB1}}{R2_{FB1}}) \times 0.6$$

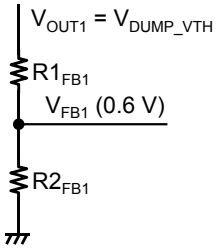

Figure 1E : Dumping voltage setting

Where

V_{DUMP_VTH} = Dumping threshold

V_{OUT1} = DCDC1 output voltage during dumping

$V_{DUMP\_VTH} = V_{OUT1}$

Below resistors are recommended for following popular output voltages.

V_{DUMP_VTH} [V]	$R1_{FB1}$ [Ω]	$R2_{FB1}$ [Ω]
10.2	32k	2k
4.5	13k	2k

V_{FB1} comparator threshold is adjusted to ±1%, but the actual output voltage accuracy becomes more than ±1% due to the influence from the circuits other than V_{FB1} comparator.

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OPERATION (Continued)

2. CH1 Storage Capacitance Estimation

The energy available from the storage capacitor can be computed as follow:

$$Storage\ Energy = 0.5C_{STG}\left(V_{CSTG}{}^2 - V_{DUMP\_VTH}{}^2\right)$$

C_{STG}: Storage capacitance
V_{CSTG}: User programmable charging voltage
V_{DUMP}: User programmable dumping threshold

Similarly, the dumping period can be computed as follow:

$$DumpingPeriod = \frac{0.5C_{STG}\left(V_{CSTG}{}^2 - V_{DUMP\_VTH}{}^2\right)}{P_{OUT}} \times 0.85$$

P_{OUT} : Power consumed during dumping

Storage Capacitance Estimation Example:

P_{OUT}	5W	9W	12W
V_{STG}	18V	18V	18V
V_{DUMP_VTH}	4.5V	4.5V	4.5V
Unit Cap*1	100uF	100uF	100uF
Quantity	4	8	10
Total Cap	400uF	800uF	1000uF
Dumping Period	~10ms	~11ms	~10ms

3. CH1 BOOST Mode Protection

(1) Over Voltage Protection (OVP) function – DCDC1

a) Output voltage abnormality occurs and starts to charge CSTG voltage higher.
b) When the OVP detection threshold level is reached, LX will stop switching. CSTG voltage will slowly discharge depending on the V_{FB_CSTG} feedback resistor and CSTG capacitor setting.
c) When CSTG voltage reaches the OVP release threshold level, LX will start switching and if OVP fault condition is still present, OVP mechanism will repeat continuously.

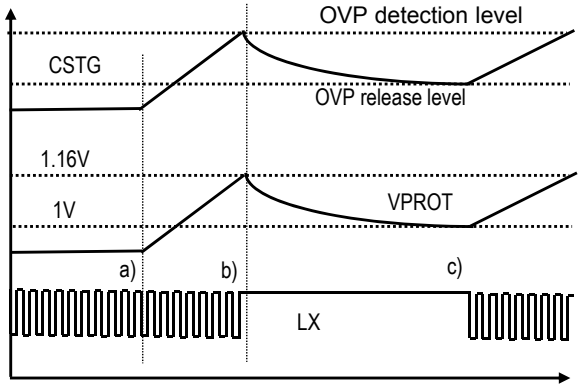

Figure 3A : DCDC1 Boost mode OVP operation

CSTG over voltage protection threshold level can be computed as follows:

$$V_{OVP} = \left(1 + \frac{R1_{PROT}}{R2_{PROT}}\right) \times 1.16V$$

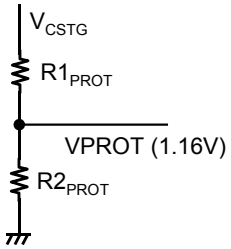

Figure 3B : DCDC1 VPROT pin resistors setting

Note: OVP threshold accuracy is defined by the electrical characteristic VPR_{OVP1} and VPR_{OVP2}

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OPERATION (Continued)

4. CH2 Buck mode Protection

(1) Over Current Protection (OCP) function and Short Circuit Protection (SCP) function - DCDC2 only

a) The Over Current Protection is activated at about 8A (Typ). This device uses pulse-by-pulse valley current protection method. When the low side power MOSFET is turned on, the voltage across the drain and source is monitored which is proportional to the inductor current. The high side power MOSFET is only allowed to turn on when the current flowing in the low side power MOSFET falls below the OCP level.

Hence, during the OCP, the output voltage continues to drop at the specified current. OCP is a non–latch type protection.

b) The Short Circuit Protection function is implemented when the output voltage decreases and the VFB pin reaches to about 60% of the set voltage (0.6V).
The SCP operates intermittently at about 2ms ON, 16ms OFF intervals.

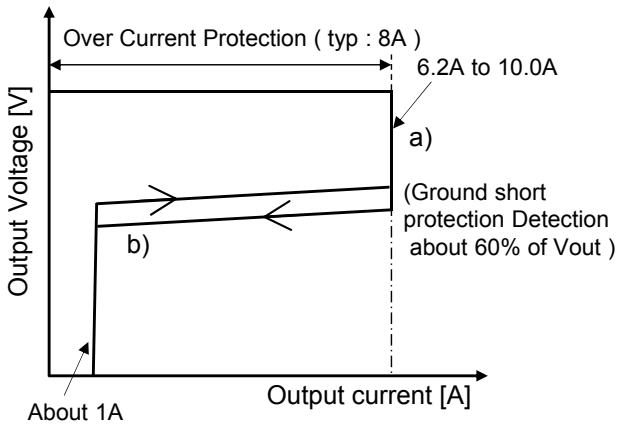

Figure 4A : OCP and SCP Operation

(2) Over Voltage Detection (OVD) and Under Voltage Detection (UVD) - DCDC2 only

a) The NMOS connected to the PGOOD pin turns ON when the output voltage rises and the VFB pin voltage reaches 115 % of its set voltage (0.6 V).

b) After (a) above, the NMOS connected to the PGOOD pin is turned OFF after 1 ms when the output voltage drops and the VFB pin voltage reaches 110% of its set voltage (0.6 V).

c) The NMOS connected to the PGOOD pin turns ON when the output voltage drops and the VFB pin voltage reaches 85% of its set voltage (0.6V).

d) After (c) above, the NMOS connected to the PGOOD pin is turned OFF after 1ms when the output voltage drops and the VFB pin voltage reaches 90% of its set voltage (0.6V).

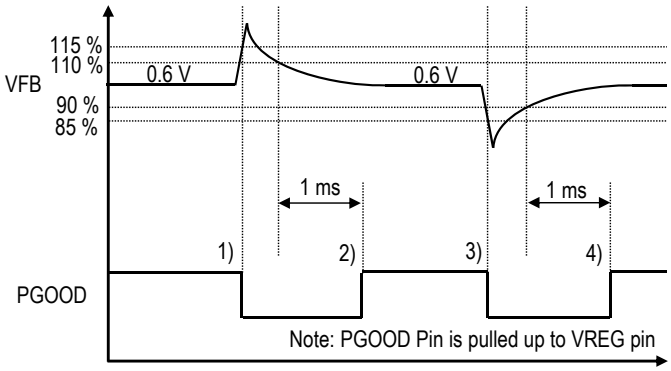

Figure 4B : OVD and UVD Operation

(3) Output discharging function - DCDC2 only

When EN2 is low, the output is discharged by an internal MOSFET that is connected to VOUT2 pin. When EN2 is high, if the controller is turned off by Under Voltage Lock Out (UVLO), Over Voltage Protection (OVP) or Short Circuit Protection (SCP), the output is also discharged by the above said internal MOSFET. The ON resistance of the internal MOSFET is about 50 Ω.

(4) Thermal Shut Down (TSD)

When the LSI internal temperature becomes more than about 130°C, TSD operates and DC-DC turns off.

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OPERATION (Continued)

5. CH2 Output Voltage Setting

The Output Voltage can be set by external resistance of FB pin, and its calculation is as follows.

$$V_{OUT2} = (1 + \frac{R1_{FB2}}{R2_{FB2}}) \times 0.6$$

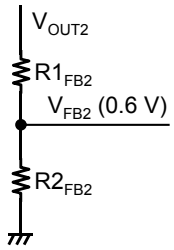

Figure 5A : DCDC2 output voltage setting

Below resistors are recommended for following popular output voltages.

V_{OUT2} [V]	$R1_{FB2}$ [Ω]	$R2_{FB2}$ [Ω]
5.00	88 k	12 k
3.30	54 k	12 k
2.85	75 k	20 k
1.80	36 k	18 k
1.10	15 k	18 k
1.00	12 k	18 k

V_{FB2} comparator threshold is adjusted to ±1%, but the actual output voltage accuracy becomes more than ±1% due to the influence from the circuits other than VFB comparator.

6. CH2 Soft Start

This IC has built-in Soft Start function without using external component. Soft Start function maintains the smooth control of the output voltage during start up to avoid overshoot & rush current. When the EN2 pin becomes High, the DCDC2 output voltage rises up in the period of about 1ms.

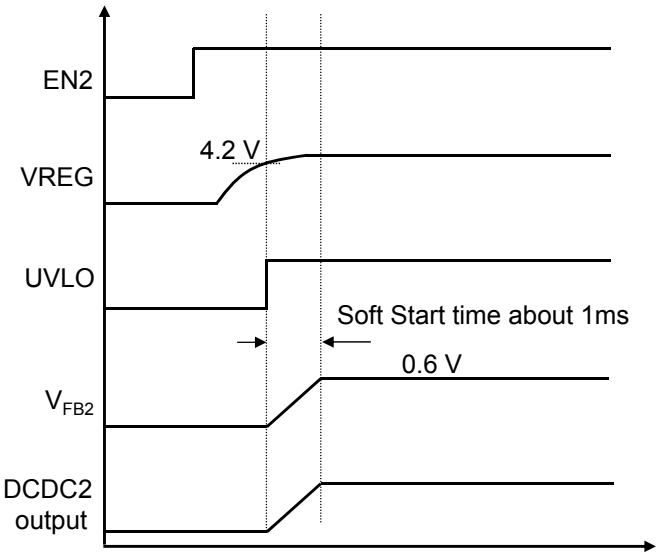

Figure 6A : Soft Start Operation

7. Internal regulator

This IC has one internal regulator which is enabled/ disabled by either EN1 or EN2.
External capacitors should be placed near the VREG for stable operation.

(1) VREG
The voltage of VREG pin regulator is 5.5V and it is used to supply internal circuits of IC. The VREG has current capability of about 100mA and has over-current protection.

OPERATION (Continued)

8. EN, MODE and SUPSEL setting

(1) EN1 and EN2

The Start up / Shut down is enabled by the EN1 / EN2 pin. The EN1 controls DCDC1 and EN2 controls DCDC2. Both EN pins are able to control internal regulator VREG. The EN1 and EN2 pin input voltages (V_{ENH}, V_{ENL}) should satisfy the conditions as defined in the electrical characteristics.

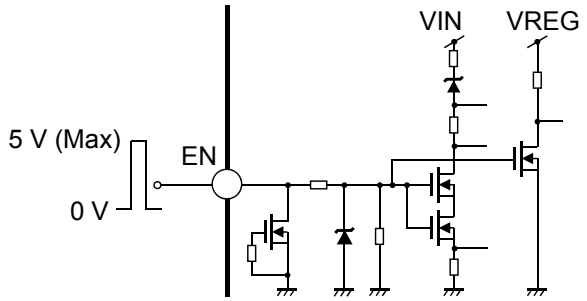

Figure 8A : Internal circuit with EN pin

(2) MODE

Mode Pin controls DCDC2 mode of operation. Mode Pin can control DCDC1 mode of operation only during storage dumping (buck mode). Please Refer to the table below for the details.

Mode Pin	Operating Mode	
	DCDC1 Buck (Dumping) only	DCDC2
Low (GND)	FCCM	FCCM
High (VREG)	SKIP	SKIP
Floating	Not Recommended	

Mode pin will select FCCM operation if left floating but is not recommended as noise may couple to this pin and cause improper mode selection.
The MODE pin input voltage (V_{MDL}, V_{MDH}) should satisfy the conditions as defined in the electrical characteristics.

(3) SUPSEL

SUPSEL Pin controls DCDC1 internal operation.

SUPSEL Pin	DCDC1 Operation
Low (GND)	5V System
High (VREG)	12V System
Floating	Not Recommended

SUPSEL pin will select 5V system operation if left floating but is not recommended as noise may couple to this pin and cause improper selection.
The SUPSEL pin input voltage ($V_{SUPSELL}$, $V_{SUPSELH}$) should satisfy the conditions as defined in the electrical characteristics.

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OPERATION (Continued)

9. Power ON / OFF Sequence

(1) When V_{IN} power up, CSTG will charge up to level one V_{BE} level below VIN voltage
(2) When the EN1 or EN2 pin is set to High after the V_{IN} settles, the BGR and the VREG start up.
(3) When the VREG pin exceeds its threshold value, the UVLO is released and the internal Soft-Start sequence is enabled.
(4) The CSTG pin (DCDC Output) voltage increases at the same rate as SS1 pin while the V_{OUT2} pin voltage increases at the same rate as the internal soft start SS2. Normal operation begins after the CSTG or V_{OUT2} pin reaches the set voltage.
(5) When both the EN pin are set to Low, the BGR, VREG and UVLO stop operation. The VOUT voltage starts to drop and the discharge time depends on the value of the feedback resistors, the output load current & output capacitors.

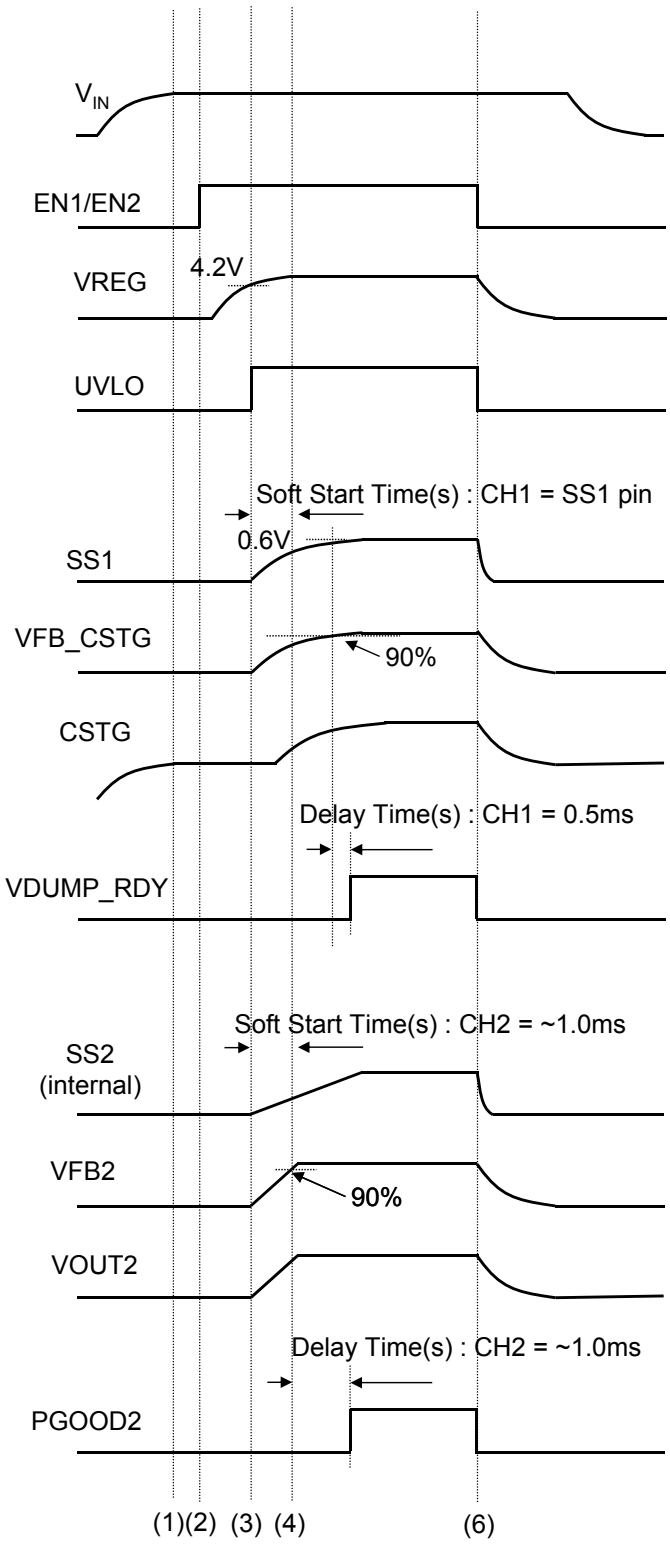

Figure 9A : Power ON/OFF sequence

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OPERATION (Continued)

10. Inductor and Output Capacitor Setting

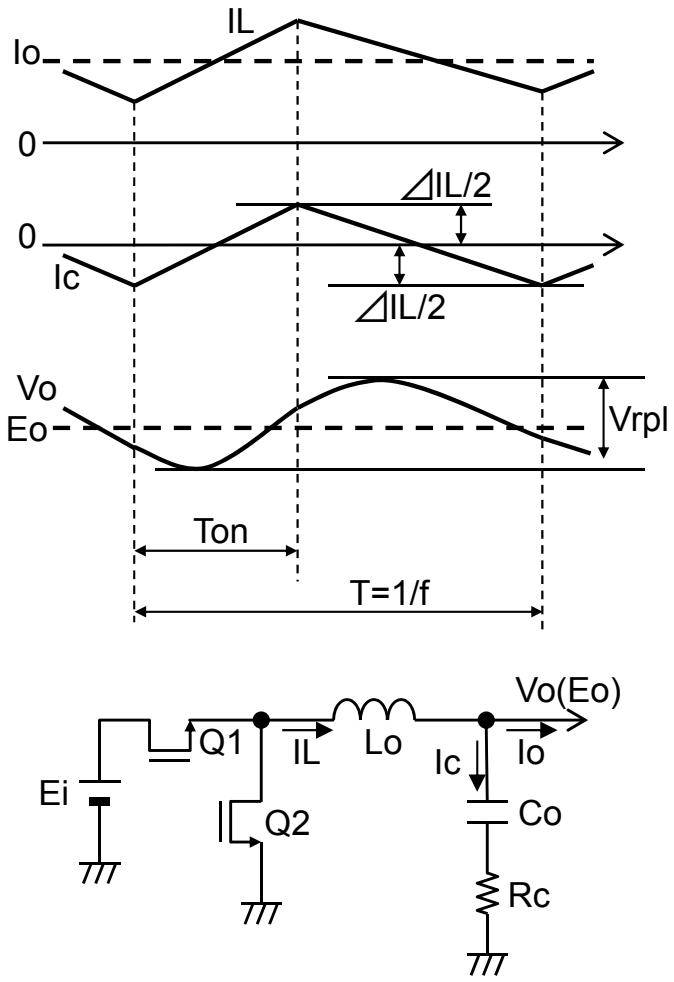

Figure 10A : Output ripple for output inductor and capacitor

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current.

$$\Delta IL = \frac{Eo \cdot (Ei - Eo)}{Ei \cdot Lo \cdot f}$$

$$Iox = \frac{\Delta IL}{2}$$

Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade off among component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 40% of IOUT(MAX). The largest ripple current occurs at the highest VIN. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$Lo \geq \frac{Eo \cdot (Ei - Eo)}{2Ei \cdot Iox \cdot f} \quad @\,\mathrm{Ei} = \mathrm{Ei\_max}$$

And its maximum current rating is

$$IL\_\max = \mathrm{Io\_max} + \frac{\Delta IL}{2} \quad (@\,\mathrm{Ei} = \mathrm{Ei\_max})$$

The selection of COUT is primarily determined by the ESR (Rc) required to minimize voltage ripple and load transients. The output ripple Vrpl is approximately bounded by:

$$Vrpl = Vop - Vob = Ei \cdot \frac{Co \cdot Rc^2}{2Lo} + \frac{\Delta IL}{8Co \cdot f}$$

$$= Ei \cdot \frac{Co \cdot Rc^2}{2Lo} + \frac{Eo \cdot (Ei - Eo)}{8Ei \cdot Lo \cdot Co \cdot f^2}$$

From the above equation, to achieve desired output ripple, low ESR ceramic capacitors are recommended, and its required RMS current rating is:

$$Ic(\mathrm{rms})\_\max = \frac{\Delta IL}{2\sqrt{3}} \quad (@\,\mathrm{Ei} = \mathrm{Ei\_max})$$

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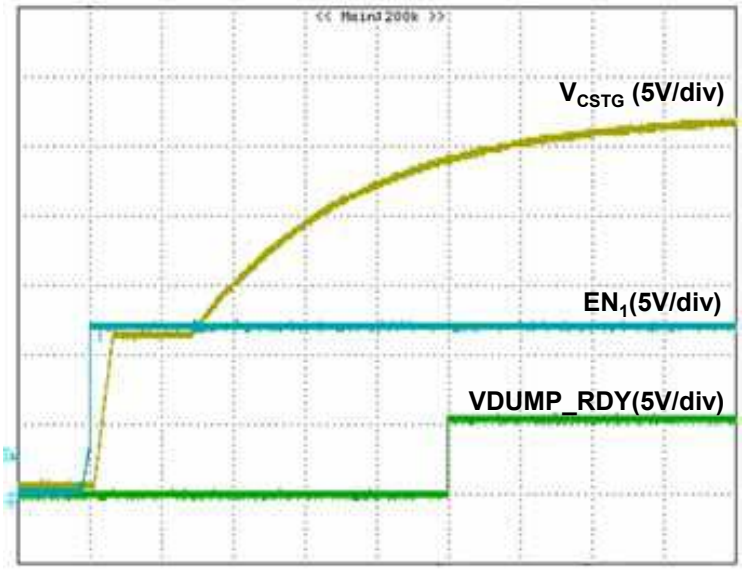
TYPICAL CHARACTERISTICS CURVES

1. CH1 Startup Boost Mode Operation

Condition : V_{IN} = 12V, V_{CSTG} = 28V, L_{OUT1} = 3.3µH, C_{OUT1} = 88µF (22µF x 4), C_{CSTG} = 720µF (120µF x 6), C_{SS1} = 0.1µF

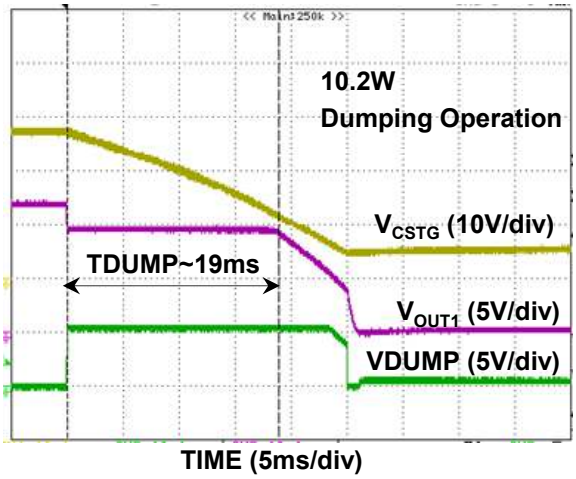
Characteristic 1-1



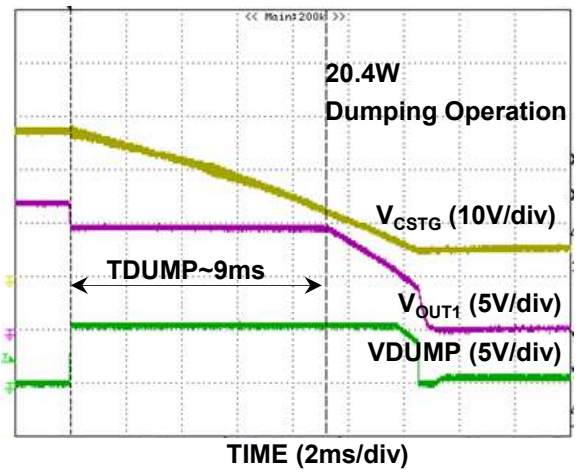
2. CH1 Dumping Buck Mode Operation

Condition : V_{IN} = 12V, V_{CSTG} = 28V, L_{OUT1} = 3.3µH, C_{OUT1} = 88µF (22µF x 4), C_{CSTG} = 720µF (120µF x 6), C_{SS1} = 0.1µF, V_{OUT1} = 10.2V

Characteristic 2-1



Characteristic 2-2



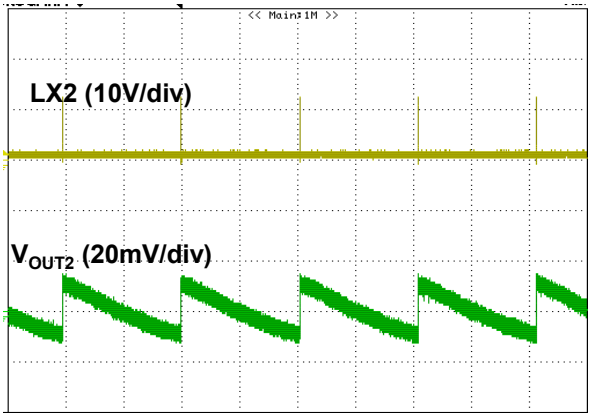
TYPICAL CHARACTERISTICS CURVES (Continued)

3. CH2 Buck Converter: Output Ripple Voltage

Condition : V_{IN} = 12V, V_{OUT2} = 1.1V, L_{OUT2} = 1µH, C_{OUT2} = 88µF (22µF x 4)

Characteristic 3-1

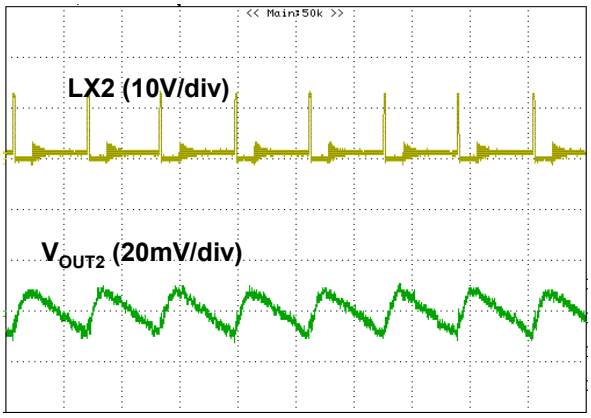
I_{OUT2} = 0A



TIME (10ms/div)

Characteristic 3-2

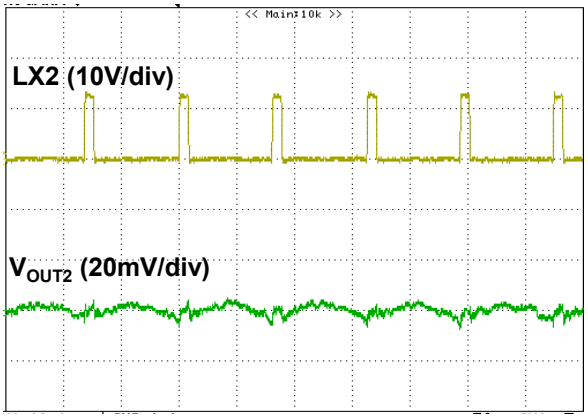
I_{OUT2} = 0.2A



TIME (5us/div)

Characteristic 3-3

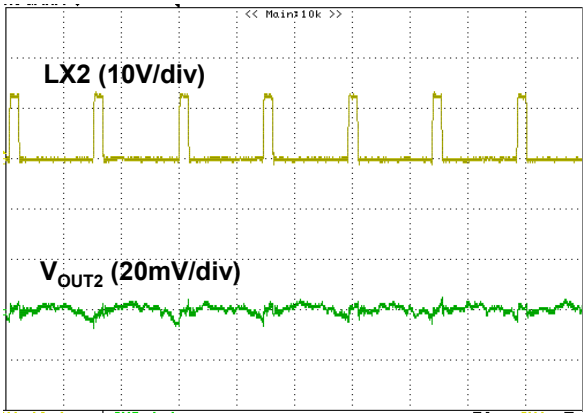
I_{OUT2} = 3A



TIME (1us/div)

Characteristic 3-4

I_{OUT2} = 6A



TIME (1us/div)

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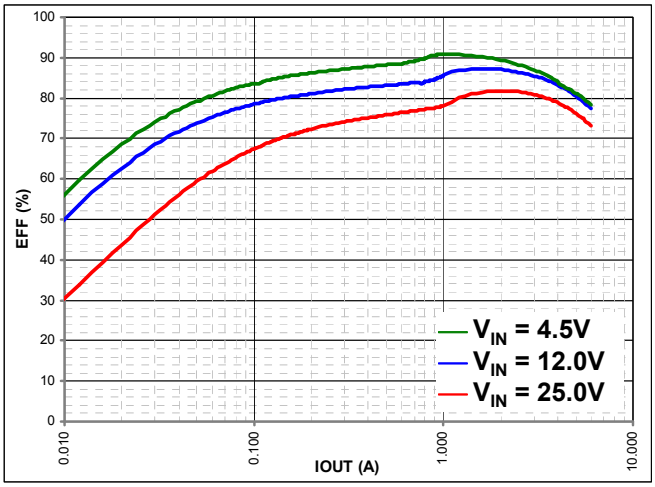
TYPICAL CHARACTERISTICS CURVES (Continued)

4. CH2 Buck Converter: Efficiency

Condition : L_{OUT2} = 1µH / 2.2µH / 3.3µH, C_{OUT2} = 88µF (22µF x 4)

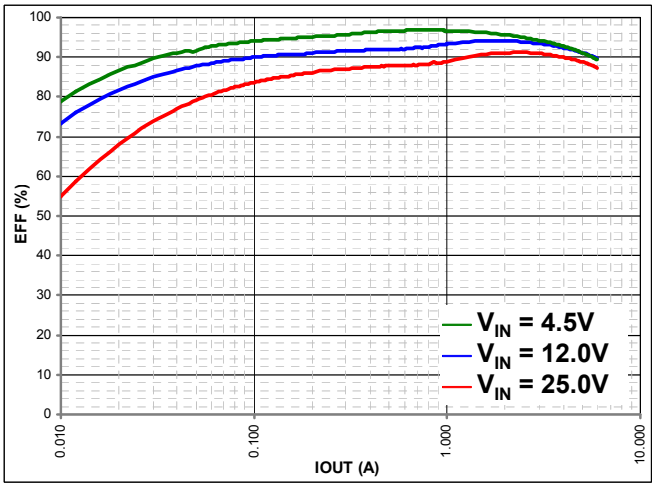
Characteristic 4-1

V_{OUT2} = 1.1V, L_{OUT2}=1µH



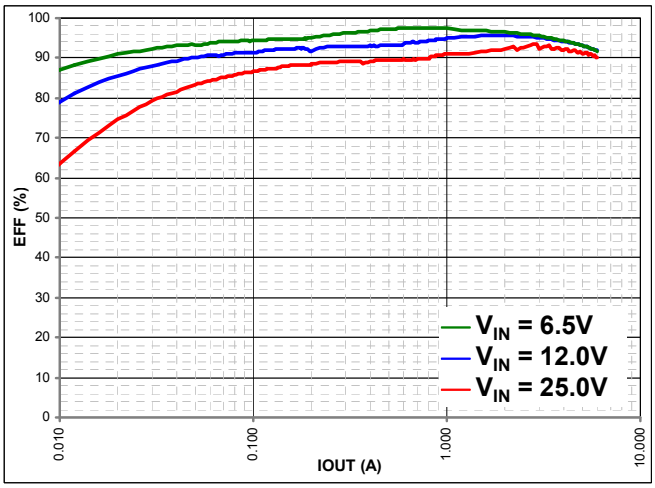
Characteristic 4-2

V_{OUT2} = 3.3V, L_{OUT2}=2.2µH



Characteristic 4-3

V_{OUT2} = 5.0V, L_{OUT2}=3.3µH

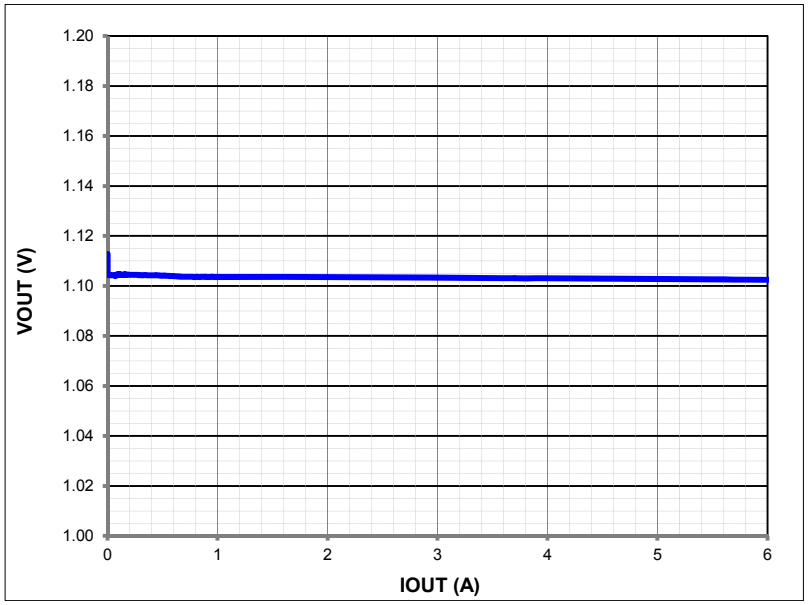


TYPICAL CHARACTERISTICS CURVES (Continued)

5. CH2 Buck Converter: Load Regulation

Condition : V_{IN} = 12V, C_{OUT2} = 88µF (22µF x 4), L_{OUT2} = 1µH, V_{OUT2} = 1.1V

Characteristic 5-1

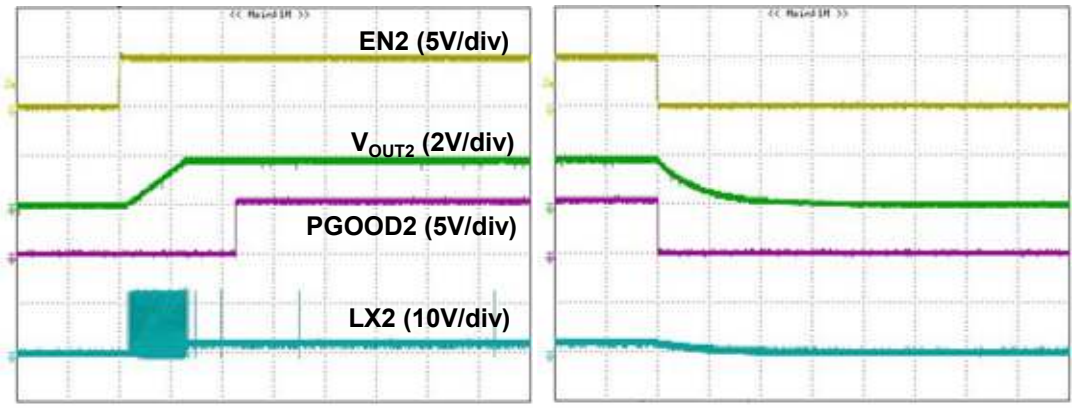


6. Start / Shut Down

Condition : V_{IN} = 12V, V_{OUT2} = 1.8V, L_{OUT2} = 2.2µH, C_{OUT2} = 88µF (22µF x 4)

Characteristic 6-1 **Characteristic 6-2**

Enable V_{OUT2} only



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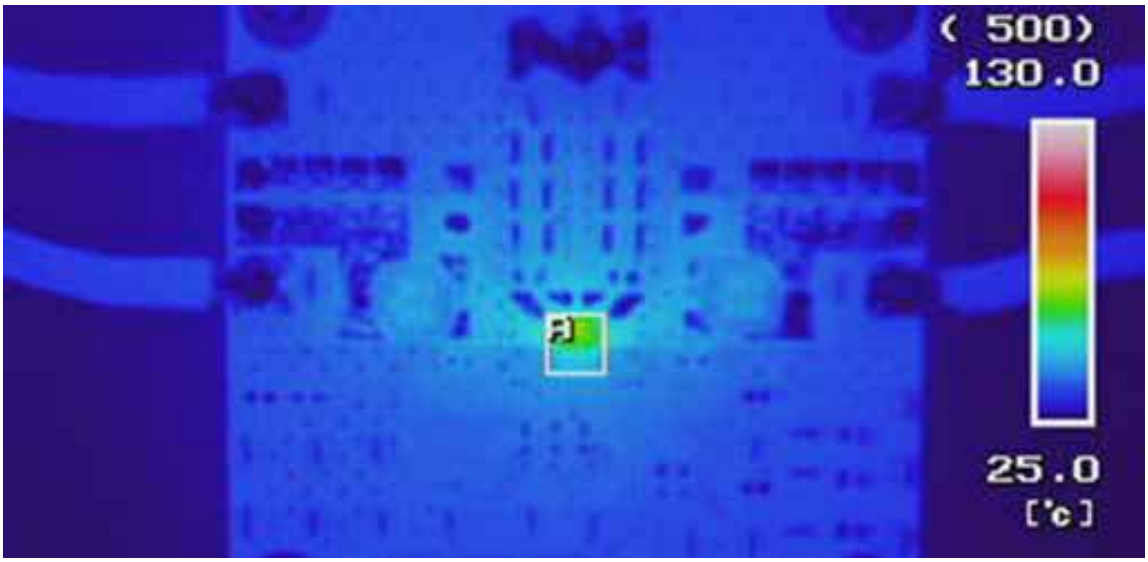
TYPICAL CHARACTERISTICS CURVES (Continued)

7. Thermal Performance and Safe Operation Area

Condition : V_{CSTG} = PV_{IN2} = 12V, V_{OUT1} = V_{OUT2} = 5V, I_{OUT1} = I_{OUT2} = 4A, L_{OUT1} = L_{OUT2} = 3.3µH,
C_{OUT1} = C_{OUT2} = 88µF (22µF x 4)
(CH1 is fix at Dumping mode with V_{CSTG} = 12V for illustration purpose only)



IC case temperature is about 70°C

Figure 7-1 : Thermal image

This IC is intended to be used for general electronic equipment. Ensure that the IC is used within the recommended safe operating region illustrated by the reference graph on the right. Do take note that thermal performance may varies with PCB design and PCB materials.

Please use the graph only as a reference for your design and discuss further with our application engineer.

It is to be understood that our company shall not be held responsible for any damage incurred as a result of application beyond the recommended safe operating region.

Recommended Safe Operation Area for VOUT from 1V to 5V with the condition of casing surface temperature below 85°C.

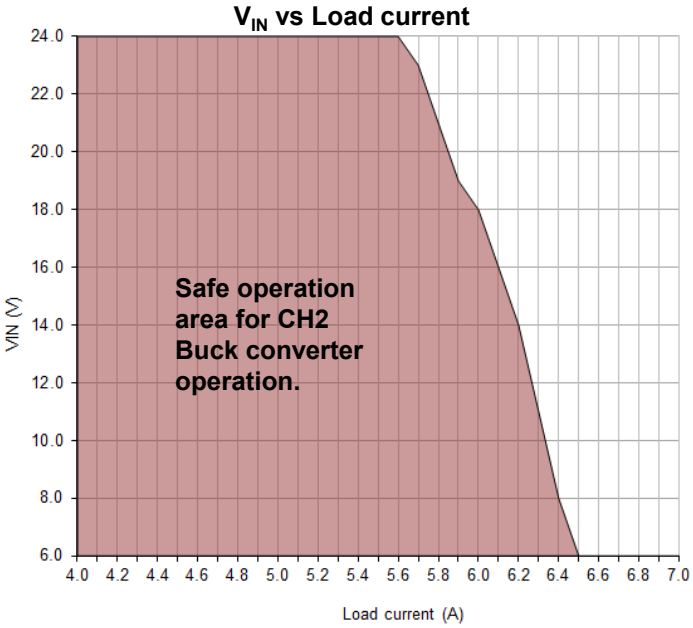


Figure 7-2 : Reference Safe Operation Area

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APPLICATIONS INFORMATION

1. Evaluation Board Information

Condition : V_{IN} = 12V, V_{CSTG} = 28V, V_{OUT1} = 4.5V, V_{OUT2} = 1.1V, L_{OUT1} = 3.3µH, L_{OUT2} = 1µH, C_{OUT} = 88µF (22µF x 4)

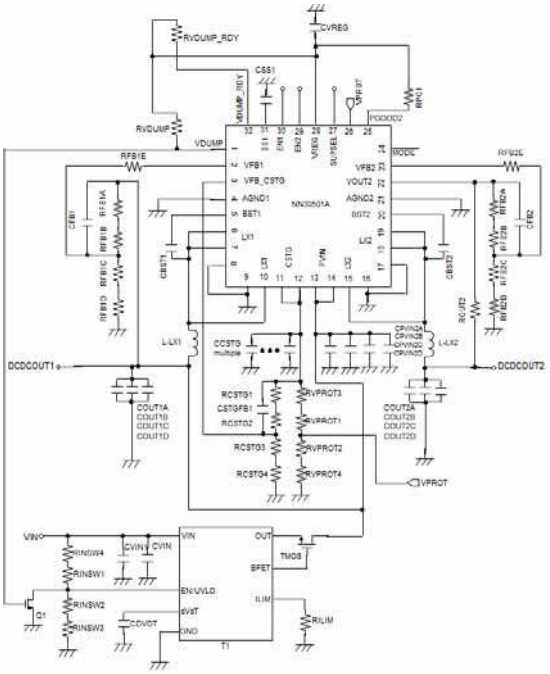

Figure A1-1 : Application circuit

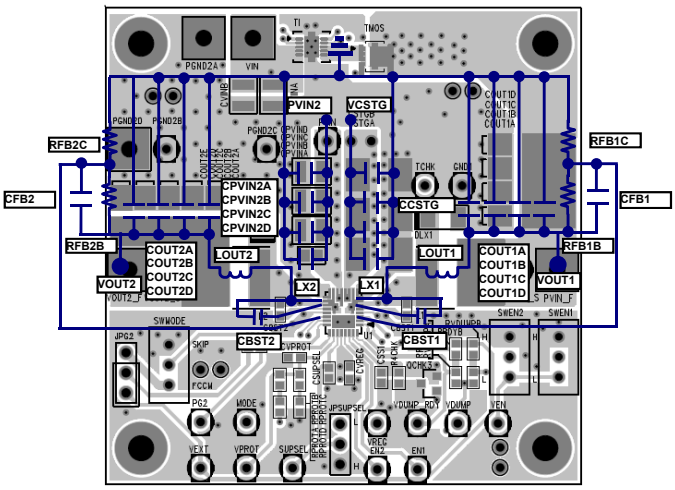

Figure A1-2 : Layout

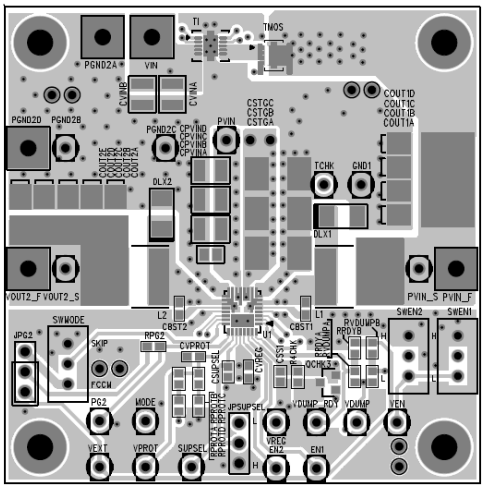

Figure A1-2 Top Layer with silk screen
(Top View)

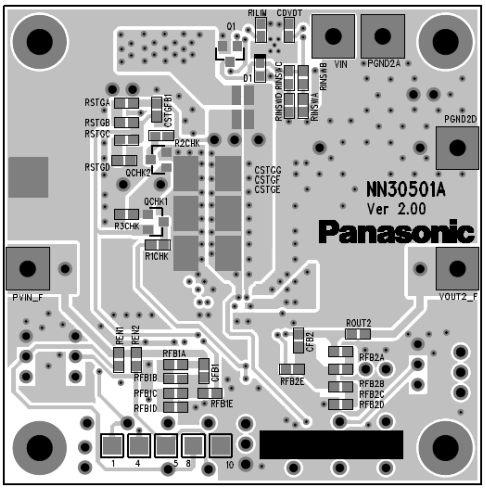

Figure A1-3. Bottom Layer with silk screen
(Bottom View)

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APPLICATIONS INFORMATION (Continued)

2. Layout Recommendations

Board layout considerations are necessary for stable operation of the DC-DC regulator. The following precautions must be used when designing the board layout.

(a) The Storage Capacitor C_{CSTG} of CH1 and Input capacitor C_{IN} of CH2 must be placed in such a way that the distance between CSTG and PGND1 of CH1 as well as PVIN and PGND2 of CH2 is minimum, in order to suppress the switching noise. Stray inductance and impedance should be reduced as indicated by loop (1) shown in the figure A2-1.

(b) A single point ground connection (2) must be used to connect PGND and AGND to improve operation stability.

(c) CH2 Output current line I_{OUT} and the output sense line VOUT2 must have small common impedance to reduce output load variations. Output sense line VOUT2 must be close to the output capacitor C_{OUT2} as indicated by (3) below.

(d) Power Loss and output ripple voltage can be reduced by placing the inductor L_{OUT} and output capacitor C_{OUT} such that the stray inductance and the impedance of loop (4) is minimum.
This is realized by :
i) Minimizing distance between inductor L_{OUT} and LX pin.
ii) Reducing distance for output capacitor Cout between single ground point connection (2) and output connection (3) as shown in Figure A2-1.

(e) Thick lines in the application circuit example represent lines with large current flow. These lines should be designed as thick as possible.

(f) VFB / VREG lines should be placed far away from LX line, BST line and inductor L_{OUT} to reduce the effects of switching noise. These lines should be designed as short as possible. This is especially true for the VFB line, which is a high impedance line.

(g) R_{FB1} / R_{FB2} and R_{STGFB1} / R_{STGFB2} should also be placed as far away as possible from LX line, BST line and inductor L_{OUT} to minimize the effects of switching noise. R_{FB1} / R_{FB2} and R_{STGFB1} / R_{STGFB2} should be placed close to the VFB pin.

(h) LX / BST lines are noisy lines. They should be designed as short as possible.

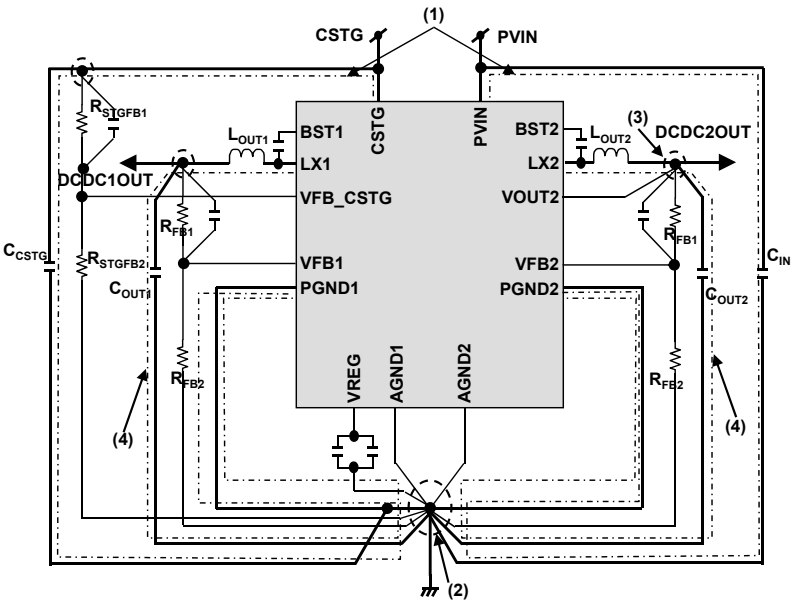

Figure A2-1 : Application circuit diagram

Note: The application circuit diagram and layout diagram explained in this section, should be used as reference examples. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit and the information attached with it, in the design of the equipment.

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APPLICATIONS INFORMATION (Continued)

3. Recommended component

Reference Designator	QTY	Value	Manufacturer	Part Number	Note
CVREG	1	2.2uF	MURATA	GRM188R71A225KE15D	–
CBST1-2 CSS1 CPVIN2A	3	0.1uF	MURATA	GRM188R72A104KA35L	–
CPVIN2B CPVIN2C CPVIN2D	4	10uF	Taiyo Yuden	UMK325AB7106MM-T	–
COUT1A -1D COUT2A -2D	8	22uF	MURATA	GRM32ER71E226KE15	–
LOUT1	1	3.3uH	Panasonic	ETQP3W3R3WFN	–
LOUT2	1	1.0uH	Panasonic	ETQP3W1R0WFN	For DCDC2 if VOUT = 1.1V
RPROT2	1	R = 10K	Panasonic	ERJ3EKF1002V	–
RPG2 RILIM RINSW1-2 RVDUMP RVDUMP_RDY	6	R = 100K	Panasonic	ERJ3EKF1003V	–
RCSTG1	1	R = 0	Panasonic	ERJ3GEY0R00V	For DCDC1 Boost (charging) VCSTG=27.8V
RCSTG2	1	R = 150K	Panasonic	ERJ3EKF1203V	
RCSTG3	1	R = 0	Panasonic	ERJ3GEY0R00V	
RCSTG4	1	R = 3.3K	Panasonic	ERJ3EKF2701V	
RFB1A	1	R = 0	Panasonic	ERJ3GEY0R00V	For DCDC1 Buck (dumping) VOUT1=4.5V
RFB1B	1	R = 13K	Panasonic	ERJ3EKF1302V	
RFB1C	1	R = 2K	Panasonic	ERJ3EKF2001V	
RFB1D	1	R = 0	Panasonic	ERJ3GEY0R00V	
RFB1E	1	R = 0	Panasonic	ERJ3GEY0R00V	–

APPLICATIONS INFORMATION (Continued)

3. Recommended component (Continued)

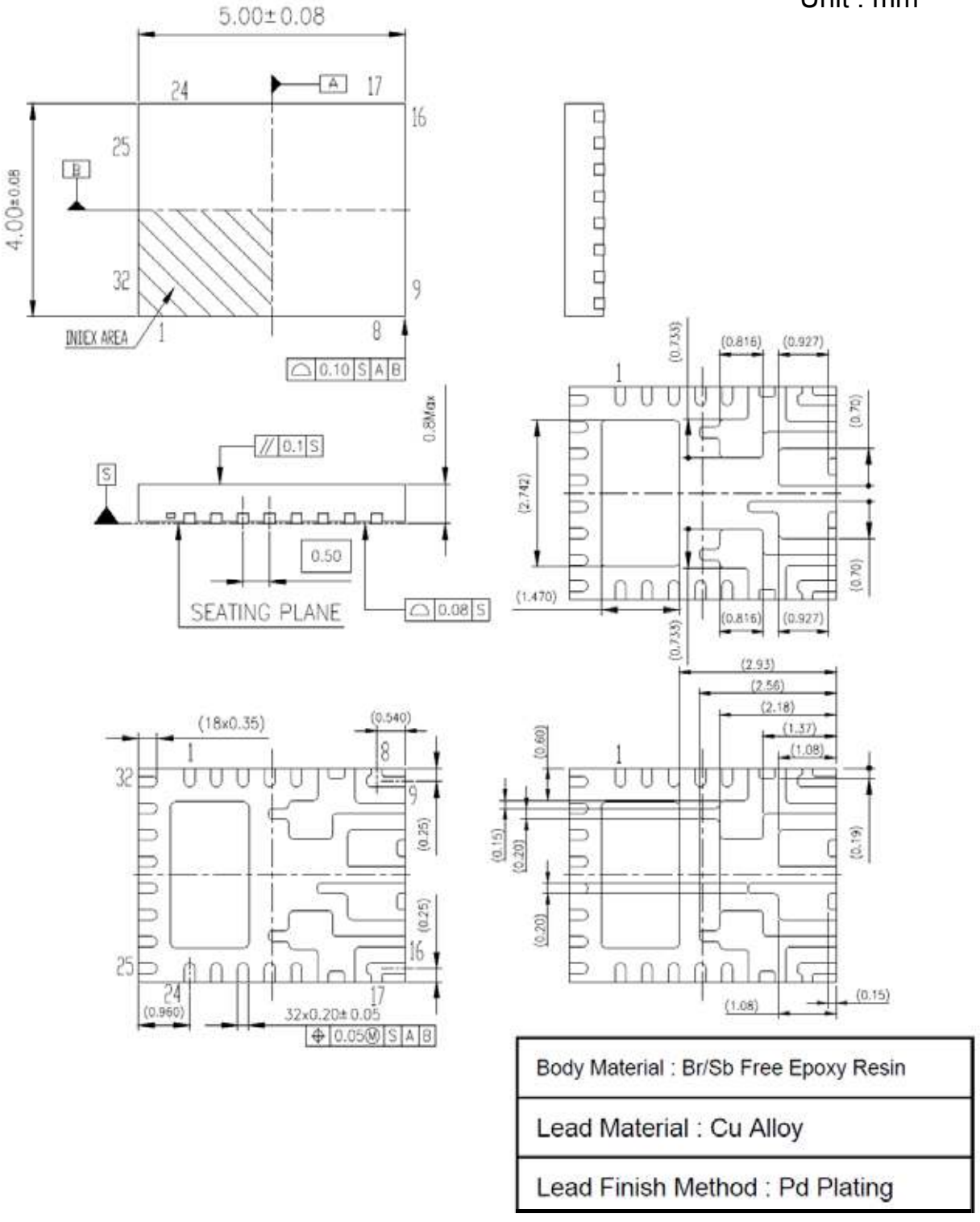
Reference Designator	QTY	Value	Manufacturer	Part Number	Note
RFB1E	1	R = 0	Panasonic	ERJ3GEY0R00V	–
RFB2A	1	R = 0K	Panasonic	ERJ3EKF7502V	For DCDC2 VOUT2=1.1V
RFB2B	1	R = 15K	Panasonic	ERJ3EKF3002V	
RFB2C	1	R = 18K	Panasonic	ERJ3EKF3602V	
RFB2D	1	R = 0	Panasonic	ERJ3GEY0R00V	
RFB2E	1	R = 0	Panasonic	ERJ3GEY0R00V	–
RPROT1	1	R = 240K	Panasonic	ERJ3EKF2403V	For DCDC1 Boost (charging) OVP Protection VOVP = 29V
RPROT2	1	R = 10K	Panasonic	ERJ3EKF1002V	
RPROT3	1	R = 0	Panasonic	ERJ3GEY0R00V	
RPROT4	1	R = 0	Panasonic	ERJ3GEY0R00V	
RINSW3-4 ROUT2	3	R = 0	Panasonic	ERJ3GEY0R00V	–
TMOS	1		Panasonic	SK830321KL	–
T1	1		Texas Instruments	TPS2592AA	–
Q1	1		FAIRCHILD	FDV301N	–
CFB1 CSTGFB1	2	1nF	MURATA		–
CDVDT	1	4.7nF	MURATA		–
CCSTG	NA	NA	Panasonic	20TQC100MYF	Low Profile POSCAP Value and Quantity depend on application requirement
CCSTG	NA	NA	Panasonic	35SVPF120M	OS-CON CAP Value and Quantity depend on application requirement

PACKAGE INFORMATION

Outline Drawing

Package Code : HQFN032-A5-0405XZF

Unit : mm



Body Material : Br/Sb Free Epoxy Resin
Lead Material : Cu Alloy
Lead Finish Method : Pd Plating

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IMPORTANT NOTICE

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
   However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the IC might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
11. Product which has specified ASO (Area of Safe Operation) should be operated in ASO
12. Verify the risks which might be caused by the malfunctions of external components.
13. Connect the metallic plate (fin) on the back side of the IC to the respective potentials (AGND, PVIN, LX). The thermal resistance and electrical characteristics are guaranteed only when the metallic plate (fin) are connected with their respective potentials.