ADV739x Evaluation Board Documentation

ADV7390, ADV7391, ADV7392, ADV7393 Video Encoder Evaluation Boards

Featuring EVAL-ADV739xFEZ Front-end board

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Document Revision history

Rev B.

- Foot note EVAL-ADV739x updated
- ADV7393 schematic corrected. Rev A had incorrect RSET and External loop filter components shown.

MicroBlaze is a Xilinx trademark.

Introduction

The purpose of this document is to assist the user in getting the ADV739x Evaluation system up and running as quickly as possible. For information on using the Register Control software, please refer to the software guide that will appear when the application is selected from the Start Menu.
For information on the installation of the CD, please refer the installation guide on the root directory on the enclosed CD.
Evaluation board Schematics and PCB drawings can also be found at the end of this document.

The ADV739x family of video encoders consists of the parts in Table 1.

Table 1: Encoder Back End Boards

Part	Package	Macrovision support	Eval board
ADV7390	32 pin LFCSP	Yes	Eval-ADV7390EBZ
ADV7391	32 pin LFCSP	No	Eval-ADV7391EBZ
ADV7392	40 pin LFCSP	Yes	Eval-ADV7392EBZ
ADV7393	40 pin LFCSP	No	Eval-ADV7393EBZ

Table 2: ADV739x Front End Board

Part	Eval board
Front end data board	Eval-ADV739xFEBZ

The Evaluation platform consists of a front-end board and a choice of 4 back-end boards. The front end board features an Analog Devices 10-bit multi-format decoder and Xilinx Spartan 3 FPGA which offers unprecedented flexibility in an encoder evaluation platform.

There are four possible back end solutions as per Table 1. All can be used interchangeably.

An expansion port is also provided to allow user-specific data sources to interface to the back end encoder.

Note: All ADV739x Evaluation boards are Pb(Lead) free.

ADV739xFEz Front End Board

Figure 1 shows the EVAL-ADV739xFEZ Eval board. The ADV739xFEZ board allows the user to supply data from various sources. The ADV7403 video decoder allows the user to supply analog video signals from various sources such as a signal generator, DVD player, tuner and so on.

A Xilinx Spartan 3 FPGA is also included on the front end board. The purpose of the FPGA is:

- To route various data formats from the ADV7403 video decoder to the input of the ADV739x boards that can plug in to the back end. The following formats are supported by the ADV7403 + ADV739x :
    - SD (CVBS, S-video, Component YPrPb)
    - ED (525p/625p) (SDR & DDR interface)
    - HD (1080i/720p)) (SDR & DDR interface)
- To direct custom data from the expansion port to the back-end encoder. This can be done SDR or DDR. Refer to the FPGA Register Map section for this operation (Page 14).

The FPGA can serve as a test pattern generator, which will be implemented in the next revision of the firmware.

The FPGA has the potential to operate in a "Driver" mode. The Xilinx soft microprocessor, MicroBlaze™ can be implemented in the FPGA to monitor the Status registers of the ADV7403 and, therefore, the input video format of the ADV7403. The processor can then write appropriate I2C writes to configure the ADV739x encoder accordingly. This feature is not ready at the time of writing this documentation. Please contact your local ADI FAE for firmware updates on this feature.

All these features can be controlled via I2C as there is an I2C slave implemented on the FPGA (Address = 0x50).

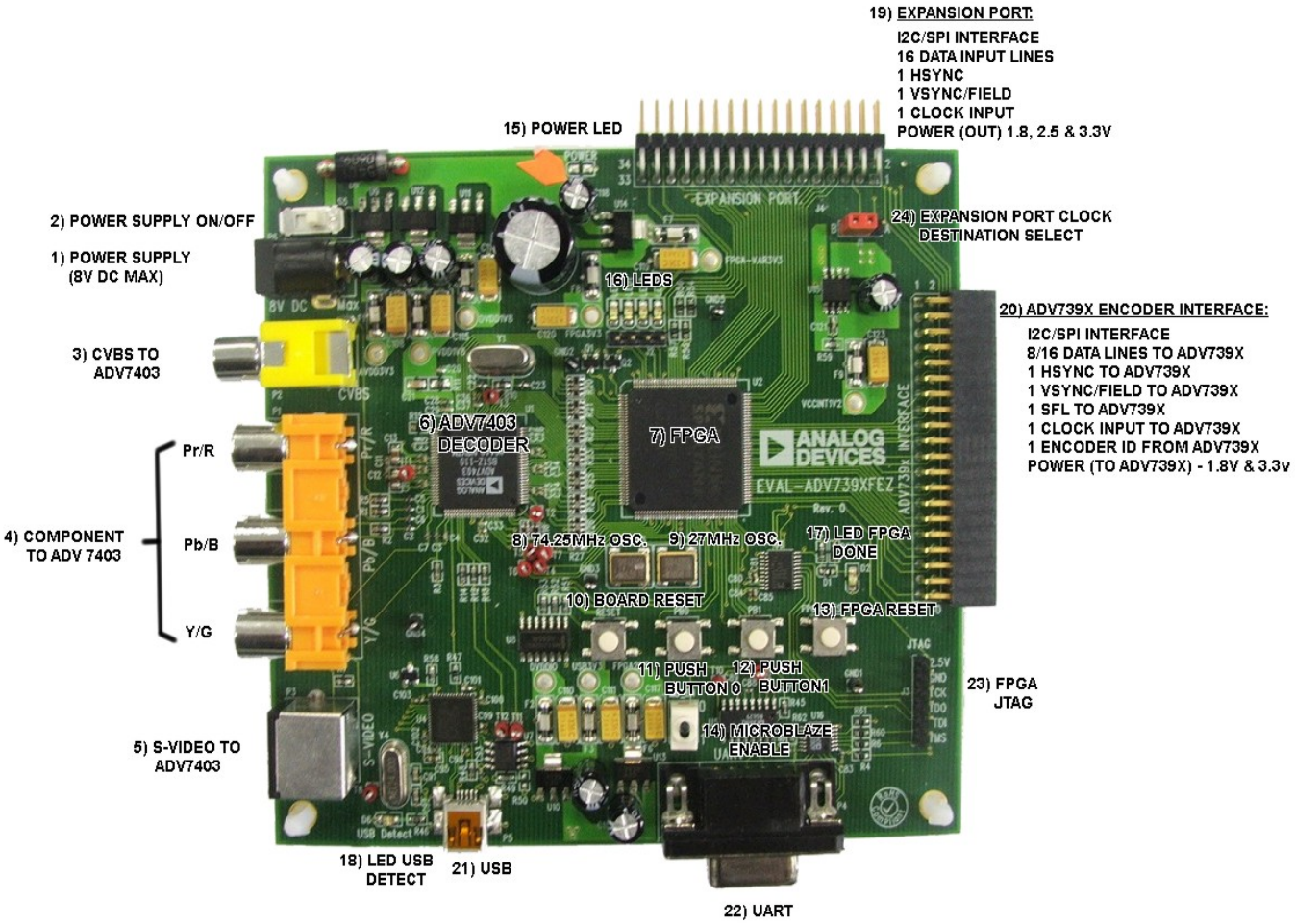


Figure 1: ADV739xFEz Eval Board

Figure 1 shows a picture of the Front end board. Figure 2 shows a block diagram version of the board.

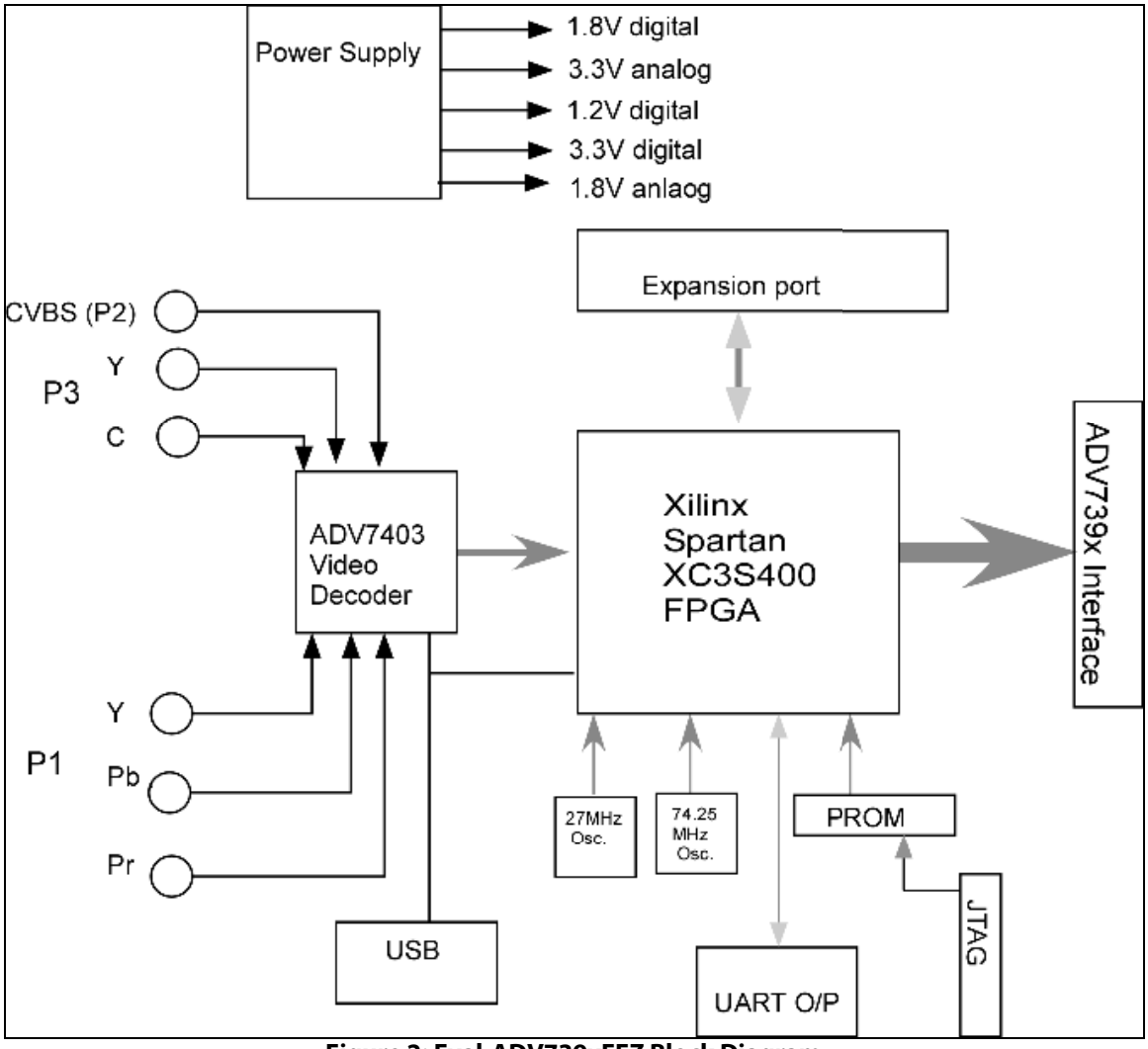


Figure 2: Eval-ADV739xFEZ Block Diagram

Expansion Port

J4 on the Eval board serves as an expansion port. This allows the user to interface an external data source to the encoder via the FPGA. All lines are registered twice through the FPGA, once at the input and again at the output. Refer to Table 5 to select the Expansion port routing. SDR and DDR data transfers are selectable.

Table 3 shows the routing from the expansion port J4 to the ADV739x interface port (J5).

Table 3: Expansion Port
See Figure 15: Data Interface Ports on page 31

J4	FPGA input pin	Function	Maps to	J5
J4-1	132	Vsync	→	J5-15
J4-2	131	Hsync	→	J5-14
J4-3	-	Gnd		J5-16
J4-4	53/125 via J1	Clock	→	J5-39
J4-5	-	Gnd	→	J5-20
J4-6	99	D0	→	J5-17
J4-7	100	D1	→	J5-18
J4-8	102	D2	→	J5-19
J4-9	-	Gnd		J5-24
J4-10	103	D3	→	J5-21
J4-11	104	D4	→	J5-22
J4-12	105	D5	→	J5-23
J4-13	-	Gnd		J5-28
J4-14	107	D6	→	J5-25
J4-15	108	D7	→	J5-26
J4-16	112	D8	→	J5-27
J4-17	113	D9	→	J5-29
J4-18	116	D10	→	J5-30
J4-19	118	D11	→	J5-31
J4-20	119	D12	→	J5-33
J4-21	-	Gnd		J5-32
J4-22	122	D13	→	J5-34
J4-23	123	D14	→	J5-35
J4-24	124	D15	→	J5-36
J4-25	-	EXP_SFL	→	J5-9
J4-26	-	EXP_ALSB	→	J5-10
J4-27	-	EXP_SDA	→	J5-11
J4-28	-	EXP_SCL	→	J5-12
J4-29	-	Gnd		J5-37
J4-30	-	3.3V		
J4-31	-	Gnd		J5-40
J4-32	-	2.5V		
J4-33	-	Gnd		J5-2,4,6,8
J4-34	-	1.8V		

Analog Inputs

The EVAL-ADV7393FEZ supports CVBS, S-video, Component YPrPb, and RGB formats via the input connectors noted in Table 4.

Table 4: ADV7403 Analog Inputs

Format	Input Connector
CVBS	P2
S-Video	P3
YPrPb	P1
Graphics RGB (SOG)	P1

Push Buttons

There are four push buttons on the EVAL-ADV739xFEZ labeled RESET, PB0, PB1, and FPGA RESET. The Reset button is a hardware reset to all devices on the board; the reset signal is also transferred over the J5 connector to the ADV739x encoder. The FPGA RESET button resets the FPGA and initiates the PROM to configure the FPGA. LED D2 illuminates when FPGA is configured.

PB0 and PB1 are general purpose push buttons connected to FPGA.

UART Port

The UART port (P4) provides a serial link to the FPGA.

General Serial Port Setup

Bits per second : 115200
DataBits : 8
Parity: None
Stop Bits: 1
Flow control : None.

PC Communication

Communication between the PC and Eval system is carried out via the mini USB connector (P5). The Cypress microcontroller converts between PC USB signaling and the Device I2C signaling. LED D6 illuminates when a USB cable is connected to P5. The ADI register control software should be used to control this Eval board via I2C.

Power Supply

The Eval kit contains a 7.5V DC power supply which should be applied to connector P6. This voltage is regulated to various voltages required by the various devices on the EVAL-ADV739xFEZ. The supplies available on the board are as follows:

Supply Voltages Available
1.2V
1.8V
3.3v

These voltage supplies are also required by back-end boards (EVAL-ADV7390/91/92/93EBz) and are, therefore, available on J5. These back-end boards do not have an independent power source and rely on the supplies coming across on J5.

JTAG Connector

The JTAG connector (J3) is located on the bottom right of the board. The function of this connector is to update the PROM device (U3) with new firmware for the FPGA (U2). It is not used for any boundary Scan type tests.

EVAL-ADV7390/ADV7391EBZ and EVAL-ADV7392/ADV7393EBZ

Figure 3 and Figure 4 show the plug-in modules available for the EVAL-ADV739xFEZ. EVAL-ADV7390/91EBZ demonstrates the 32 pin LFCSP package and the EVAL-ADV7392/93EBZ demonstrates the 40 pin LFCSP.

It should be noted that the PCB space required for the encoder and ancillary components are surrounded by a white border. This emphasizes the small form factor advantage of the ADV739x video encoder. The components inside the white border are as follows:

- ADV739x video encoder
- 510R RSET Resistor
- 2nF Comp capacitor
- Decoupling capacitors
- 75R Rload Resistors

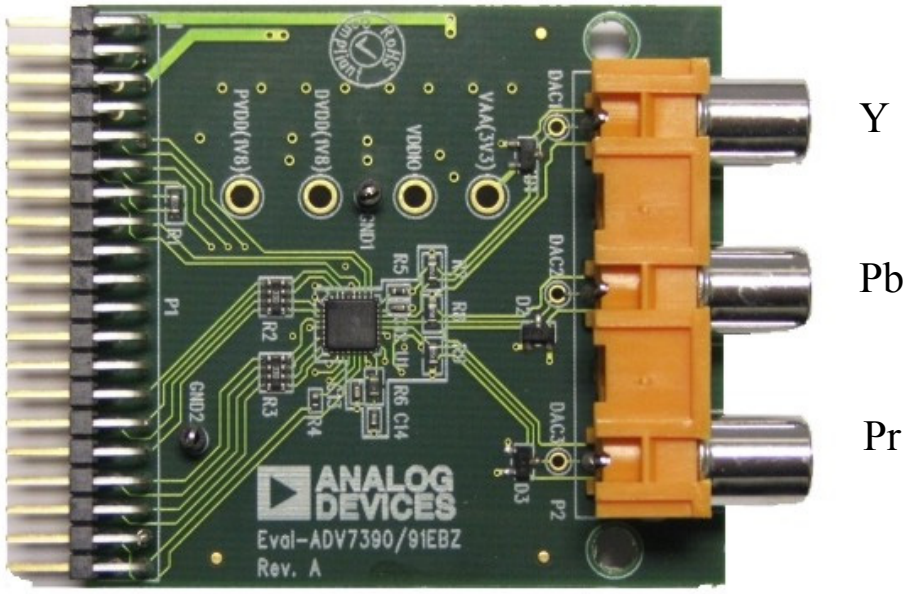


Figure 3: ADV7390/91EBZ Plug In Board

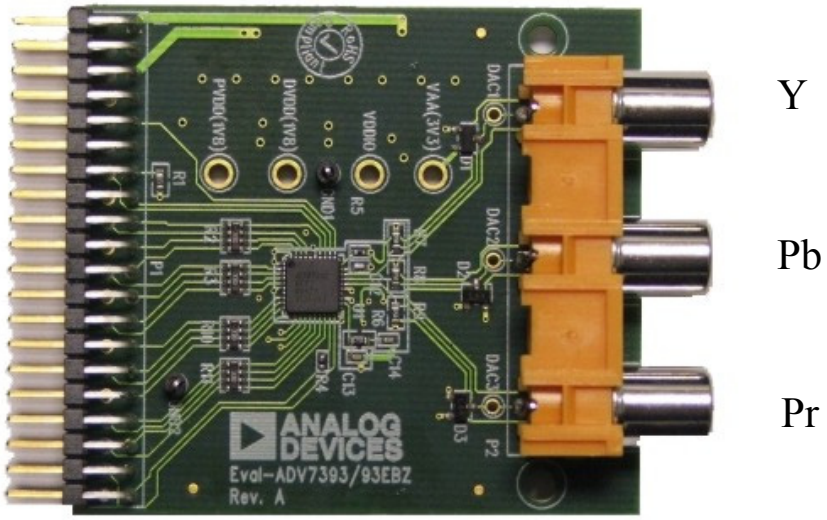


Figure 4: ADV7392/93EBZ Plug In Board

EVAL-ADV739xFEz + EVAL-ADV739xEBZ Operation

The operation of this Eval system can be controlled via the Register control software that is enclosed on the CD. To evaluate the ADV739x series of encoders, the following steps must be taken.

1. Install the Register control Software to a PC. Do not run application at this point.
2. Plug in EVAL-ADV7390*(/1/2/3)*EBZ back end board to the EVAL-ADV739xFEZ.
3. Plug in power supply and USB cable.
4. Plug in video cables (input and output)
5. Turn on Eval board; S5 to the right hand position.
6. Load the pre-installed Register Control software application.
7. Select device to evaluate
8. Select scripts from "Settings " Menu. (refer to Software guide for details)

FPGA Register Map

FPGA is I²C device address0x50

Table 5: Video Source Register

Register Address	Register	Bit Description	Bit Number								Register Setting	Reset Value
			7	6	5	4	3	2	1	0		
0x00	Video Source Select Register	Video Mux Select [4:0]	Muxing options for 32-pin devices:									0x00
						0	0	0	0	0	SD YCrCb from ADV7403 decoder to 32-pin devices (8-Bit Data)	
						0	0	0	0	1	ED/HD YCrCb (DDR) from ADV7403 decoder to 32-pin devices (8-Bit Data)	
						0	0	0	1	0	SD YCrCb from test pattern generator to 32-pin devices (8-Bit Data)	
						0	0	0	1	1	ED YCrCb (DDR) from test pattern generator to 32-pin devices (8-Bit Data)	
						0	0	1	0	0	HD YCrCb (DDR) from test pattern generator to 32-pin devices (8-Bit Data)	
						0	0	1	0	1	Expansion port to 32-pin devices (8-Bit Data)	
			Muxing options for 40-pin devices:									
						0	0	1	1	0	SD YCrCb from ADV7403 decoder (8-Bit Data)	
						0	0	1	1	1	SD YCrCb from ADV7403 decoder (10-Bit Data)	
						0	1	0	0	0	SD YCrCb from ADV7403 decoder (16-Bit Data)	
						0	1	0	0	1	SD RGB from ADV7403 decoder (16-Bit Data)	
						0	1	0	1	0	ED/HD YCrCb (DDR) from ADV7403 decoder (8-Bit Data)	
						0	1	0	1	1	ED/HD YCrCb (DDR) from ADV7403 decoder (10-Bit Data)	
						0	1	1	0	0	ED/HD YCrCb (SDR) from ADV7403 (16-Bit Data)	
						0	1	1	0	1	SD YCrCb from test pattern generator (8-Bit Data)	
						0	1	1	1	0	ED YCrCb (DDR) from test pattern generator (8-Bit Data)	
						0	1	1	1	1	HD YCrCb (DDR) from test pattern generator (8-Bit Data)	
						1	0	0	0	0	ED YCrCb (SDR) from test pattern	

Register Address	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
											generator (16-Bit Data)	
						1	0	0	0	1	HD YCrCb (SDR) from test pattern generator (16-Bit Data)	
						1	0	0	1	0	Expansion port (16-Bit Data)	
			Miscellaneous:									
						1	0	0	1	1	Debug Mode. Drive the encoder interface via I2C (16-Bit Data)	
						1	0	1	0	0	Not Used	
						1	0	1	0	1	Not Used	
						1	0	1	1	0	Not Used	
						1	1	0	0	0	Not Used	
						1	1	0	0	1	Not Used	
						1	1	0	1	0	Not Used	
						1	1	0	1	1	Not Used	
						1	1	1	0	0	Not Used	
						1	1	1	0	1	Not Used	
						1	1	1	1	0	Not Used	
						1	1	1	1	1	Not Used	
		Unused										
		ADV7403 Decoder VSYNC/Field Select		0							Pass ADV7403 VSYNC to Encoder	
				1							Pass field signal to Encoder	
		Test Pattern Generator VSYNC/Field Select	0								From Test Pattern Generator to Encoder..	
			1								..	

Table 6: Test Pattern Generator Mode Select Register 0x01

Register Address	Register	Bit Description	Bit Number								Register Setting	Reset Value
			7	6	5	4	3	2	1	0		
0x01	Test Pattern Generator Mode Select Register	Test Pattern Generator Pattern Select [3:0]					0	0	0	0	Black flat field	0x00
							0	0	0	1	Grey flat field	
							0	0	1	0	White flat field	
							0	0	1	1	Ramp	
							0	1	0	0	Color bars	
							0	1	0	1	Not Used	
							0	1	1	0	Not Used	
							0	1	1	1	Not Used	
							1	0	0	0	Not Used	
							1	0	0	1	Not Used	
							1	0	1	0	Not Used	
							1	0	1	1	Not Used	
							1	1	0	0	Not Used	
							1	1	0	1	Not Used	
							1	1	1	0	Not Used	
							1	1	1	1	Not Used	
		Test Pattern Generator Standard Select [7:4]	0	0	0	0					SD NTSC	
			0	0	0	1					SD PAL	
			0	0	1	0					ED 525p	
			0	0	1	1					ED 625p	
			0	1	0	0					HD 720p	
			0	1	0	1					HD 1080i	
			0	1	1	0					Not Used	
			0	1	1	1					Not Used	
			1	0	0	0					Not Used	
			1	0	0	1					Not Used	
			1	0	1	0					Not Used	
			1	0	1	1					Not Used	
			1	1	0	0					Not Used	
			1	1	0	1					Not Used	
			1	1	1	0					Not Used	
			1	1	1	1					Not Used	

Table 7: Clock Control Register 0x10

Register Address	Register	Bit Description	Bit Number								Register Setting	Reset Value
			7	6	5	4	3	2	1	0		
0x10	Clock Control Register	External Clock DCM Source Select								0	Clock from ADV7403 Decoder	0x00
										1	Clock form Expansion Port	
		Oscillator DCM Source Select							0		HD 74.25 MHz Oscillator	
									1		SD 27 MHz Oscillator	
		Clock Out to Encoder Source Select						0			Clock from ADV7403/Expansion Port	
								1			Clock from HD/SD Oscillator	
		Data Clock Source Select					0				Clock from ADV7403/Expansion Port	
							1				Clock from HD/SD Oscillator	
		I2C Clock Control Enable				0					I2C Clock is configured automatically	
						1					I2C Clock is configured manually	
		SDR/DDR Select			0						Single data rate (I2C DDR Control Enable bit has to be set to 1)	
					1						Double data rate (I2C DDR Control Enable bit has to be set to 1)	
		I2C DDR Control Enable		0							Data rate is configured automatically	
				1							Data rate is configured manually	
		Unused										

Table 8: DCM Control Register

Register Address	Register	Bit Description	Bit Number								Register Setting	Reset Value
			7	6	5	4	3	2	1	0		
0x11	DCM Control Register	External Clock DCM Reset								0	External Clock DCM in Normal state	0x03
										1	External Clock DCM in Reset State	
		Oscillator DCM Reset							0		Oscillator DCM in Normal state	
									1		Oscillator DCM in Reset State	
		Unused										
		Unused										
		Unused										
		Unused										
		Unused										
		Unused										

Table 9: DCM Status Register 0x12

Register Address	Register	Bit Description	Bit Number								Register Setting	Reset Value
			7	6	5	4	3	2	1	0		
0x12	DCM Status Register	External Clock DCM Locked								0	External Clock DCM unlocked	0x00
										1	External Clock DCM locked	
		Oscillator DCM Locked							0		Oscillator DCM unlocked	
									1		Oscillator DCM locked	
		Unused										
		Unused										
		Unused										
		Unused										
		Unused										
		Unused										

Table 10: Debug Register 0

Register Address	Register	Bit Description	Bit Number								Register Setting	Reset Value
			7	6	5	4	3	2	1	0		
0xF0	Debug Register 0	Encoder Interface Positive Edge Data 7 – Data 0 [7:0]										0x00

Table 11: Debug Register 1

Register Address	Register	Bit Description	Bit Number								Register Setting	Reset Value
			7	6	5	4	3	2	1	0		
0xF1	Debug Register 1	Encoder Interface Positive Edge Data 15 – Data 8 [7:0]										0xB1

Table 12: Debug Register 2

Register Address	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0xF2	Debug Register 2	Encoder Interface Negative Edge Data 7 – Data 0 [7:0]										0x00

Table 13: Debug Register 3

Register Address	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0xF3	Debug Register 3	Encoder Interface Negative Edge Data 15 – Data 8 [7:0]										0x00

Table 14: Debug Register 4

Register Address	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0xF4	Debug Register 4	Encoder Interface HSYNC Out										0x00
		Encoder Interface VSYNC/FIELD Out										
		Encoder Interface SFL Out										
		Unused										
		Unused										
		Unused										
		Unused										
		Unused										

Table 15: FPGA Firmware Revision Register

Register Address	Register	Bit Description	Bit Number								Register Setting	Reset Value
			7	6	5	4	3	2	1	0		
0xFF	FPGA Firmware Revision Register	FPGA Firmware Revision [7:0]										0xB1

Eval Board Schematics and Layout

EVAL-ADV739xFEz Front End Board Files

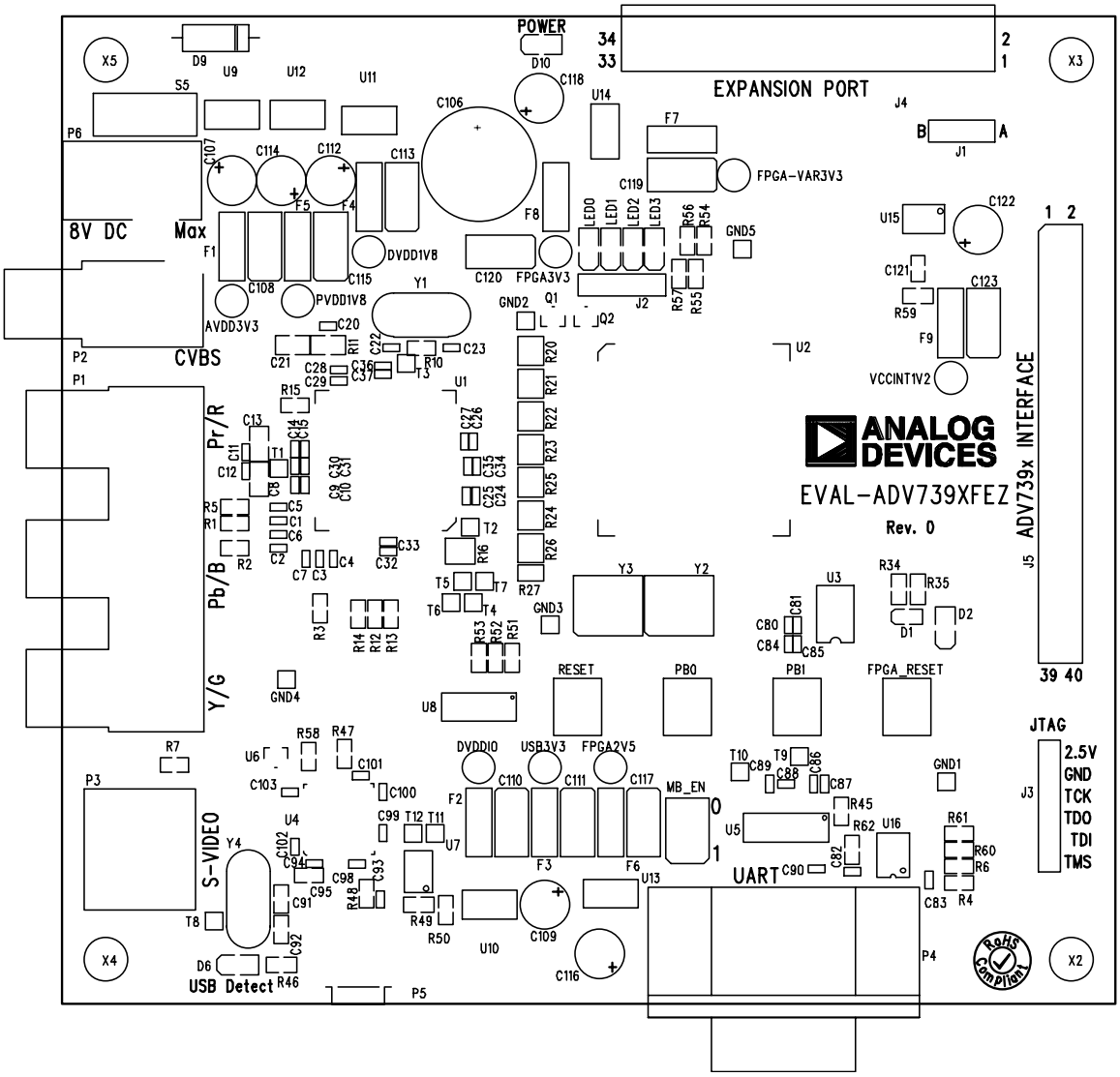


Figure 5: EVAL-ADV739xFEZ Silkscreen Top

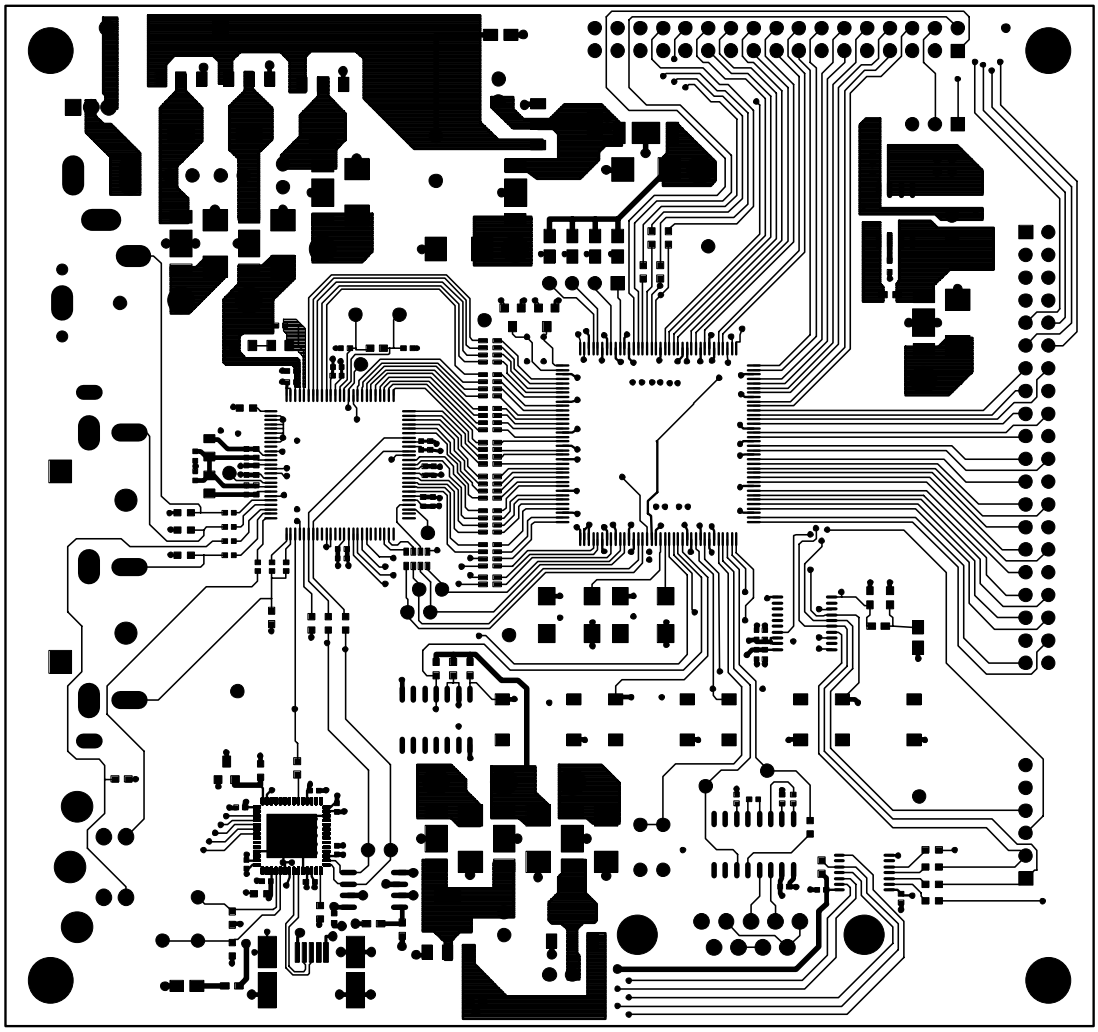


Figure 6: EVAL-ADV739xFEZ Layer 1

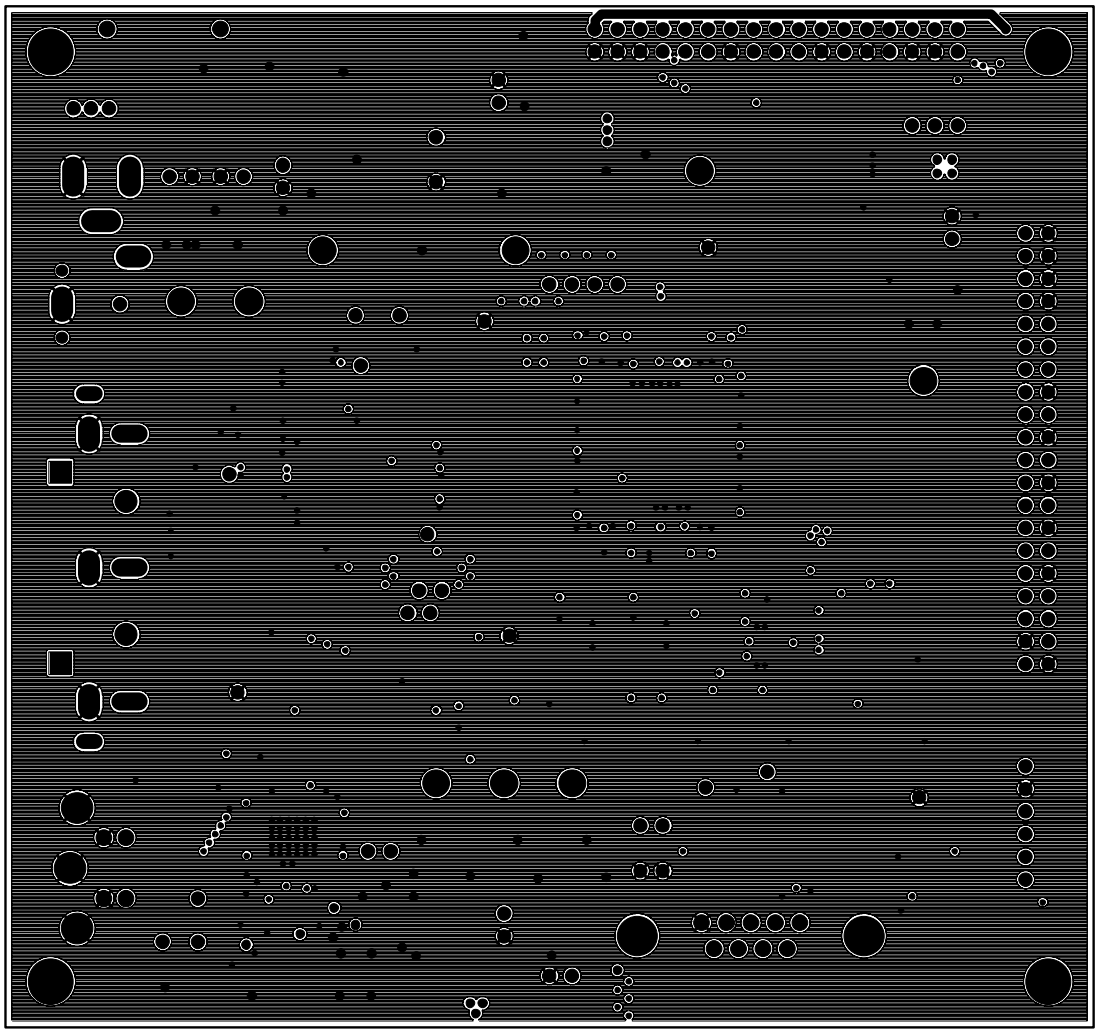


Figure 7: EVAL-ADV739xFEZ Layer 2 (GND Plane)

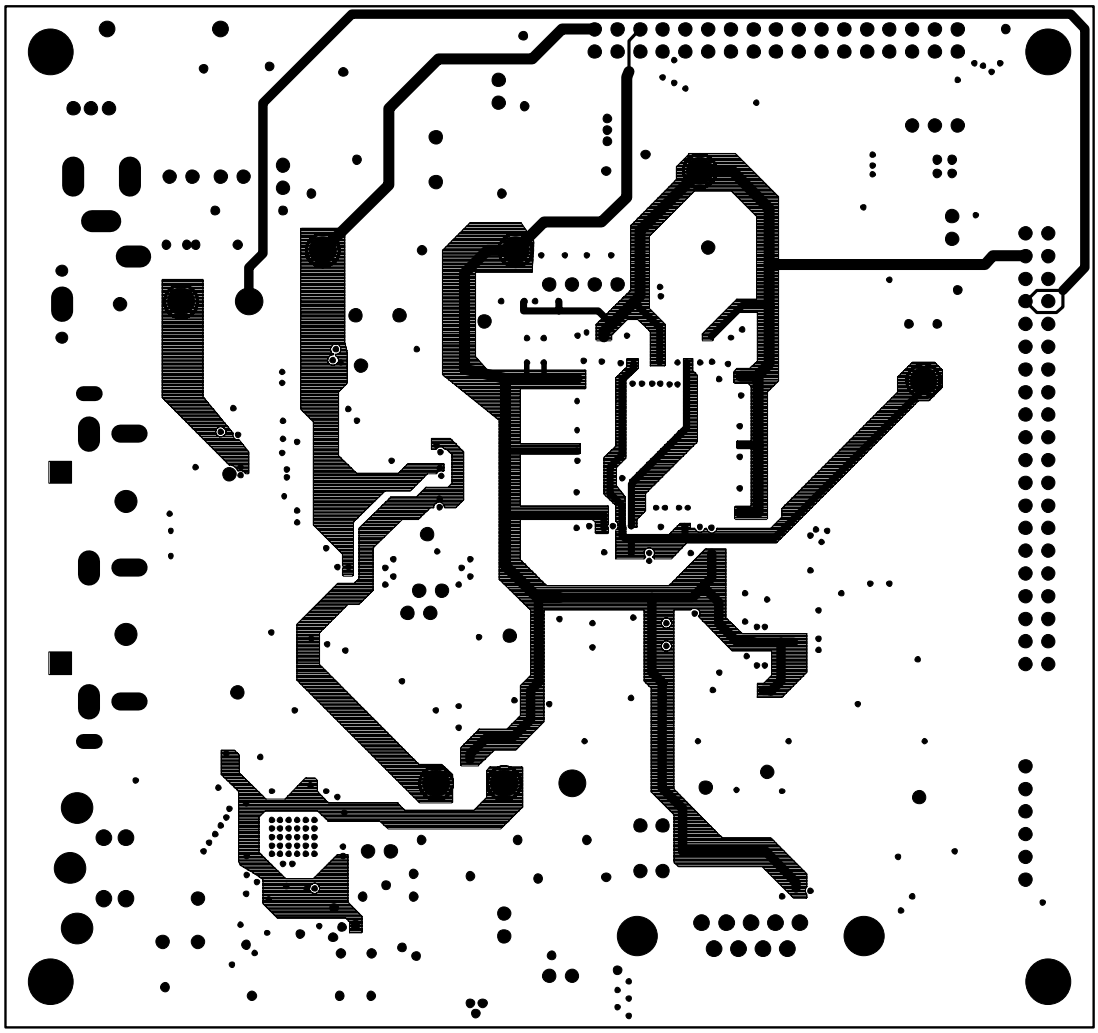


Figure 8: EVAL-ADV739xFEZ Layer 3 (Power plane)

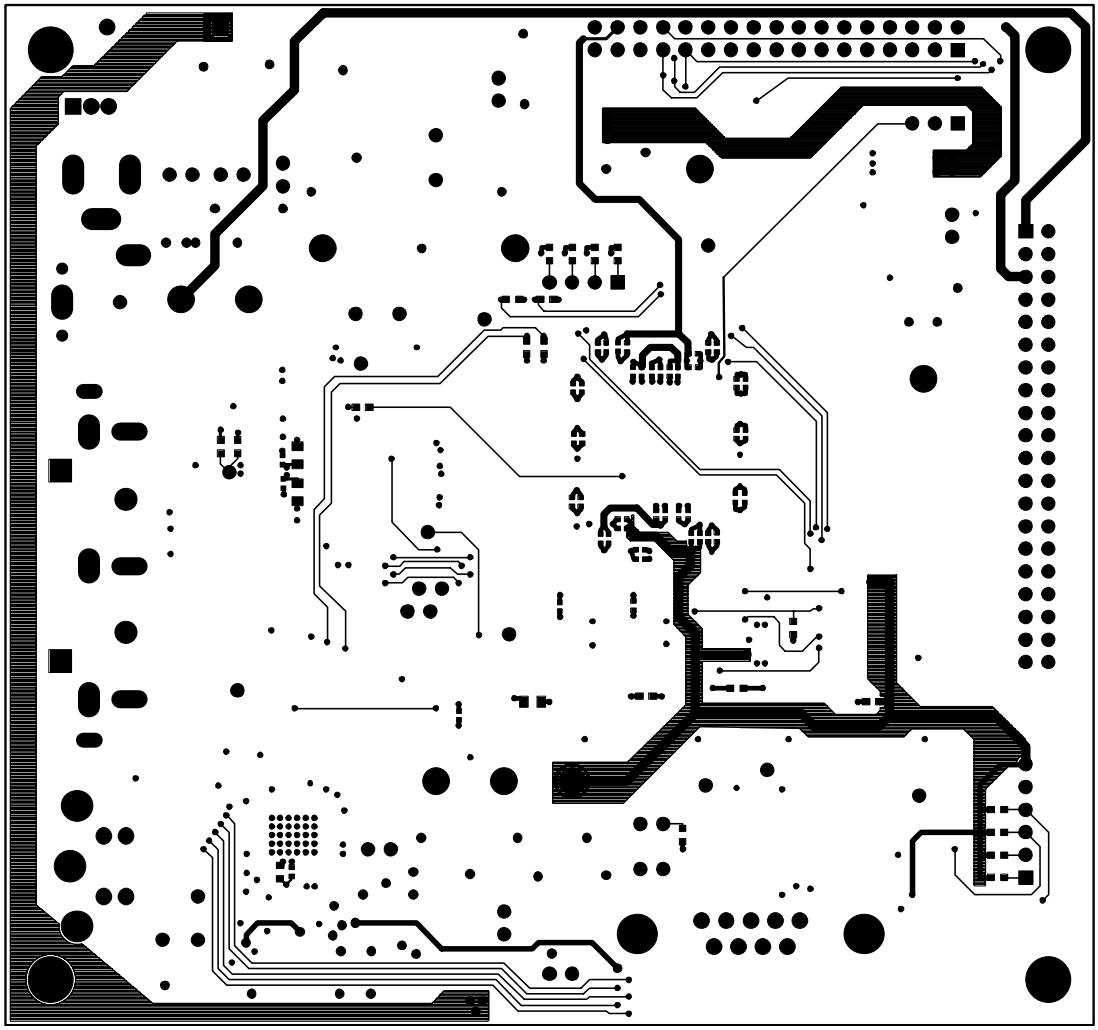


Figure 9: EVAL-ADV739xFEZ Layer 4

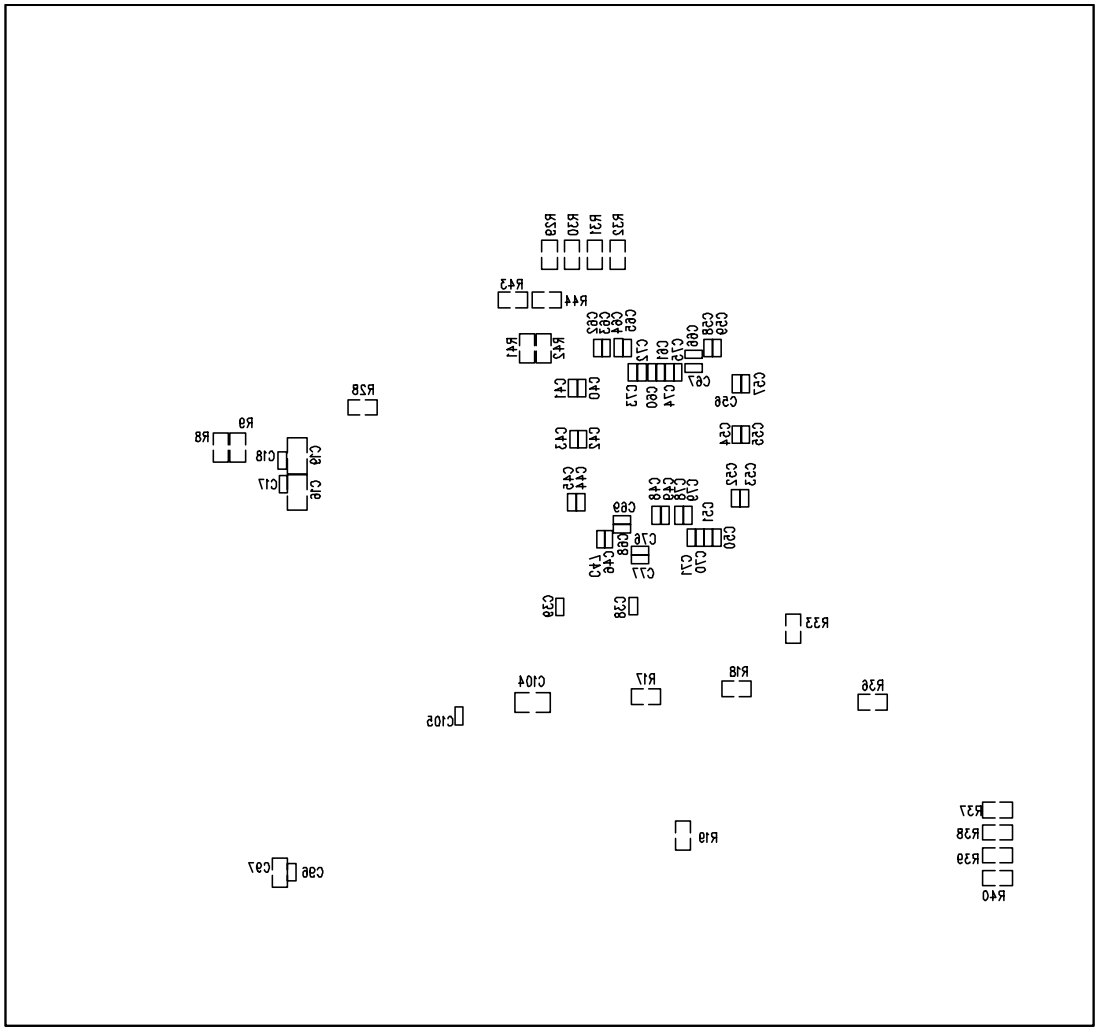


Figure 10: EVAL-ADV739xFEZ Silkscreen Bottom

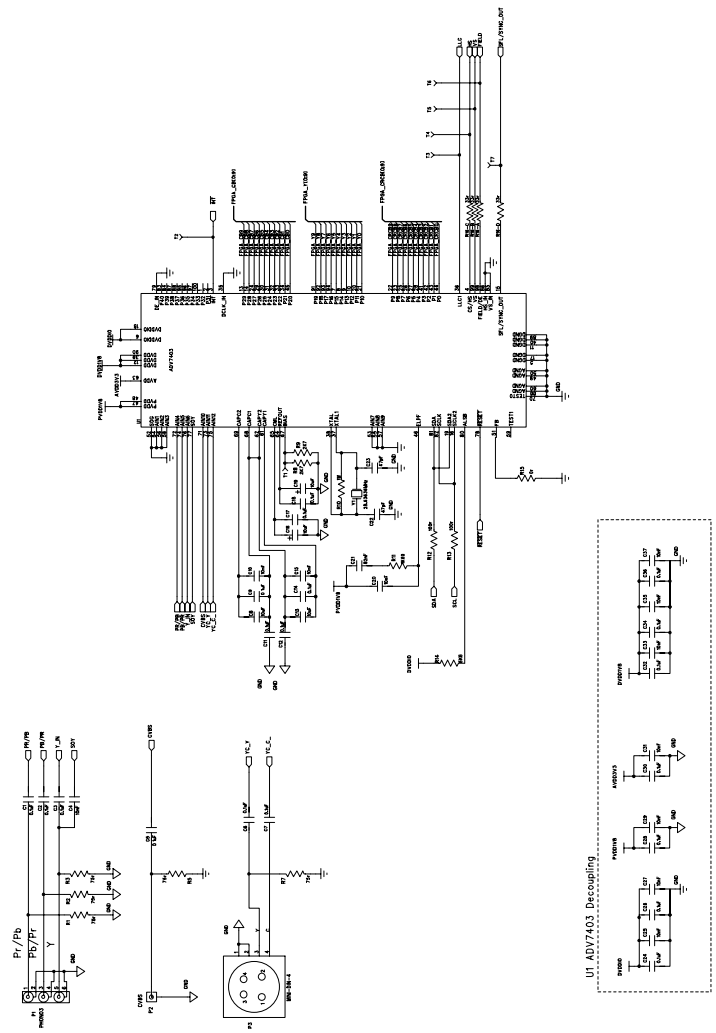


Figure 11: ADV7403 Video Decoder

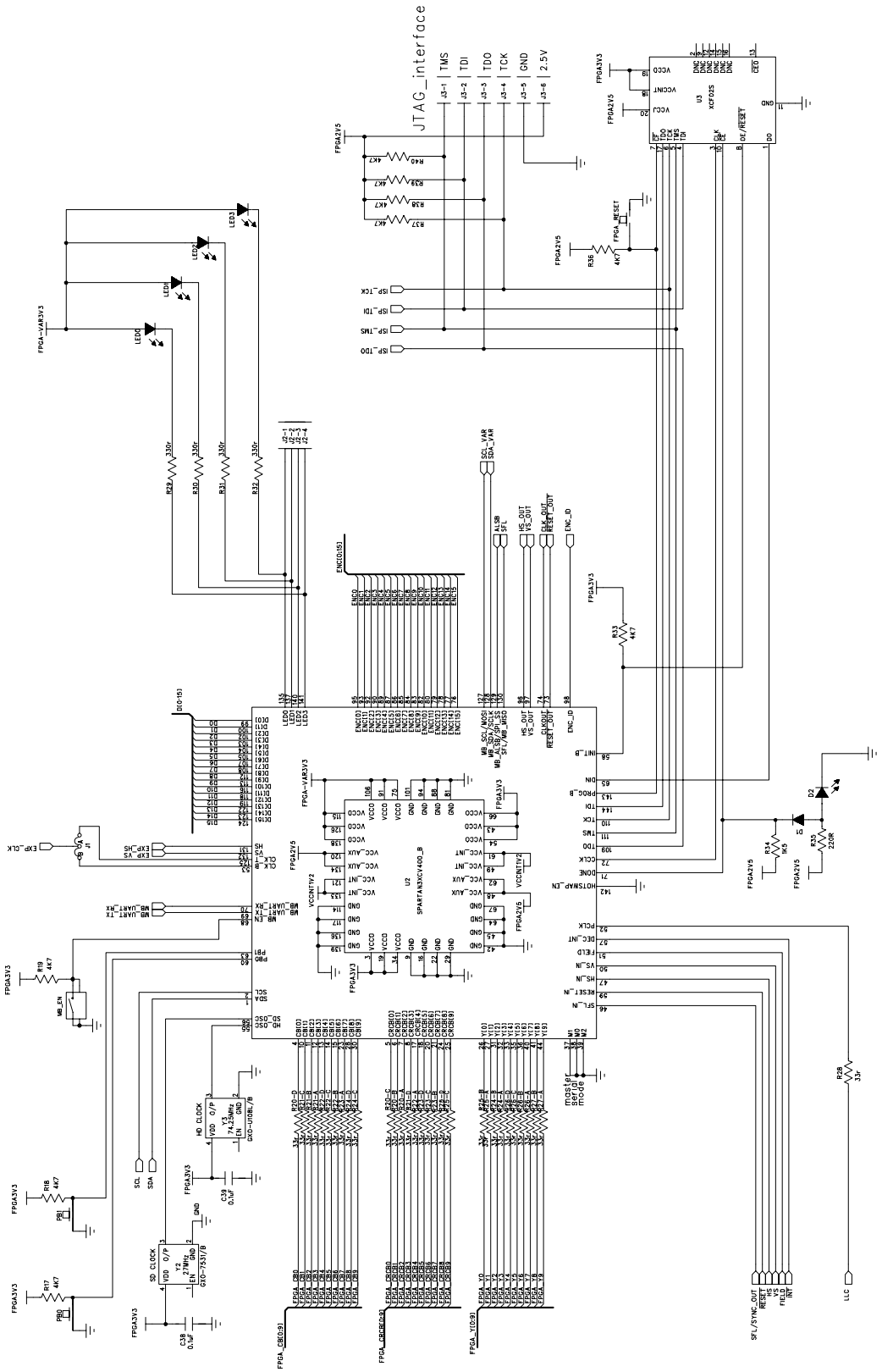
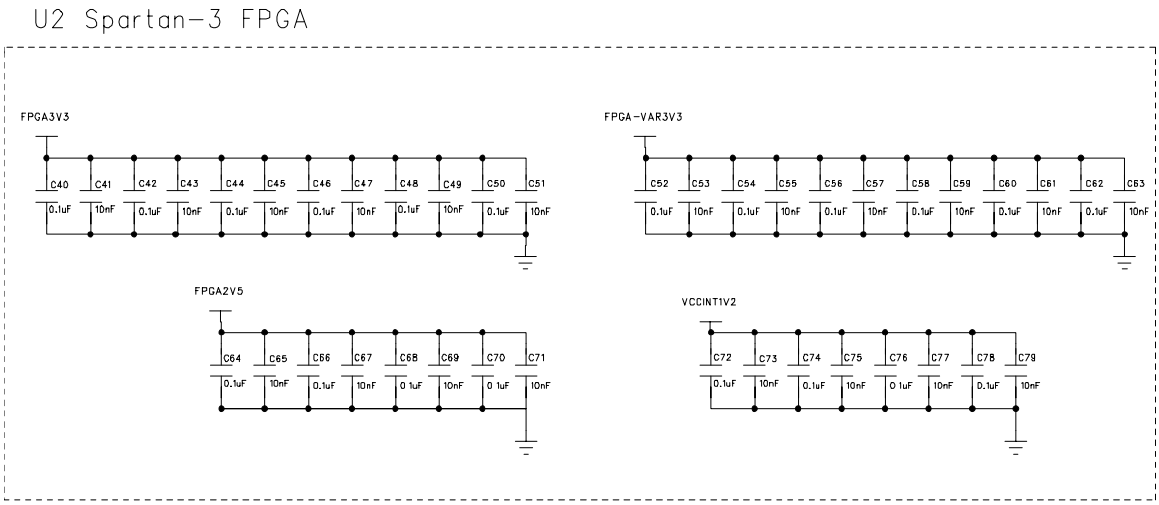


Figure 12: FPGA and Flash PROM



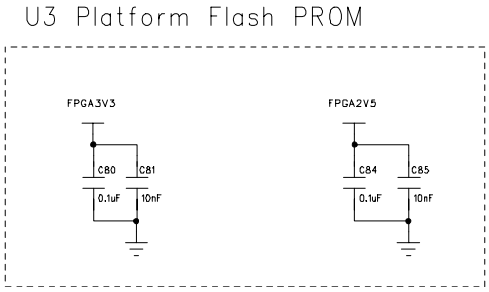


Figure 13: FPGA and PROM Decoupling

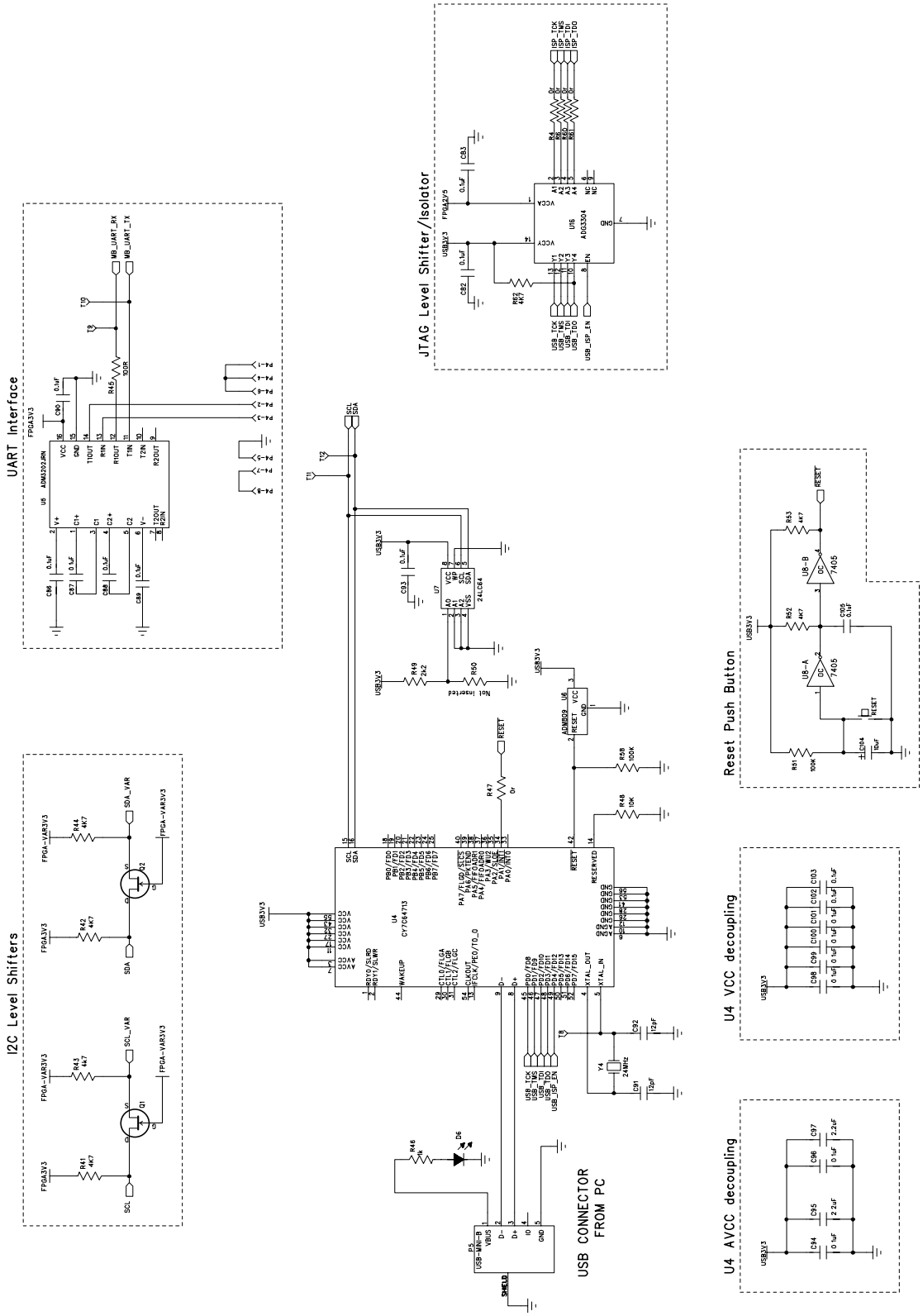


Figure 14: USB and UART Interfaces

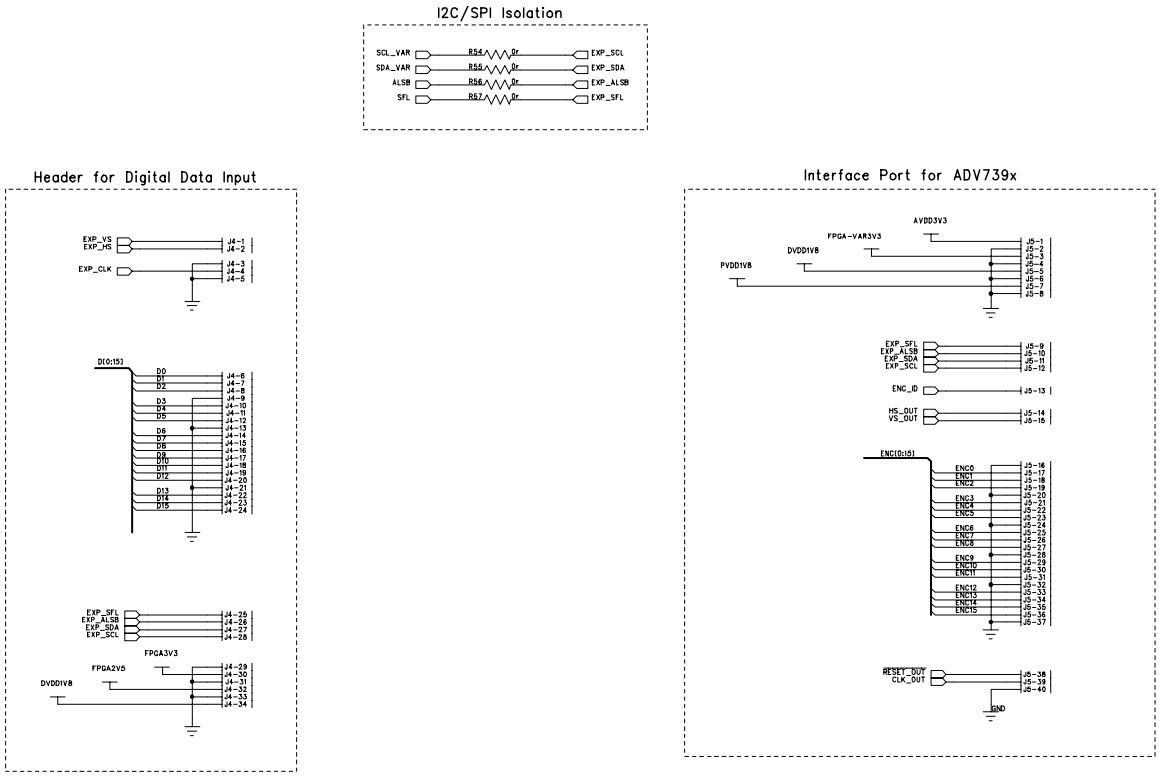


Figure 15: Data Interface Ports

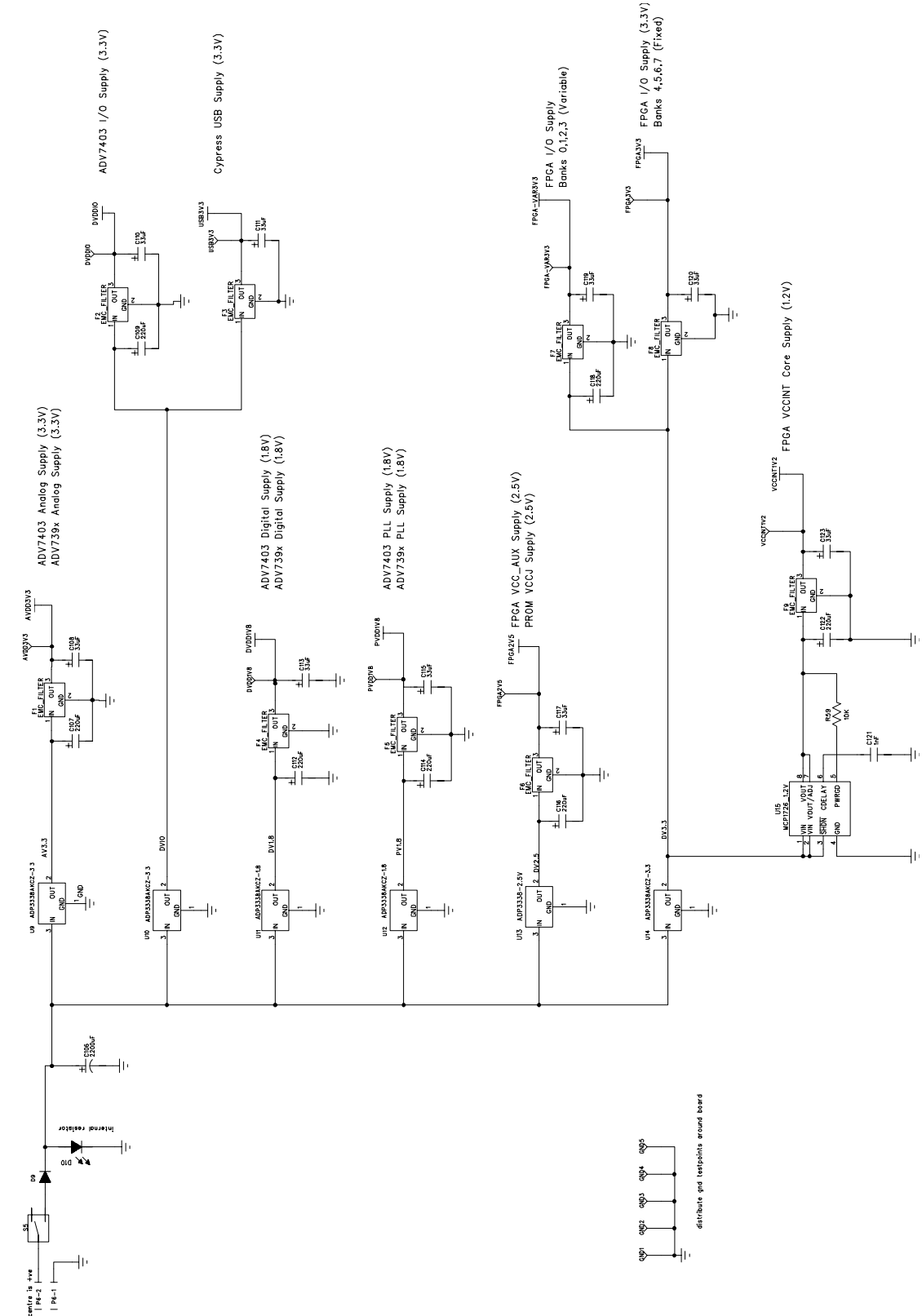


Figure 16: Power Supplies

EVAL-ADV7390/91EBZ PCB Drawings

Note: Layer 2 and 3 are both GND planes. All power traces are routed on Layer 4

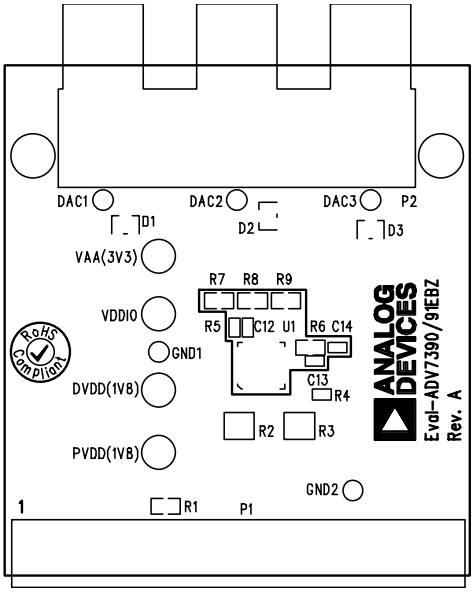


Figure 17: EVAL-ADV7390/91EBZ Silkscreen Top

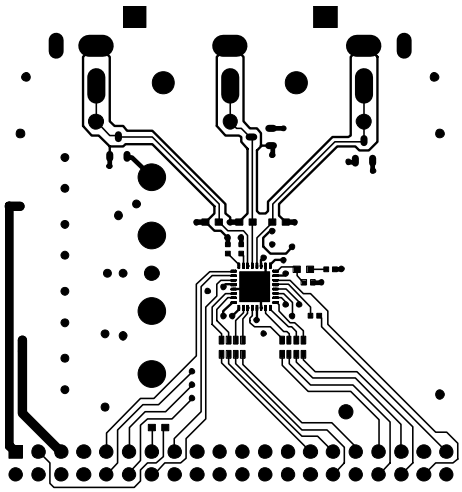


Figure 18: EVAL-ADV7390/91EBZ Component Side Layer 1

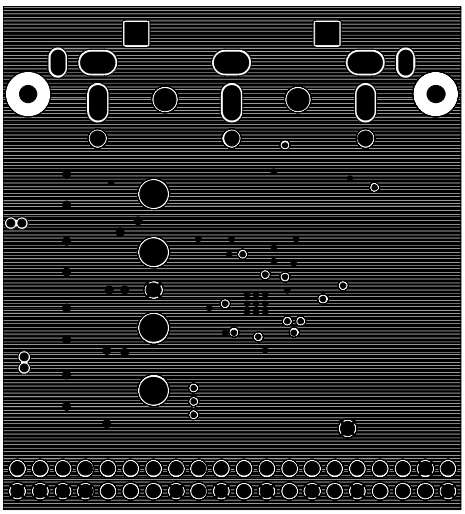


Figure 19: EVAL-ADV7390/91EBZ Ground Plane Layer 2

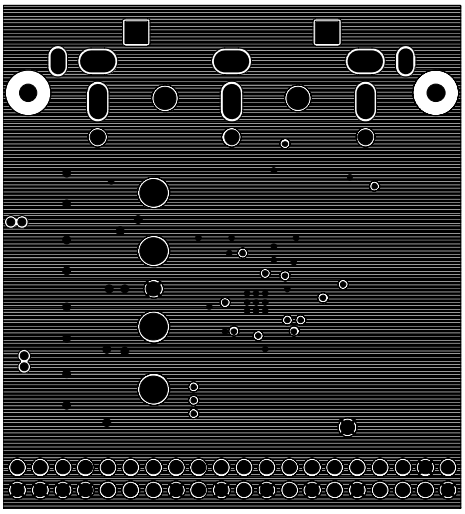


Figure 20: EVAL-ADV7390/91EBZ Ground Plane Layer 3

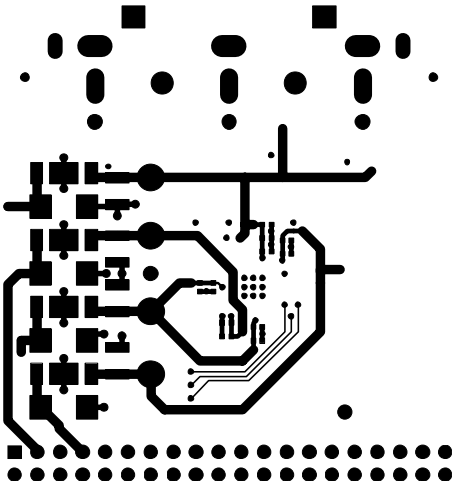


Figure 21: EVAL-ADV7390/91EBZ Solder Side Layer 4

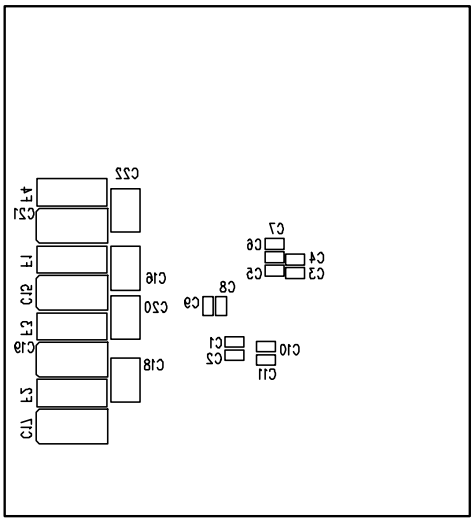


Figure 22: EVAL-ADV7390/91EBZ Silkscreen Bottom

EVAL-ADV7390/91EBZ Schematics

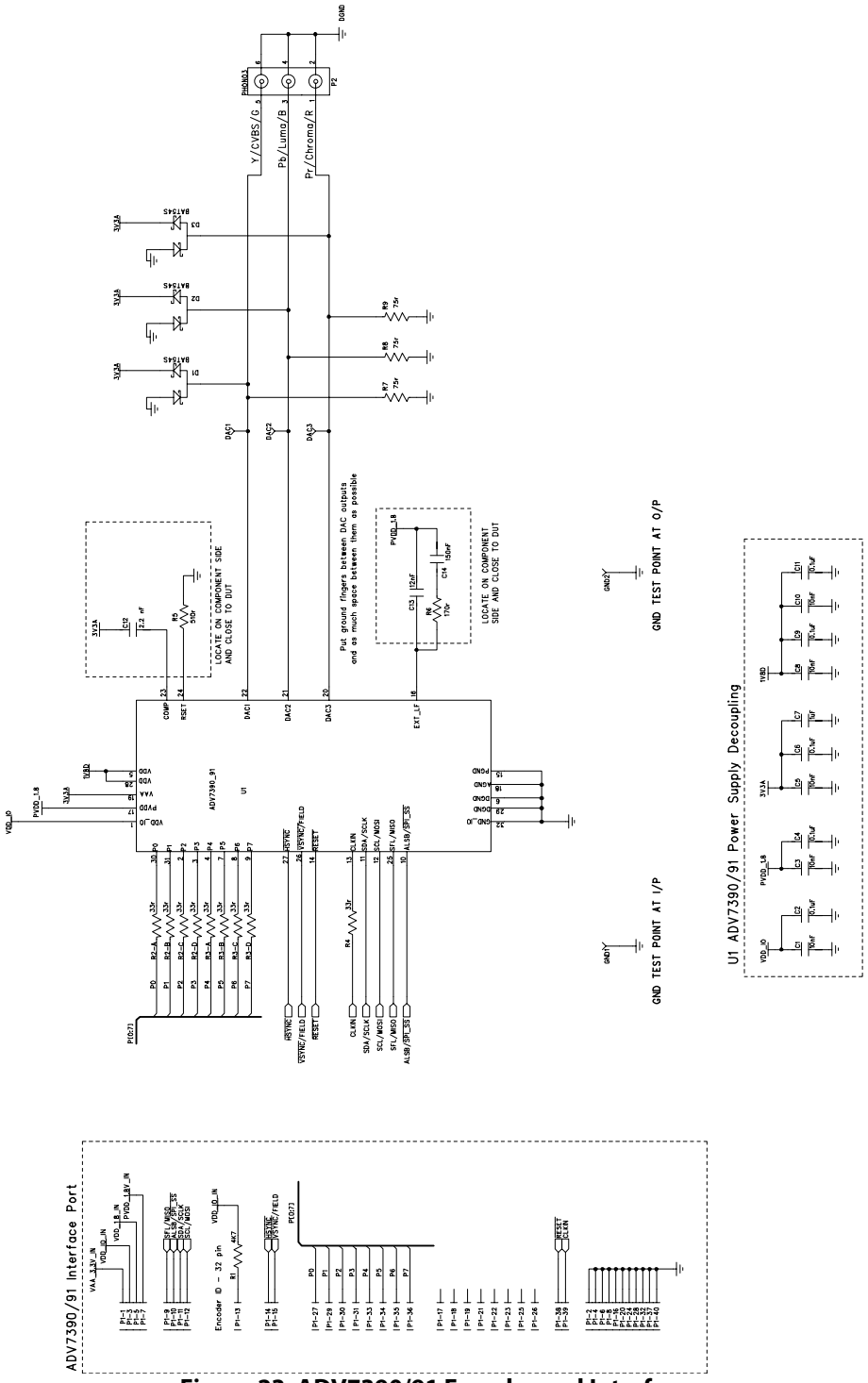


Figure 23: ADV7390/91 Encoder and Interface

LOCATE ON UNDERSIDE OF BOARD

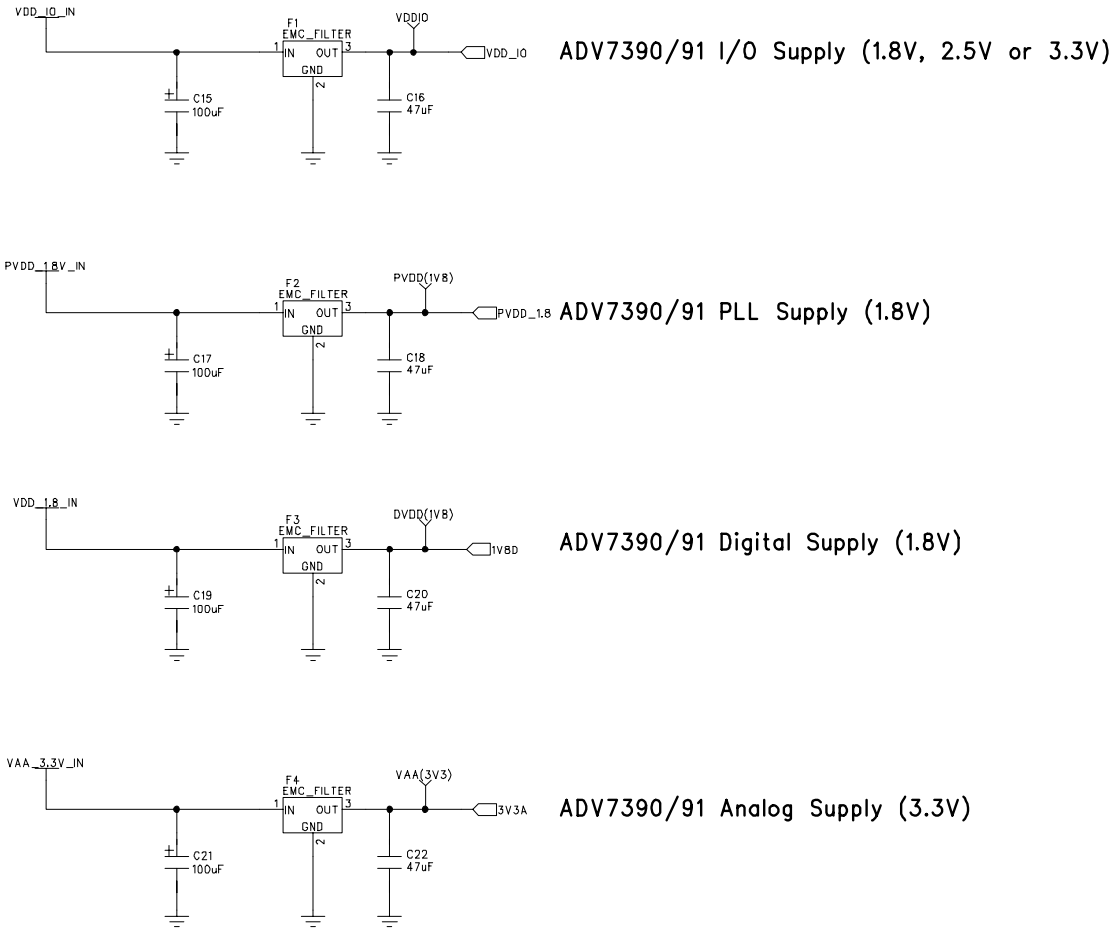


Figure 24: ADV7390/91 Power Supplies

EVAL-ADV7392/93EBZ PCB Drawings

Note: Layer 2 and 3 are both GND planes. All power traces are routed on Layer 4

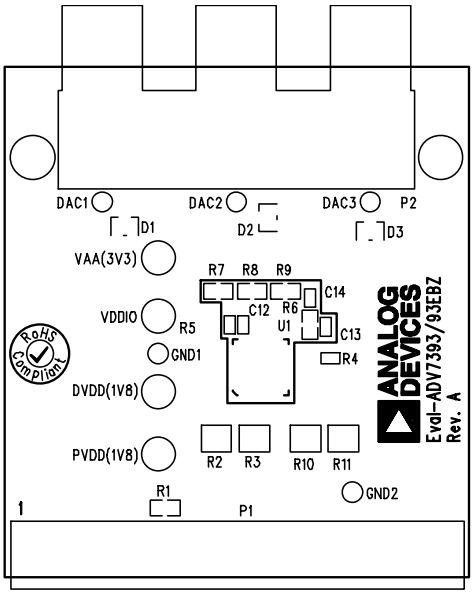


Figure 25: EVAL-ADV7392/93EBZ Silkscreen Top

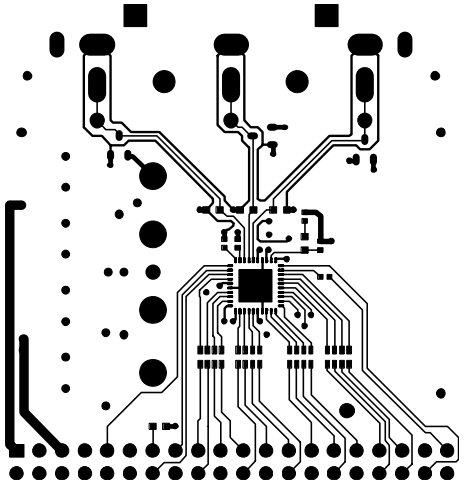


Figure 26: EVAL-ADV7392/93EBZ Layer 1

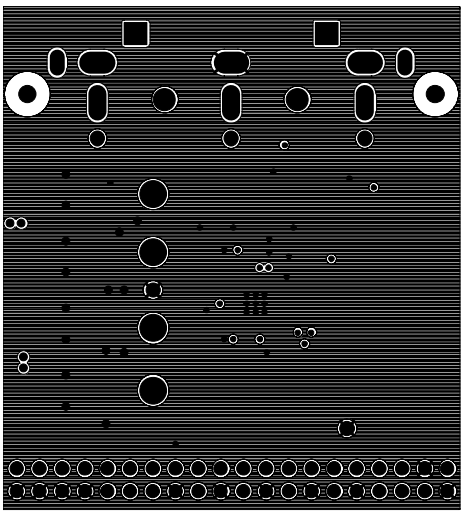


Figure 27: EVAL-ADV7392/93EBZ Layer 2

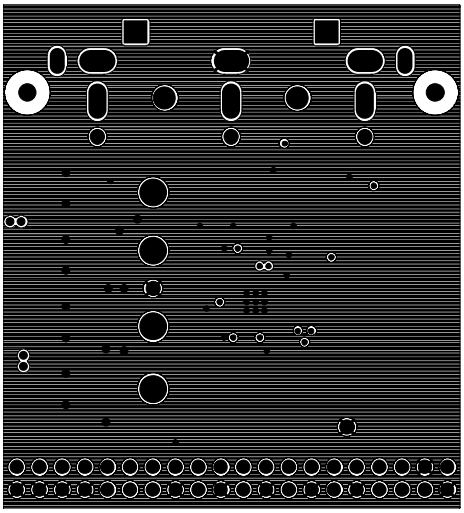


Figure 28: EVAL-ADV7392/93EBZ Layer 3 (power Plane)

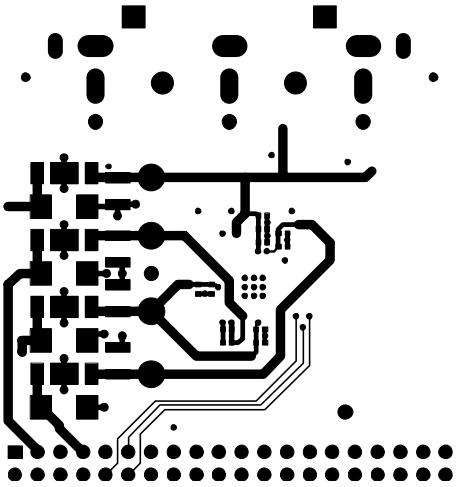


Figure 29: EVAL-ADV7392/93EBZ Layer 4

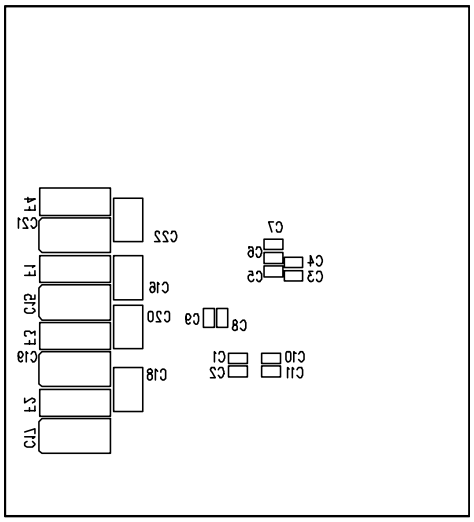


Figure 30: EVAL-ADV7392/93EBZ Silkscreen Bottom

EVAL-ADV7392/93EBZ Schematics

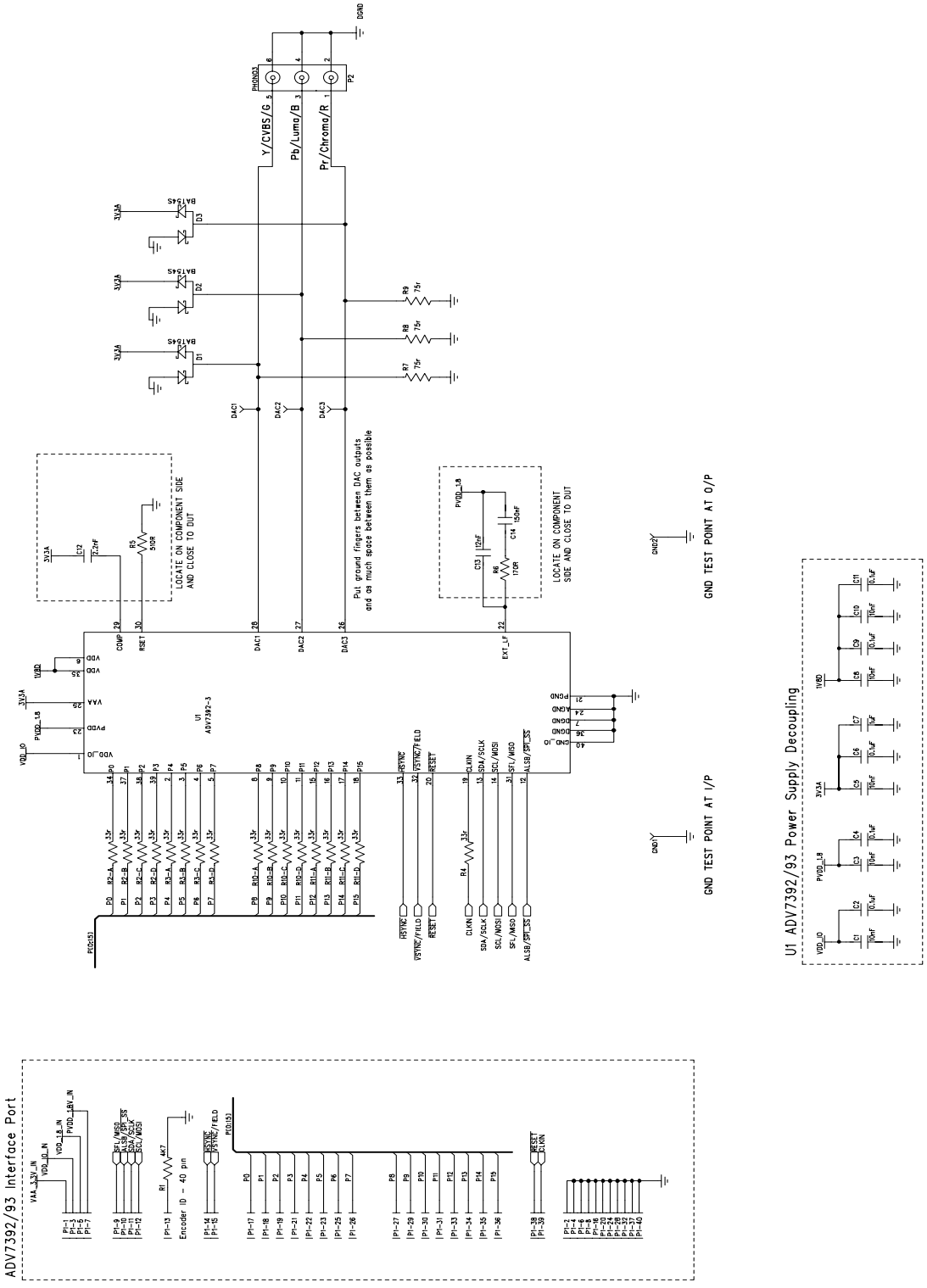


Figure 31: EVAL-ADV7392/93EBZ Encoder and Interface

LOCATE ON UNDERSIDE OF BOARD

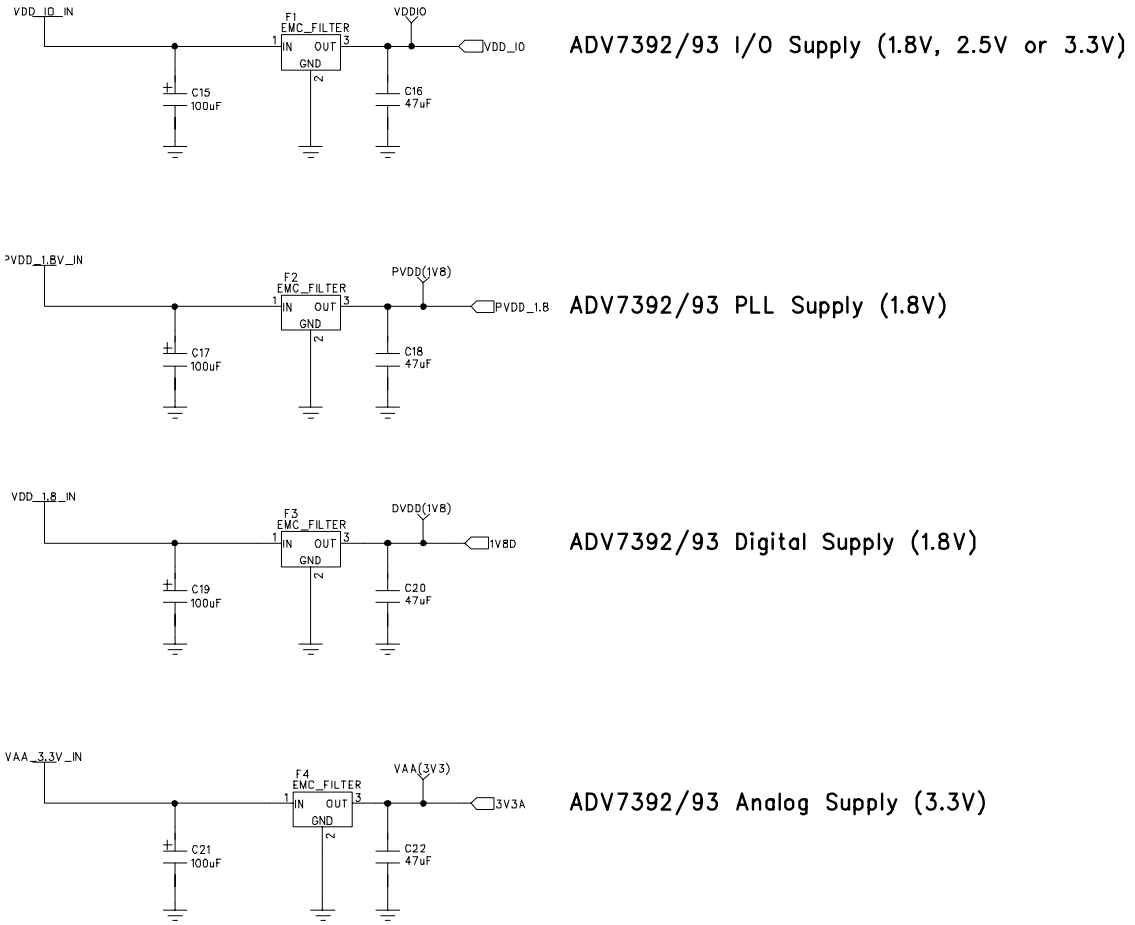


Figure 32: EVAL-ADV7392/93EBZ Power Supplies

Bill of materials