To our customers,

# Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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# HD74HC160/HD74HC161/HD74HC162/ HD74HC163

## Synchronous Decade Counter (Direct Clear)
## Synchronous 4-bit Binary Counter (Direct Clear)
## Synchronous Decade Counter (Synchronous Clear)
## Synchronous 4-bit Binary Counter (Synchronous Clear)

REJ03D0579-0200
(Previous ADE-205-455)
Rev.2.00
Oct 11, 2005



### Description

The HD74HC160 and the HD74HC162 are 4 bit decade counters, and the HD74HC161 and the HD74HC163 are 4 bit binary counters All flip-flops are clocked simultaneously on the low to high to transition (positive edge) of the clock input waveform.

These counters may be preset using the load input. Presetting of all four flip-flops is synchronous to the rising edge of clock. When load is held low counting is disabled and the data on the A, B, C, and D inputs is loaded into the counter on the rising edge of clock. If the load input is taken high before the positive edge of clock the count operation will be unaffected.

All of these counters may be cleared by the utilizing clear input. The clear function on the HD74HC162 and HD74HC163 counters are synchronous to the clock. That is, the counters are cleared on the positive edge of clock while the clear input is held low.

The HD74HC160 and HD74HC161 counters are cleared asynchronously. When the clear is taken low the counter is cleared immediately regardless of the clock.

Two active high enable inputs Enable P and Enable T and a ripple carry output are provided to enable easy cascading of counters. Both enable inputs must be high to count. The Enable T input also enables the Ripple Carry output. When enabled, the Ripple Carry outputs a positive pulse when the counter overflows. This pulse is approximately equal in duration to the high level portion of the $Q_A$ outputs. The Ripple Carry output is fed to successive cascaded stages to facilitate easy implementation of N-bit counters.

### Features

- High Speed Operation: $t_{pd}$ (Clock to Q) = 18 ns typ ($C_L$ = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC}$ = 2 to 6 V
- Low Input Current: 1 ∝A max
- Low Quiescent Supply Current: $I_{CC}$ (static) = 4 ∝A max (Ta = 25°C)

- Ordering Information

| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|---|---|---|---|---|
| HD74HC160P<br>HD74HC161P<br>HD74HC162P<br>HD74HC163P | DILP-16 pin | PRDP0016AE-B<br>(DP-16FV) | P | — |
| HD74HC160FPEL<br>HD74HC161FPEL<br>HD74HC162FPEL<br>HD74HC163FPEL | SOP-16 pin (JEITA) | PRSP0016DH-B<br>(FP-16DAV) | FP | EL (2,000 pcs/reel) |
| HD74HC160RPEL<br>HD74HC162RPEL<br>HD74HC163RPEL | SOP-16 pin (JEDEC) | PRSP0016DG-A<br>(FP-16DNV) | RP | EL (2,500 pcs/reel) |
| HD74HC161TELL | TSSOP-16 pin | PTSP0016JB-A<br>(TTP-16DAV) | T | ELL (2,000 pcs/reel) |

Note: Please consult the sales office for the above package availability.

## Function Table

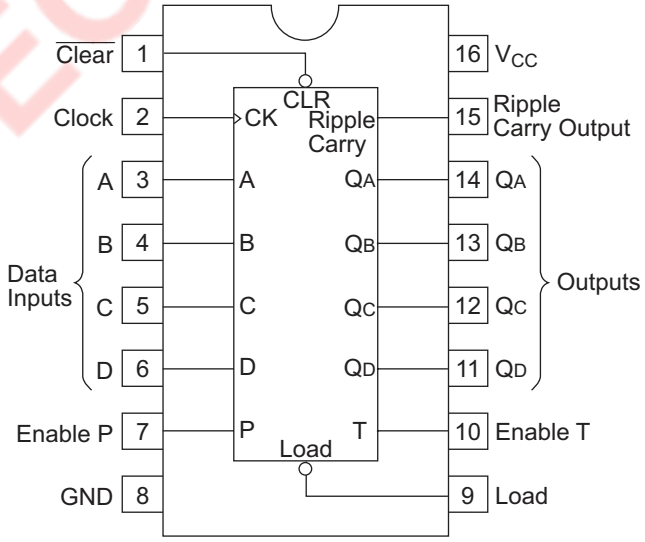
| Inputs | | | | | Outputs |
|---|---|---|---|---|---|
| Clock | $\overline{\text{Clear}}$*1 | $\overline{\text{Load}}$ | Enable P | Enable T | $Q_n$ |
| ↑ | L | X | X | X | Reset-clear |
| ↑ | H | L | X | X | Load input data |
| ↑ | H | H | H | H | Count |
| ↑ | H | H | L | X | No count |
| ↑ | H | H | X | L | No count |

H : High level L : Low level X : Irrelevant

Note: 1. 162 and 163 Only-160 and 161 are Asynchronous Clear Devices

| | Decade Counter | Binary Counter |
|---|---|---|
| Asynchronous clear | HD74HC160 | HD74HC161 |
| Synchronous clear | HD74HC162 | HD74HC163 |

## Pin Arrangement

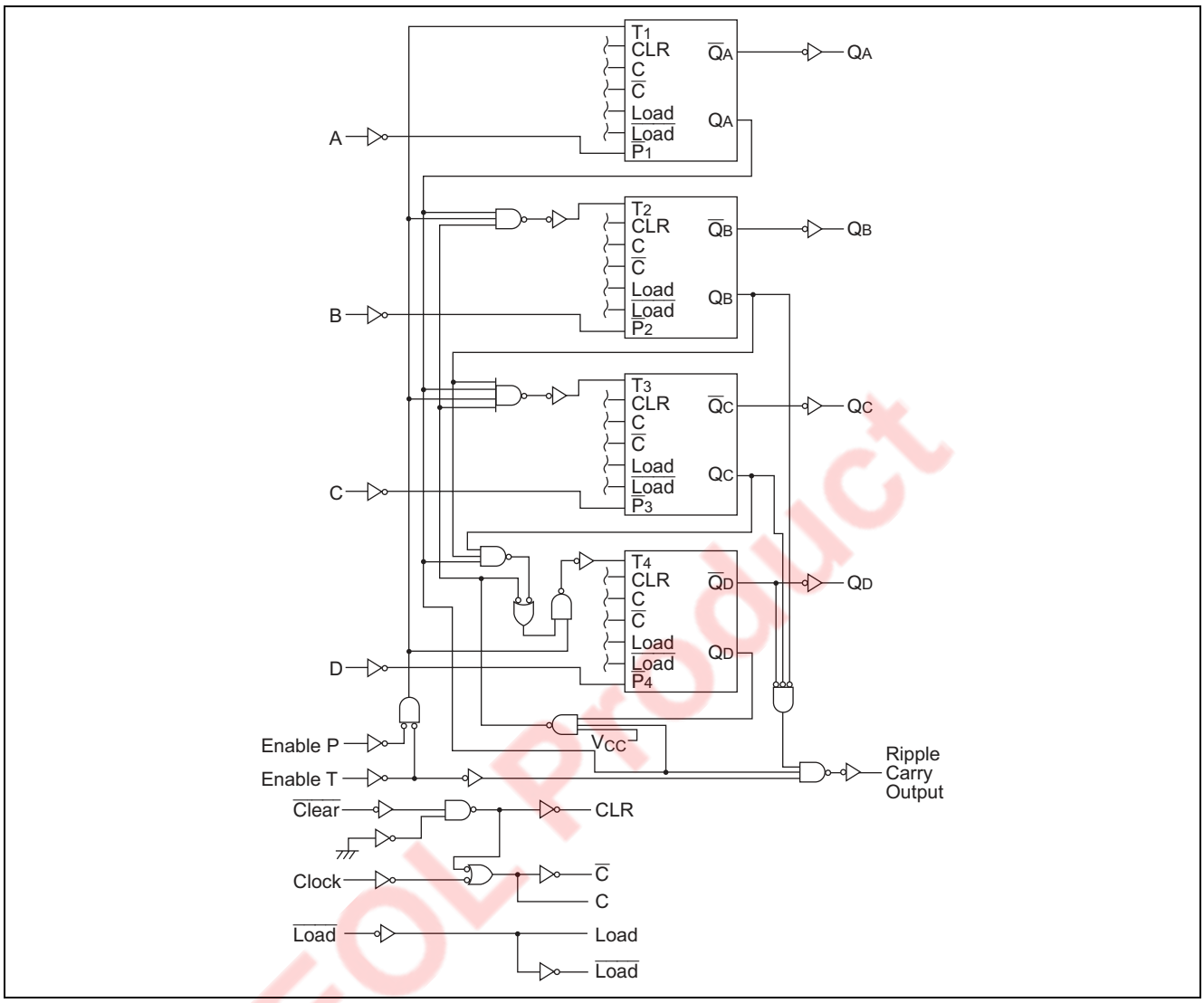



(Top view)

## Logic Diagram

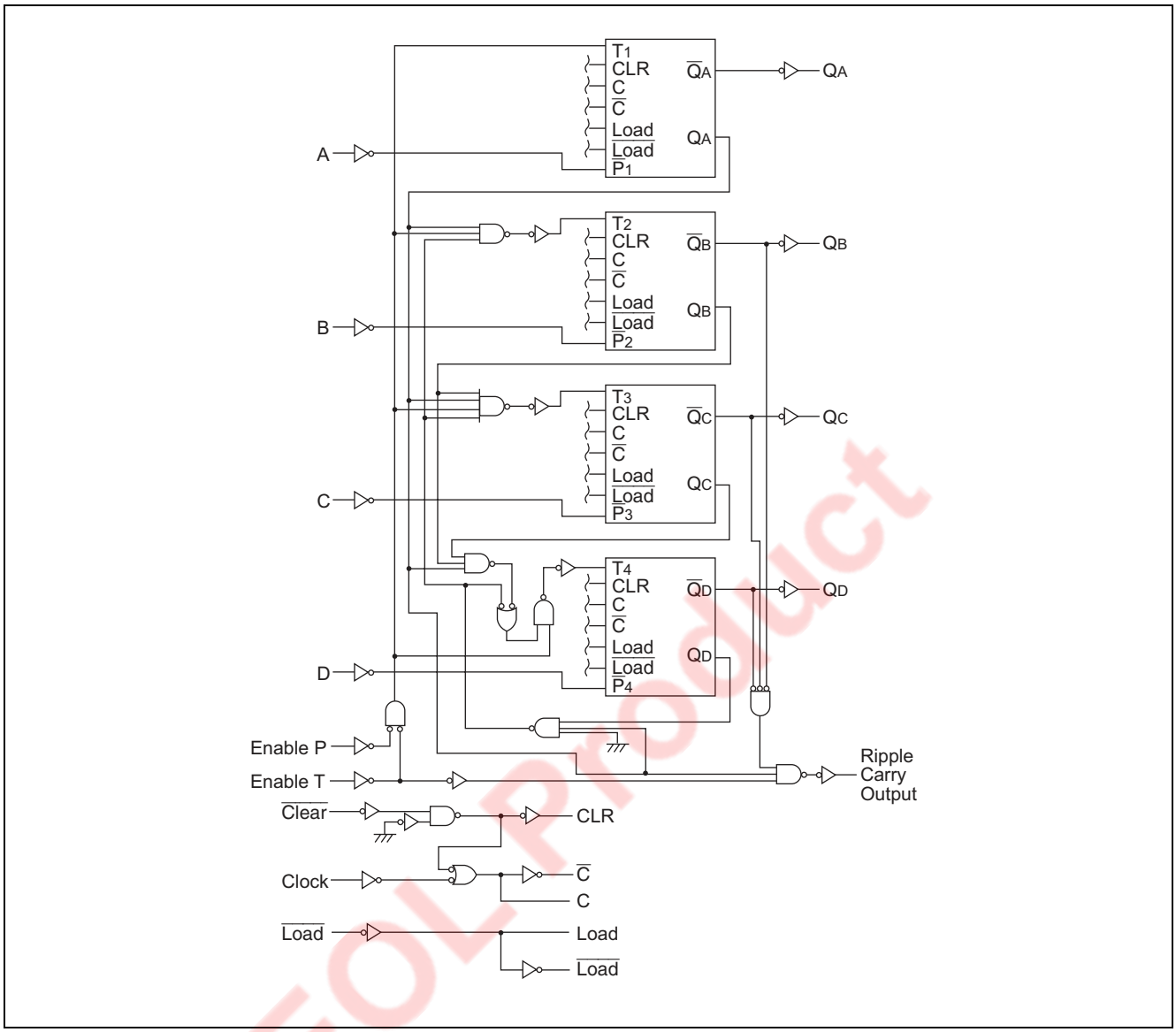
### HD74HC160

Decade Counter with Asynchronous Clear



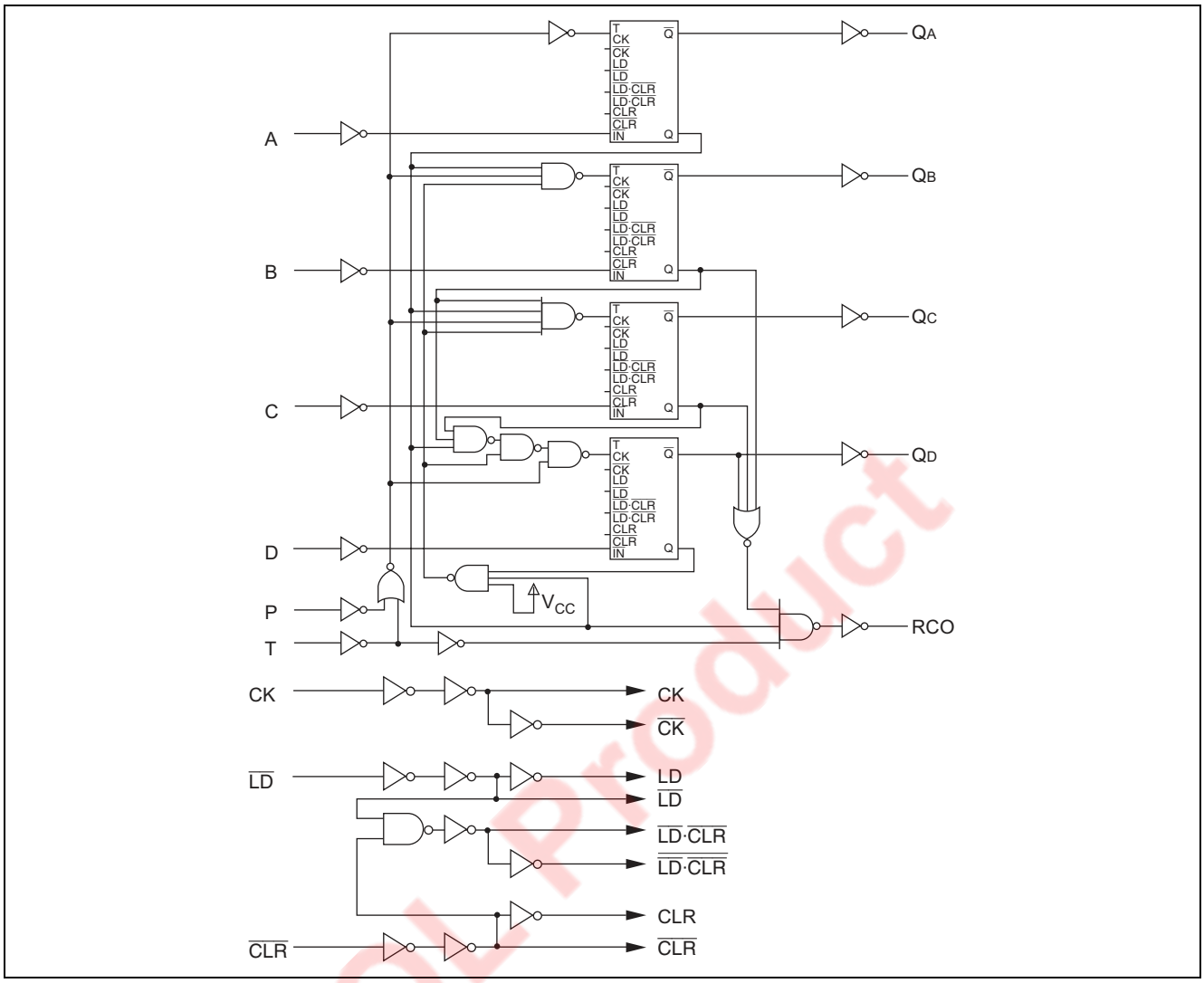
## HD74HC161

4-bit Binary Counter with Asynchronous Clear



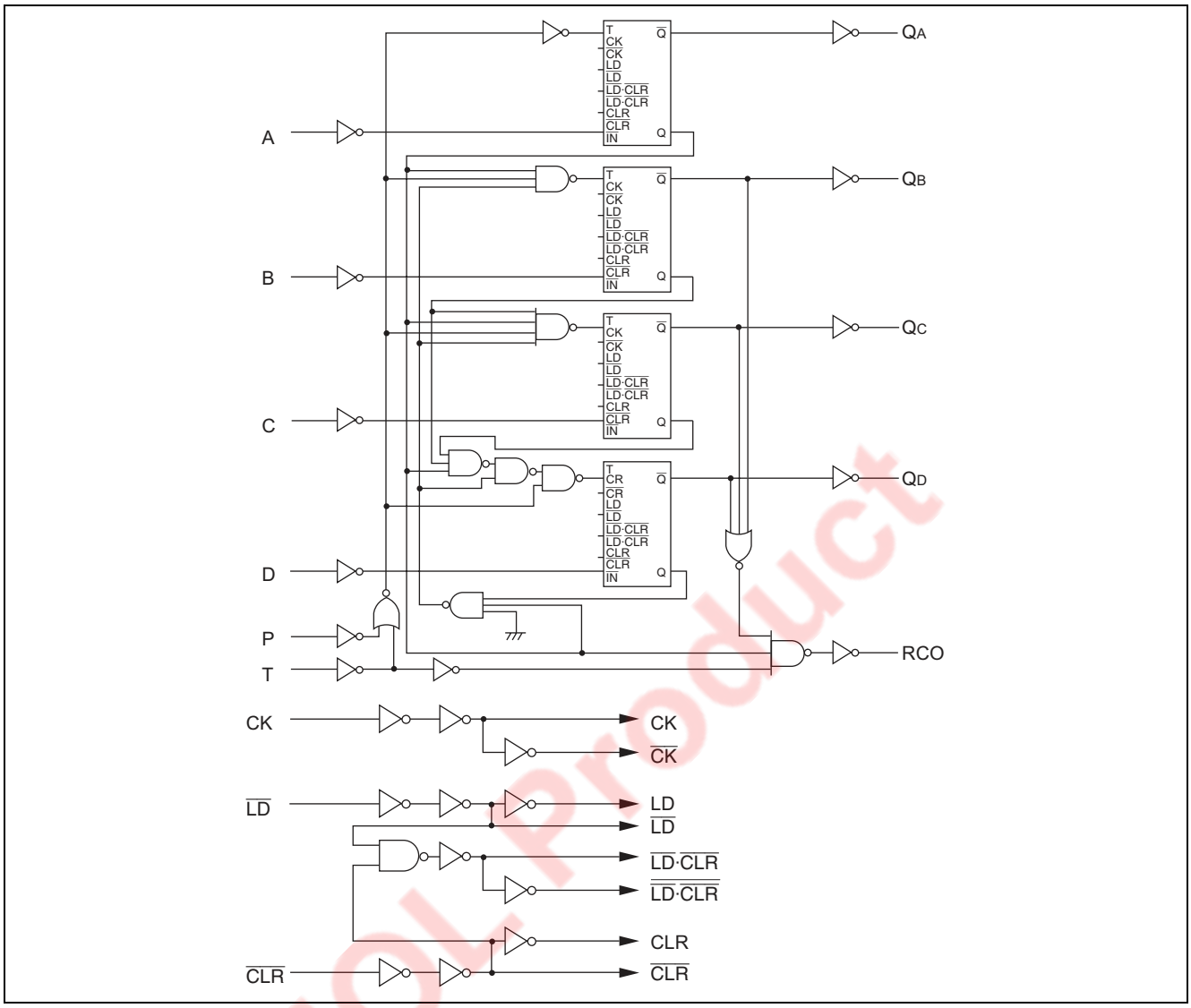
## HD74HC162

Decade Counter with Synchronous Clear



## HD74HC163

4-bit Binary Counter with Synchronous Clear

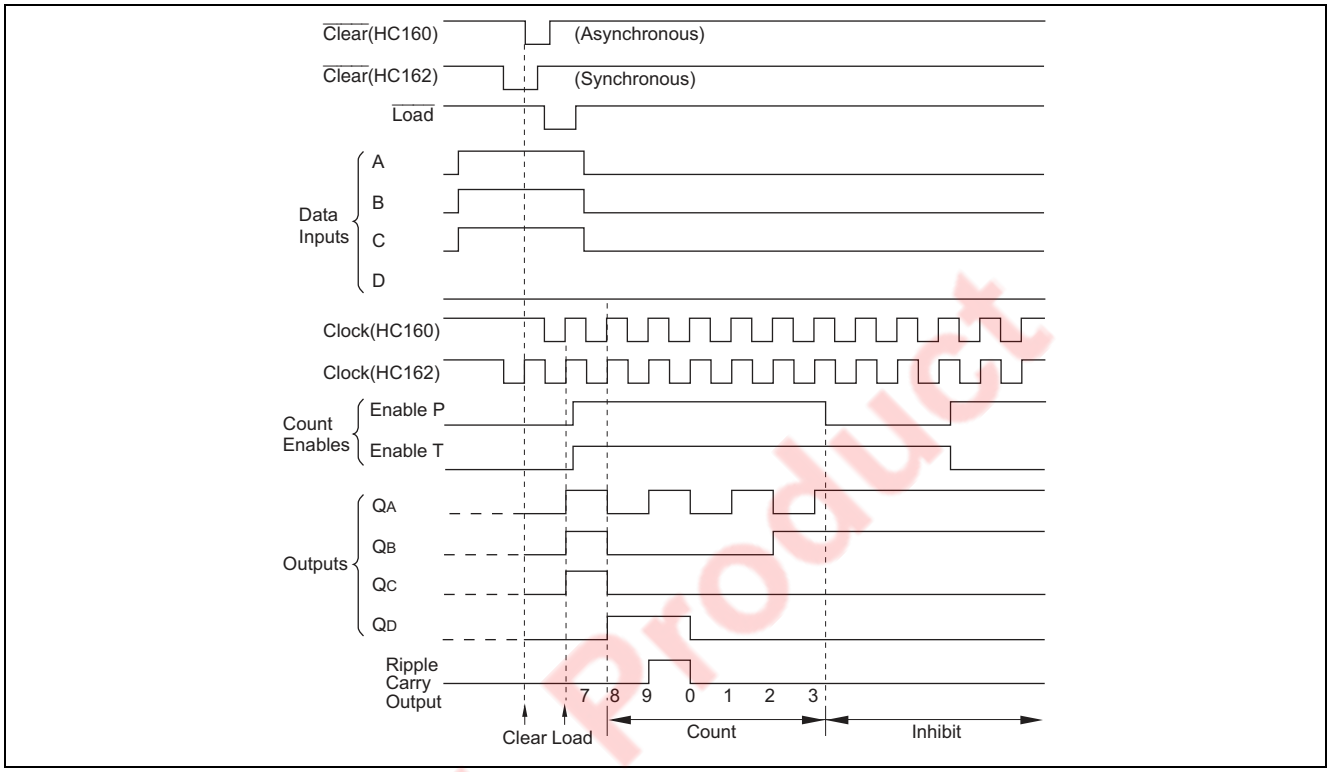


## Timing Diagram

### HD74HC160/HD74HC162

Sequence illustrated in waveforms.

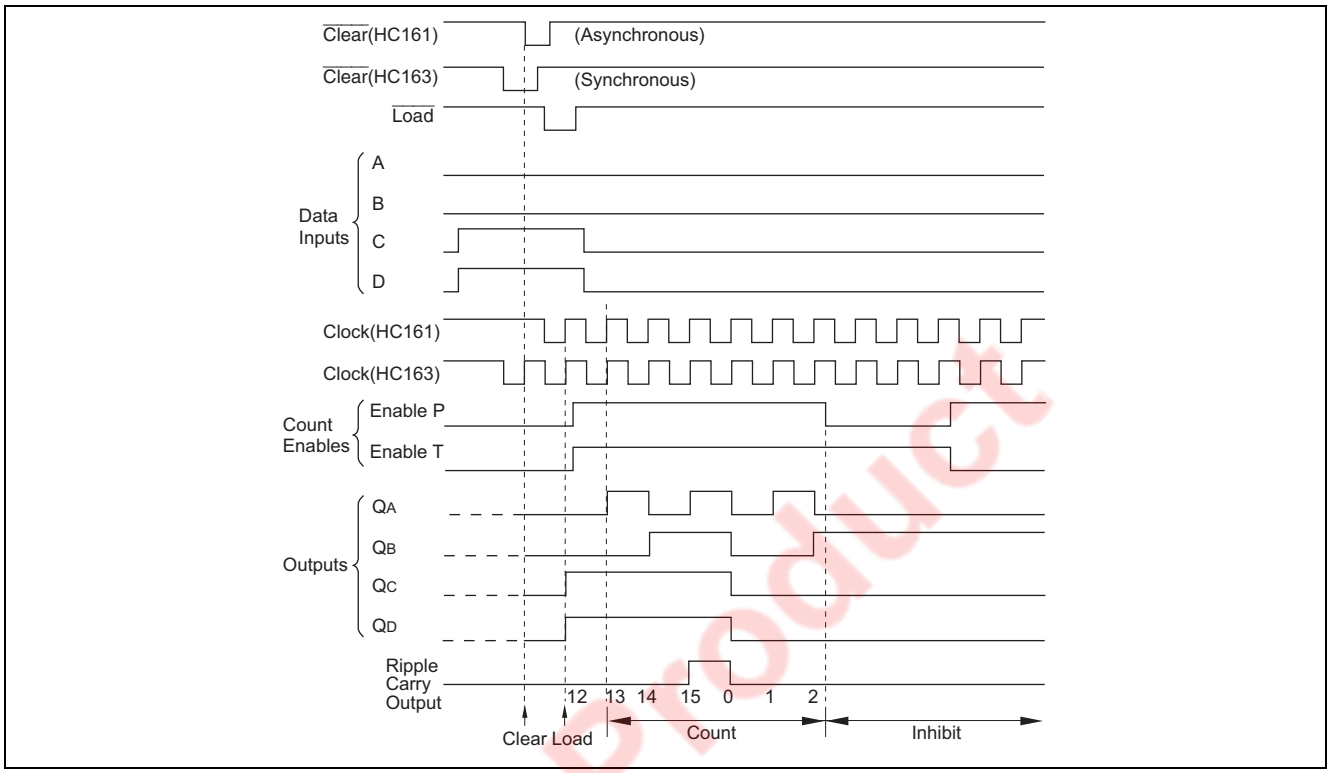
1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two and three.
4. Inhibit



### HD74HC161/HD74HC163

Sequence illustrated in waveforms.

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one and two.
4. Inhibit



## Absolute Maximum Ratings

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | $V_{CC}$ | –0.5 to +7.0 | V |
| Input voltage | $V_{IN}$ | –0.5 to $V_{CC}$ + 0.5 | V |
| Output voltage | $V_{OUT}$ | –0.5 to $V_{CC}$ + 0.5 | V |
| Output current | $I_{OUT}$ | ±25 | mA |
| DC current drain per VCC, GND | $I_{CC}$, $I_{GND}$ | ±50 | mA |
| DC input diode current | $I_{IK}$ | ±20 | mA |
| DC output diode current | $I_{OK}$ | ±20 | mA |
| Power dissipation per package | $P_T$ | 500 | mW |
| Storage temperature | Tstg | –65 to +150 | °C |

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

## Recommended Operating Conditions

| Item | Symbol | Ratings | Unit | Conditions |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2 to 6 | V | |
| Input / Output voltage | $V_{IN}$, $V_{OUT}$ | 0 to $V_{CC}$ | V | |
| Operating temperature | Ta | –40 to 85 | °C | |
| Input rise / fall time*1 | $t_r$, $t_f$ | 0 to 1000 | ns | $V_{CC}$ = 2.0 V |
| | | 0 to 500 | | $V_{CC}$ = 4.5 V |
| | | 0 to 400 | | $V_{CC}$ = 6.0 V |

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

## Electrical Characteristics

| Item | Symbol | $V_{CC}$ (V) | Ta = 25°C | | | Ta = –40 to+85°C | | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | | |
| Input voltage | $V_{IH}$ | 2.0 | 1.5 | — | — | 1.5 | — | V | | |
| | | 4.5 | 3.15 | — | — | 3.15 | — | | | |
| | | 6.0 | 4.2 | — | — | 4.2 | — | | | |
| | $V_{IL}$ | 2.0 | — | — | 0.5 | — | 0.5 | V | | |
| | | 4.5 | — | — | 1.35 | — | 1.35 | | | |
| | | 6.0 | — | — | 1.8 | — | 1.8 | | | |
| Output voltage | $V_{OH}$ | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V | Vin = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 ∝A |
| | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | | | |
| | | 6.0 | 5.9 | 6.0 | — | 5.9 | — | | | |
| | | 4.5 | 4.18 | — | — | 4.13 | — | | | $I_{OH}$ = –4 mA |
| | | 6.0 | 5.68 | — | — | 5.63 | — | | | $I_{OH}$ = –5.2 mA |
| | $V_{OL}$ | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V | Vin = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 ∝A |
| | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | | | |
| | | 6.0 | — | 0.0 | 0.1 | — | 0.1 | | | |
| | | 4.5 | — | — | 0.26 | — | 0.33 | | | $I_{OL}$ = 4 mA |
| | | 6.0 | — | — | 0.26 | — | 0.33 | | | $I_{OL}$ = 5.2 mA |
| Input current | Iin | 6.0 | — | — | ±0.1 | — | ±1.0 | ∝A | Vin = $V_{CC}$ or GND | |
| Quiescent supply current | $I_{CC}$ | 6.0 | — | — | 4.0 | — | 40 | ∝A | Vin = $V_{CC}$ or GND, Iout = 0 ∝A | |

## Switching Characteristics ($C_L$ = 50 pF, Input $t_r$ = $t_f$ = 6 ns)

| Item | Symbol | $V_{CC}$ (V) | Ta = 25°C | | | Ta = –40 to +85°C | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | |
| Maximum clock frequency | $f_{max}$ | 2.0 | — | — | 5 | — | 4 | MHz | |
| | | 4.5 | — | — | 25 | — | 20 | | |
| | | 6.0 | — | — | 29 | — | 23 | | |
| Propagation delay time | $t_{PLH}$, $t_{PHL}$ | 2.0 | — | — | 160 | — | 200 | ns | Clock to Q |
| | | 4.5 | — | 18 | 32 | — | 40 | | |
| | | 6.0 | — | — | 27 | — | 34 | | |
| | | 2.0 | — | — | 225 | — | 280 | ns | $\overline{\text{Clear}}$ to Q (HC160, HC161 only) |
| | | 4.5 | — | 23 | 45 | — | 56 | | |
| | | 6.0 | — | — | 38 | — | 48 | | |
| | | 2.0 | — | — | 150 | — | 190 | ns | Enable T to Ripple Carry output |
| | | 4.5 | — | 15 | 30 | — | 38 | | |
| | | 6.0 | — | — | 26 | — | 33 | | |
| | | 2.0 | — | — | 200 | — | 250 | ns | Clock to Ripple carry output |
| | | 4.5 | — | 16 | 40 | — | 50 | | |
| | | 6.0 | — | — | 34 | — | 43 | | |
| Setup time | $t_{su}$ | 2.0 | 125 | — | — | 156 | — | ns | Data to Clock |
| | | 4.5 | 25 | 9 | — | 31 | — | | |
| | | 6.0 | 21 | — | — | 26 | — | | |
| | | 2.0 | 125 | — | — | 156 | — | ns | $\overline{\text{Load}}$ to Clock |
| | | 4.5 | 25 | 15 | — | 31 | — | | |
| | | 6.0 | 21 | — | — | 26 | — | | |
| | | 2.0 | 125 | — | — | 156 | — | ns | $\overline{\text{Clear}}$ to Clock (HC162, HC163 only) |
| | | 4.5 | 25 | — | — | 31 | — | | |
| | | 6.0 | 21 | — | — | 26 | — | | |
| Hold time | $t_h$ | 2.0 | 0 | — | — | 0 | — | ns | |
| | | 4.5 | 0 | –7 | — | 0 | — | | |
| | | 6.0 | 0 | — | — | 0 | — | | |
| Removal time | $t_{rem}$ | 2.0 | 100 | — | — | 125 | — | ns | |
| | | 4.5 | 20 | 7 | — | 25 | — | | |
| | | 6.0 | 17 | — | — | 21 | — | | |
| Pulse width | $t_w$ | 2.0 | 80 | — | — | 100 | — | ns | |
| | | 4.5 | 16 | 6 | — | 20 | — | | |
| | | 6.0 | 14 | — | — | 17 | — | | |
| Output rise/fall time | $t_{TLH}$, $t_{THL}$ | 2.0 | — | — | 75 | — | 95 | ns | |
| | | 4.5 | — | 5 | 15 | — | 19 | | |
| | | 6.0 | — | — | 13 | — | 16 | | |
| Input capacitance | Cin | — | — | — | 5 | 10 | — | 10 | pF | |

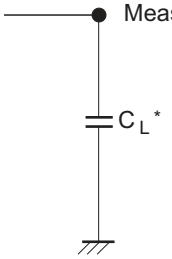
## Function Table

### Count Enable/Disable

| Control Inputs | | | Result at Outputs | |
|---|---|---|---|---|
| $\overline{\text{Load}}$ | Enable P | Enable T | $Q_A$ to $Q_D$ | Ripple Carry Output |
| H | H | H | Count | High when $Q_A$ to $Q_D$ are maximum |
| L | H | H | No count | |
| X | L | H | No count | High when $Q_A$ to $Q_D$ are maximum |
| X | H | L | No count | L |
| X | L | L | No count | L |

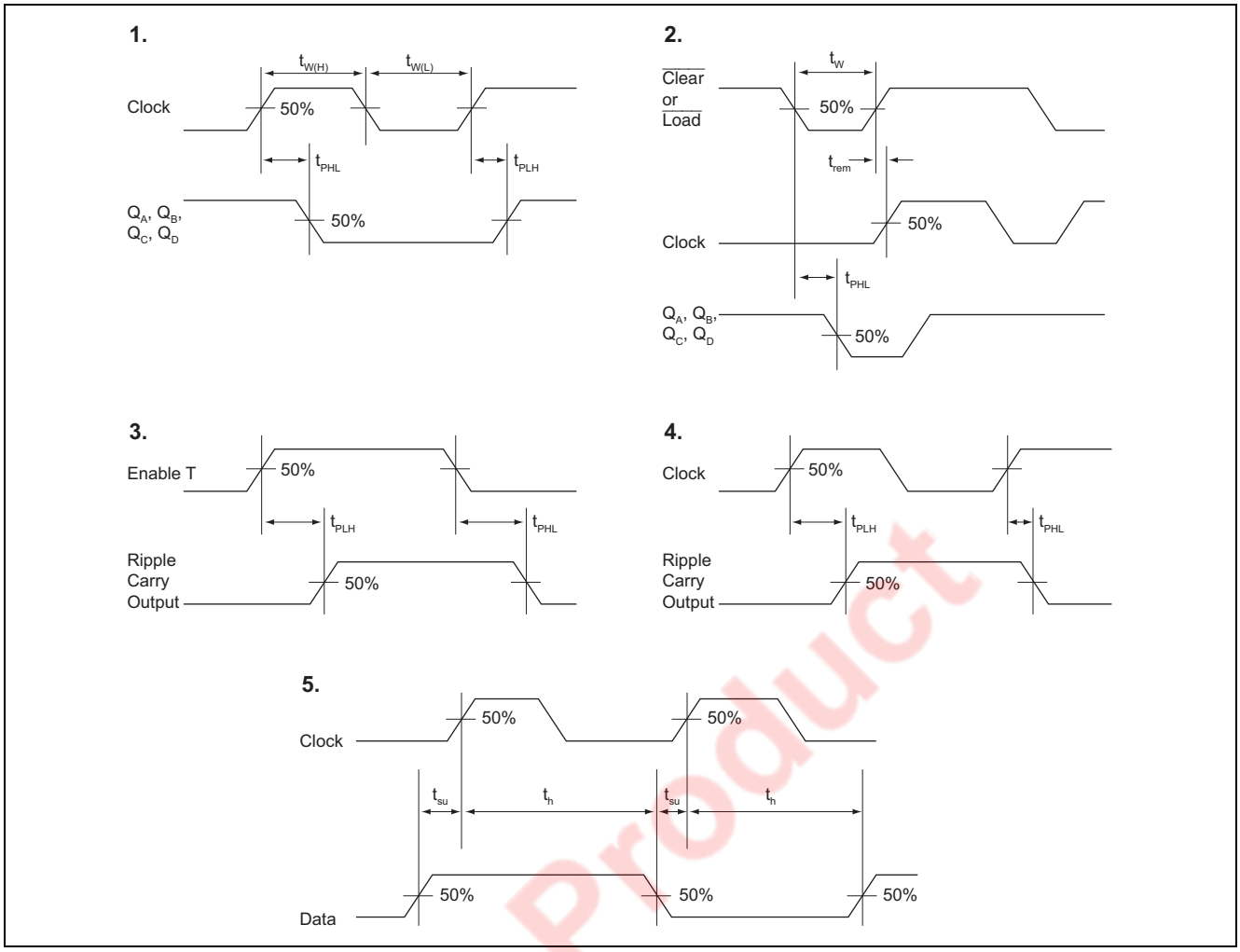
H : High level L : Low level X : Irrelevant

## Test Circuit



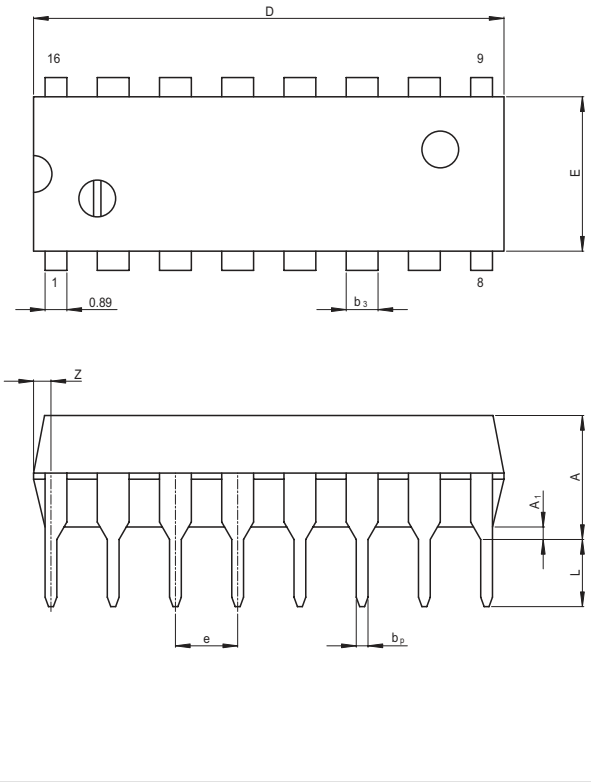

Note: $C_L$ includes the probe and fig capacitance.

## Waveforms



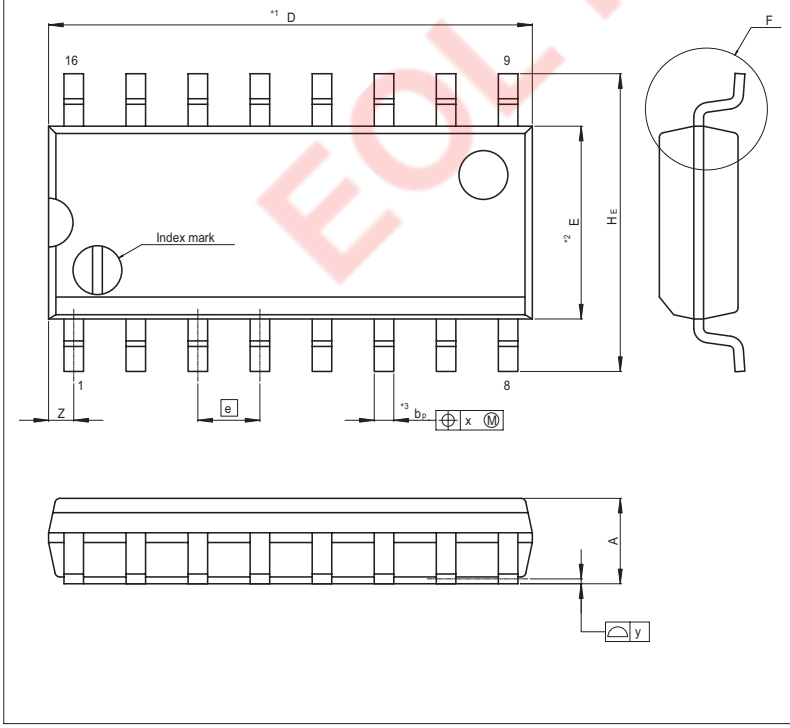
## Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-DIP16-6.3x19.2-2.54 | PRDP0016AE-B | DP-16FV | 1.05g |

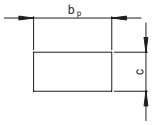



| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| e 1 | —— | 7.62 | —— |
| D | —— | 19.2 | 20.32 |
| E | —— | 6.3 | 7.4 |
| A | —— | —— | 5.06 |
| A 1 | 0.51 | —— | —— |
| b p | 0.40 | 0.48 | 0.56 |
| b 3 | —— | 1.30 | —— |
| c | 0.19 | 0.25 | 0.31 |
| θ | 0° | —— | 15° |
| e | 2.29 | 2.54 | 2.79 |
| Z | —— | —— | 1.12 |
| L | 2.54 | —— | —— |

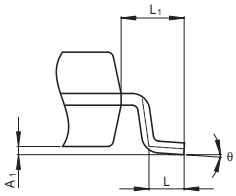
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SOP16-3.95x9.9-1.27 | PRSP0016DG-A | FP-16DNV | 0.15g |




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



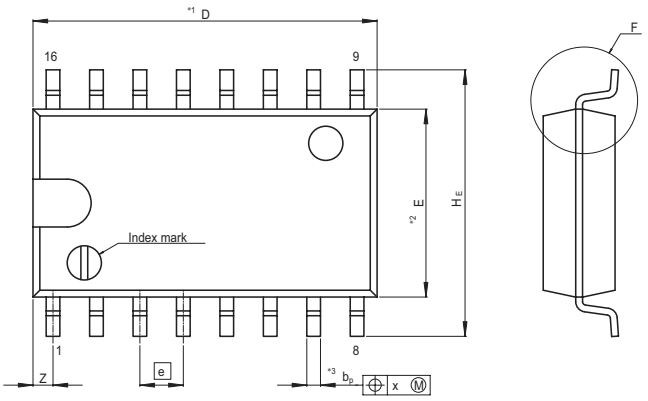

Terminal cross section
( Ni/Pd/Au plating )



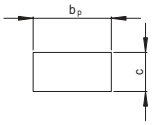

Detail F

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | —— | 9.90 | 10.30 |
| E | —— | 3.95 | —— |
| A 2 | —— | —— | —— |
| A 1 | 0.10 | 0.14 | 0.25 |
| A | —— | —— | 1.75 |
| b p | 0.34 | 0.40 | 0.46 |
| b 1 | —— | —— | —— |
| c | 0.15 | 0.20 | 0.25 |
| c 1 | —— | —— | —— |
| θ | 0° | —— | 8° |
| H E | 5.80 | 6.10 | 6.20 |
| e | —— | 1.27 | —— |
| x | —— | —— | 0.25 |
| y | —— | —— | 0.15 |
| Z | —— | —— | 0.635 |
| L | 0.40 | 0.60 | 1.27 |
| L 1 | —— | 1.08 | —— |

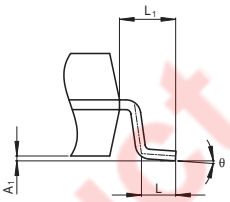
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SOP16-5.5x10.06-1.27 | PRSP0016DH-B | FP-16DAV | 0.24g |




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



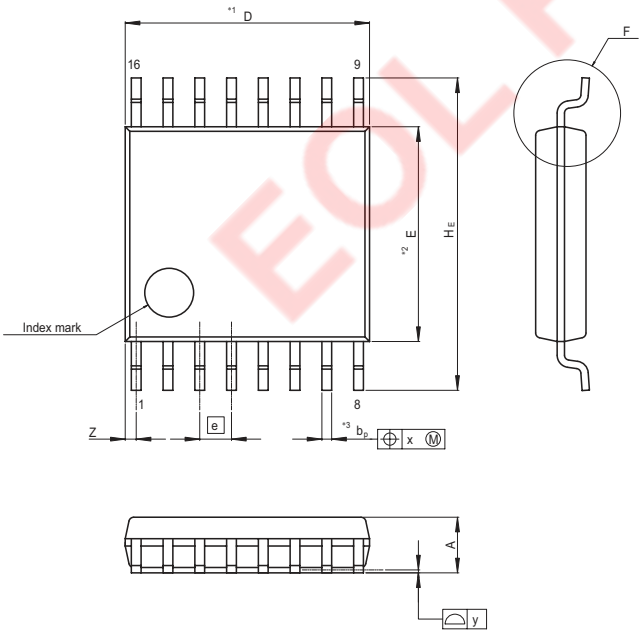

Terminal cross section
( Ni/Pd/Au plating )



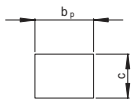

Detail F

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 10.06 | 10.5 |
| E | — | 5.50 | — |
| $A_2$ | — | — | — |
| $A_1$ | 0.00 | 0.10 | 0.20 |
| A | — | — | 2.20 |
| $b_p$ | 0.34 | 0.40 | 0.46 |
| $b_1$ | — | — | — |
| c | 0.15 | 0.20 | 0.25 |
| $c_1$ | — | — | — |
| θ | 0° | — | 8° |
| $H_E$ | 7.50 | 7.80 | 8.00 |
| e | — | 1.27 | — |
| x | — | — | 0.12 |
| y | — | — | 0.15 |
| Z | — | — | 0.80 |
| L | 0.50 | 0.70 | 0.90 |
| $L_1$ | — | 1.15 | — |

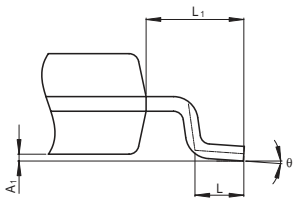
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TSSOP16-4.4x5-0.65 | PTSP0016JB-A | TTP-16DAV | 0.05g |




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.




Terminal cross section
( Ni/Pd/Au plating )




Detail F

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 5.0 | 5.3 |
| E | — | 4.40 | — |
| $A_2$ | — | — | — |
| $A_1$ | 0.03 | 0.07 | 0.10 |
| A | — | — | 1.10 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | — | — |
| c | 0.10 | 0.15 | 0.20 |
| $c_1$ | — | — | — |
| θ | 0° | — | 8° |
| $H_E$ | 6.20 | 6.40 | 6.60 |
| e | — | 0.65 | — |
| x | — | — | 0.13 |
| y | — | — | 0.10 |
| Z | — | — | 0.65 |
| L | 0.4 | 0.5 | 0.6 |
| $L_1$ | — | 1.0 | — |

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## RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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Colophon .3.0