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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

## TFT Display Module

Part Number

E30RA-I-MW400-N

### Overview:

- 3.0-inch TFT (42.04x73.67 I I)
- 480x854 i
- 2-lane MIPI DSI Interface
- ° C
- All View
- Transmissive, IPS
- No Touch Panel
- 400 nits
- TFT IC: ST7701S
- RoHS Compliant

## Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT LCD Panel, driver circuit and a backlight unit. The resolution of the 3.0" TFT LCD contains 480(RGB)x854 pixels and can display up to 16.7M colors.

## TFT Features

Low Input Voltage: 3.3V

Display Colors: 16.7M

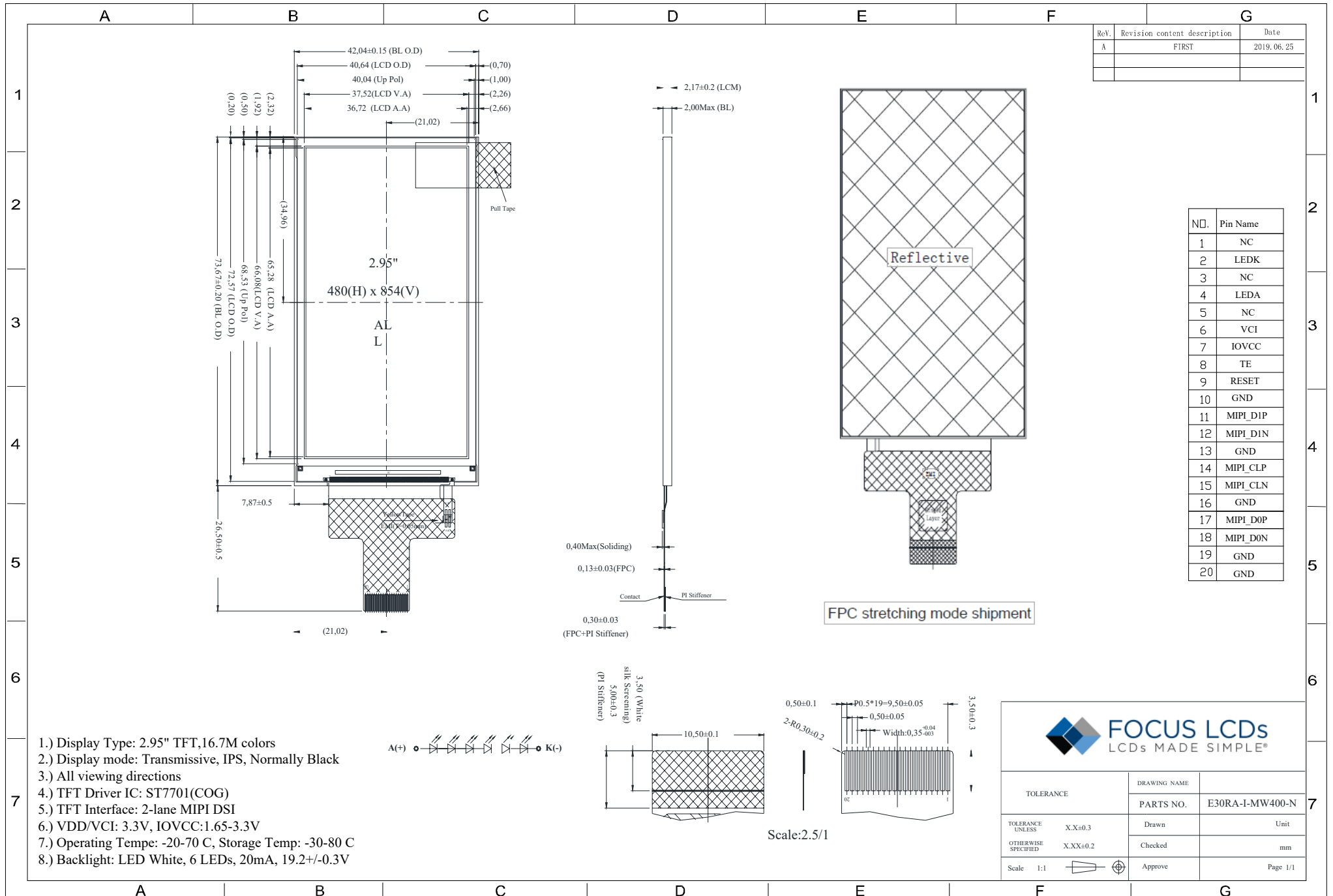
Interface: 2-lane MIPI DSI

| General Information Items | Specification                   | Unit    | Note |
|---------------------------|---------------------------------|---------|------|
|                           | Main Panel                      |         |      |
| TFT Display area (AA)     | 36.72(H) x 65.28(V) (2.95 inch) | mm      | -    |
| Driver Element            | TFT active matrix               | -       | -    |
| Display Colors            | 16.7M                           | colors  | -    |
| Number of pixels          | 480(RGB)x854                    | pixels  | -    |
| TFT Pixel arrangement     | RGB vertical stripe             | -       | -    |
| Pixel Pitch               | 0.0765(H)x0.07644(V)            | mm      | -    |
| Viewing angle             | All                             | o'clock | -    |
| TFT Controller IC         | ST7701S                         | -       | -    |
| TFT Interface             | 2-lane MIPI                     | -       | -    |
| Display mode              | Transmissive/ Normally Black    | -       | -    |
| Operating temperature     | -20-+70                         | °C      | -    |
| Storage temperature       | -30-+80                         | °C      | -    |

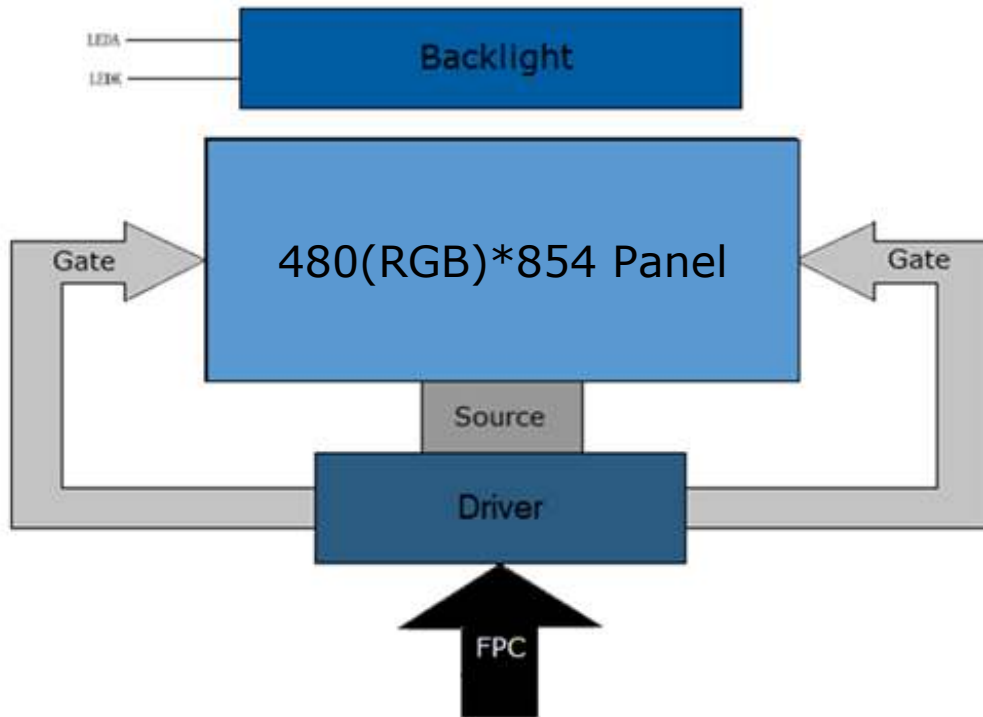
## Mechanical Information

| Item        |                | Min | Typ.  | Max | Unit | Note |
|-------------|----------------|-----|-------|-----|------|------|
| Module Size | Horizontal (H) |     | 42.04 |     | mm   | -    |
|             | Vertical (V)   |     | 73.67 |     | mm   | -    |
|             | Depth (D)      |     | 2.17  |     | mm   | -    |
|             | Weight         |     | 10    |     | g    | -    |

# 1. Outline Dimensions



## 2. Block Diagram



### 3. Input Terminal Pin Assignment

Recommended TFT Connector: FH19C-20S-0.5SH(10)

| NO. | Symbol | Description  | I/O |
|-----|--------|--|-----|
| 1   | NC     | Not connected  |     |
| 2   | LEDK   | Cathode pin of the backlight                               | P   |
| 3   | NC     | Not connected  |     |
| 4   | LEDA   | Anode pin of the backlight                                 | P   |
| 5   | NC     | Not connected  |     |
| 6   | VCI    | Supply voltage (3.3V)                                      | P   |
| 7   | IOVCC  | I/O power supply voltage (1.65-3.3V)                       | P   |
| 8   | TE     | Tearing effect output                                      | O   |
| 9   | RESET  | External reset signal. Initializes the chip at active low. | I   |
| 10  | GND    | Ground   | P   |
| 11  | D1P    | MIPI DSI differential data pair lane 1                     | I/O |
| 12  | D1N    |  |     |
| 13  | GND    | Ground   | P   |
| 14  | CLKP   | MIPI DSI differential clocking pair                        | I/O |
| 15  | CLKN   |  |     |
| 16  | GND    | Ground   | P   |
| 17  | D0P    | MIPI DSI differential data pair lane 0                     | I/O |
| 18  | D0N    |  |     |
| 19  | GND    | Ground   | P   |
| 20  | GND    | Ground   | P   |

*I: Input, O: Output, P: Power*

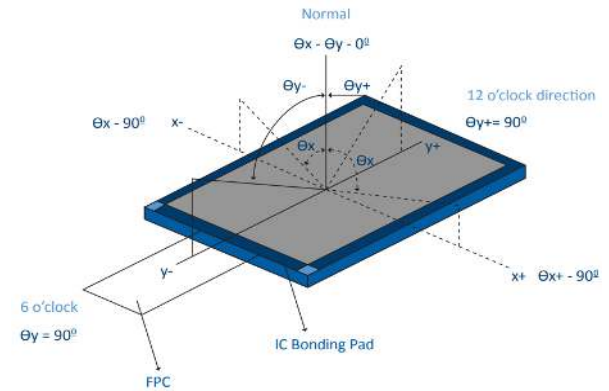
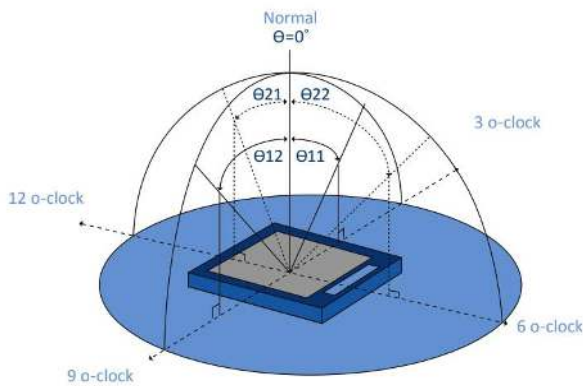
## 4. LCD Optical Characteristics

### 4.1 Optical Specifications

| Item                      | Symbol  | Condition                             | Min    | Typ.   | Max    | Unit    | Note   |        |
|---------------------------|---------|---------------------------------------|--------|--------|--------|---------|--------|--------|
| Color Gamut               | S%      | $\theta=0$<br>Normal viewing<br>angle | 49     | 54     | --     | %       | (3)    |        |
| Contrast Ratio            | CR      |                                       | 1000   | 1500   | --     | %       | (2)    |        |
| Response Time             | Rising  |                                       | TR+TF  | --     | 25     | 35      | ms     | (4)    |
|                           | Falling |                                       |        |        |        |         |        |        |
| Color Filter Chromaticity | White   |                                       | $W_X$  | 0.2669 | 0.3069 | 0.3469  |        | (5)(6) |
|                           |         |                                       | $W_Y$  | 0.2937 | 0.3337 | 0.3737  |        |        |
|                           | Red     |                                       | $R_X$  | 0.5499 | 0.6099 | 0.6499  |        |        |
|                           |         |                                       | $R_Y$  | 0.3301 | 0.3701 | 0.4101  |        |        |
|                           | Green   |                                       | $G_X$  | 0.2917 | 0.3317 | 0.3717  |        |        |
|                           |         |                                       | $G_Y$  | 0.5291 | 0.5691 | 0.6097  |        |        |
|                           | Blue    | $B_X$                                 | 0.1078 | 0.1478 | 0.1878 |         |        |        |
|                           |         | $B_Y$                                 | 0.0467 | 0.0867 | 0.1267 |         |        |        |
| Viewing Angle             | Hor.    | $\Theta_L$                            | 80     | 85     | --     | degrees | (1)(6) |        |
|                           |         | $\Theta_R$                            | 80     | 85     | --     |         |        |        |
|                           | Ver.    | $\Theta_T$                            | 80     | 85     | --     |         |        |        |
|                           |         | $\Theta_B$                            | 80     | 85     | --     |         |        |        |
| Option View Direction     | All     |                                       |        |        |        |         | (1)    |        |

**Optical Specification Reference Notes:**

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.

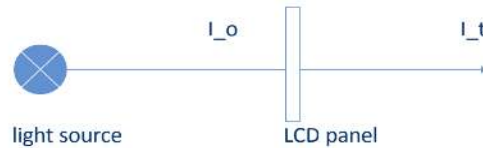


(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{L_w}{L_d}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving. The equation for transmittance Tr is:

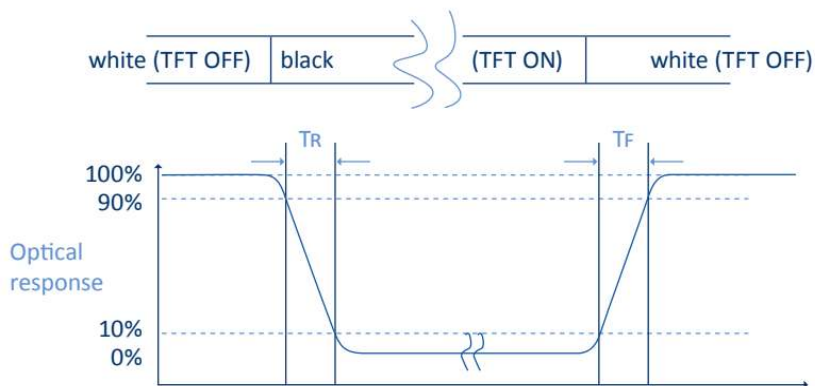
$$Tr = \frac{I_t}{I_o} \times 100\%$$



I<sub>o</sub> = the brightness of the light source.

I<sub>t</sub> = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut:

Measuring machine CFT-01. NTSC's Primaries:  $R(x,y,Y), G(x,y,Y), B(x,y,Y)$ . FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics. The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

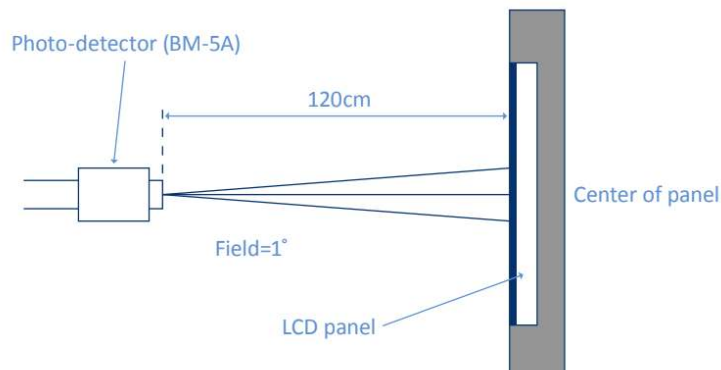
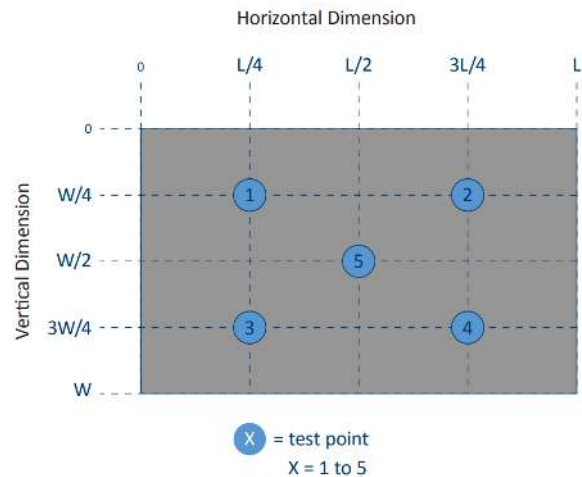
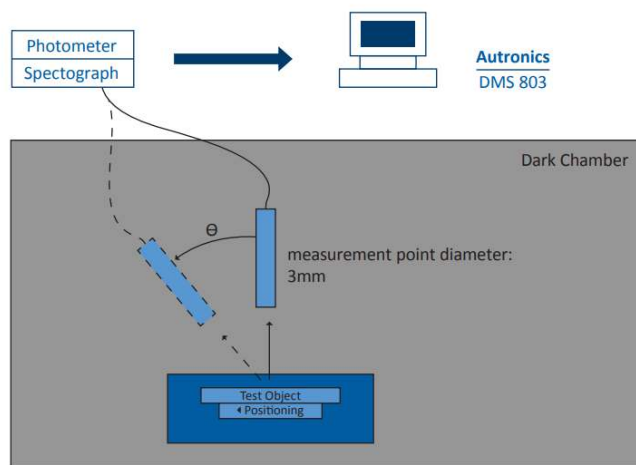


Fig. 1931 CIE chromacity diagram

$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

(6) Definition of Optical Measurement Setup:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.





## 5. TFT Electrical Characteristics

### 5.1 Absolute Maximum Rating (Ta=25 °C, VSS=0V)

| Characteristics        | Symbol | Min  | Max | Unit |
|------------------------|--------|------|-----|------|
| Digital Supply Voltage | VCI    | -0.3 | 4.6 | V    |
| DC/DC Supply Voltage   | IOVCC  | -0.3 | 4.6 |      |
| Operating Temperature  | TOP    | -20  | +70 | °C   |
| Storage Temperature    | TST    | -30  | +80 | °C   |

*NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.*

### 5.2 DC Electrical Characteristics

| Characteristics        | Symbol | Min      | Typ. | Max      | Unit | Note |
|------------------------|--------|----------|------|----------|------|------|
| Power Supply Voltage   | VCI    | 2.5      | 3.3  | 3.6      | V    |      |
| Digital Supply Voltage | IOVCC  | 1.65     | 1.8  | 3.6      | V    |      |
| Normal Mode Current    | IDD    | --       | 38   | --       | mA   |      |
| Level Input Voltage    | VIH    | 0.7IOVCC | --   | IOVCC    | V    |      |
|                        | VIL    | GND      | --   | 0.3IOVCC | V    |      |
| Level Output Voltage   | VOH    | 0.8IOVCC | --   | IOVCC    | V    |      |
|                        | VOL    | GND      | --   | 0.2IOVCC | V    |      |

## 5.4 LED Backlight Characteristics

| Item            | Symbol | Min | Typ.  | Max | Unit              | Note      |
|-----------------|--------|-----|-------|-----|-------------------|-----------|
| Forward Current | IF     | 15  | 20    | --  | mA                |           |
| Forward Voltage | VF     | --  | 19.2  | --  | V                 |           |
| LCM Luminance   | LV     | 350 | 400   | --  | cd/m <sup>2</sup> | Note 3    |
| LED lifetime    | Hr     | --  | 50000 | --  | hour              | Note1 & 2 |
| Uniformity      | AVg    | 80  | --    | --  | %                 | Note 3    |

The back-light system is edge-lighting type with 6 white LEDs.

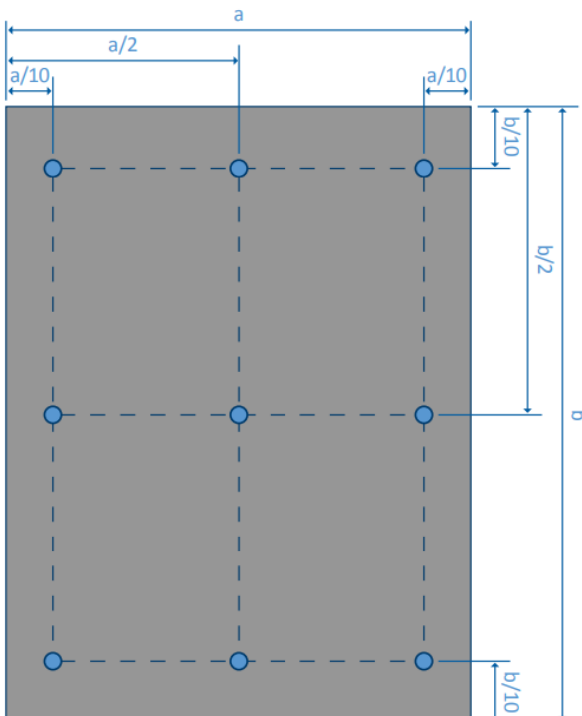
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition:  $T_a=25\pm 3\text{ }^\circ\text{C}$ , typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED lifetime” is defined as the module brightness decrease to 50% original brightness at  $T_a=25^\circ\text{C}$  and  $I_L=20\text{mA}$ . The LED lifetime could be decreased if operating  $I_L$  is larger than 20mA. The constant current driving method is suggested.



Backlight LED Circuit

Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

## 6. MIPI Interface AC Characteristics

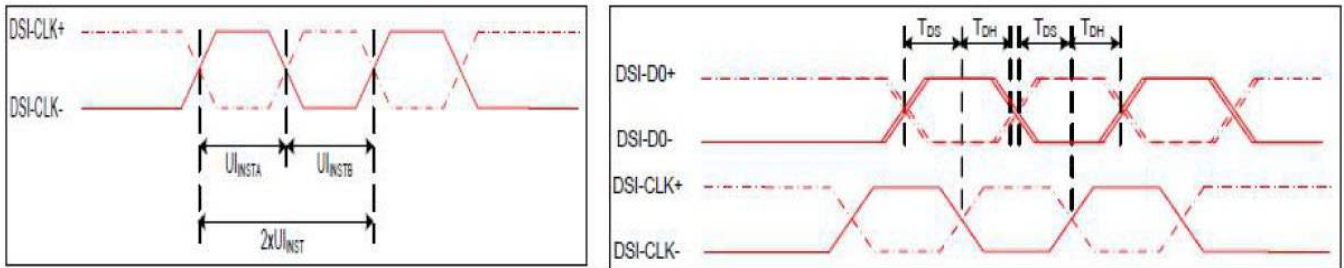


Figure 6.1: DSI Clock Channel Timing Diagram

| Signal     | Symbol                       | Parameter                | Min  | Max  | Unit | Note                           |
|------------|------------------------------|--------------------------|------|------|------|--------------------------------|
| DSI-CLK+/- | $2 \times UI_{INSTA}$        | Double UI Instantaneous  | 4    | 25   | ns   |                                |
| DSI-CLK+/- | $UI_{INSTA}$<br>$UI_{INSTB}$ | UI Instantaneous Halves  | 2    | 12.5 | ns   | $UI = UI_{INSTA} = UI_{INSTB}$ |
| DSI-Dn+/-  | $t_{DS}$                     | Data to clock setup time | 0.15 | --   | UI   |                                |
| DSI-Dn+/-  | $t_{DH}$                     | Data to clock hold time  | 0.15 | --   | UI   |                                |

Table 6.1: MIPI Interface High Speed Mode Timing Characteristics

## 6.2 Low Power Mode

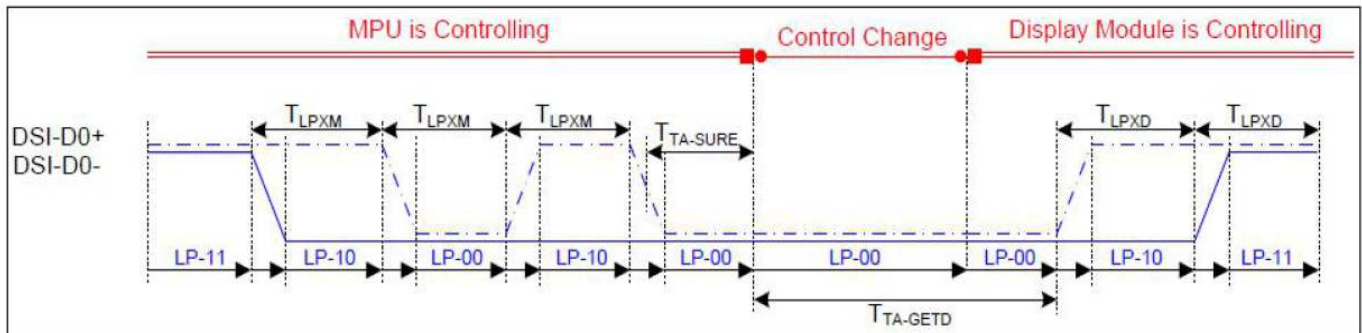


Figure 6.2: Bus Turnaround (BTA) from Display Module to MPU Timing Diagram

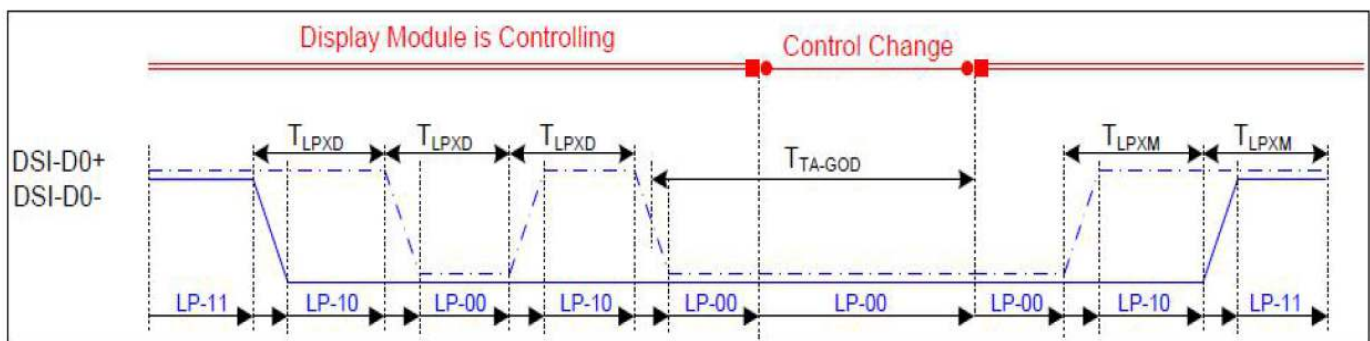


Figure 6.3: Bus Turnaround (BTA) from MPU to Display Module Timing Diagram

| Signal    | Symbol    | Parameter   | Min     | Max     | Unit | Note   |
|-----------|-----------|---|---------|---------|------|--------|
| DSI-D0+/- | TLPXM     | Length of LP-00, LP_01, LP-10 or LP-11 periods MPU-> Display Module | 50      | 75      | ns   | Input  |
| DSI-D0+/- | TLPXD     | Length of LP-00, LP_01, LP-10 or LP-11 periods MPU-> Display Module | 50      | 75      | ns   | Output |
| DSI-D0+/- | TTA-SURED | Time-out before the MPU starts driving                              | TLPXD   | 2xTLPXD | ns   | Output |
| DSI-D0+/- | TTA-GETD  | Time to drive LP-00 by display module                               | 5xTLPXD |         | ns   | Input  |
| DSI-D0+/- | TTA-GOD   | Time to drive LP-00 after turnaround request-MPU                    | 4xTLPXD |         | ns   | Output |

Table 6.2: MIPI Interface Low Power Mode Timing Characteristics

### 6.3 Bursts Mode

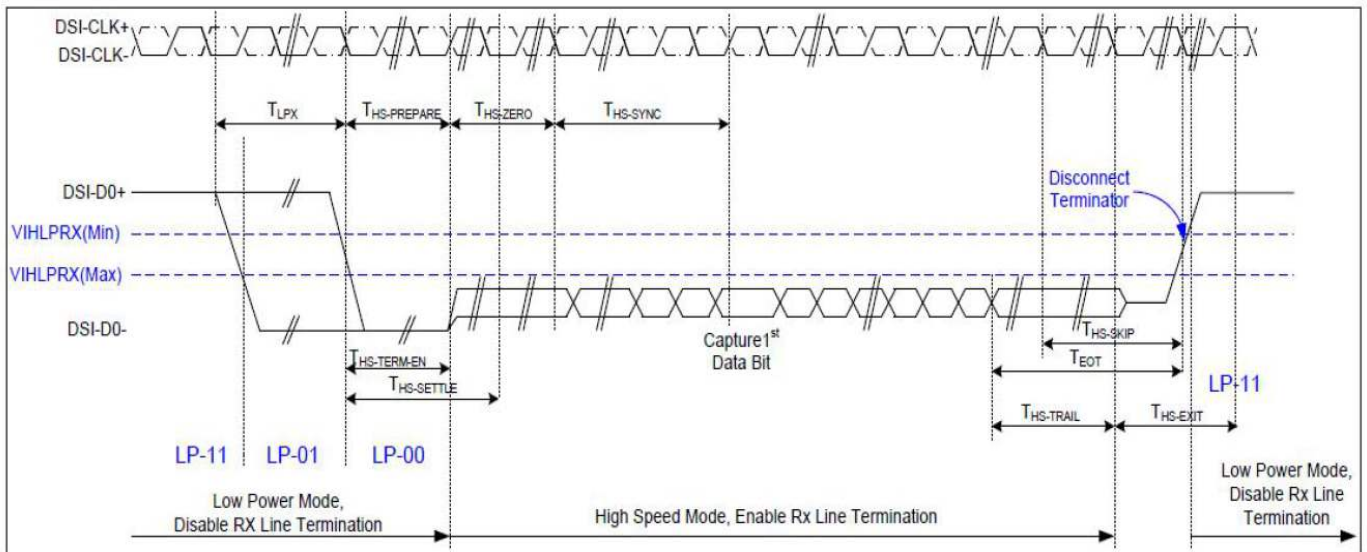


Figure 6.4: Data Lanes Low Power Mode to/from High Speed Mode Timing Diagram

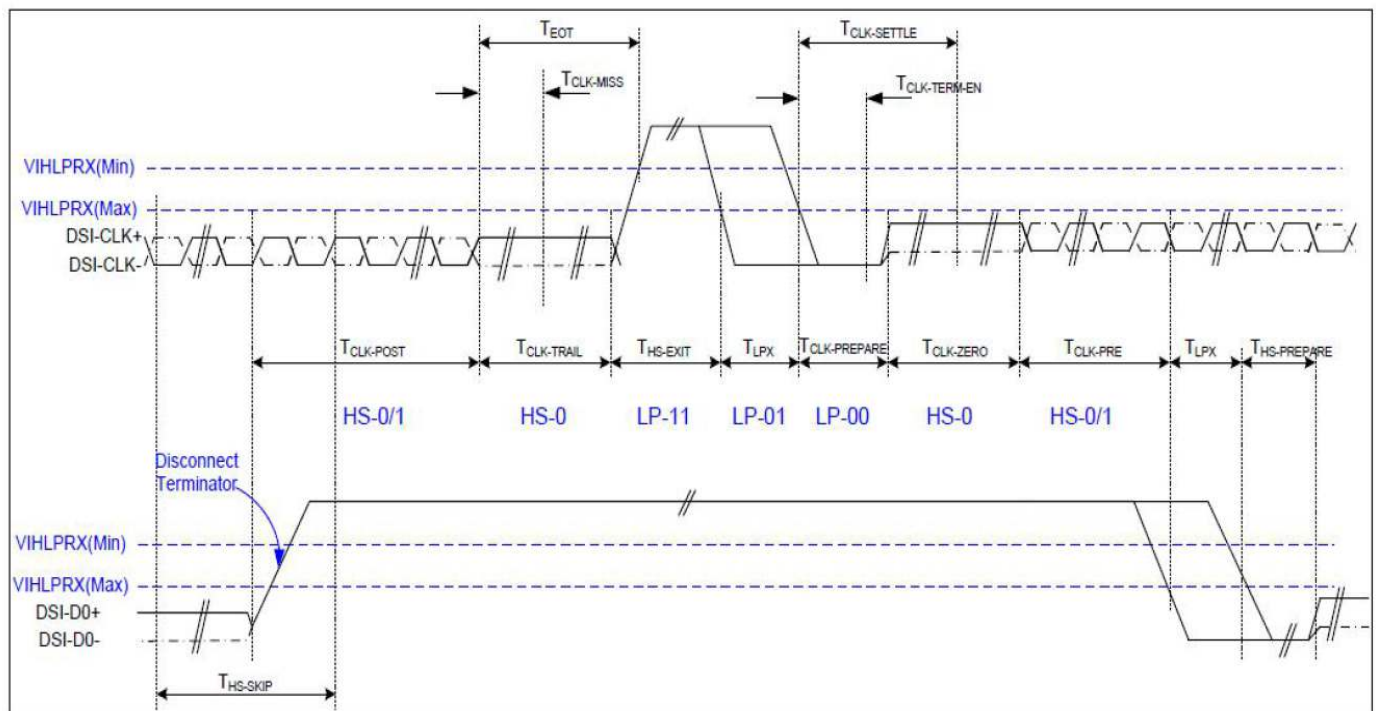


Figure 6.5: Clock Lanes High Speed Mode to/from Low Power Mode Timing Diagram

| Signal  | Symbol                     | Parameter  | Min      | Max      | Unit | Note  |
|---|----------------------------|--|----------|----------|------|-------|
| Low Power Mode to High Speed Mode Timing      |                            |  |          |          |      |       |
| DSI-Dn+/-                                     | TLPX                       | Length of any low power state period   | 50       | --       | ns   | Input |
| DSI-Dn+/-                                     | THS-PREPARE                | Time to drive LP-00 to prepare for HS transmission   | 40+4UI   | 85+6UI   | ns   | Input |
| DSI-Dn+/-                                     | THS-TERM-EN                | Time to enable data receiver line termination measured from when Dn crosses VILMAX                                   | --       | 35+4UI   | ns   | Input |
| DSI-Dn+/-                                     | THS-PREPARE+<br>THS-ZERO   | THS-PREPARE+time to drive HS-0 before the sync sequence  | 140+10UI | --       | ns   | Input |
| High Speed Mode to Low Power Mode Timing      |                            |  |          |          |      |       |
| DSI-Dn+/-                                     | THS-SKIP                   | Time-out at display module to ignore transition period of EoT  | 40       | 55+4UI   | ns   | Input |
| DSI-Dn+/-                                     | THS-EXIT                   | Time to drive LP-11 after HS burst   | 100      | --       | ns   | Input |
| DSI-Dn+/-                                     | THS-TRIAL                  | Time to drive flipped differential state after last payload data bit of a HS transmission burst                      | 60+4UI   | --       | ns   | Input |
| High Speed Mode to/from Low Power Mode Timing |                            |  |          |          |      |       |
| DSI-CLK+/-                                    | TCLK-POS                   | Time that the MPU shall continue sending HS clock after the last associated data lane has transitioned to LP mode    | 60+52UI  | --       | ns   | Input |
| DSI-CLK+/-                                    | TCLK-TRAIL                 | Time to drive HS differential state after last payload clock bit of a HS transmission burst                          | 60       | --       | ns   | Input |
| DSI-CLK+/-                                    | THS-EXIT                   | Time to drive LP-11 after HS burst   | 100      | --       | ns   | Input |
| DSI-CLK+/-                                    | TCLK-PREPARE               | Time to drive LP-00 to prepare for HS transmission   | 38       | 95       | ns   | Input |
| DSI-CLK+/-                                    | TCLK-TERM-EN               | Time out at clock and display module to enable HS transmission   | --       | 38       | ns   | Input |
| DSI-CLK+/-                                    | TCLK-PREPARE+<br>TCLK-ZERO | Minimum lead HS-0 drive period before starting clock   | 300      | --       | ns   | Input |
| DSI-CLK+/-                                    | TCLK-PRE                   | Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode | 8UI      | --       | ns   | Input |
| DSI-CLK+/-                                    | TEOT                       | Time from start of TCLK-TRAIL period to start of LP-11 state   | --       | 105+12UI | ns   | Input |

Table 6.3: Bursts Mode LP to/from HS Mode Timing Characteristics



## 6.4 Reset Timing

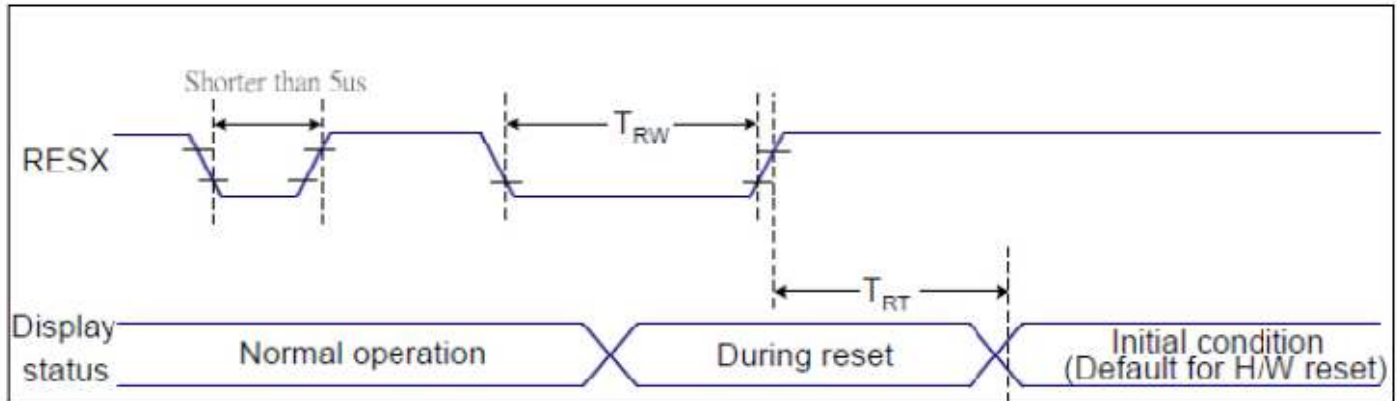


Figure 6.6: Reset Timing Diagram

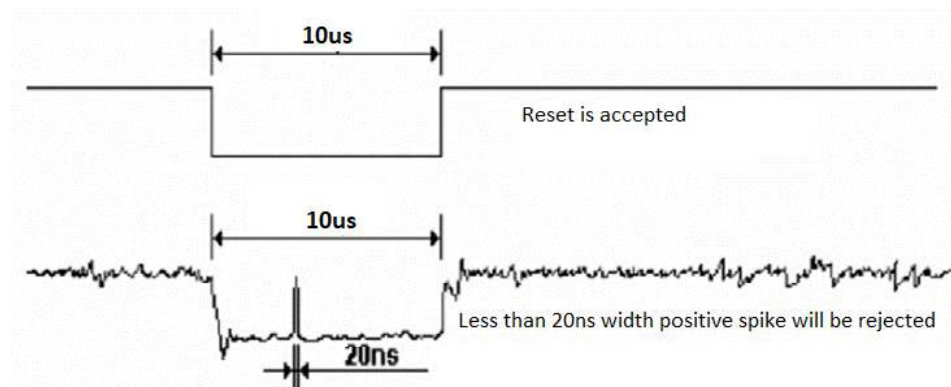
| Related Pins | Symbol | Parameter            | Min | Max                | Unit |
|--------------|--------|----------------------|-----|--------------------|------|
| RESX         | TRW    | Reset pulse duration | 10  | -                  | us   |
|              | TRT    | Reset cancel         | -   | 5 (Note 1,5)       | ms   |
|              |        |                      |     | 120 (Note 1, 6, 7) | ms   |

Notes:

- The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time ( $t_{RT}$ ) within 5ms after a rising edge of RESX.
- Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

| RESX Pulse           | Action         |
|----------------------|----------------|
| Shorter than 5us     | Reset Rejected |
| Longer than 9us      | Reset          |
| Between 5us and 9 us | Reset starts   |

- During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.
- Spike Rejection also applies during a valid reset pulse as shown below:



- When Reset applied during Sleep In Mode.
- When Reset applied during Sleep Out Mode.
- It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

## **7. Cautions and Handling Precautions**

### **7.1 Handling and Operating the Module**

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

### **7.2 Storage and Transportation.**

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.