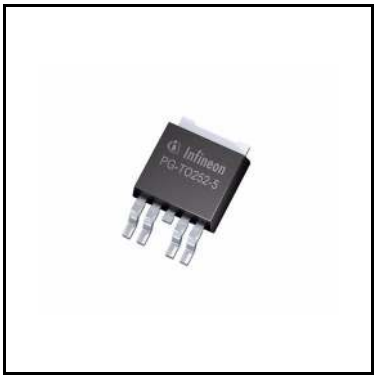
TLS850B0TEV33

Low dropout linear voltage regulator

AEC Qualified RoHS



1 Overview

Features

- Wide input voltage range from 3.0 V to 40 V
- Fixed output voltage 3.3 V
- Output voltage accuracy ≤ ±2 %
- Output current capability up to 500 mA
- Ultra low current consumption, typical 20 µA
- Very low dropout voltage, typical 120 mV at 100 mA
- Stable with ceramic output capacitor of 1 µF
- Enable
- Overtemperature shutdown
- Output current limitation
- Wide temperature range
- Green Product (RoHS compliant)

Potential applications

- Automotive or other supply systems that are connected to the battery permanently
- Automotive supply systems that need to operate in cranking condition

Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100/101

Description

The TLS850B0TEV33 is a high performance, very low dropout linear voltage regulator for 3.3 V supply in a PG-TO252-5 package.

The input voltage range of 3 V to 40 V and a very low quiescent current of 20 µA make it the perfect match for automotive or other supply systems connected to the battery permanently.

The new loop concept combines fast regulation and very high stability. Below an output current of 100 mA the typical dropout voltage is below 100 mV. The operating range starts at an input voltage of only 3 V (extended

operating range). This makes the TLS850B0TEV33 suitable for automotive systems that need to operate during cranking condition.

The device can be switched on and off by the Enable feature.

Internal protection features such as output current limitation and overtemperature shutdown protect the device from immediate damage due to failures such as output shorted to GND, overcurrent and overtemperature.

Choosing external components

An input capacitor C_I is recommended to compensate line influences.

The output capacitor C_Q is necessary for the stability of the regulating circuit. TLS850B0TEV33 is designed to operate stable with low ESR ceramic capacitors.

Type	Package	Marking
TLS850B0TEV33	PG-TO252-5	850B0V33

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2 Block diagram

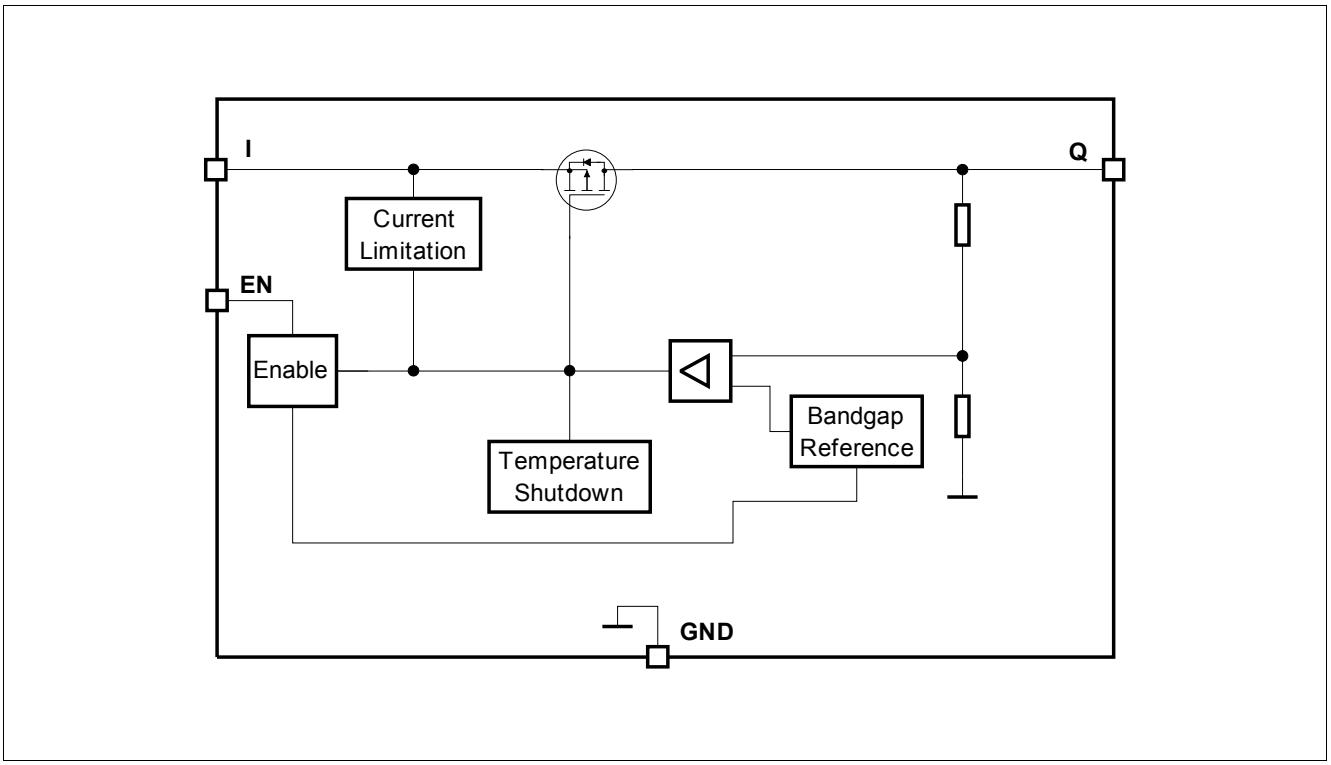


Figure 1 Block diagram TLS850B0TEV33

3 Pin configuration

3.1 Pin assignment TLS850B0TEV33

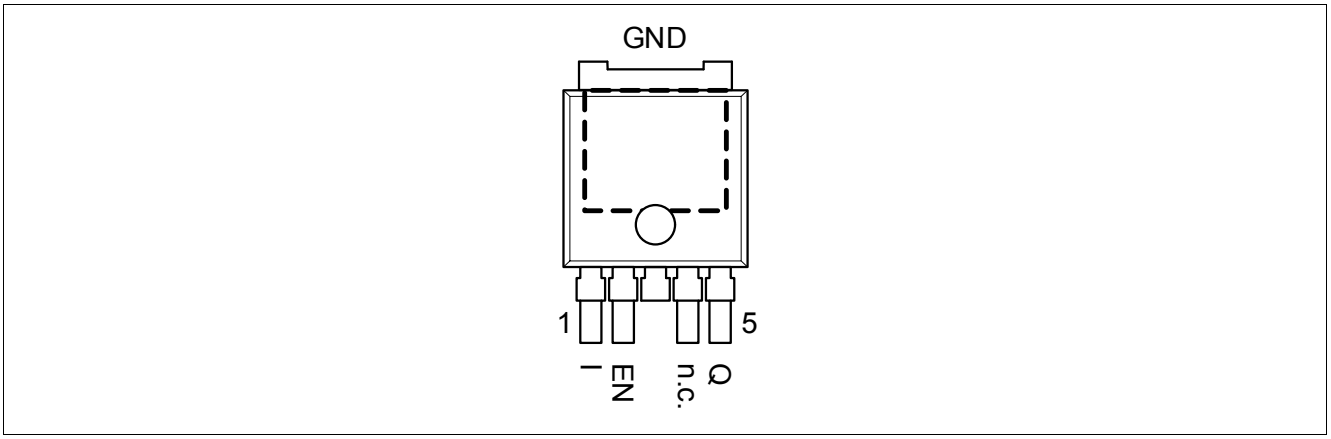


Figure 2 Pin configuration

3.2 Pin definitions and functions TLS850B0TEV33

Pin	Symbol	Function
1	I	**Input** It is recommended to place a small ceramic capacitor (for example 100 nF) to GND, close to the pins, in order to compensate line influences.
2	EN	**Enable** (integrated pull-down resistor) Enable the IC with “high” level input signal; Disable the IC with “low” level input signal;
3	GND	**Ground**
4	n.c.	**Not connected** Leave open or connect to GND
5	Q	**Output** Connect output capacitor C_Q to GND close to the pin, respecting the values specified for its capacitance and ESR in **“Functional range” on Page 7**.
Heat Slug	GND	**Heat Slug** Connect to GND Connect to heatsink area

4 General product characteristics

4.1 Absolute maximum ratings

Table 1 Absolute maximum ratings[1)]

T_j = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I, Enable EN							
Voltage	V_I, V_{EN}	-0.3	–	45	V	–	P_4.1.1
Output Q							
Voltage	V_Q	-0.3	–	7	V	–	P_4.1.2
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.3
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.4
ESD absorption							
ESD susceptibility to GND	V_{ESD}	-2	–	2	kV	[2)] HBM	P_4.1.5
ESD susceptibility to GND	V_{ESD}	-500	–	500	V	[3)] CDM	P_4.1.6
ESD susceptibility of Corner Pins to GND	$V_{ESD1,7}$	-750	–	750	V	[3)] CDM	P_4.1.7

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
3) ESD susceptibility, Charged Device Model (CDM) according to JEDEC JESD22-C101

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent device destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional range

Table 2 Functional range

T_j = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range	V_I	$V_{Q,nom} + V_{dr}$	–	40	V	1) –	P_4.2.1
Extended input voltage range	$V_{I,ext}$	3.0	–	40	V	2) –	P_4.2.2
Enable voltage range	V_{EN}	0	–	40	V	–	P_4.2.3
Output capacitor's requirements for stability	C_Q	1	–	–	µF	3)4) –	P_4.2.4
ESR	$ESR(C_Q)$	–	–	50	Ω	3) –	P_4.2.5
ESR	$ESR(C_Q)$	–	–	100	Ω	3) V_{IN} < 25 V	P_4.2.5
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.6

1) Output current is limited internally and depends on the input voltage, see Electrical Characteristics for more details.
2) If $V_{I,ext,min} \le V_I \le V_{Q,nom} + V_{dr}$, then $V_Q = V_I - V_{dr}$. If $V_I < V_{I,ext,min}$, then V_Q can drop to 0 V.
3) Not subject to production test, specified by design.
4) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

Note: Within the functional or operating range, the device operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal ResistancePG-TO252-5

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	3.1	–	K/W	1) –	P_4.3.6
Junction to ambient	R_{thJA}	–	26	–	K/W	1)2) 2s2p board	P_4.3.7
Junction to ambient	R_{thJA}	–	85	–	K/W	1)3) 1s0p board, footprint only	P_4.3.8
Junction to ambient	R_{thJA}	–	43	–	K/W	1)3) 1s0p board, 300 mm^2 heatsink area on PCB	P_4.3.9
Junction to ambient	R_{thJA}	–	36	–	K/W	1)3) 1s0p board, 600 mm^2 heatsink area on PCB	P_4.3.10

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip + Package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 x 70 µm Cu).

5 Block description and electrical characteristics

5.1 Voltage regulation

The output voltage V_Q is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and the pass transistor is driven accordingly.

The control loop stability depends on the following factors:

- output capacitor C_Q
- load current
- chip temperature
- internal circuit design

To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor (ESR) requirements given in **"Functional range" on Page 7** must be maintained. Because the output capacitor must buffer load steps, it must be sized according to the requirements of the application.

An input capacitor C_I is recommended to compensate line influences. In order to block influences such as pulses and HF distortion at the input, an additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the component's terminals.

In order to prevent overshoots during start-up, a slope control function is implemented. This significantly reduces output voltage overshoots during start-up, mostly independent from load.

If the load current exceeds the specified limit, for example due to a short circuit, then the TLS850B0TEV33 limits the output current and the output voltage decreases.

The overtemperature shutdown circuit prevents the TLS850B0TEV33 from immediate destruction in fault condition, for example due to a permanent short-circuit at the output, by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, any junction temperature above 150°C is outside the maximum ratings and therefore significantly reduces the life time of the TLS850B0TEV33.

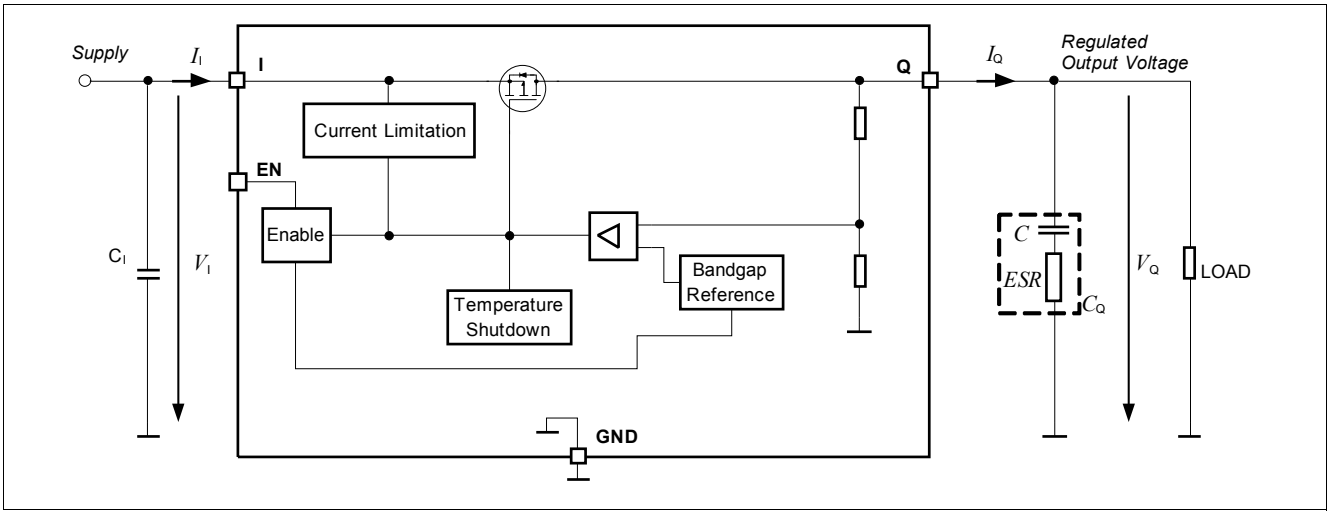


Figure 3 Voltage regulation

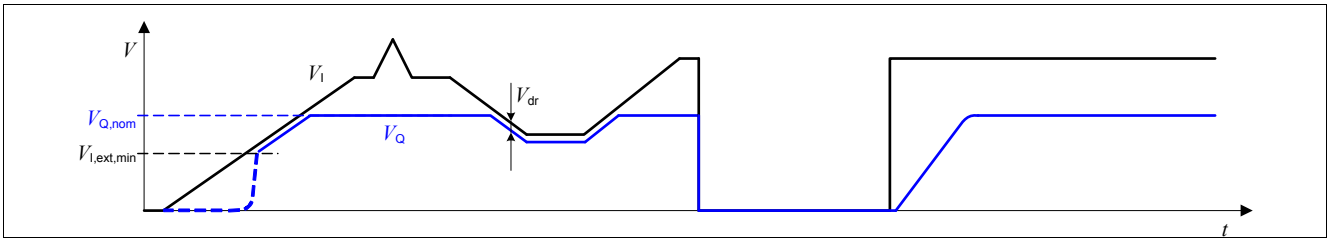


Figure 4 Output voltage vs. input voltage

Table 4 Electrical characteristics voltage regulator 3.3 V version

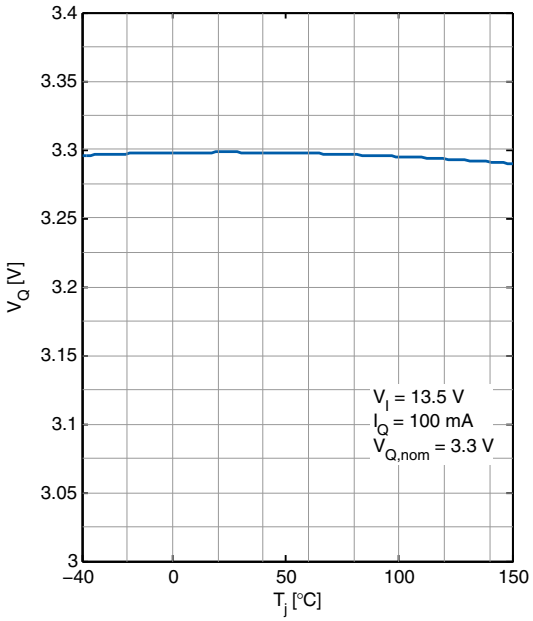
T_j = -40°C to +150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage accuracy	V_Q	3.23	3.3	3.37	V	0.05 mA < I_Q < 500 mA 4.6 V < V_I < 28 V	P_5.1.19
Output voltage accuracy	V_Q	3.23	3.3	3.37	V	0.05 mA < I_Q < 200 mA 3.85 V < V_I < 40 V	P_5.1.20
Output voltage startup slew rate	dV_Q/dt	3.0	35	90	V/ms	V_I > 18 V/ms C_Q = 1 µF 0.33 V < V_Q < 2.97 V	P_5.1.27
Output current limitation	$I_{Q,max}$	501	750	1100	mA	0 V < V_Q < $V_{Q,nom}$ - 0.1 V	P_5.1.28
Load regulation steady-state	$\Delta V_{Q,load}$	-15	-5	–	mV	I_Q = 0.05 mA to 500 mA V_I = 6.5 V	P_5.1.30
Line regulation steady-state	$\Delta V_{Q,line}$	–	1	10	mV	V_I = 8 V to 32 V I_Q = 5 mA	P_5.1.31
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	300	600	mV	[1] I_Q = 250 mA	P_5.1.32
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	120	240	mV	[1] I_Q = 100 mA	P_5.1.33
Power Supply Ripple Rejection	*PSRR*	–	63	–	dB	[2] f_{ripple} = 100 Hz V_{ripple} = 0.5 Vpp	P_5.1.34
Overtemperature shutdown threshold	$T_{j,sd}$	151	–	200	°C	[2] T_j increasing	P_5.1.35
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	15	–	K	[2] T_j decreasing	P_5.1.36

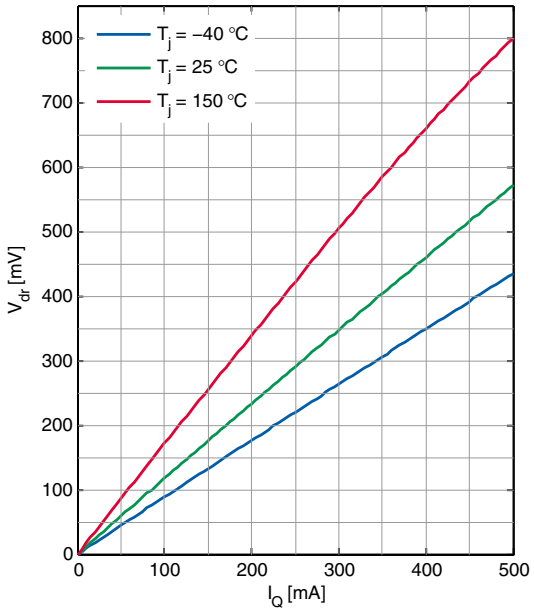
1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V
2) Not subject to production test, specified by design

5.2 Typical performance characteristics voltage regulator

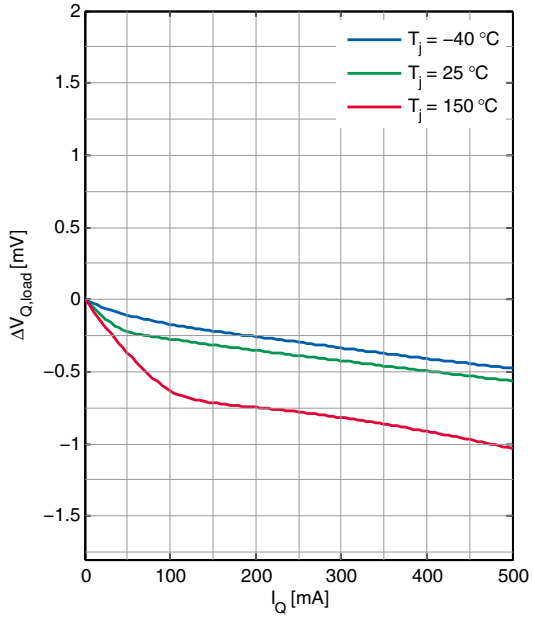
Output voltage V_Q versus junction temperature T_j



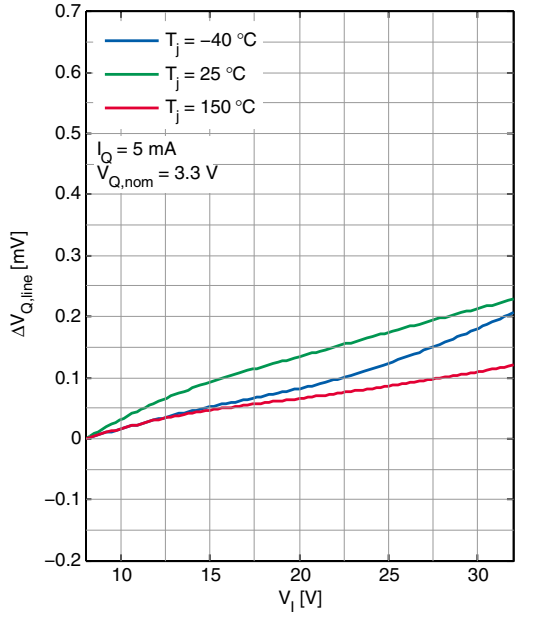
Dropout voltage V_{dr} versus output current I_Q



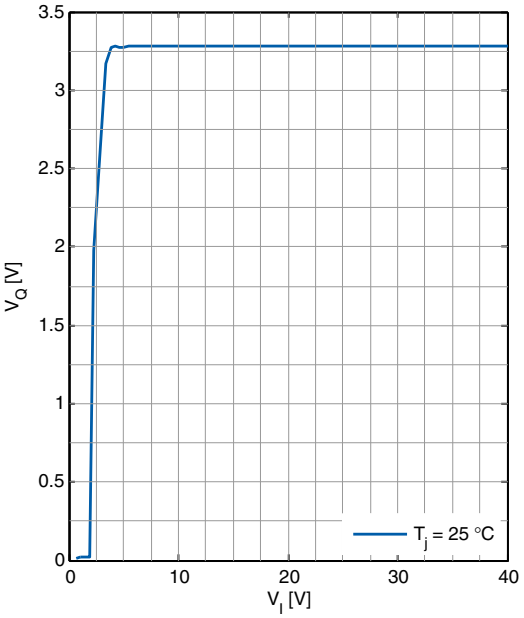
Load regulation $\Delta V_{Q,load}$ versus output current I_Q



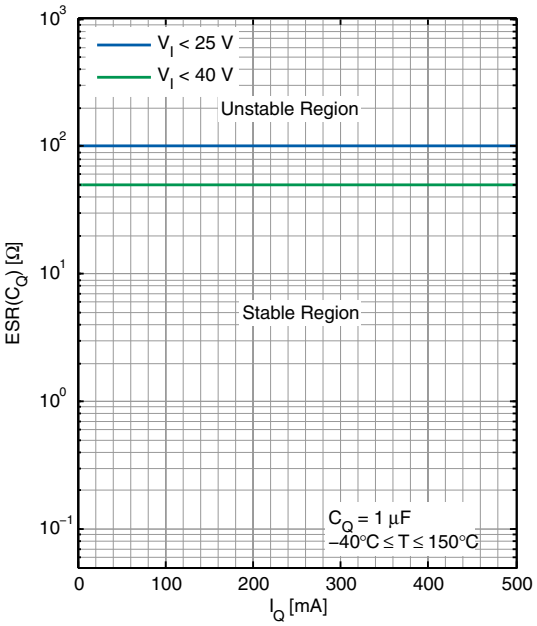
Line regulation $\Delta V_{Q,line}$ versus input voltage V_I



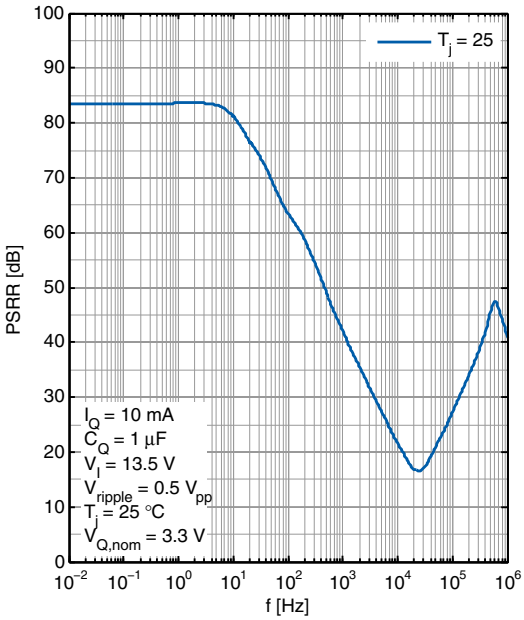
Output voltage V_Q versus input voltage V_I



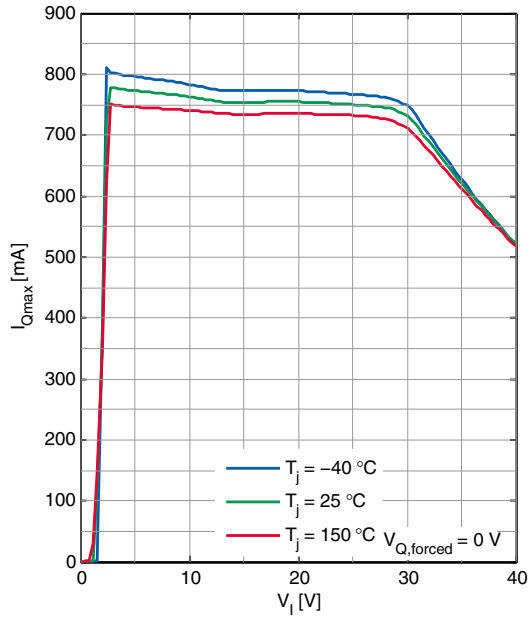
Output capacitor *ESR*(C_Q) versus output current I_Q



Power Supply Ripple Rejection *PSRR* versus ripple frequency *f*



Maximum output current I_Q versus input voltage V_I



5.3 Current consumption

Table 5 Electrical characteristics current consumption

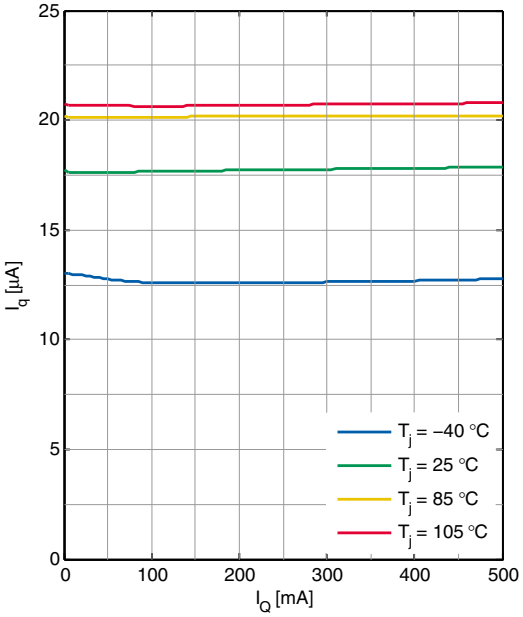
T_j = -40°C to +150°C, V_I = 13.5 V (unless otherwise specified)
Typical values are given at T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption $I_q = I_I$	$I_{q,off}$	–	–	1	µA	V_{EN} = 0 V; T_j < 105°C	P_5.3.1
Current consumption $I_q = I_I$	$I_{q,off}$	–	–	2	µA	V_{EN} = 0.4 V; T_j < 125°C	P_5.3.3
Current consumption $I_q = I_I - I_Q$	I_q	–	20	25	µA	I_Q = 0.05 mA T_j = 25°C	P_5.3.4
Current consumption $I_q = I_I - I_Q$	I_q	–	23	30	µA	I_Q = 0.05 mA T_j < 125°C	P_5.3.5
Current consumption $I_q = I_I - I_Q$	I_q	–	25	33	µA	[1] I_Q = 500 mA T_j < 125°C	P_5.3.6

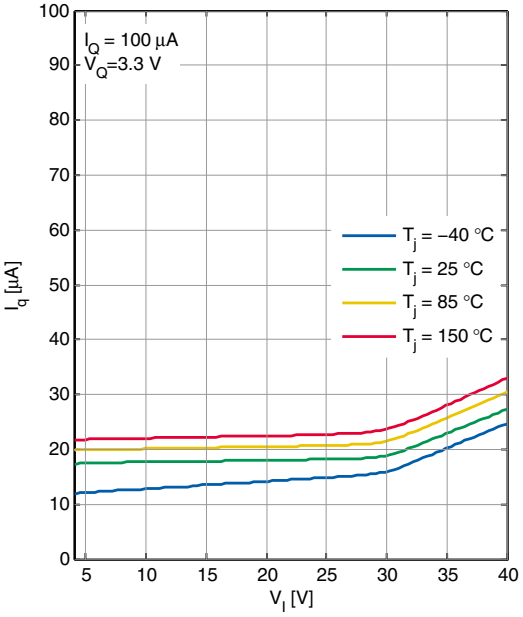
1) Not subject to production test, specified by design

5.4 Typical performance characteristics current consumption

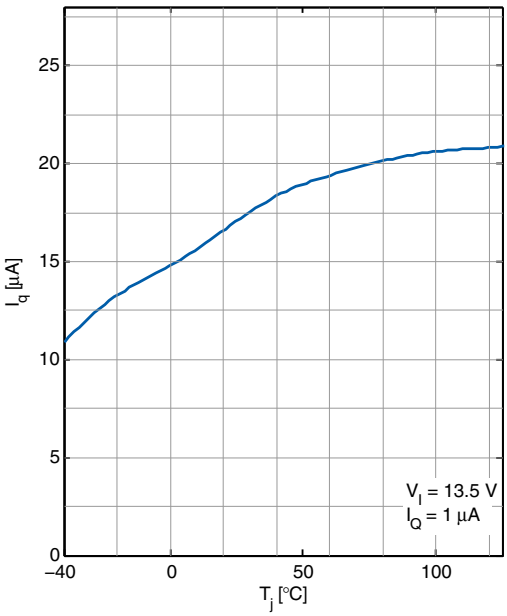
Current consumption I_q versus output current I_Q



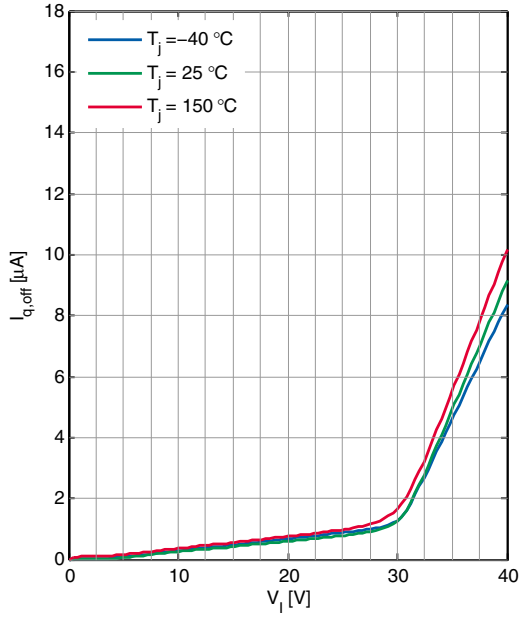
Current consumption I_q versus input voltage V_I



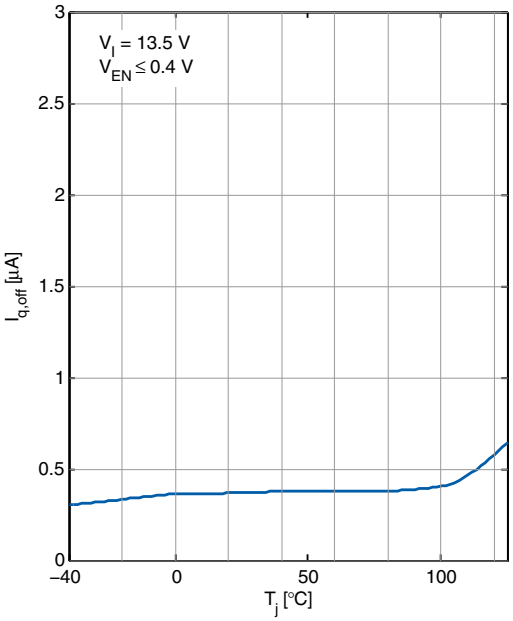
Current consumption I_q versus junction temperature T_j



Current consumption $I_{q,off}$ versus input voltage V_I (disabled)



Current consumption $I_{q,off}$ versus junction temperature T_j (disabled)



5.5 Enable

The TLS850B0TEV33 can be switched on and off by the enable feature. Applying a “high” level as specified below (for example battery voltage) to the EN pin enables the device. Applying a “low” level as specified below (for example GND) shuts down the device. If a signal with slow slope is applied to the EN pin, then the built in hysteresis of the enable feature avoids toggling between ON/OFF state.

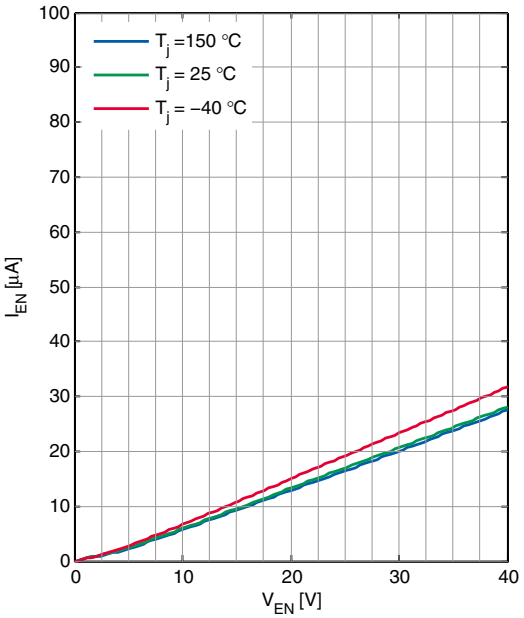
Table 6 Electrical characteristics enable

T_j = -40°C to +150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25°C

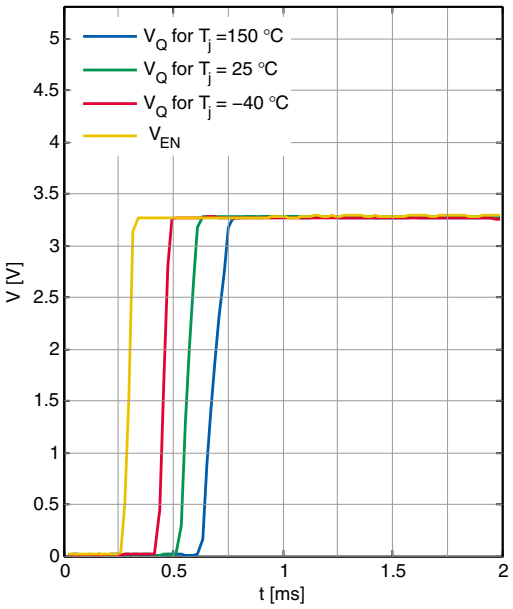
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
“High” level input voltage	$V_{EN,H}$	2	–	–	V	V_Q settled	P_5.5.1
“Low” level input voltage	$V_{EN,L}$	–	–	0.8	V	$V_Q \leq 0.1$ V	P_5.5.2
Enable threshold hysteresis	$V_{EN,Hy}$	90	–	–	mV	–	P_5.5.3
“High” level input current	$I_{EN,H}$	–	–	4	µA	V_{EN} = 5 V	P_5.5.4
“High” level input current	$I_{EN,H}$	–	–	20	µA	$V_{EN} \leq 18$ V	P_5.5.5
Enable internal pull-down resistor	R_{EN}	1.25	2	3.5	MΩ	–	P_5.5.6

5.6 Typical performance characteristics enable

Enable input current I_{EN} versus Enable input voltage V_{EN}



Output voltage V_Q versus time t (EN switched ON)



6 Application information

6.1 Application diagram

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

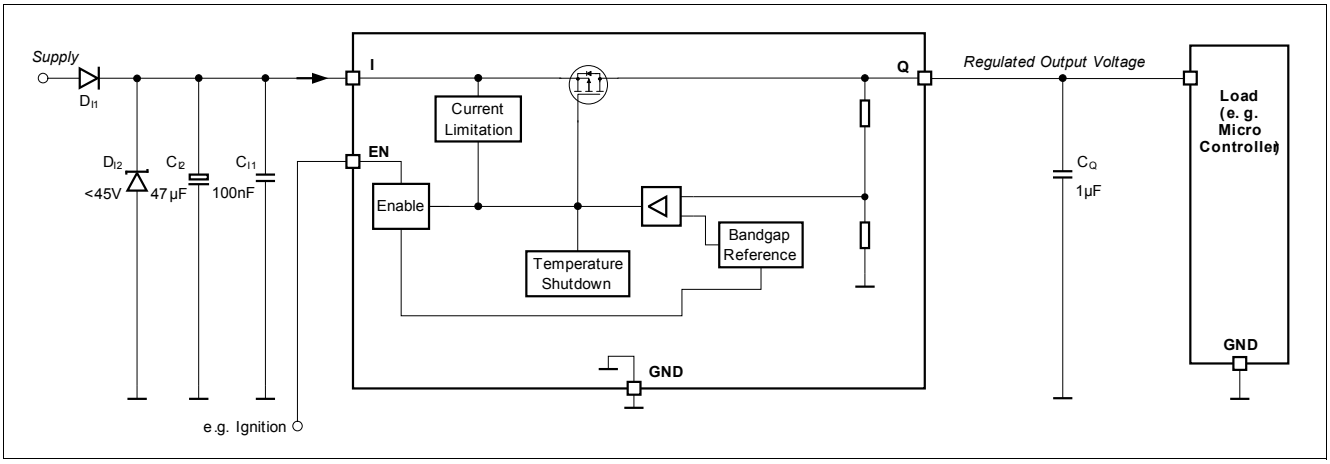


Figure 5 Application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

6.2 Selection of external components

6.2.1 Input pin

Figure 5 shows the typical input circuitry for a linear voltage regulator. A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter the high frequency disturbances imposed by the line, for example ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to damp high energy pulses, such as ISO pulse 2a. This capacitor must be placed close to the input pin of the linear voltage regulator.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and to protect the device from damage due to overvoltage.

The external components at the input pin are optional, but they are recommended in case of possible external disturbances.

6.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **“Functional range” on Page 7**.

TLS850B0TEV33 is designed to be also stable with low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the voltage regulator's output pin and GND pin, on the same side of the PCB as the regulator itself.

In case of input voltage transients or load current transients, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

6.3 Thermal considerations

the total power dissipation can be calculated from the known input voltage, the output voltage and the load profile of the application:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (6.1)$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_Q: output voltage
- I_Q: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} is:

$$R_{thJA,max} = (T_{j,max} - T_a) / P_D \quad (6.2)$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **"Thermal resistance" on Page 8**.

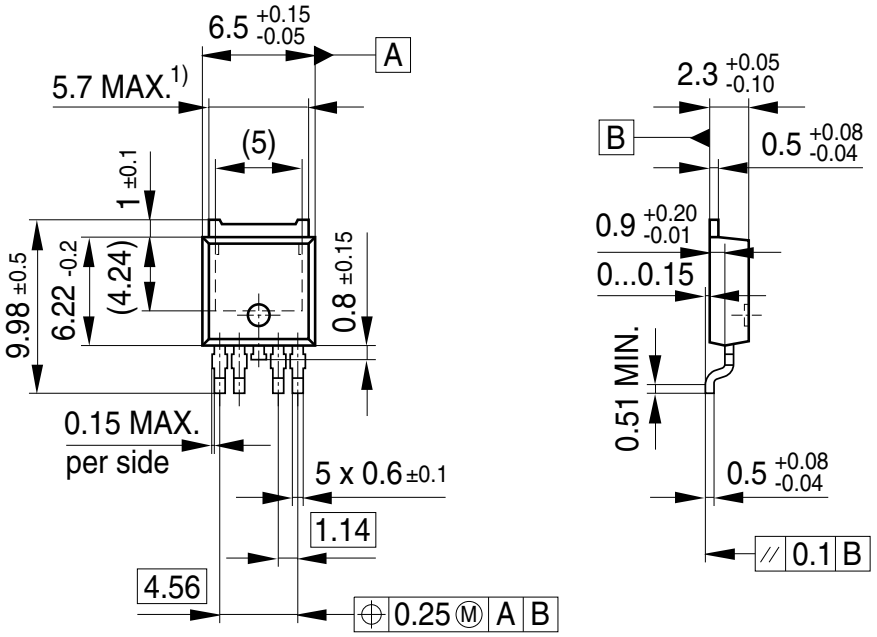
6.4 Reverse polarity protection

TLS850B0TEV33 is not protected against reverse polarity faults and must be protected by external components against negative supply voltage. An external reverse polarity diode is necessary. The absolute maximum ratings of the device as specified in **"Absolute maximum ratings" on Page 6** must be maintained.

6.5 Further application information

For further information you may contact **http://www.infineon.com/**

7 Package outlines



1) Includes mold flashes on each side.
All metal surfaces tin plated, except area of cut.

Figure 6 PG-TO252-5

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

8 Revision history

Revision	Date	Changes
1.00	2017-10-16	Initial Version

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Do you have a question about any aspect of this document?
Email: erratum@infineon.com

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