To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Not recommend for new design

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RENESAS

MOS FIELD EFFECT TRANSISTOR
μPA2591T1H

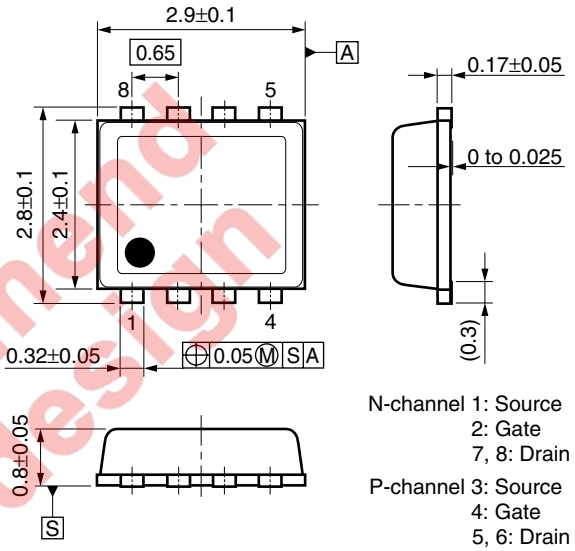
N- AND P-CHANNEL MOSFET FOR SWITCHING

DESCRIPTION

The μPA2591T1H is N- and P-channel MOSFETs designed for DC/DC converters and power management applications of portable equipments.

N- and P-channel MOSFETs are assembled in one package, to contribute minimize the equipments.

PACKAGE DRAWING (Unit: mm)



N-channel 1: Source
2: Gate
7, 8: Drain

P-channel 3: Source
4: Gate
5, 6: Drain

FEATURES

- 2.5 V drive available
- Low on-state resistance

N-channel $R_{DS(on)1}$ = 55 mΩ MAX. (V_{GS} = 4.5 V, I_D = 2 A)

$R_{DS(on)2}$ = 70 mΩ MAX. (V_{GS} = 2.5 V, I_D = 2 A)

P-channel $R_{DS(on)1}$ = 88 mΩ MAX. (V_{GS} = –4.5 V, I_D = –2 A)

$R_{DS(on)2}$ = 150 mΩ MAX. (V_{GS} = –2.5 V, I_D = –1 A)

- Built-in gate protection diode
- Small and surface mount package (8-pin VSOF (2429))

Not recommend for new design

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μPA2591T1H-T1-AT Note	Pure Sn	8 mm embossed taping 3000 p/reel	8-pin VSOF (2429)
μPA2591T1H-T2-AT Note			

Note Pb-free (This product does not contain Pb in the external electrode and other parts.)

Marking: 2591

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Date Published February 2010 NS
Printed in Japan

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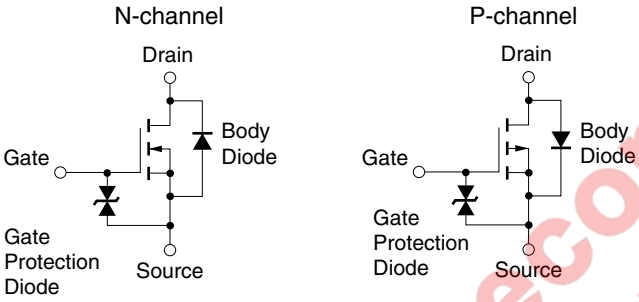
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	−30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±12	∓12	V
Drain Current (DC)	$I_{D(DC)}$	±4.0	∓3.0	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±16	∓12	A
Total Power Dissipation (1 unit, 5 s) Note2	P_{T1}	1.5		W
Total Power Dissipation (2 units, 5 s) Note2	P_{T2}	1.24		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 to +150		°C

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on FR-4 board of 25.4 mm x 25.4 mm x 0.8 mm

EQUIVALENT CIRCUIT



Not recommend for new design

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Caution This product is electrostatic-sensitive device due to low ESD capability and should be handled with caution for electrostatic discharge.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

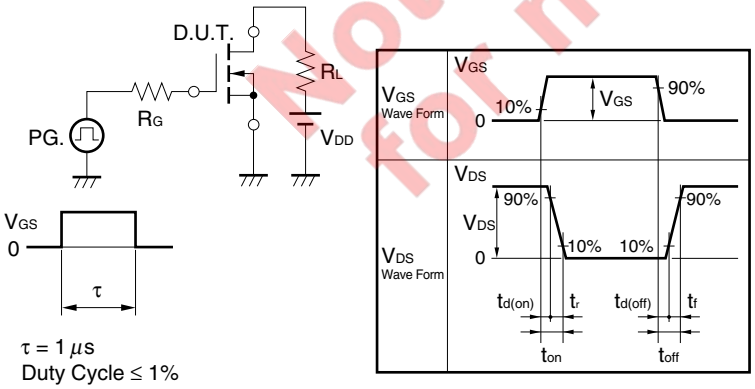
N-channel MOSFET

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±12 V, V_{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	0.5		1.5	V
Forward Transfer Admittance **Note**	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 2 A	1			S
Drain to Source On-state Resistance **Note**	$R_{DS(on)1}$	V_{GS} = 4.5 V, I_D = 2 A		38	55	mΩ
	$R_{DS(on)2}$	V_{GS} = 2.5 V, I_D = 2 A		48	70	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V,		475		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		62		pF
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz		34		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 2 A,		7		ns
Rise Time	t_r	V_{GS} = 4.5 V,		6		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 6 Ω		22		ns
Fall Time	t_f			5		ns
Total Gate Charge	Q_G	V_{DD} = 24 V, V_{GS} = 4.5 V,		5.4		nC
Gate to Source Charge	Q_{GS}	I_D = 4 A		0.8		nC
Gate to Drain Charge	Q_{GD}			1.5		nC
Body Diode Forward Voltage **Note**	$V_{F(S-D)}$	I_F = 4 A, V_{GS} = 0 V		0.85		V

Note Pulsed

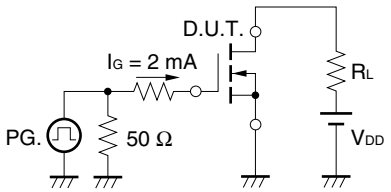
Not recommend for new design

TEST CIRCUIT 1 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

TEST CIRCUIT 2 GATE CHARGE



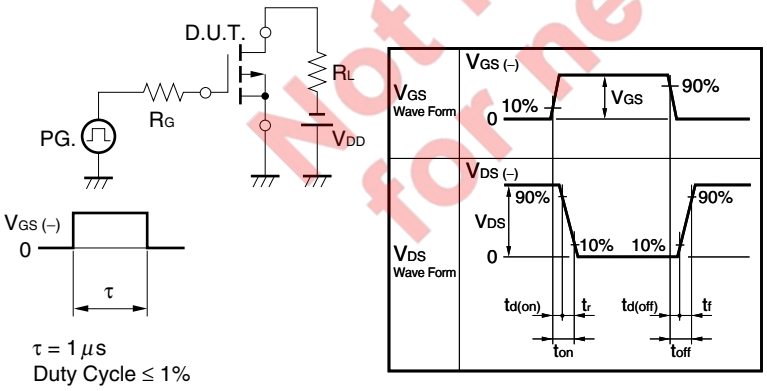
P-channel MOSFET

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓12 V, V_{DS} = 0 V			∓10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–0.5		–1.5	V
Forward Transfer Admittance **Note**	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –1.5 A	1.5			S
Drain to Source On-state Resistance **Note**	$R_{DS(on)1}$	V_{GS} = –4.5 V, I_D = –2 A		66	88	mΩ
	$R_{DS(on)2}$	V_{GS} = –2.5 V, I_D = –1 A		98	150	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V,		450		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		77		pF
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz		63		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –15 V, I_D = –1.5 A,		12		ns
Rise Time	t_r	V_{GS} = –4.5 V,		5		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 6 Ω		37		ns
Fall Time	t_f			27		ns
Total Gate Charge	Q_G	V_{DD} = –24 V, V_{GS} = –4.5 V,		5.2		nC
Gate to Source Charge	Q_{GS}	I_D = –3 A		1.1		nC
Gate to Drain Charge	Q_{GD}			2.3		nC
Body Diode Forward Voltage **Note**	$V_{F(S-D)}$	I_F = –3 A, V_{GS} = 0 V		0.89		V

Note Pulsed

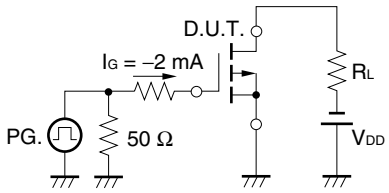
Not recommend for new design

TEST CIRCUIT 1 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

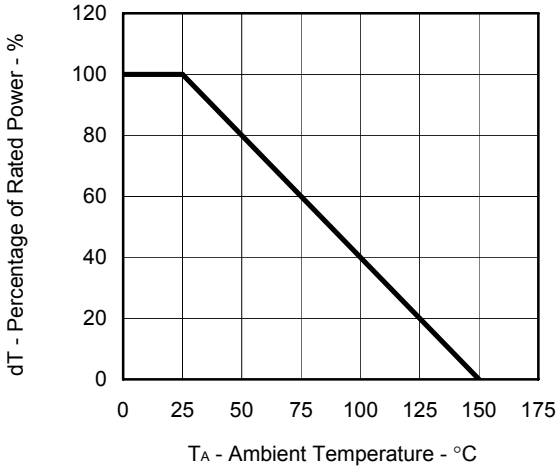
TEST CIRCUIT 2 GATE CHARGE



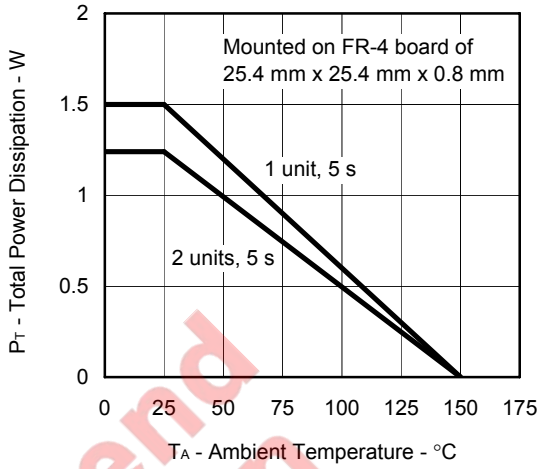
TYPICAL CHARACTERISTICS (T_A = 25°C)

(1) N-channel MOSFET

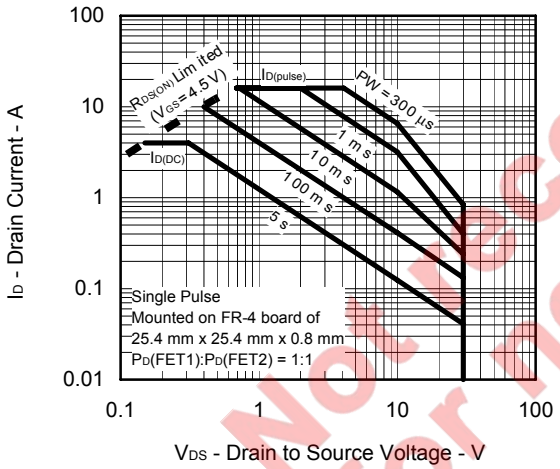
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



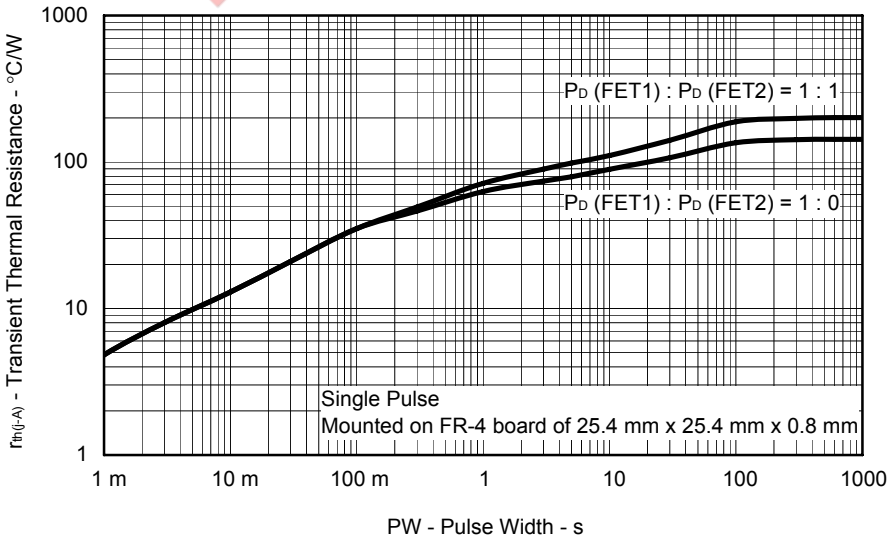
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



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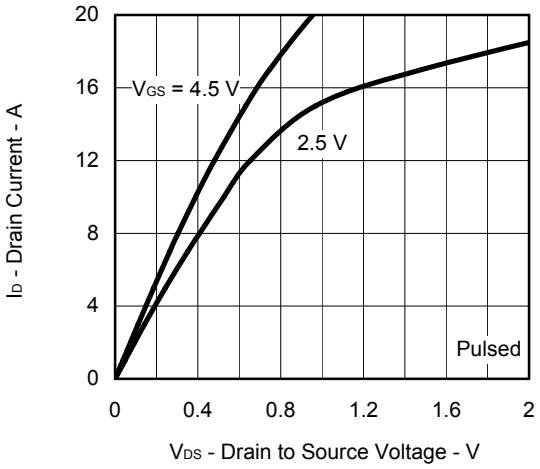
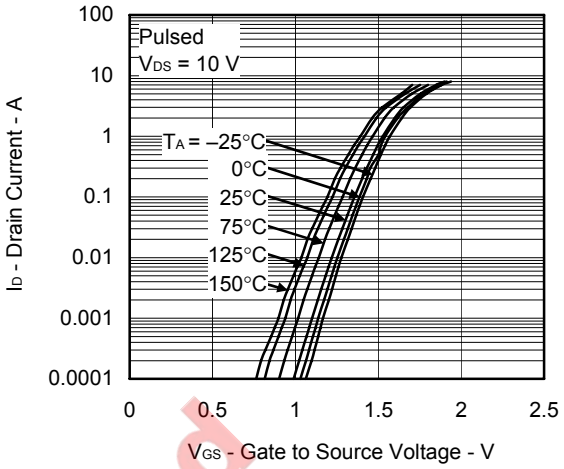
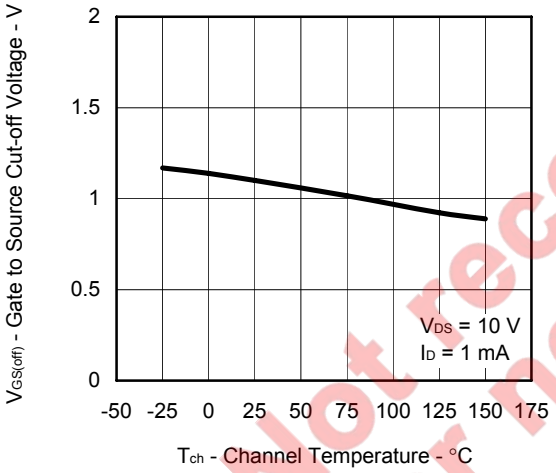
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



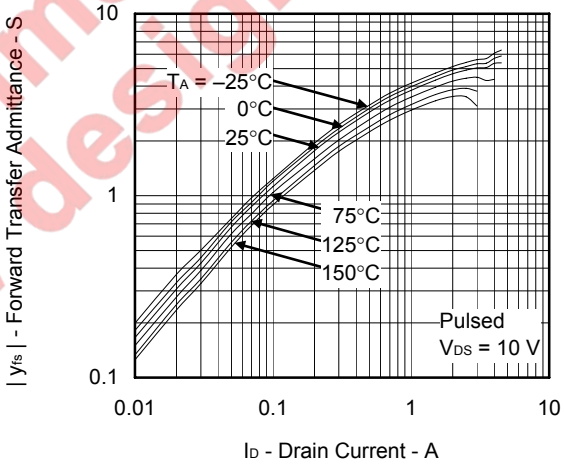
FORWARD TRANSFER CHARACTERISTICS



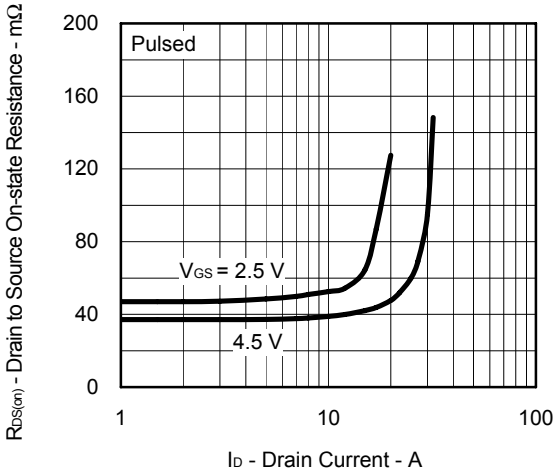
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



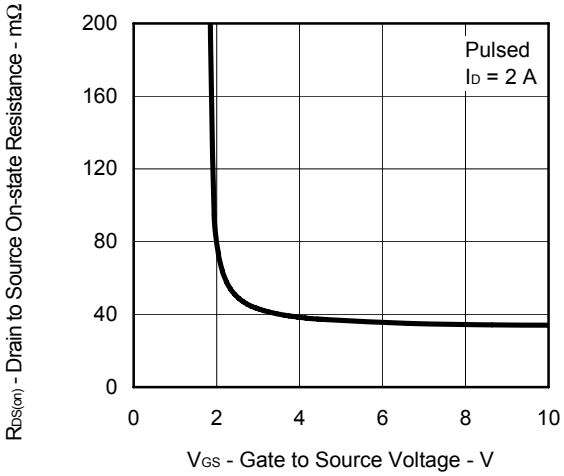
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT

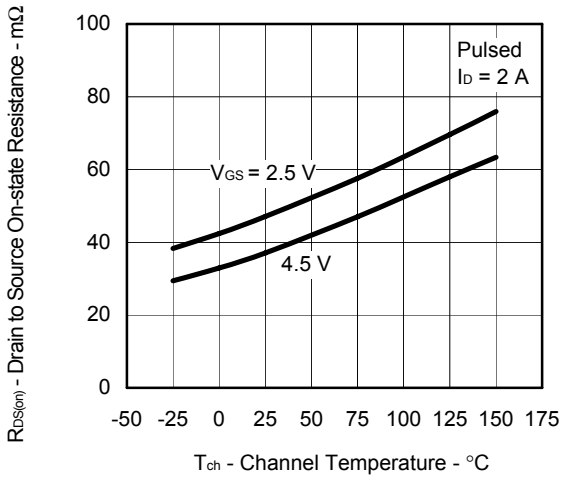


DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE

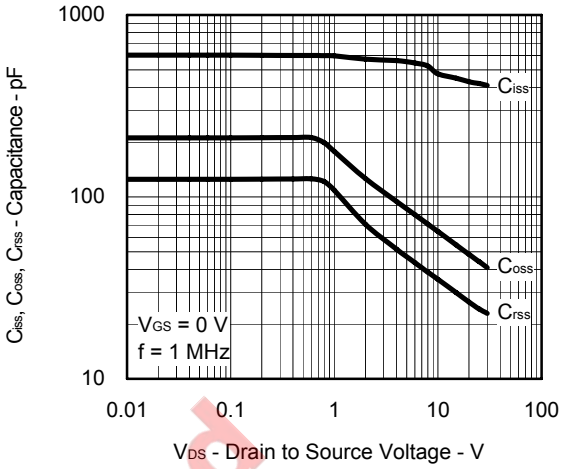


Not recommend for new design

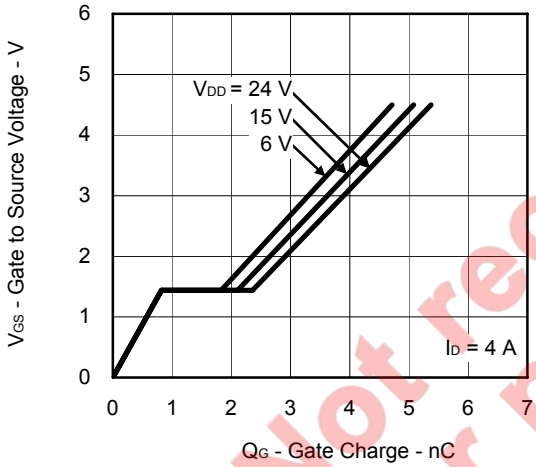
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



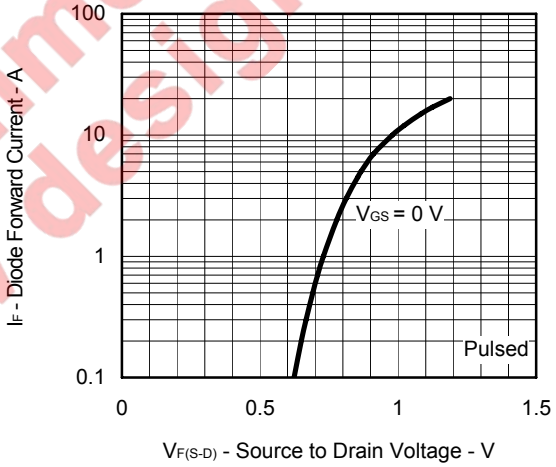
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



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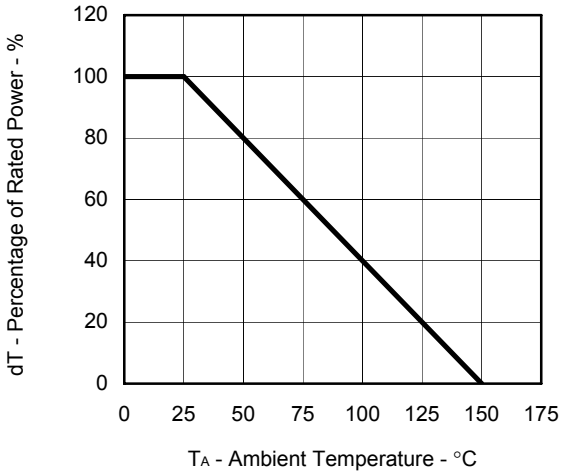
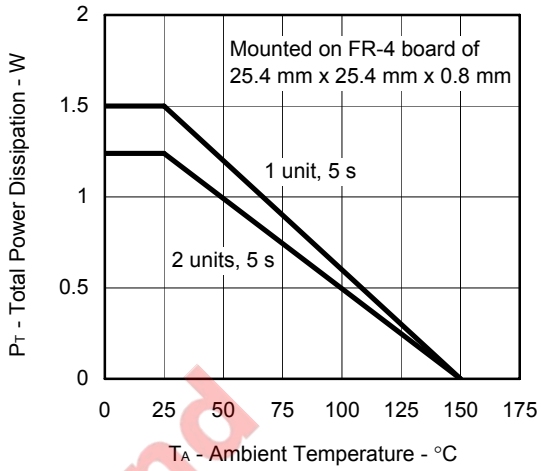
(2) P-channel MOSFET

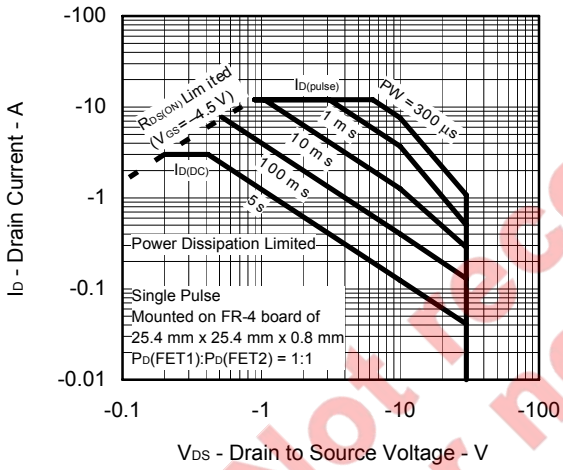
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



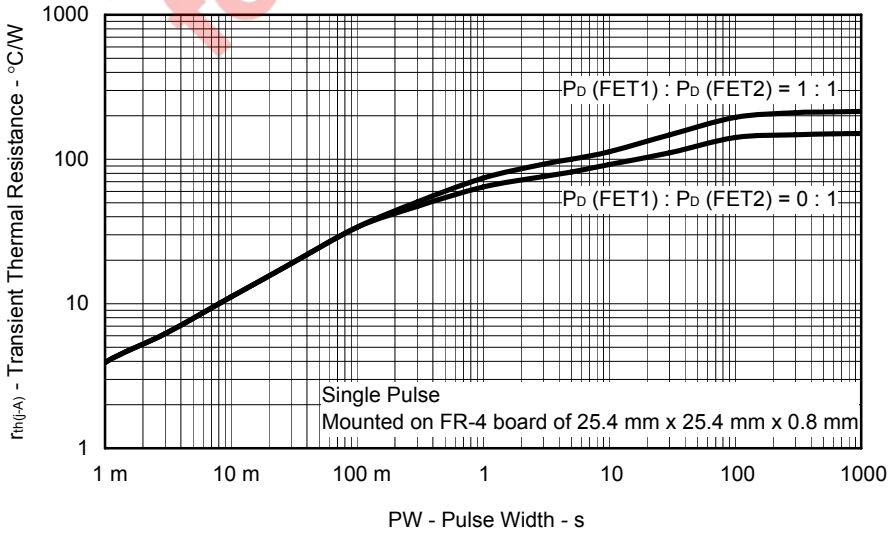
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



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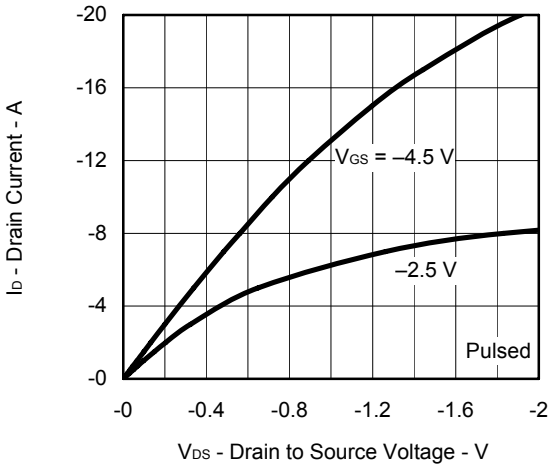
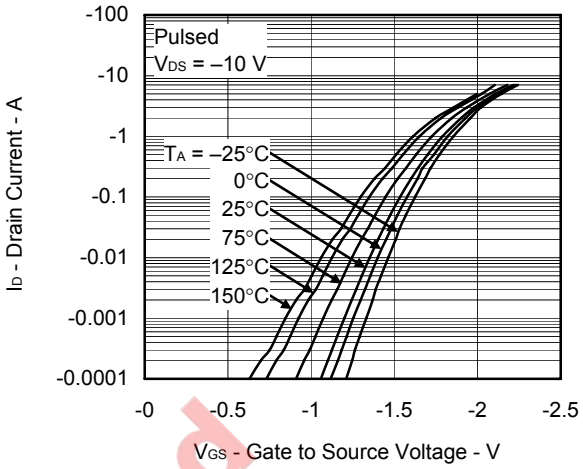
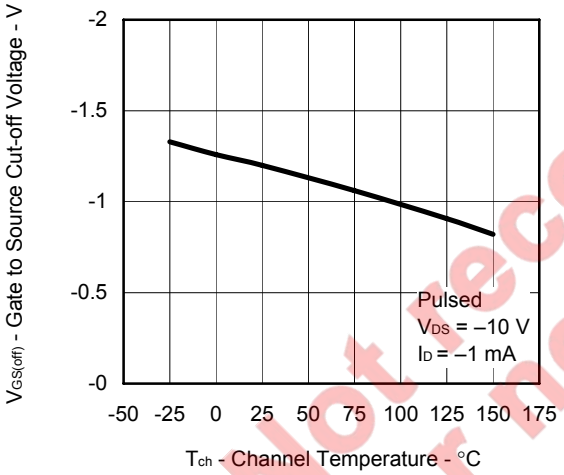
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



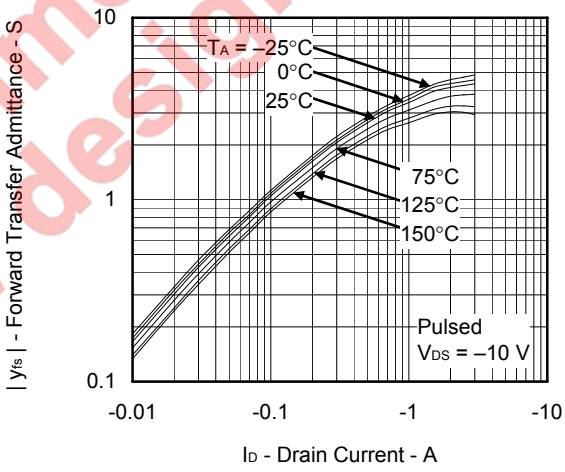
FORWARD TRANSFER CHARACTERISTICS



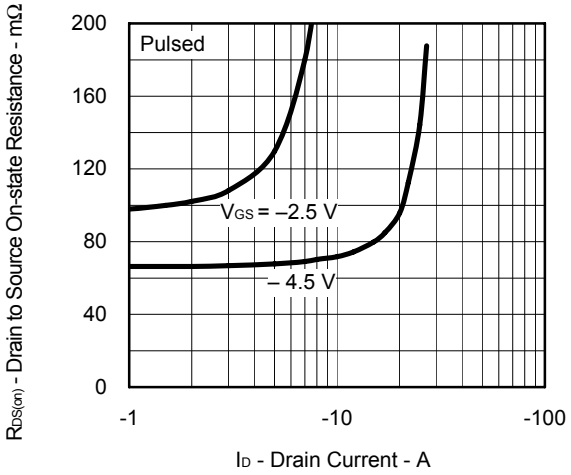
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



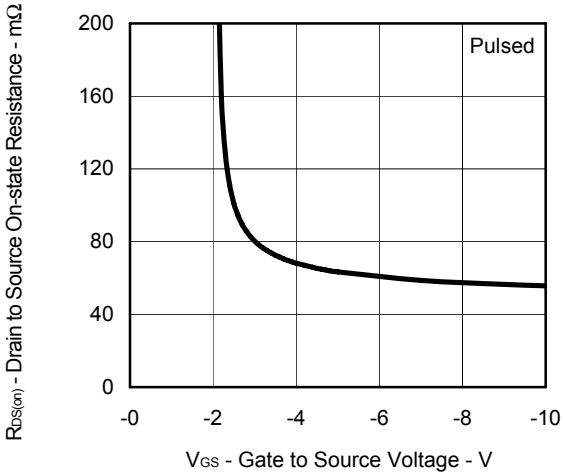
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



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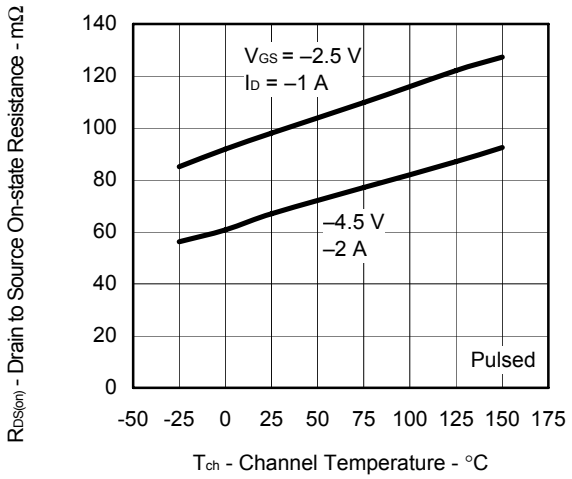
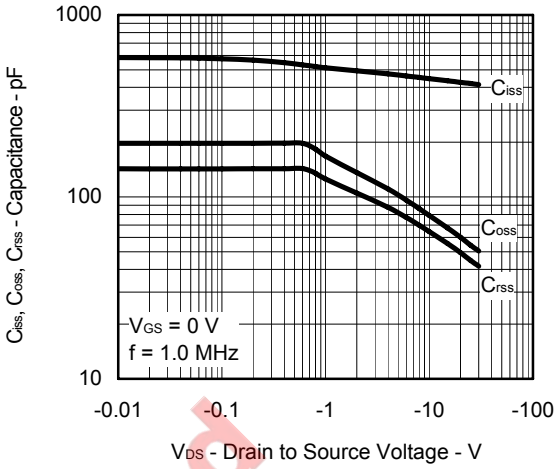
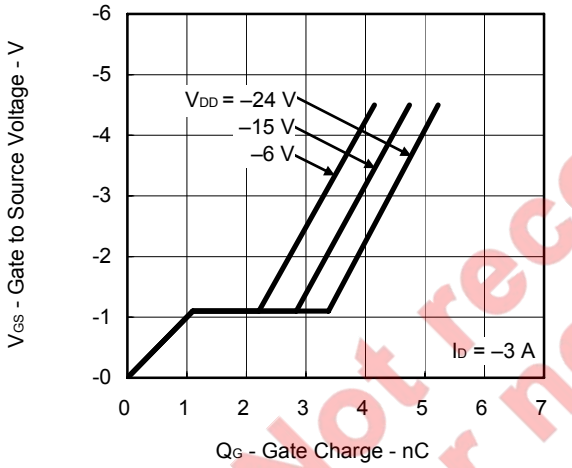
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



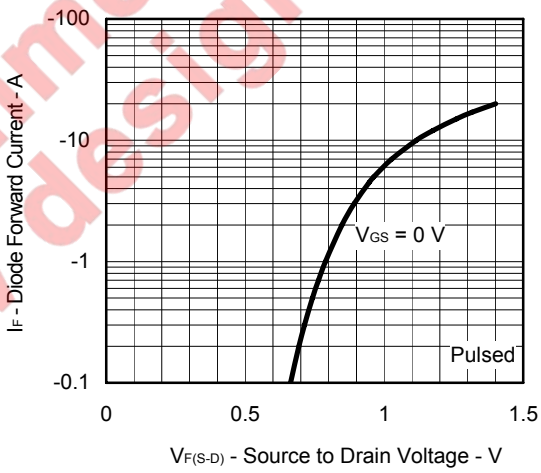
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



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