MAX22203

65V, 3.8A Dual Brushed or Single Stepper Motor Driver with Integrated Current Sense

General Description

The MAX22203 is a dual 65V, $3.8A_{MAX}$ H-Bridge with PWM inputs and accurate Current Drive Regulation (CDR). Each H-Bridge can be controlled individually and has a very low typical R_{ON} (high-side + low-side) of 0.3Ω, resulting in high driving efficiency and low heat generation. The MAX22203 can be used to drive two Brushed DC motors or a single Stepper Motor.

The integrated CDR can limit the start up or stall the current of a Brushed DC motor or control the phase current for stepper operation.

The bridge output current is sensed by a non-dissipative Integrated Current Sensing (ICS) eliminating the bulky external power resistors (which are normally required for this function) and compared with a configurable threshold current (I_{TRIP}). The I_{TRIP} threshold can be set independently for the two full bridges by connecting the external resistors to pins R_{EFA} and R_{EFB} .

The maximum output current per H-Bridge is I_{MAX} = 3.8A and is limited by the Overcurrent Protection (OCP) circuit. This current can be driven for very short transients and is aimed to effectively drive small capacitive loads. The maximum user-configurable current regulation threshold is I_{TRIP_MAX} = 3A. The maximum RMS current (I_{RMS}) per H-Bridge is $2A_{RMS}$ on a standard JEDEC 4-layer board. The maximum RMS current can be limited by thermal considerations and depends on the thermal characteristic of the application (PCB ground planes, heat sinks, forced air ventilation, etc).

The MAX22203 features Overcurrent Protection (OCP), Thermal Shutdown (TSD), and Undervoltage Lockout (UVLO). An open-drain active low nFAULT pin is activated every time a fault condition is detected. During Thermal Shutdown and Undervoltage Lockout, the driver is tristated until normal operations are restored.

The MAX22203 is packaged into a small TQFN38 5mm x 7mm package.

Applications

- Brushed DC Motor Driver
- Stepper Motor Driver
- Solenoid Driver
- Latched Valves

Benefits and Features

- Two H-Bridges with 65V Maximum Operating Voltage
  - Total R_{ON} (High-Side + Low-Side): 300mΩ typical (T_A = 25°C)
- Current Ratings Per H-Bridge (Typical at 25°C):
  - I_{MAX} = 3.8A (Impulsive Current for Driving Capacitive Loads)
  - I_{TRIP_MAX} = 3A (Maximum Current Setting for Internal Current Drive Regulation)
  - $I_{RMS} = 2A_{RMS}$
- Integrated Current Drive Regulation (CDR)
  - Internal Current Sensing (ICS) Eliminates External Bulky Resistors and Improves Efficiency
  - Current Drive Regulation Monitor Output Pins (CDRA and CDRB)
  - Multiple Decay Modes (Slow, Mixed, Fast)
  - Fixed Off Time Configurable with External Resistance.
- Current-Sense Output (Current Monitor)
- Fault Indicator Pin ($\overline{FAULT}$)
- Protections
  - Overcurrent Protection for Each Individual Channel (OCP)
  - Undervoltage Lockout (UVLO)
  - Thermal Shutdown (TSD) T_J = +165°C
- TQFN38 5mm x 7mm package (TSSOP38 4.4mm x 9.7mm available in the future)

Ordering Information appears at end of data sheet.

19-101012; Rev 0; 5/21

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Simplified Block Diagram

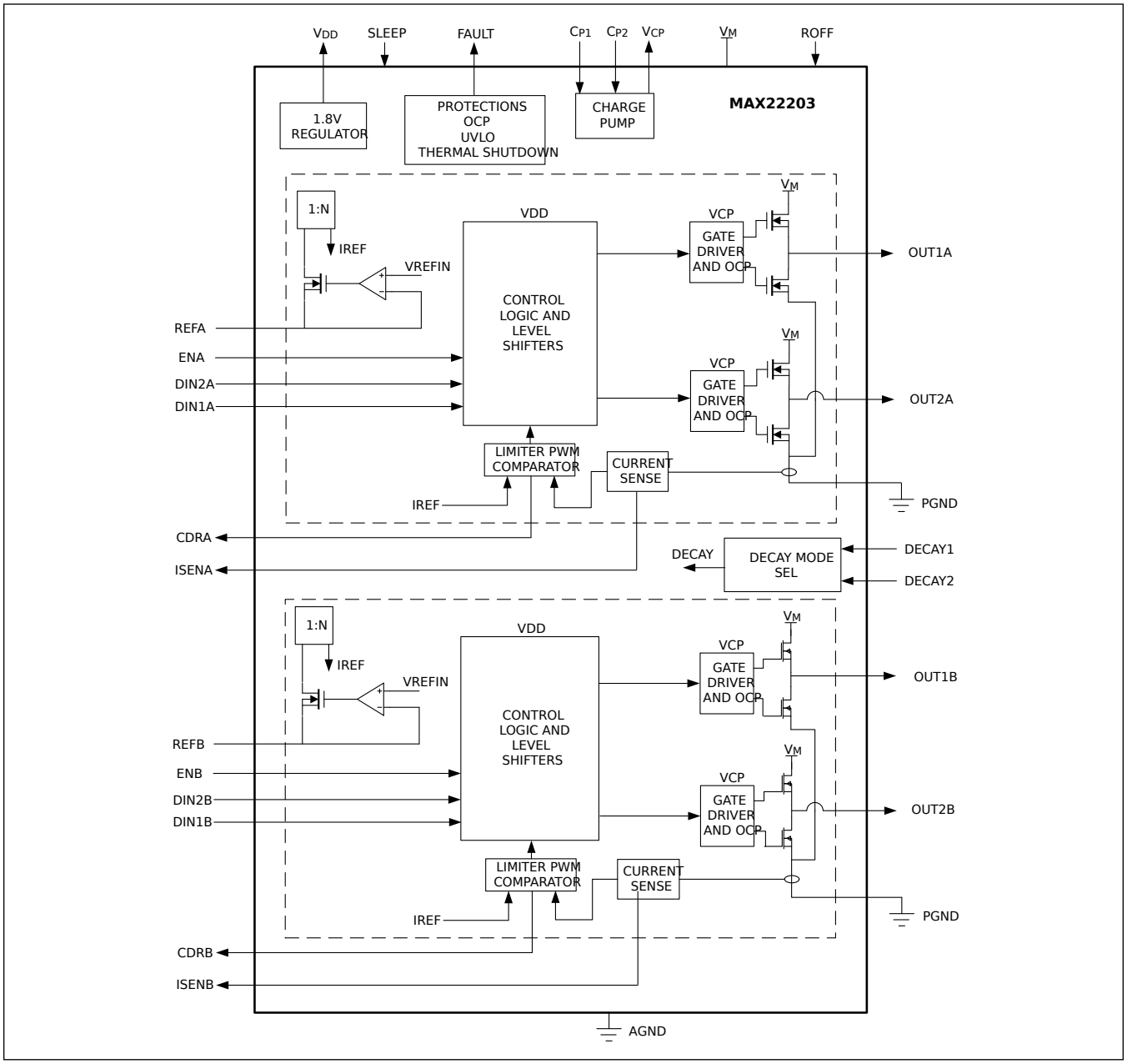


TABLE OF CONTENTS

General Description . . . 1
Applications . . . 1
Benefits and Features . . . 1
Simplified Block Diagram . . . 2
Absolute Maximum Ratings . . . 6
Package Information . . . 6
TQFN 38 - 5x7mm . . . 6
Electrical Characteristics . . . 6
Typical Operating Characteristics . . . 9
Pin Configuration . . . 10
Pin Configuration . . . 10
Pin Description . . . 11
Detailed Description . . . 12
Sleep Mode (SLEEP Pin) . . . 12
PWM Control . . . 12
Current-Sense Output (CSO) - Current Monitor . . . 13
Current Drive Regulation . . . 15
Integrated Current Sense (ICS) . . . 15
Setting the Current Regulation Threshold – Pin REF . . . 15
Setting the Fixed OFF_TIME (t_{OFF}) . . . 15
CDR Open-Drain Output . . . 15
Operating Modes . . . 17
Setting the Decay Mode . . . 18
Protections . . . 18
Overcurrent Protection (OCP) . . . 18
Thermal Shutdown Protection (TSD) . . . 19
Undervoltage Lockout Protection (UVLO) . . . 19
Applications Information . . . 20
Recommended Layout . . . 20
Typical Application Circuits . . . 21
Application Diagram . . . 21
Ordering Information . . . 22
Revision History . . . 23

LIST OF FIGURES

Figure 1. ISEN Current 14
Figure 2. CDR Monitor Timing Diagram 17
Figure 3. Current Flow During ON and Decay Modes 18
Figure 4. Recommended Layout 20

LIST OF TABLES

Table 1. MAX22203 Truth Table 12
Table 2. Decay Mode Truth Table 18

Absolute Maximum Ratings

V_M to GND ..... -0.3V to +70V
V_{DD} to GND.....-0.3V to min(+2.2V, V_M + 0.3V)
PGND to GND ..... -0.3V to +0.3V
OUT_ ..... -0.3V to V_M + 0.3V
V_{CP} to GND..... V_M - 0.3V to min(+74V, V_M + 6V)
C_{P2} to GND ..... V_M - 0.3V to V_{CP} + 0.3V
C_{P1} to GND ..... -0.3V to V_M + 0.3V
FAULT to GND ..... -0.3V to 6V
CDR_ to GND..... -0.3V to 6V
REF_ to GND .....-0.3V to min(+2.2V, V_{DD} + 0.3V)
ROFF to GND ..... -0.3V to min(+2.2V, V_{DD} + 0.3V)
ISEN_ to GND.....-0.3 to min(+2.2V, V_{DD} + 0.3V)
DIN_ to GND.....-0.3V to 6V
EN_ to GND .....-0.3V to 6V
DECAY_ to GND.....-0.3V to 6V
SLEEP to GND ..... -0.3V to Min(+70V, V_M + 0.3V)
Operating Temperature Range .....-40°C to 125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (reflow) .....260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN 38 - 5x7mm

Package Code	T3857-1C
Outline Number	21-0172
Land Pattern Number	90-0076
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	38°C/W
Junction to Case (θ_{JC})	1°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_M = +36V, R_{ROFF} = from 15kΩ to 120kΩ , $R_{REF_}$ = from 12kΩ to 72kΩ , Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	V_M		4.5		65	V
Sleep Mode Current consumption	I_{VM}	$\overline{SLEEP}$ = logic low			20	µA
Quiescent Current Consumption	I_{VM}	$\overline{SLEEP}$ = logic high			5	mA
1.8V Regulator Output Voltage	V_{VDD}	V_M = +4.5V, I_{LOAD} = 20mA		1.8		V
V_{DD} Current Limit	$I_{VDD(LIM)}$	V_{DD} shorted to GND	18			mA
Charge Pump Voltage	V_{CP}			V_M + 2.7		V

Electrical Characteristics (continued)

(V_M = +36V, R_{ROFF} = from 15kΩ to 120kΩ , $R_{REF_}$ = from 12kΩ to 72kΩ , Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC LEVEL INPUTS-OUTPUTS						
Input Voltage Level - High	V_{IH}		1.2			V
Input Voltage Level - Low	V_{IL}				0.65	V
Input Hysteresis	V_{HYS}			110		mV
Pulldown Current	I_{PD}	Logic supply (V_L) = +3.3V	16	34	60	µA
Open-Drain Output Logic-Low Voltage	V_{OL}	I_{LOAD} = 5mA			0.4	V
Open-Drain Output Logic-High Leakage Current	I_{OH}	V_{PIN} = +3.3V	-1		1	µA
$\overline{SLEEP}$ Voltage Level High	$V_{IH(\overline{SLEEP})}$		0.9			V
$\overline{SLEEP}$ Voltage Level Low	$V_{IL(\overline{SLEEP})}$				0.6	V
$\overline{SLEEP}$ Pulldown Input Resistance	$R_{PD(\overline{SLEEP})}$		0.8	1.5		MΩ
OUTPUT SPECIFICATIONS						
Output ON-Resistance Low Side	$R_{ON(LS)}$			150	270	mΩ
Output ON-Resistance High Side	$R_{ON(HS)}$			150	300	mΩ
Output Leakage	I_{LEAK}	Driver OFF	-12		12	µA
Dead Time	t_{DEAD}			100		ns
Output Slew Rate	SR			300		V/µs
PROTECTION CIRCUITS						
Overcurrent Protection Threshold	OCP		3.8			A
Overcurrent Protection Blanking Time	t_{OCP}			2.2	3.5	µs
Autoretry OCP Time	t_{RETRY}			3		ms
UVLO Threshold on V_M	UVLO	V_M rising	3.75	4	4.25	V
UVLO Threshold on VM Hysteris	$UVLO_{HYS}$			0.12		V
Thermal Protection Threshold Temperature	T_{SD}			155		°C
Thermal Protection Temperature Hysteresis	T_{SD_HYST}			20		°C
CURRENT REGULATION						
REF_ Pin Resistor Range	R_{REF}		12		72	KΩ

Electrical Characteristics (continued)

(V_M = +36V, R_{ROFF} = from 15kΩ to 120kΩ , $R_{REF_}$ = from 12kΩ to 72kΩ , Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

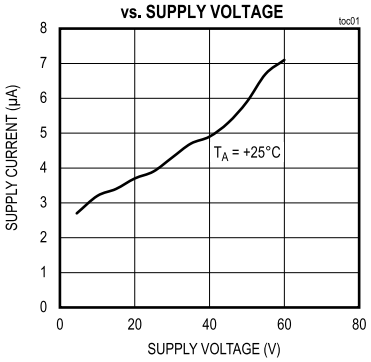
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REF Output Voltage	V_{REF}			900		mV
ITRIP Current Regulation Constant	KI			36		KV
Current Trip Regulation Accuracy (*Note 1*)	DITRIP1	I_{TRIP} from 1.75A to 3A	-5		5	%
	DITRIP2	I_{TRIP} from 500mA to 1.75A	-10		+10	
Fixed OFF – Time Internal	t_{OFF}	ROFF shorted to V_{DD}	16	20	24	µs
Fixed OFF – Time Constant	KTOFF	R_{ROFF} from 15KΩ to 120KΩ		0.667		µs/kΩ
PWM Blanking time	t_{BLK}			2.5		µs
CURRENT SENSE MONITOR						
ISEN_ Voltage Range	ISEN	Voltage Range at Pin ISEN	0		1.1	V
Current Monitor Scaling Factor	KISEN	Refer to the ISEN Output Current Equation in the *Current Sense Output (CSO) - Current Monitor* Section		7500		A/A
Current Monitor Accuracy (*Note 1*)	DKISEN1	I_{OUT} from 1.1A to 3A	-5		+5	%
	DKISEN2	I_{OUT} from 500mA to 1.1A	-10		+10	
Current Monitor Accuracy	DKISEN3	I_{OUT} from 250mA to 500mA	-15		+15	%
Settling Time	t_S	$I_{FS} = I_{MAX}$		0.5		µs
FUNCTIONAL TIMINGS						
Sleep Time	t_{SLEEP}	$\overline{SLEEP}$ = 1 to OUT_ tristate		40		µs
Wakeup Time From Sleep	t_{WAKE}	$\overline{SLEEP}$ = 0 to normal operation			2.7	ms
Enable Time	t_{EN}	Time from EN pin rising edge to driver on			0.6	µs
Disable Time	t_{DIS}	Time from EN pin falling edge to driver off			1.4	µs

Note 1: Guaranteed by design, not production tested.

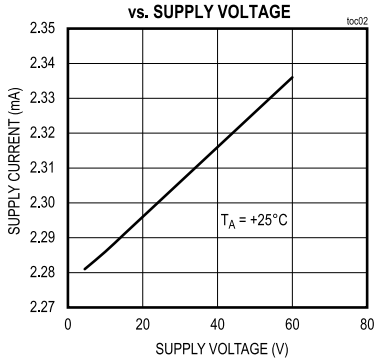
Typical Operating Characteristics

(V_M = +4.5V TO +60V; T_A = 25°C unless otherwise noted.)

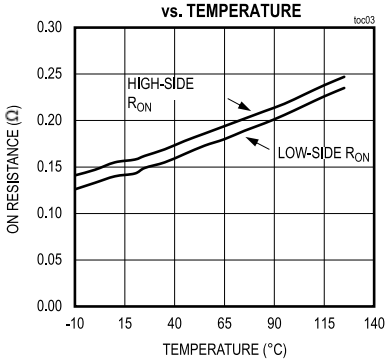
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



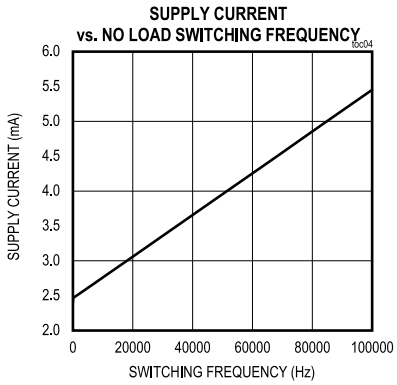
QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



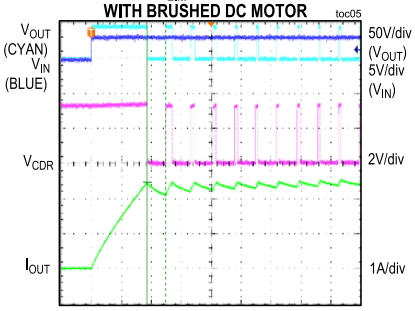
ON RESISTANCE vs. TEMPERATURE



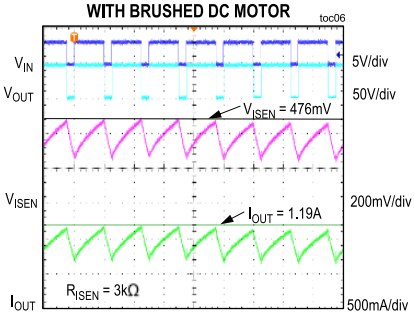
SUPPLY CURRENT vs. NO LOAD SWITCHING FREQUENCY



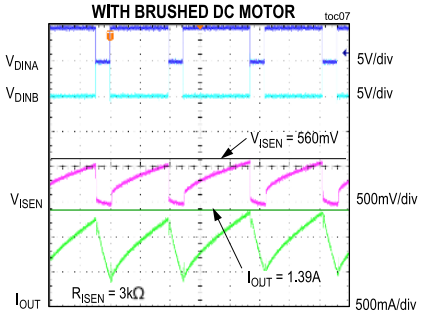
INRUSH CURRENT LIMIT (ZOOMED) 2.4A I_{LIM} THRESHOLD WITH BRUSHED DC MOTOR



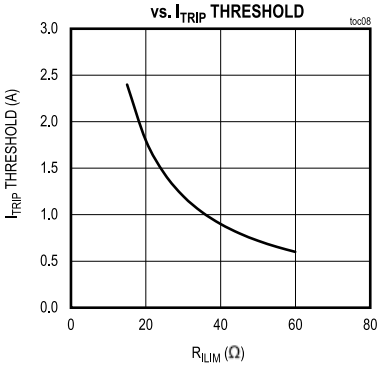
LOAD CURRENT AND ISEN VOLTAGE AT 20kHz PWM AND SLOW DECAY WITH BRUSHED DC MOTOR



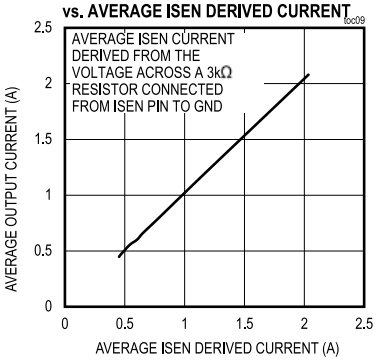
LOAD CURRENT AND ISEN VOLTAGE AT 50kHz PWM AND FAST DECAY WITH BRUSHED DC MOTOR



R_{ILIM} RESISTANCE vs. I_{TRIP} THRESHOLD

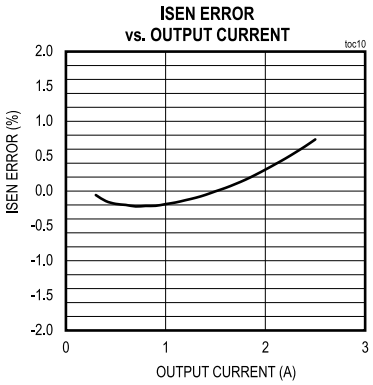


AVERAGE OUTPUT CURRENT vs. AVERAGE ISEN DERIVED CURRENT



Typical Operating Characteristics (continued)

(V_M = +4.5V TO +60V; T_A = 25°C unless otherwise noted.)



Pin Configuration

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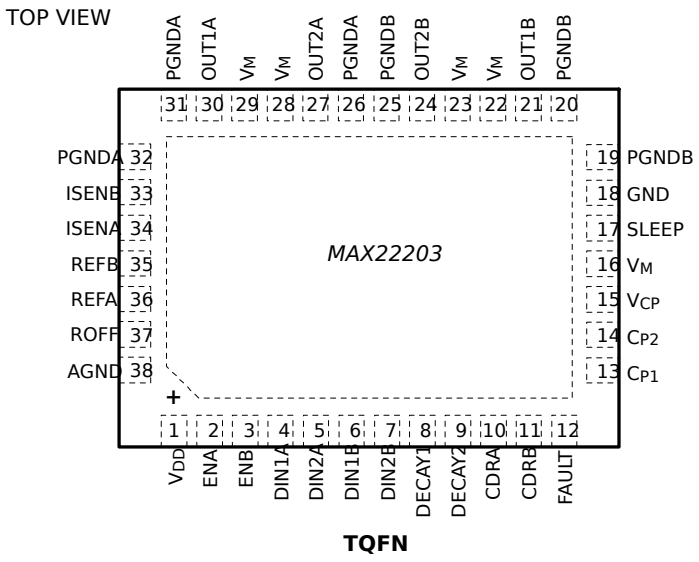


Pin Description

PIN	NAME	FUNCTION	TYPE
16, 22, 23, 28, 29	V_M	Supply Voltage Input. Connect at least 1µF SMD plus 10µF electrolytic bypass capacitors to GND. Higher values can be considered depending on application requirements.	Supply
15	V_{CP}	Charge Pump Output. Connect a 5V, 1µF capacitor between V_{CP} and V_M as close as possible to the device	Output
13	C_{P1}	Charge Pump Flying Capacitor Pin1. Connect a V_M-rated 22nF capacitor between C_{P1} C_{P2} as close as possible to the device.	Output
14	C_{P2}	Charge Pump Flying Capacitor Pin 2. Connect a V_M-rated 22nF capacitor between C_{P1} C_{P2} as close as possible to the device.	Output
1	V_{DD}	1.8V LDO Output. Connect a 5V, 2.2µF to GND close to the device	Analog Output
17	$\overline{SLEEP}$	Active Low Sleep Pin	Logic Input
21, 24, 27, 30	OUT_	Driver Output Pins.	Output
12	$\overline{FAULT}$	Open Drain Output Active Low Fault Indicator. Connect a 2KΩ resistor to the controller supply voltage.	Open Drain Output
33, 34	ISEN_	Current Sense Output Monitor. Connect a resistor to GND (ref. Current sense Output Detailed Description)	Output
2,3	EN_	Logic Input Pin. Enable Pin	Logic Input
4, 5, 6, 7	DIN_	CMOS PWM Input	Logic Input
8, 9	DECAY_	Logic Input. Set the Decay Mode	Logic Input
10, 11	CDR_	Open-Drain Output - Current Drive Regulator. Add a pullup resistor to the controller supply voltage. The pullup resistor value depends on the application requirements. Values between 1KΩ to 5KΩ meet the requirements for a majority of applications.	Open Drain Output
36	REFA	Programmable Current Analog Input. Connect a resistor from R_{EFA} to GND to set the current regulation threshold for Full Bridge A.	Analog Input
35	REFB	Programmable Current Analog Input. Connect a resistor from REFB to GND to set the current regulation threshold for Full Bridge B.	Analog Input
37	ROFF	t_{OFF} Programmable Off Time Pin. Connect R_{OFF} to V_{DD} to use the internal fixed t_{OFF} time. Connect a resistor from R_{OFF} to GND to set the fixed OFF time to a desired value.	Analog Input
18, 38	GND	Analog Ground. Connect to Ground Plane.	GND
19, 20, 25, 26, 31, 32	PGND	Power GND. Connect to GND ground plane.	GND
EP	EP	Exposed PAD. Connect to GND.	GND

Detailed Description

The MAX22203 is a Dual 65V, $3.8A_{MAX}$ H-Bridge. It can be used to drive two Brushed DC motors or a Single Stepper Motor. The H-Bridge FETs have very low impedance, resulting in high driving efficiency and low heat generated. The typical total R_{ON} (high-side + lowpside) is 0.3Ω. Each H-Bridge can be individually PWM controlled by means of three logic inputs (DIN1, DIN2, and EN).

The MAX22203 features an accurate Current Drive Regulation (CDR), which can be used to limit the start up current of a Brushed DC motor or to control the phase current for stepper operation. The bridge output current is sensed by a non-dissipative Integrated Current Sensing (ICS) and it is then compared with the desired threshold current. As soon as the bridge current exceeds the threshold I_{TRIP}, the device enforces the decay for a fixed OFF time (t_{OFF}).

The non-dissipative ICS eliminates the bulky external power resistors, which are normally required for this function, resulting in a dramatic space and power saving compared with mainstream applications based on the external sense resistor.

A current proportional to the internally sensed motor current is output to an external pin (ISEN). By connecting an external resistor to this pin, a voltage proportional to the motor current is generated. The voltage built up on such external resistor can be input into the controller ADC whenever the motor control algorithm requires the current/torque information.

Also, two open-drain output pins (C_{DRA}, C_{DRB}) are asserted every time the internal current regulation takes control of the driver. This allows the external controller to monitor the activity of the internal current loop.

The maximum output current per H-Bridge is $I_{MAX} = 3.8A_{MAX}$ and is limited by the Overcurrent Protection (OCP) circuit. This current can be driven for very short transients and is aimed to effectively drive small capacitive loads.

The maximum user configurable current regulation threshold is I_{TRIP_MAX} = 3A. Current thresholds can be set independently for the two full bridges by connecting the external resistors to pins R_{EFA} and R_{EFB}.

The maximum RMS current per H-Bridge is $I_{RMS} = 2A_{RMS}$ on a standard JEDEC 4-layer board. Since this current is limited by thermal considerations, the actual maximum RMS current depends on the thermal characteristic of the application (PCB ground planes, heatsinks, forced air ventilation, etc).

The MAX22203 features Overcurrent Protection (OCP), Thermal Shutdown (TSD), and Undervoltage Lockout (UVLO). An open-drain active low $\overline{FAULT}$ pin is activated every time a fault condition is detected.

During Thermal shutdown and Undervoltage Lockout, the driver is tristated until normal operations are restored.

Sleep Mode ($\overline{SLEEP}$ Pin)

Drive this pin low to enter in the lowest power mode. All outputs are tristated and the internal circuits are biased off. The charge pump is also disabled. A pulldown resistor is connected between $\overline{SLEEP}$ and GND to ensure the part is disabled whenever this pin is not actively driven. This mode corresponds to the lowest power consumption possible. Waking up from Sleep Mode to Normal Mode takes up to 2.7ms max.

PWM Control

When an H-Bridge is Enabled (EN_ = Logic High) and the H-Bridge current is below the configured current limit, the average output voltage can be controlled by DIN1_ and DIN1_ logic input pins using PWM techniques. Setting Enable logic low causes the Output to enter a high impedance mode and the motor to coast. The Enable input pin frequency must not exceed 1KHz and cannot be used for PWM control.

Table 1 shows the control Truth Table.

Table 1. MAX22203 Truth Table

EN_	DIN1_	DIN2_	OUT1	OUT2	DESCRIPTION
0	X	X	High-Z	High-Z	H bridge disabled. High impedance (HiZ)
1	0	0	L	L	Brake Low; Slow decay
1	1	0	H	L	Reverse (Current from OUT2 to OUT1)
1	0	1	L	H	Forward (Current from OUT1 to OUT2)

Table 1. MAX22203 Truth Table (continued)

1	1	1	H	H	Brake High; Slow Decay

PWM techniques can be used to control the output duty cycle and hence to implement motor speed control. Typically, for brushed DC motor drivers, Slow Decay is preferred as it results in less ripple and higher efficiency. With this approach, during the OFF phase, both the low side FETs are activated effectively grounding the motor winding terminals. The current built up into the motor winding slowly decays. This decay is often referred to as Slow Decay. Alternatively, Fast Decay can also be implemented by reversing the bridge during the OFF phase.

Current-Sense Output (CSO) - Current Monitor

Currents proportional to the internally sensed motor currents are output to pins ISENA and ISENB for H-bridge A and B respectively. The current is sensed when one of the two low side FETs sinks the output current and it is therefore meaningful for both during the energizing (t_{ON}) phase and during the Slow Decay phase (Brake). In Fast Decay, the current is not monitored and ISEN outputs a zero current. The following equation shows the relationship between the current sourced at ISEN and the output current.

$$I_{ISEN}(A) = \frac{I_{OUT}(A)}{K_{ISEN}}$$

Equation - ISEN Output Current

in which K_{ISEN} represents the current scaling factor between the output current and its replica at pin ISEN. K_{ISEN} is typically 7500 A/A. For instance, if the instantaneous output current is 2A, the current sourced at ISEN is 266µA.

Figure Figure 1 shows an idealized behavior of the ISEN current when Slow or Fast Decay are used. Blanking times, delays, and rise/fall edges have been ignored.

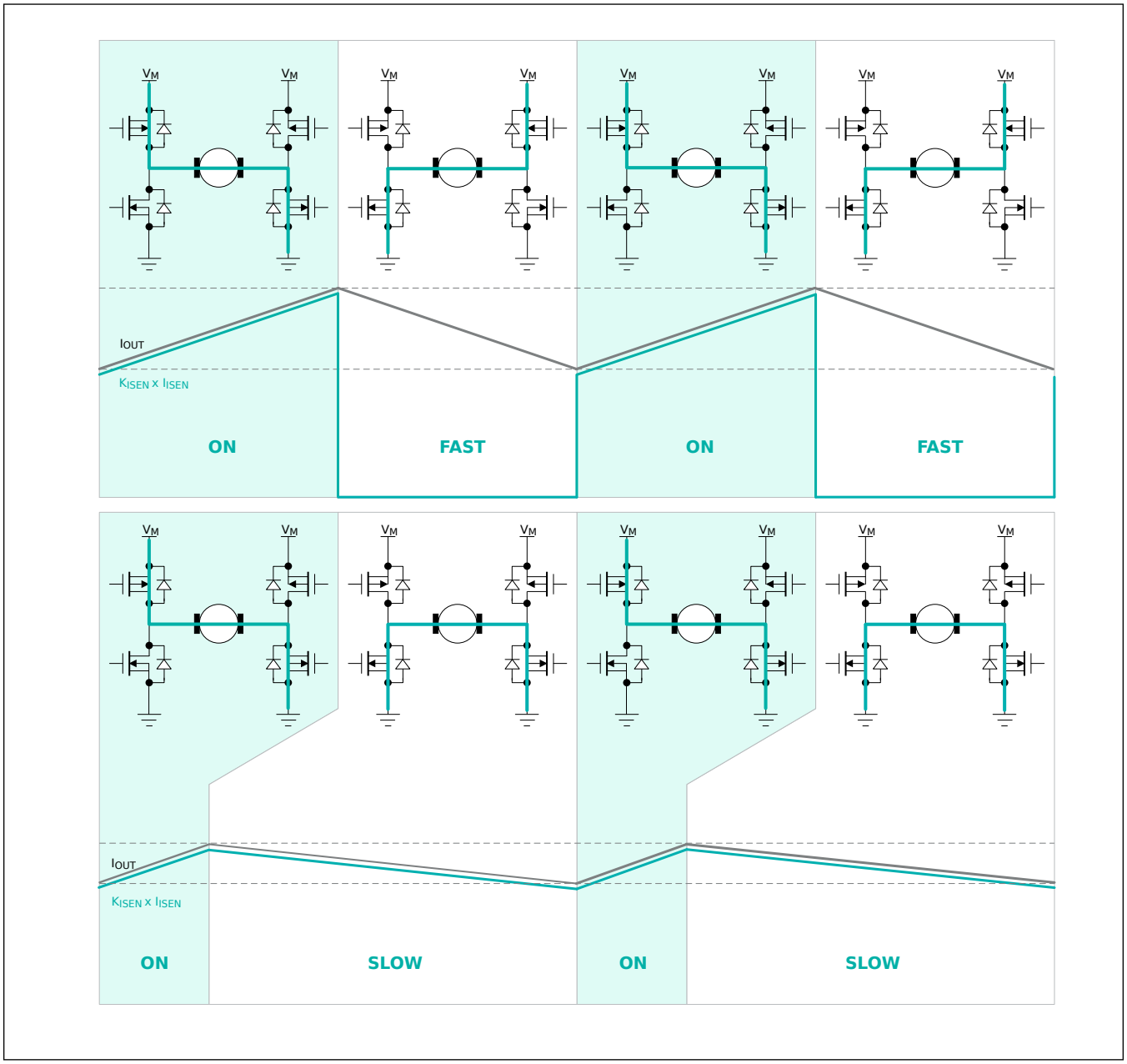


Figure 1. ISEN Current

By connecting an external signal resistor, R_{ISEN} , between ISEN and GND a voltage proportional to the motor current is generated. The voltage built up on R_{ISEN} can be input into the ADC of an external controller in applications in which the motor control algorithm requires the current/torque information. The following equation shows the design formula to calculate R_{ISEN} once the ADC full scale voltage (V_{FS}) and the maximum operating current (I_{MAX}) is known.

$$R_{ISEN}(\Omega) = K_{ISEN} \times \frac{V_{FS}(V)}{I_{MAX}(A)}$$

Equation - RISEN Setting

For example, if the ADC operates up to 1V FS and the maximum operating output current is 2A, then R_{ISEN} is 7500 x 1V/2A = 3.75KΩ.

The R_{ISEN} value also sets the output impedance of the Current-Sense Output circuit (ISEN output impedance). Normally, the input impedance of the ADC is much higher than R_{ISEN} enabling a direct connection to the ISEN pin without attenuation. In case a low input impedance ADC is used, a preamplifier (buffer) is required.

The Current-Sense Output circuit bandwidth and step response performances (see Specifications) ensure the current monitor tracks the driver current in motor drive applications.

Current Drive Regulation

The MAX22203 features embedded Current Drive Regulation (CDR).

The embedded current drive regulation provides an accurate control of the current flowing into the motor windings.

The bridge current is sensed by a non-dissipative Integrated Current Sensing circuit (ICS) and it is then compared with the threshold current (I_{TRIP}). As soon as the bridge current exceeds the threshold, the device enforces the decay for a fixed OFF-time (t_{OFF}). The device supports different decay modes as described in the following paragraphs.

Once t_{OFF} has elapsed, the driver is re-enabled for the next PWM cycle. During current regulation, the PWM duty cycle and frequency depend on the supply voltage, on the motor inductance, and on motor speed and load conditions.

The t_{OFF} duration can be configured with an external resistor connected to the ROFF pin.

Integrated Current Sense (ICS)

A non-dissipative Current Sensing is integrated. This feature eliminates the bulky external power resistors normally required for this function. This feature results in a dramatic space and power saving compared with mainstream applications based on the external sense resistor.

Setting the Current Regulation Threshold – Pin REF

Connect resistors from REFA and REFB to GND to set the current regulation thresholds for Full Bridge A and Full Bridge B respectively (I_{TRIPA}, I_{TRIPB}) .

The equation below shows the typical I_{TRIP} current as a function of the $R_{REF_}$ shunt resistor connected to pin REF_. The proportionality constant K_I is typically 36KV. The external resistor $R_{REF_}$ can range between 12KΩ and 72KΩ, which correspondents to I_{TRIP} setting ranging from about 3A down to 0.5A.

$$I_{TRIP} = \frac{K_I(KV)}{R_{REF}(K\Omega)}$$

Setting the Fixed OFF_TIME (t_{OFF})

The current regulation circuit is based on a constant t_{OFF} PWM control. When the bridge current exceeds the target I_{TRIP} current, an OFF phase begins and Decay modes are activated. The OFF phase has a fixed time duration (t_{OFF}). t_{OFF} can be configured to a desired value by connecting an external resistor (R_{ROFF}) to pin ROFF. When the ROFF pin is shorted to V_{DD}, the t_{OFF} time is internally set at a fixed value (20µs typical).

By connecting an external resistor to the pin R_{OFF}, the user can configure t_{OFF} as shown in the equation below in which R_{ROFF} is an external resistor connected to the R_{OFF} pin (in KΩ) and KT_{OFF} is an internal constant equal to 0.667µs/KΩ.

$$t_{OFF}(\mu s) = R_{ROFF} \times K_{TOFF}$$

t_{OFF} can be programmed from a range of 10µs to 80µs.

CDR Open-Drain Output

The CDR_ pins are active-low open-drain outputs, which are asserted during the fixed t_{OFF} decay interval enforced by the integrated current drive regulation loop. An external controller monitoring the CDR_ pins can determine whether the integrated current drive regulation loop has taken control of the driver overwriting the status of the PWM logic inputs (DIN1, DIN2).

The CDR_ signals can be used by an external controller for a variety of reasons and provides information about the actual load during current regulation. For example, in the use case where the PWM are permanently held in Forward or Reverse mode, control of the motor current is entrusted to the internal Current Drive Regulation loop and the CDR_ pin status directly reflects the driver output status. In this example, the duty cycle of the CDR_ pin can be used to detect stall conditions.

A pullup resistor must be connected from the CDR_ pins to the controller voltage supply. The pullup resistor choice depends on the PCB line capacitance, PWM frequency, and power consumption. Values between 1KΩ to 5KΩ satisfy the requirement for most applications.

The time diagram in Figure 2 shows the behavior of this function when the motor spins in forward direction respectively with DIN2 held firmly High (Case A) or when DIN2 is toggling (Case B and C).

The CDR output is asserted only when the slow decay mode is forced by the internal CDR.

Notice that any PWM transitions resets the fixed OFF Time of the CDR circuit. In Case B, the actual Slow Decay Interval is longer than t_{OFF} whereas in Case C, the actual Slow Decay OFF interval is shorter.

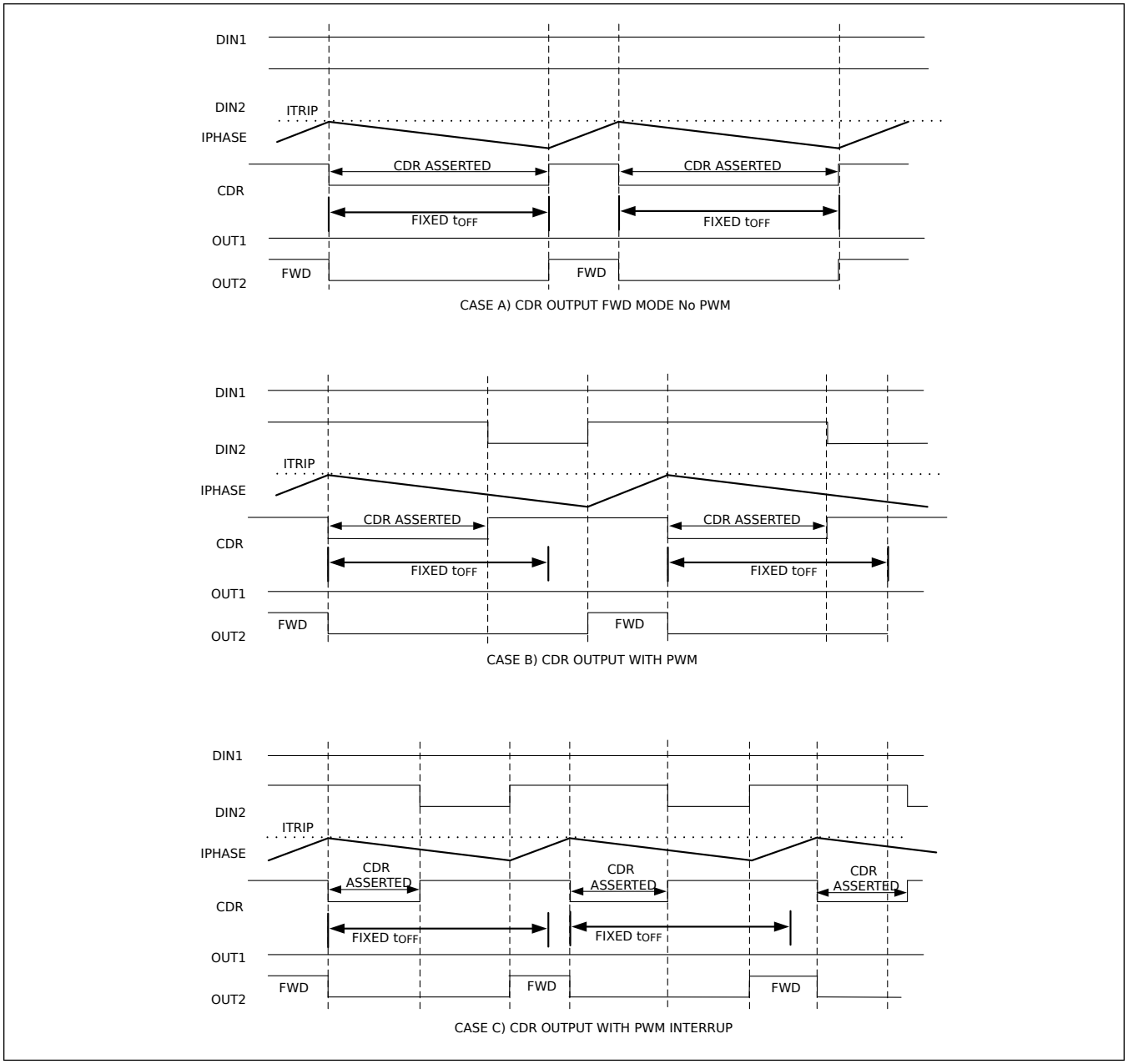


Figure 2. CDR Monitor Timing Diagram

Operating Modes

During PWM chopping, the driver output alternates Energizing (ON) and Decay phases. The MAX22203 supports different Decay modes. Slow Decay, Fast Decay, and different combination between Slow and Fast are supported.

Figure 3 shows the current path in the three different modes of operation.

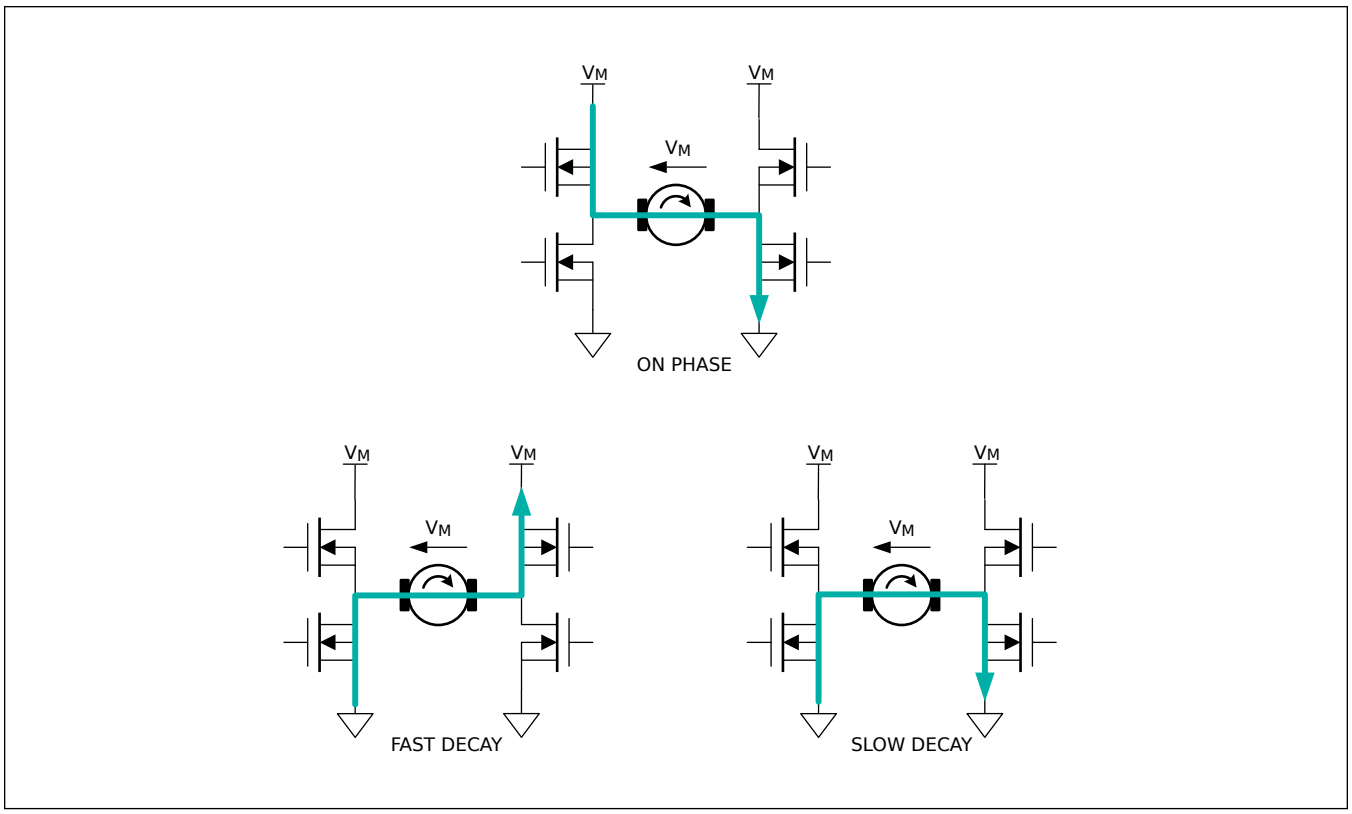


Figure 3. Current Flow During ON and Decay Modes

Setting the Decay Mode

Two logic input pins allow the user to set the Decay Mode during t_{OFF}. The MAX22203 supports Slow, Fast, and Mixed Decay modes.

Table 2 shows the Truth Table for the Decay selection.

Table 2. Decay Mode Truth Table

DECAY2	DECAY1	DECAY MODE
0	0	SLOW
0	1	MIXED 30% FAST* / 70% SLOW
1	0	MIXED 60% FAST* / 40% SLOW
1	1	FAST*

* To prevent reversal of current during fast decay, outputs go to the high-impedance state as the current approaches 0A.

Protections

Overcurrent Protection (OCP)

An Overcurrent Protection (OCP) protects the device against short circuits to the rails (supply voltage and ground) and across the load terminals. The OCP threshold is set at 3.8A minimum. If the output current is larger than the OCP threshold for longer than the OCP blanking time, then an OCP event is detected.

When an OCP event is detected, the H-Bridge is immediately disabled, and a fault indication is output on the pin $\overline{FAULT}$. The H-Bridge is kept in a high impedance mode for 3ms (see t_{RETRY} specification). After that, the H-Bridge is re-enabled according to the current state. If the short circuit is still present, this cycle repeats. Otherwise, normal operation resumes.

It is recommended to avoid prolonged operation under the short-circuit failure mode since a prolonged OCP auto-retry could affect the device reliability.

Thermal Shutdown Protection (TSD)

If the die temperature exceeds 155°C (typical value), a fault indication is output on pin $\overline{\text{FAULT}}$ and the driver is tri-stated until the junction temperature drops below 135°C. After that, the driver is re-enabled.

Undervoltage Lockout Protection (UVLO)

The device features Undervoltage Lockout Protection (UVLO). UVLO on V_M is set at 4.25V maximum. When an UVLO event occurs, a fault indication is output on pin $\overline{\text{FAULT}}$ and the driver outputs are tristated. Normal operation is then resumed (and the $\overline{\text{FAULT}}$ pin deasserted) as soon as the supply voltages are back in the nominal operating range.

Applications Information

Recommended Layout

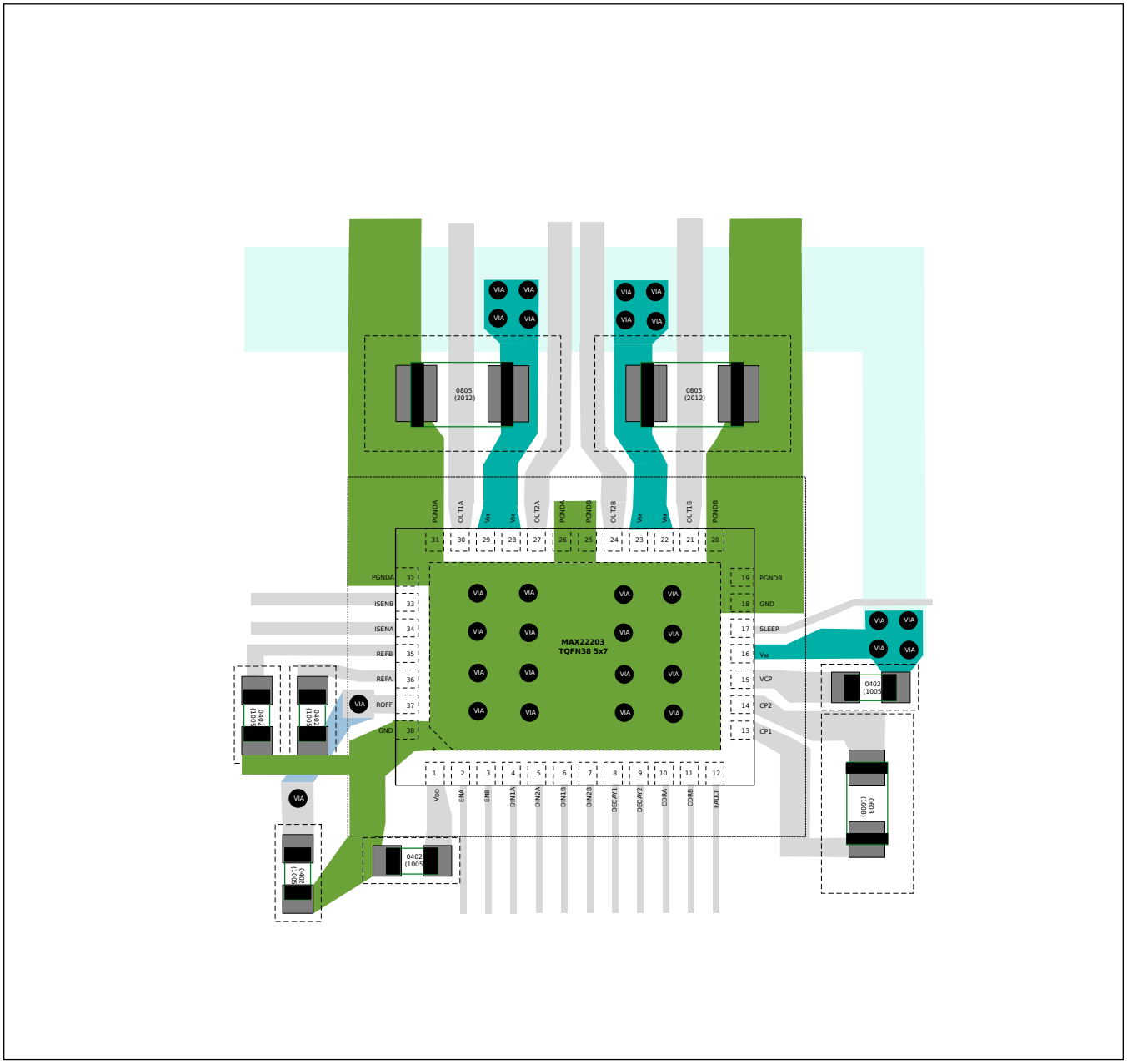
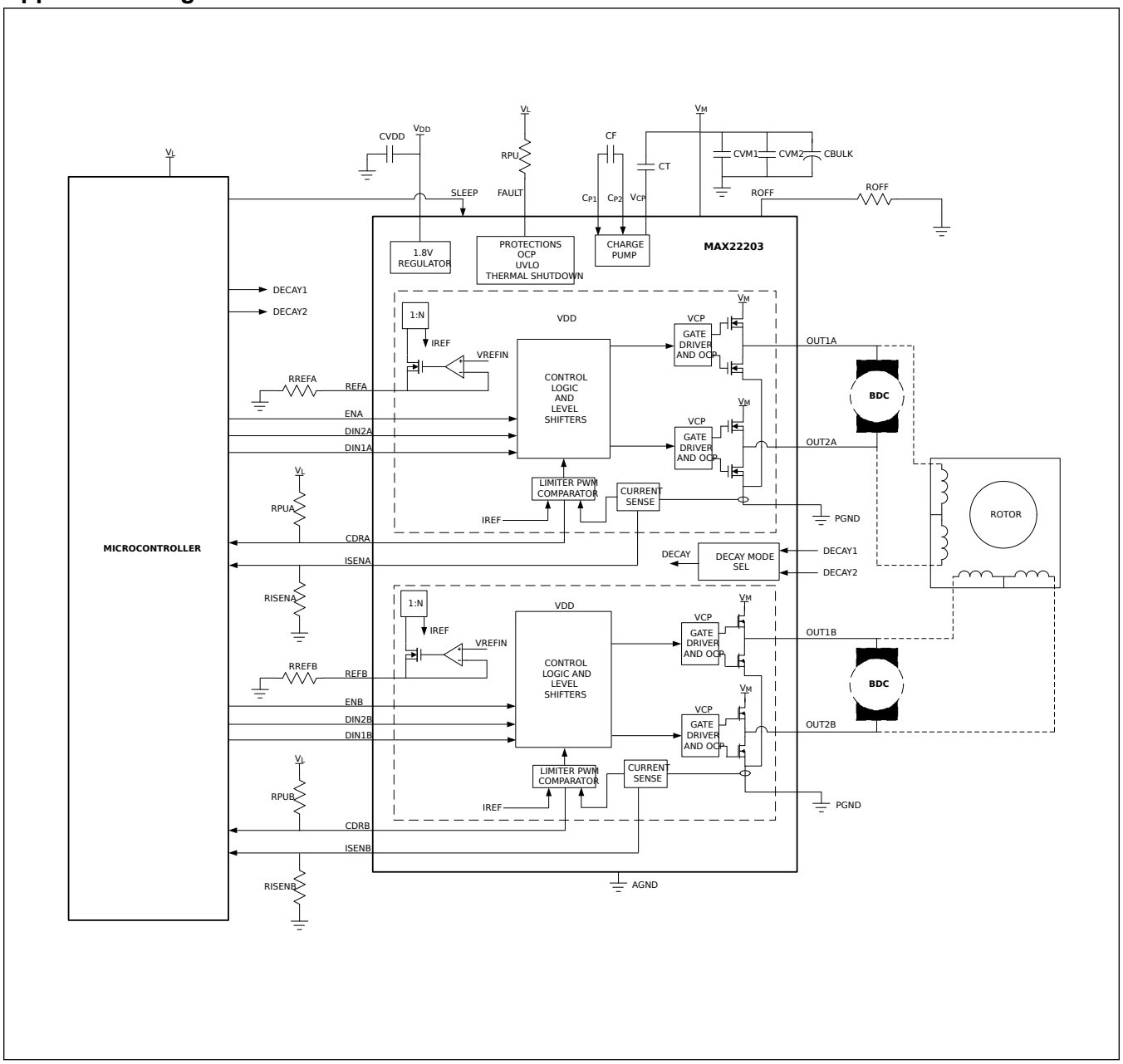


Figure 4. Recommended Layout

Typical Application Circuits

Application Diagram



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX22203ATU+	-40°C to +125°C	38 TQFN
MAX22203AHU+*	-40°C to +125°C	38 TSSOP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

** Denotes future product. Contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/21	Initial release	—

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