K Band Downconverter with Integrated Fractional-N PLL and VCO

Data Sheet

ADMV4420

FEATURES

- RF front end with integrated RF balun and LNA
- Double balanced, active mixer with high dynamic range IF amplifier
- Fractional-N synthesizer with low phase noise, multicore VCO
- 5 V supply operation with integrated LDO regulators
- Output P1dB: 7 dBm
- Output IP3: 16 dBm
- Conversion gain: 36 dB
- Noise figure: 7 dB
- RF input frequency range: 16.95 GHz to 22.05 GHz
- Internal LO frequency range: 16.35 GHz to 21.15 GHz
- IF frequency range: 900 MHz to 2500 MHz
- Single-ended 50 Ω input impedance and 75 Ω IF output impedance
- Programmable via 4-wire SPI
- 32-lead, 5 mm × 5 mm LFCSP

APPLICATIONS

- Satellite communication
- Point to point microwave communication

GENERAL DESCRIPTION

The ADMV4420 is a highly integrated, double balanced, active mixer with an integrated fractional-N synthesizer, ideally suited for next generation K band satellite communications.

The RF front end consists of an integrated RF balun and low noise amplifier (LNA) for an optimal, 7 dB, single-sideband noise figure while minimizing external components. Additionally, the high dynamic range IF output amplifier provides a nominal conversion gain of 36 dB.

An integrated low phase noise, fractional-N, phase-locked loop (PLL) with a multicore voltage controlled oscillator (VCO) and internal 2× multiplier generate the necessary on-chip LO signal for the double balanced mixer, eliminating the need for external frequency synthesis. The multicore VCO uses an internal autocalibration routine that allows the PLL to select the necessary settings and lock in approximately 400 µs.

The reference input to the PLL employs a differentially excited 50 MHz crystal oscillator. Alternatively, the reference input can be driven by an external, singled-ended, 50 MHz source. The phase frequency detector (PFD) comparison frequency of the PLL operates up to 50 MHz.

The ADMV4420 is fabricated on a silicon germanium (SiGe), bipolar complementary metal-oxide semiconductor (BiCMOS) process, and is available in a 32-lead, RoHS compliant, 5 mm × 5 mm LFCSP package with an exposed pad. The device is specified over the −40°C to +85°C temperature range on a 5 V power supply.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

4/2019—Rev. 0 to Rev. A

Change to Features Section....1
Changes to Local Oscillator (LO) Internal Frequency Range Parameter, VCO Frequency Range Parameter, and Conversion Gain Parameter, Table 1....5
Changes to IF = 900 MHz, Low-Side Injection LO Performance Section....10
Changes to IF = 1700 MHz, Low-Side Injection LO Performance Section....14
Changes to IF = 2500 MHz, Low-Side Injection LO Performance Section....18

10/2018—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

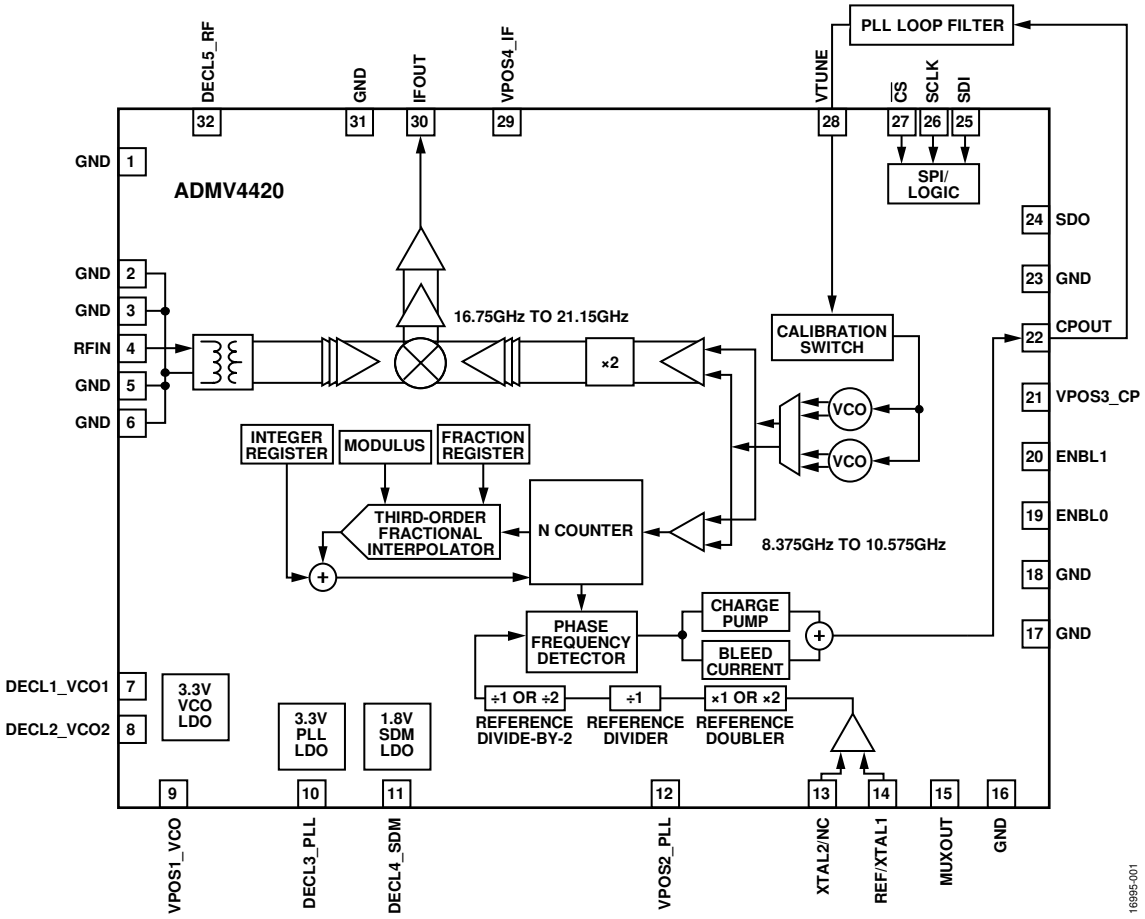


Figure 1.

SPECIFICATIONS

The measurements are performed at T_A = 25°C with 0 dBm external reference at 50 MHz when V_{VPOS1_VCO} = V_{VPOS2_PLL} = V_{VPOS3_CP} = V_{VPOS4_IF} = 5 V, RF input power = −40 dBm, and PLL loop filter bandwidth = 60 kHz with 45° of phase margin, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF INPUT					
Frequency Range	16.95		22.05	GHz	
Input Return Loss		−8.5		dB	
Input Impedance		50		Ω	Single-ended
LOCAL OSCILLATOR (LO) INTERNAL FREQUENCY RANGE	16.35		21.15	GHz	
VCO					
Frequency Range	8.175		10.575	GHz	
Tuning Sensitivity (k_{VCO})		50		MHz/V	Calculated with f_{VCO}/VTUNE
VTUNE	0		3	V	
IF OUTPUT					
IF Frequency Range	900		2500	MHz	
Conversion Gain					
IF = 900 MHz					
Low-Side Injection					
LO = 16.75 GHz	31	35		dB	RF = 17.65 GHz
LO = 18.95 GHz	33	39		dB	RF = 19.85GHz
LO = 21.15 GHz		32		dB	RF = 22.05 GHz
High-Side Injection					
LO = 17.85 GHz	28.5	33		dB	RF = 16.95 GHz
LO = 18.95 GHz	32.5	37		dB	RF = 18.05 GHz
LO = 21.15 GHz	29	40		dB	RF = 20.25 GHz
IF = 950 MHz					
Low-Side Injection					
LO = 16.35 GHz	29	32		dB	RF = 17.30 GHz
IF = 2500 MHz					
Low-Side Injection					
LO = 16.75 GHz	28.5	36		dB	RF = 19.25 GHz
LO = 17.95 GHz		38		dB	RF = 20.45 GHz
LO = 19.55 GHz		30		dB	RF = 22.05 GHz
High-Side Injection					
LO = 19.45 GHz	27	31		dB	RF = 16.95 GHz
LO = 20.45 GHz		35		dB	RF = 17.95 GHz
LO = 21.15 GHz		37		dB	RF = 18.65 GHz
Output 1 dB Compression Point (Output P1dB)		7		dBm	
Output Third-Order Intercept (Output IP3)		16		dBm	
Noise Figure		7		dB	Single sideband with appropriate filtering
Gain Flatness					
		±1		dB	Across any 250 MHz bandwidth for an IF of 900 MHz to 2000 MHz
		±2		dB	Across any 250 MHz bandwidth for an IF of 2000 MHz to 2500 MHz
Output Impedance		75		Ω	Single-ended
Output Return Loss		−6.5		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
V_{VPOS1_VCO}, V_{VPOS2_PLL}, V_{VPOS3_CP}, V_{VPOS4_IF}	4.75	5.00	5.25	V	
TOTAL POWER CONSUMPTION					
Active Mode		1900		mW	
Sleep Mode		80		mW	All blocks powered down
EXTERNAL PLL REFERENCE					
Frequency		50		MHz	
Amplitude	0.3		2.5	V p-p	Single-ended input, high impedance
CRYSTAL REFERENCE					
Crystal Frequency		50		MHz	Fundamental mode
Capacitance		10		pF	
PHASE FREQUENCY DETECTOR (PFD) FREQUENCY		50		MHz	Compare frequency
REFERENCE SPURS		−70		dBm	
FREQUENCY SETTLING		400		µs	After frequency change programmed; within 50 kHz resolution
CLOSED-LOOP PHASE NOISE					LO frequency = 16.75 GHz to 21.15 GHz
		−80		dBc/Hz	10 kHz offset
		−85		dBc/Hz	100 kHz offset
		−116		dBc/Hz	1 MHz offset
		−125		dBc/Hz	10 MHz offset
LOGIC					
(ENBL0, ENBL1, SDO, SDI, SCLK, $\overline{CS}$)					
Logic Low	−0.3	0	+0.5	V	
Logic High	1.2	3.3	3.6	V	

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (V_{VPOS1_VCO}, V_{VPOS2_PLL}, V_{VPOS3_CP}, and V_{VPOS4_IF}	5.5 V
Digital Input/Output Signal (SCLK, SDI, SDO, $\overline{CS}$, ENBL1, and ENBL0)	3.6 V
RFIN	0 dBm
Source and Sink Current (MUXOUT)	300 µA
Maximum Junction Temperature	125°C
Peak Reflow Temperature	260°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	500 V[1]
	2000 V[2]
	1500 V[3]
Field Induced Charged Device Model (FICDM)[1]	500 V

[1] Applies to all pins of the ADMV4420.
[2] Applies to all pins except the MUXOUT, ENBL0, ENBL1, SDO, SDI, SCLK, and $\overline{CS}$ pins.
[3] Applies to the MUXOUT, ENBL0, ENBL1, SDO, SDI, SCLK, and $\overline{CS}$ pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

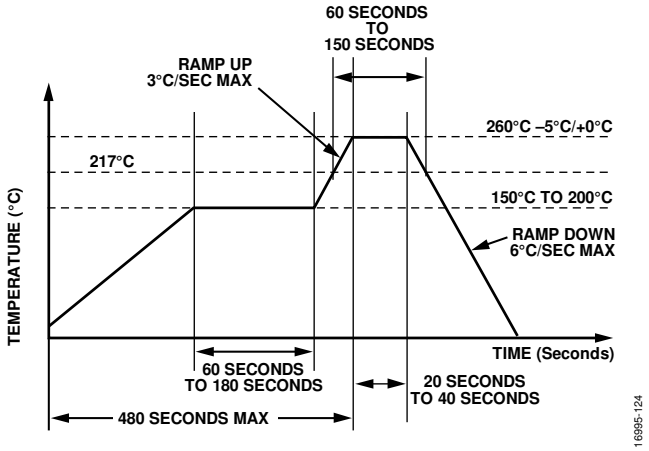


Figure 2. Pb-Free Reflow Solder Profile

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	θ_{JA}[1]	Unit
CP-32-12	7.25	39.6	°C/W

[1] The θ_{JA} and θ_{JC} values are determined by measuring the thermally designed PCB with a heat sink.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

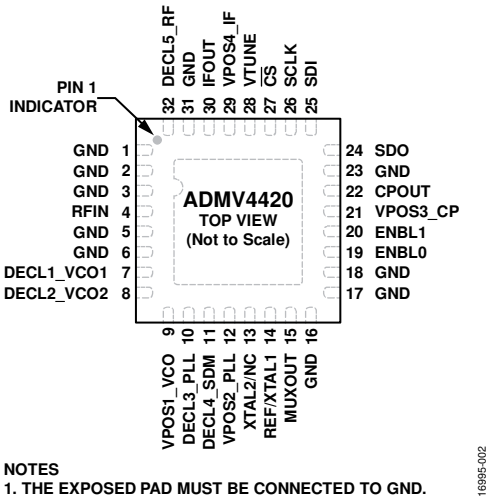


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 3, 5, 6, 16, 17, 18, 23, 31	GND	Ground. Connect these pins and package bottom to RF and dc ground. See Figure 4 for the GND interface schematic.
4	RFIN	RF Input Pin. This pin has a 50 Ω input impedance.
7, 8	DECL1_VCO1, DECL2_VCO2	LDO Regulator Decoupling Pin. Place a 10 µF capacitor close to this pin.
9	VPOS1_VCO	5 V Power Supply Pin. Place 0.1 µF and 100 pF decoupling capacitors close to this pin.
10, 11, 32	DECL3_PLL, DECL4_SDM, DECL5_RF	LDO Decoupling Pin. Place a 10 µF capacitor close to this pin.
12	VPOS2_PLL	5 V Power Supply. Place the 0.1 µF and 100 pF decoupling capacitor close to this pin.
13	XTAL2/NC	Crystal Input or No Connect. When using an external crystal, place the crystal between the REF/XTAL1 and XTAL2/DNC pins. When an external reference input signal is applied through the REF/XTAL1 pin, this pin is used as a No Connect pin. Connect this pin to ground with a 1 nF capacitor (ac ground) when an external reference input signal is applied through the REF/XTAL1 pin.
14	REF/XTAL1	External Reference Input or Crystal Input. When using an external crystal, place the crystal between the XTAL1 and XTAL2 pins. When using as external reference input, apply an external reference signal to this pin with a 0.01 µF, dc blocking capacitor. Refer to Figure 121 for the external reference input configuration. This pin is internally biased to 1.65 V.
15	MUXOUT	PLL Multiplexer Output.
19	ENBL0	Device Enable 0. For nominal operation, keep this pin tied to 3.3 V.
20	ENBL1	Device Enable 1. For nominal operation, keep this pin tied to 3.3 V
21	VPOS3_CP	5 V Power Supply. Place the 0.1 µF and 100 pF decoupling capacitor close to this pin.
22	CPOUT	Synthesizer Charge Pump Output. Connect this pin to VTUNE (Pin 28) through the loop filter
24	SDO	Serial Peripheral Interface (SPI) Data Output. 3.3 V logic.
25	SDI	SPI Data Input. 3.3 V logic.
26	SCLK	SPI Clock. 3.3 V logic.
27	$\overline{CS}$	SPI Chip Select. 3.3 V logic. Active low.
28	VTUNE	VCO Tuning Voltage. This pin is driven by the output of the loop filter.
29	VPOS4_IF	5 V Power Supply. Place 0.1 µF and 100 pF decoupling capacitors close to this pin.
30	IFOUT	IF Output. This pin has a 75 Ω output impedance. The output stage of the IF amplifier is an open-collector configuration and requires a dc bias of 5 V. Use a bias choke inductor. See the IF Output—External Inductor/Biasing section for more details.
	EPAD	Exposed Pad. The exposed pad must be connected to GND.

INTERFACE SCHEMATICS

Figure 4. GND Interface Schematic

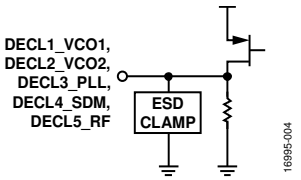


Figure 5. DECL1_VCO1, DECL2_VCO2, DECL3_PLL, DECL4_SDM, and DECL5_RF Interface Schematic

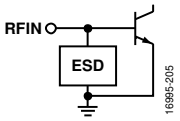


Figure 6. RFIN Interface Schematic

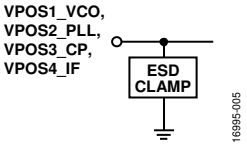


Figure 7. VPOS1_VCO, VPOS2_PLL, VPOS3_CP, and VPOS4_IF Interface Schematic

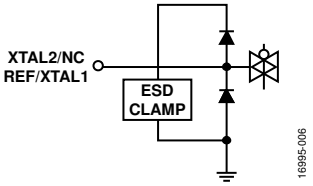


Figure 8. XTAL2/NC and REF/XTAL1 Interface Schematic

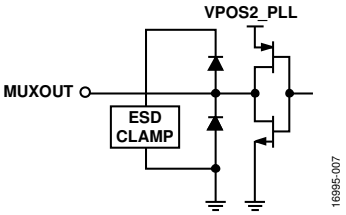


Figure 9. MUXOUT Interface Schematic

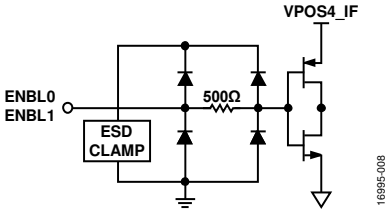


Figure 10. ENBL0 and ENBL1 Interface Schematic

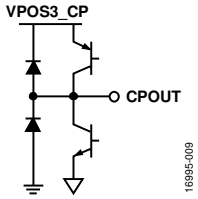


Figure 11. CPOUT Interface Schematic

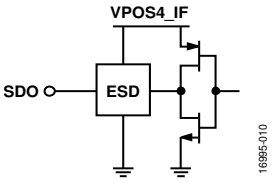


Figure 12. SDO Interface Schematic

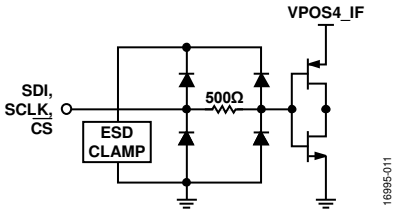


Figure 13. SDI, SCLK, and $\overline{CS}$ Interface Schematic

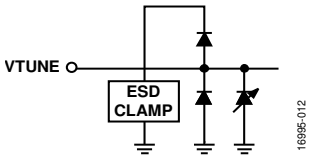


Figure 14. VTUNE Interface Schematic

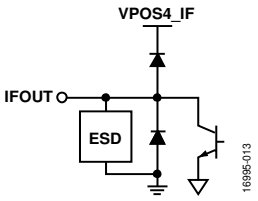


Figure 15. IFOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

A 0 dBm external reference at 50 MHz is used with $V_{VPOS1\_VCO} = V_{VPOS2\_PLL} = V_{VPOS3\_CP} = V_{VPOS4\_IF} = 5$ V, RF input power = −40 dBm, and the PLL loop filter bandwidth = 60 kHz with 45° of phase margin, unless otherwise noted.

IF = 900 MHz, LOW-SIDE INJECTION LO PERFORMANCE

RF minimum and maximum frequencies are limited by the LO frequency = 16.75 GHz to 21.15 GHz.

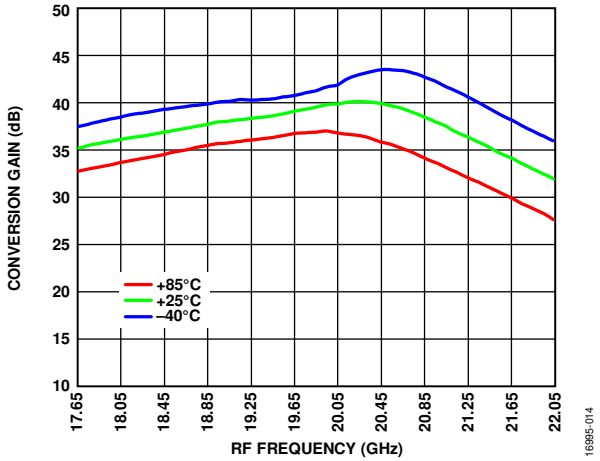


Figure 16. Conversion Gain vs. RF Frequency at Various Temperatures

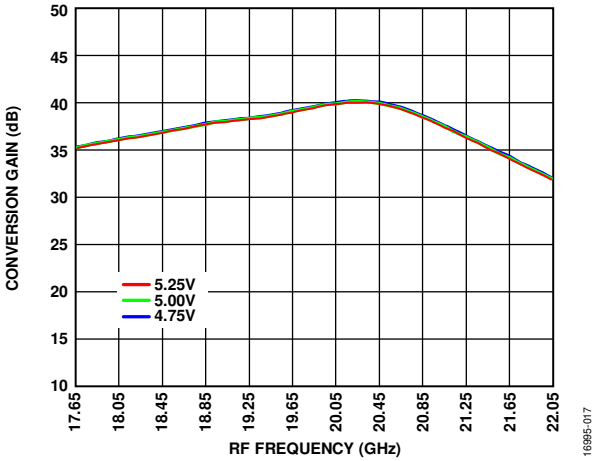


Figure 18. Conversion Gain vs. RF Frequency at Various Supply Voltages, $T_A = 25°C$

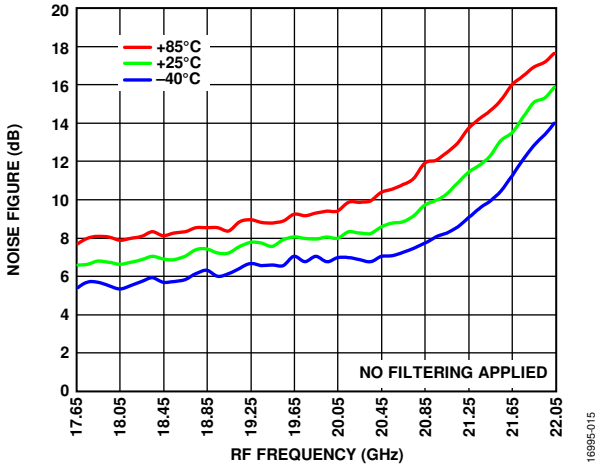


Figure 17. Noise Figure vs. RF Frequency at Various Temperatures

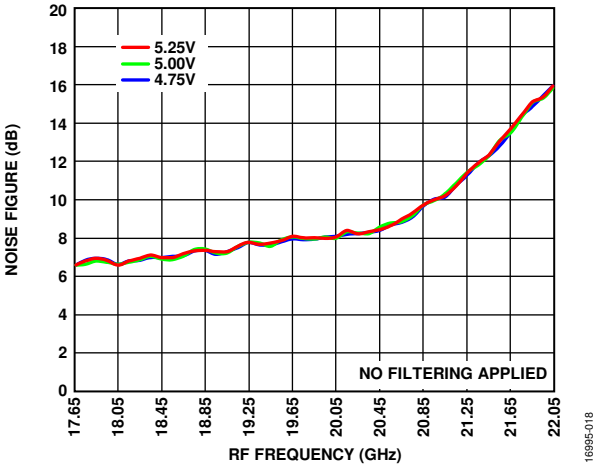


Figure 19. Noise Figure vs. RF Frequency at Various Supply Voltages, $T_A = 25°C$

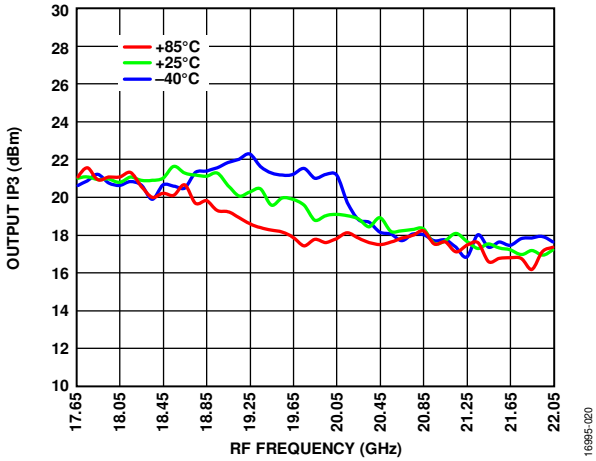


Figure 20. Output IP3 vs. RF Frequency at Various Temperatures

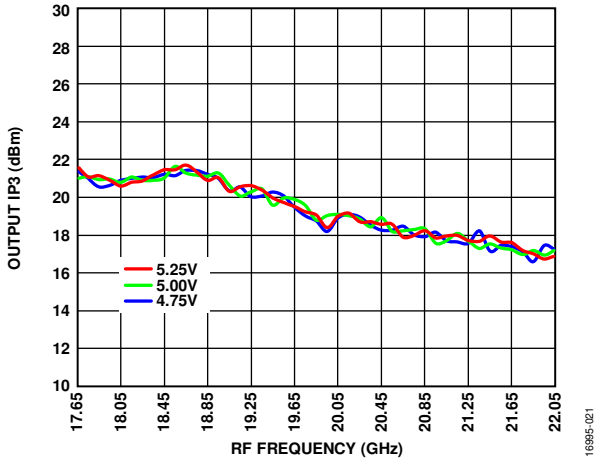


Figure 22. Output IP3 vs. RF Frequency at Various Supply Voltages, T_A = 25°C

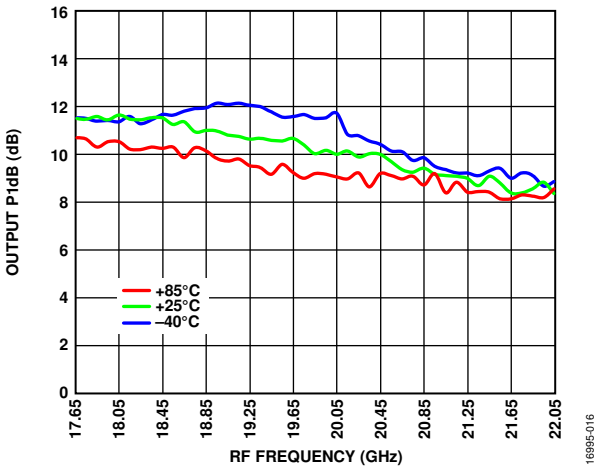


Figure 21. Output P1dB vs. RF Frequency at Various Supply Voltages, T_A = 25°C

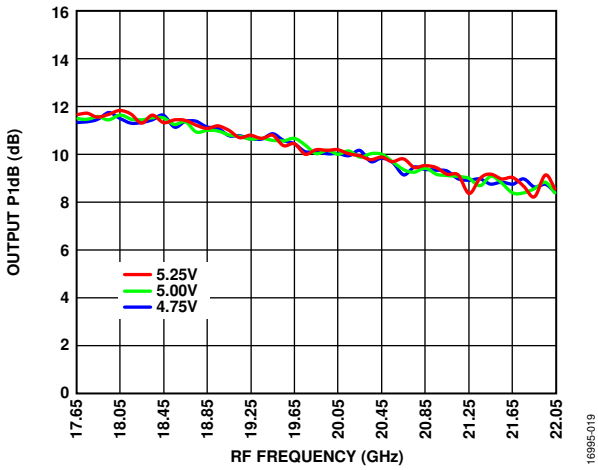


Figure 23. Output P1dB vs. RF Frequency at Various Temperatures

IF = 900 MHz, HIGH-SIDE INJECTION LO PERFORMANCE

The RF minimum frequency is limited at 16.95 GHz for optimal performance and the RF maximum frequency is limited at the maximum LO frequency (21.15 GHz).

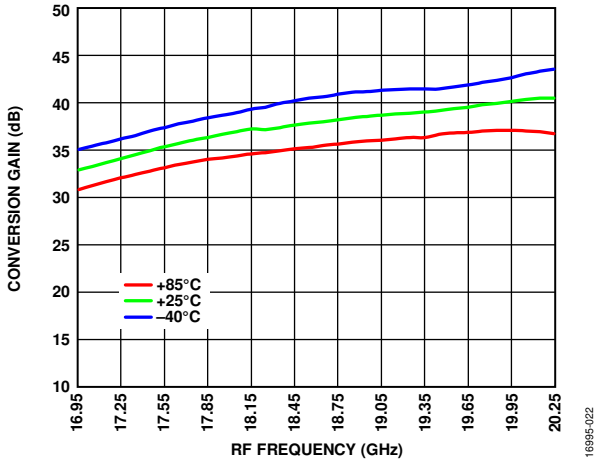


Figure 24. Conversion Gain vs. RF Frequency at Various Temperatures

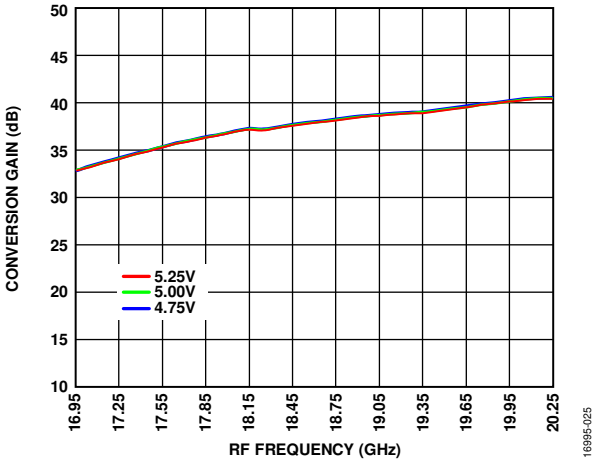


Figure 27. Conversion Gain vs. RF Frequency at Various Supply Voltages, T_A = 25°C

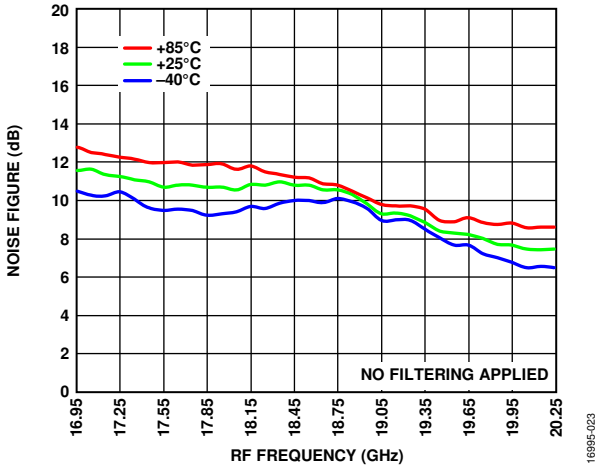


Figure 25. Noise Figure vs. RF Frequency at Various Temperatures

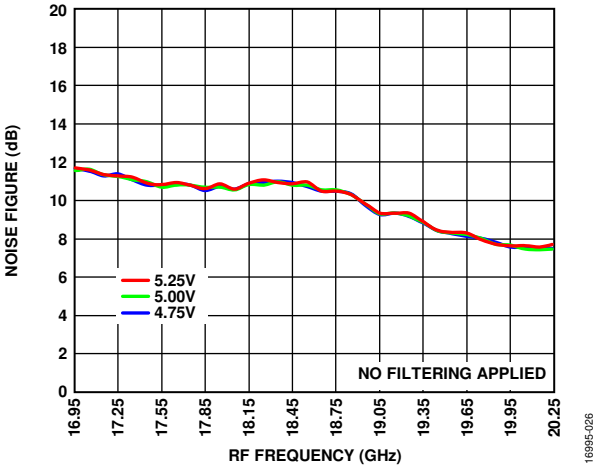


Figure 28. Noise Figure vs. RF Frequency at Various Supply Voltages, T_A = 25°C

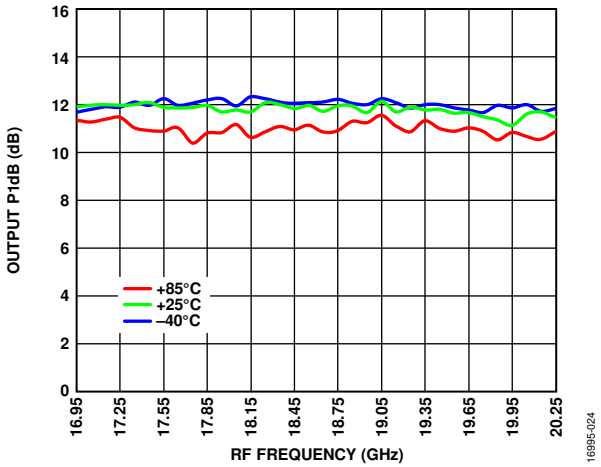


Figure 26. Output P1dB vs. RF Frequency at Various Temperatures

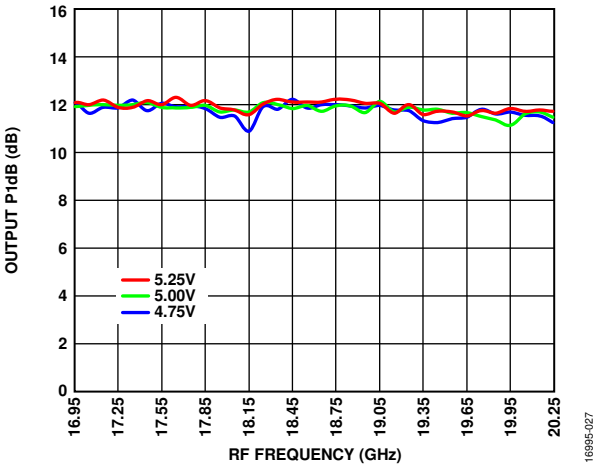


Figure 29. Output P1dB vs. RF Frequency at Various Supply Voltages, T_A = 25°C

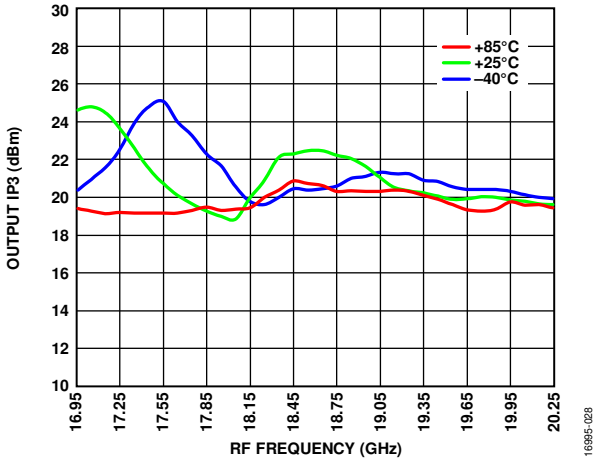


Figure 30. Output IP3 vs. RF Frequency at Various Temperatures

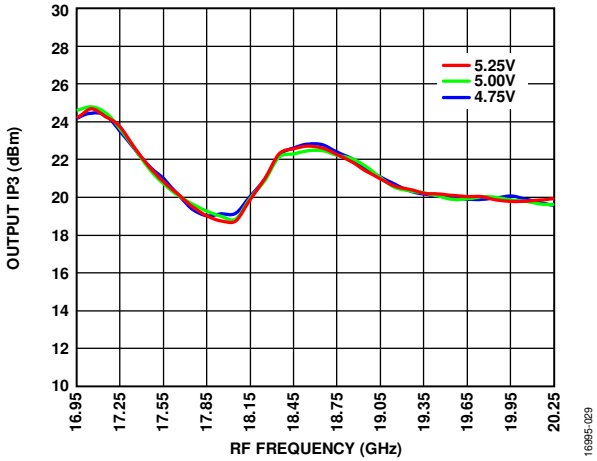


Figure 31. Output IP3 vs. RF Frequency at Various Supply Voltages, T_A = 25°C

IF = 1700 MHz, LOW-SIDE INJECTION LO PERFORMANCE

The RF minimum frequency is limited at the LO frequency of 16.75 GHz and the RF maximum frequency is limited at 22.05 GHz for optimal performance.

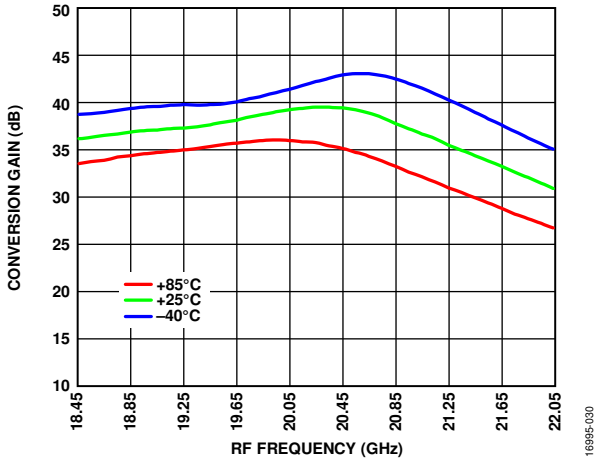


Figure 32. Conversion Gain vs. RF Frequency at Various Temperatures

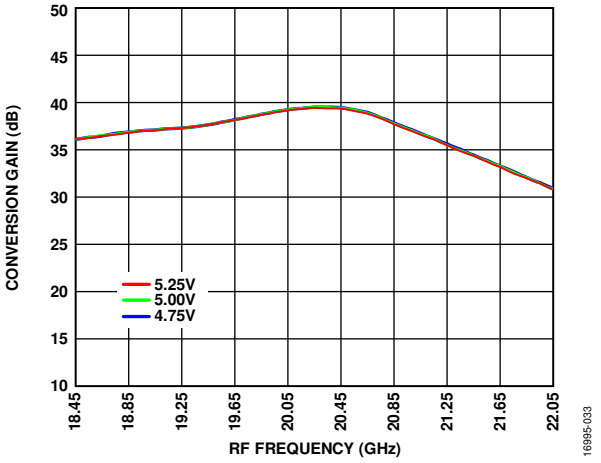


Figure 35. Conversion Gain vs. RF Frequency at Various Supply Voltages, T_A = 25°C

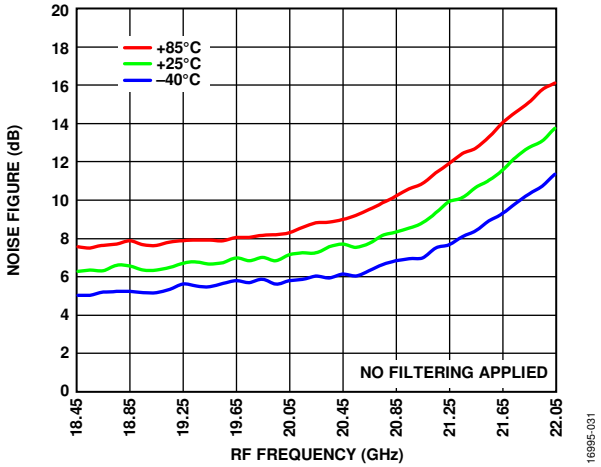


Figure 33. Noise Figure vs. RF Frequency at Various Temperatures

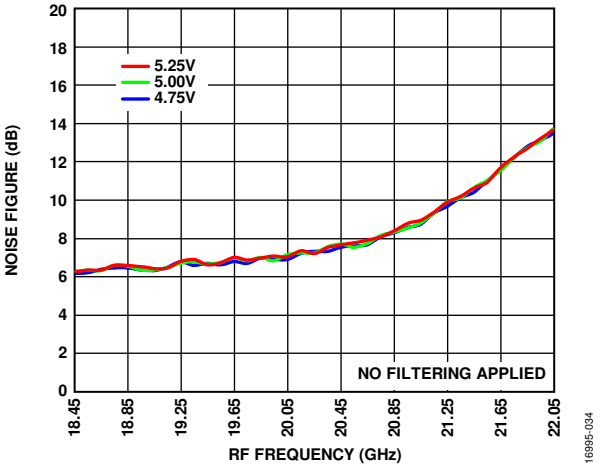


Figure 36. Noise Figure vs. RF Frequency at Various Supply Voltages, T_A = 25°C

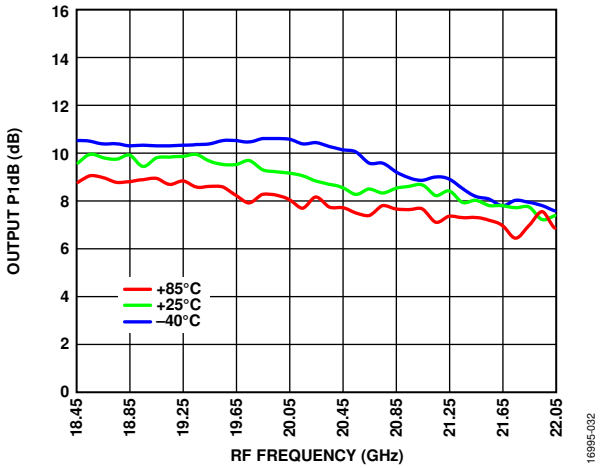


Figure 34. Output P1dB vs. RF Frequency at Various Temperatures

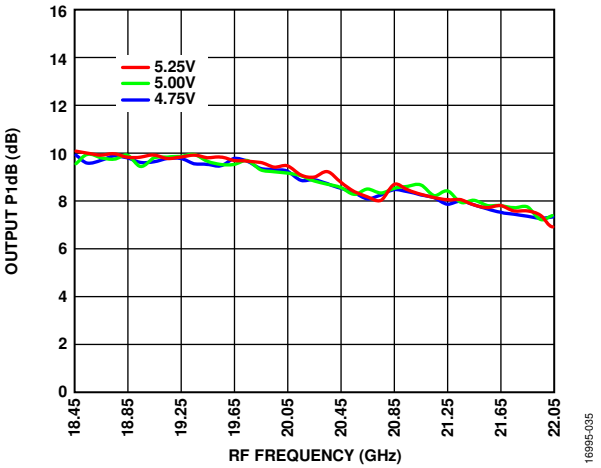


Figure 37. Output P1dB vs. RF Frequency at Various Supply Voltages, T_A = 25°C

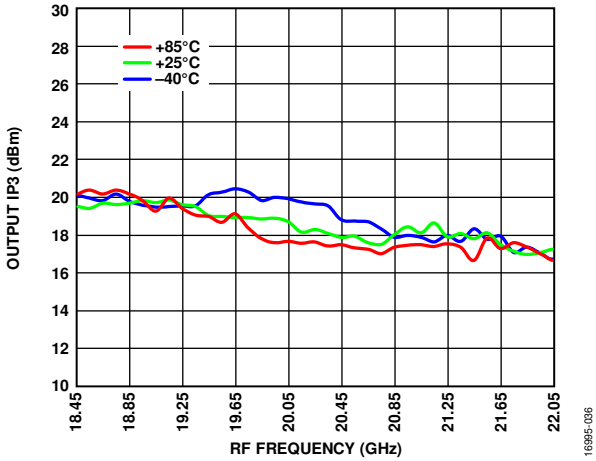


Figure 38. Output IP3 vs. RF Frequency at Various Temperatures

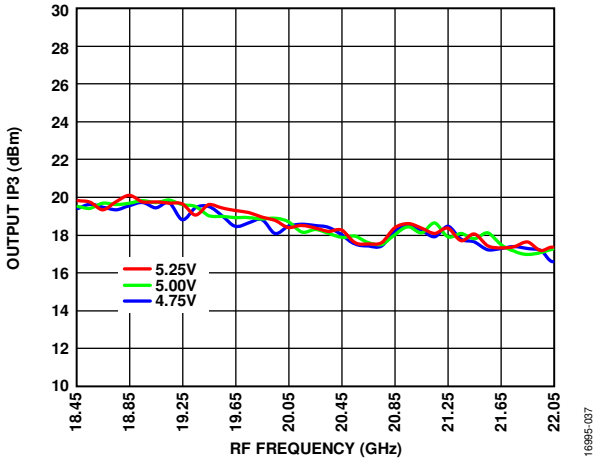


Figure 39. Output IP3 vs. RF Frequency at Various Supply Voltages, $T_A = 25°C$

IF = 1700 MHz, HIGH-SIDE INJECTION LO PERFORMANCE

The RF minimum frequency is limited at 16.95 GHz for optimum performance and the RF maximum frequency is limited at the maximum LO frequency (21.15 GHz).

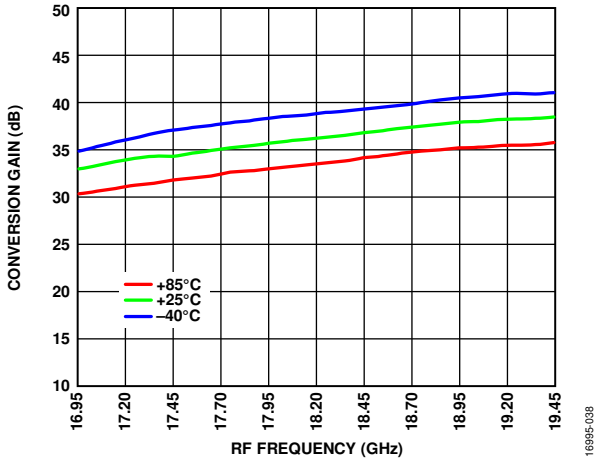


Figure 40. Conversion Gain vs. RF Frequency at Various Temperatures

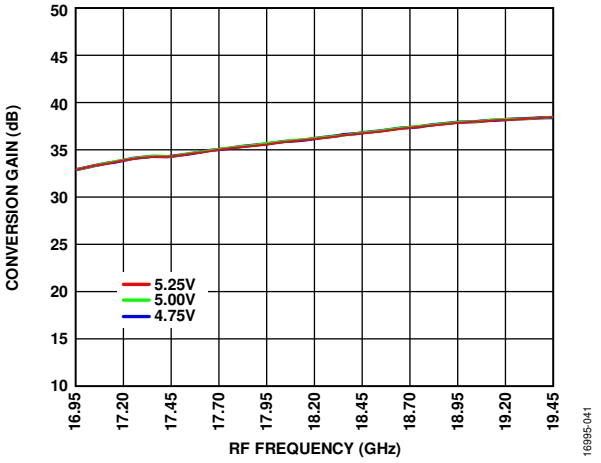


Figure 43. Conversion Gain vs. RF Frequency at Various Supply Voltages, T_A = 25°C

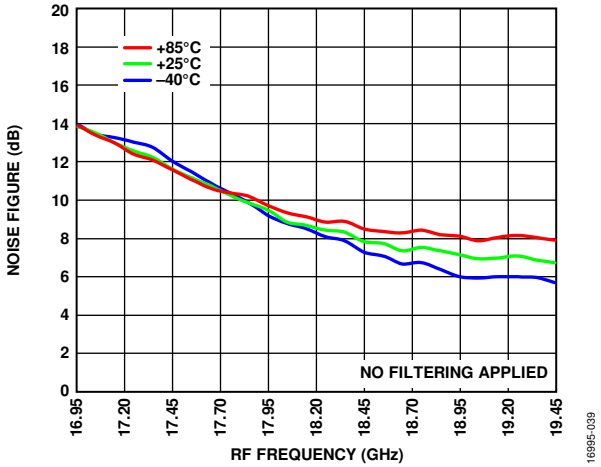


Figure 41. Noise Figure vs. RF Frequency at Various Temperatures

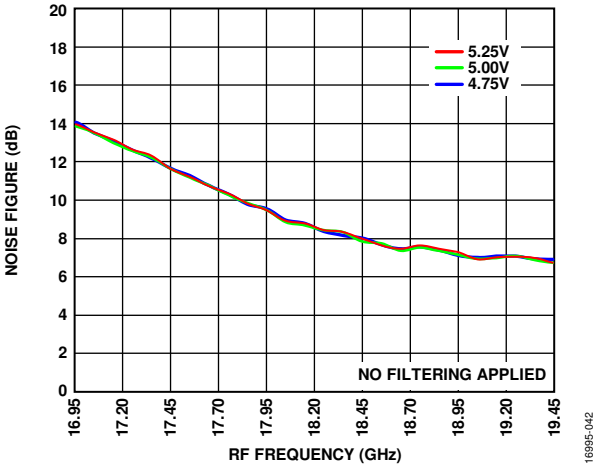


Figure 44. Noise Figure vs. RF Frequency at Various Supply Voltages, T_A = 25°C

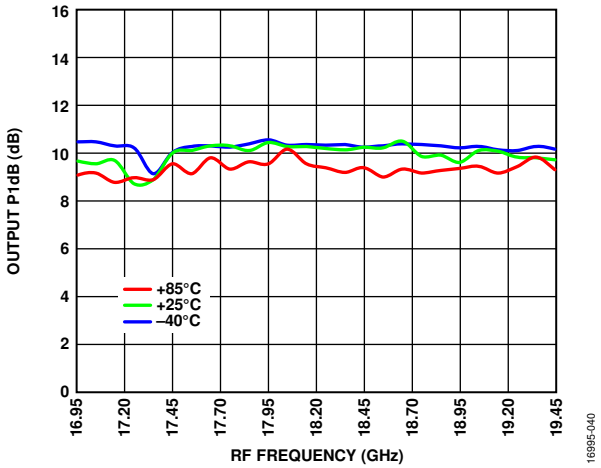


Figure 42. Output P1dB vs. RF Frequency at Various Temperatures

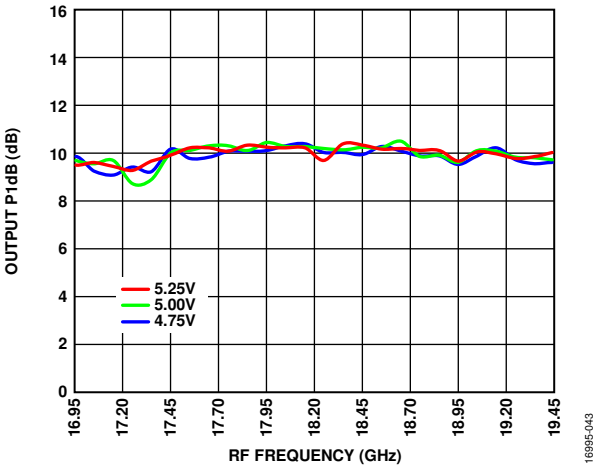


Figure 45. Output P1dB vs. RF Frequency at Various Supply Voltages, T_A = 25°C

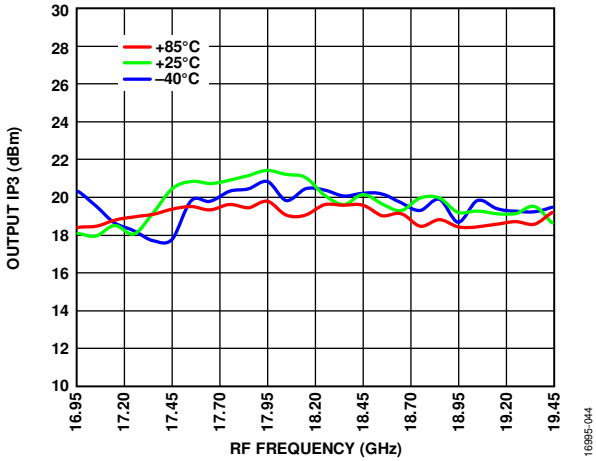


Figure 46. Output IP3 vs. RF Frequency at Various Temperatures

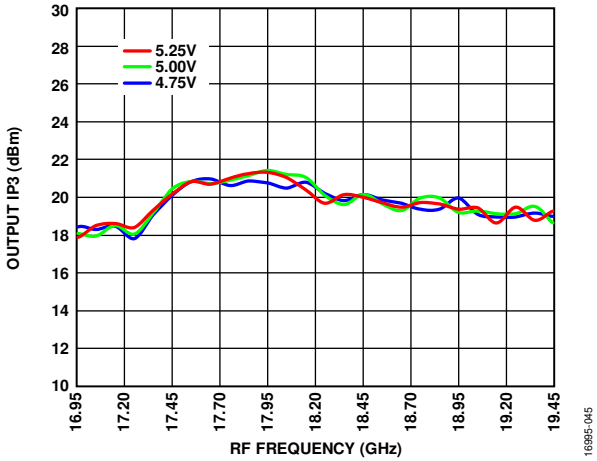


Figure 47. Output IP3 vs. RF Frequency at Various Supply Voltages, T_A = 25°C

IF = 2500 MHz, LOW-SIDE INJECTION LO PERFORMANCE

In this configuration, the RF minimum frequency is limited at the LO frequency of 16.75 GHz and the RF maximum frequency is limited at 22.05 GHz for optimal performance.

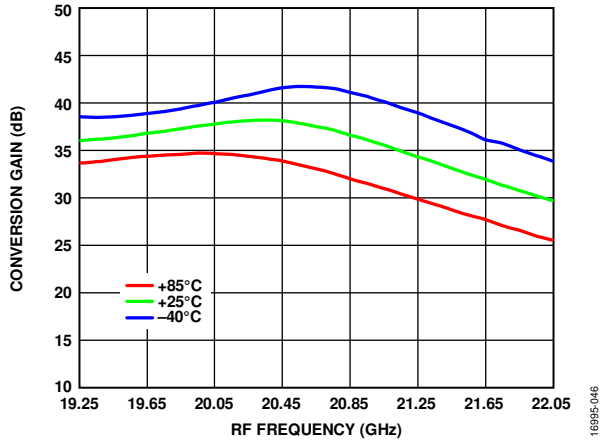


Figure 48. Conversion Gain vs. RF Frequency at Various Temperatures

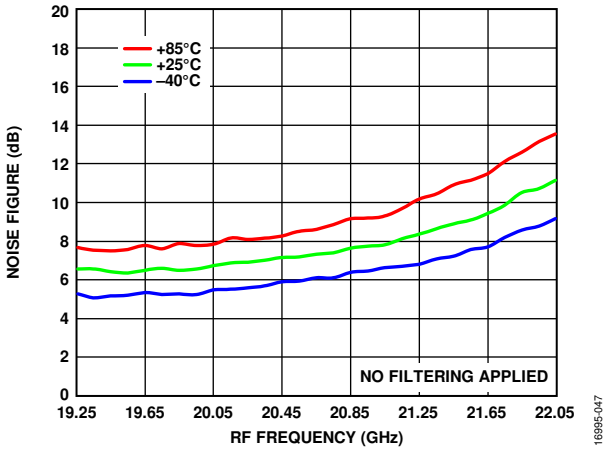


Figure 49. Noise Figure vs. RF Frequency at Various Temperatures

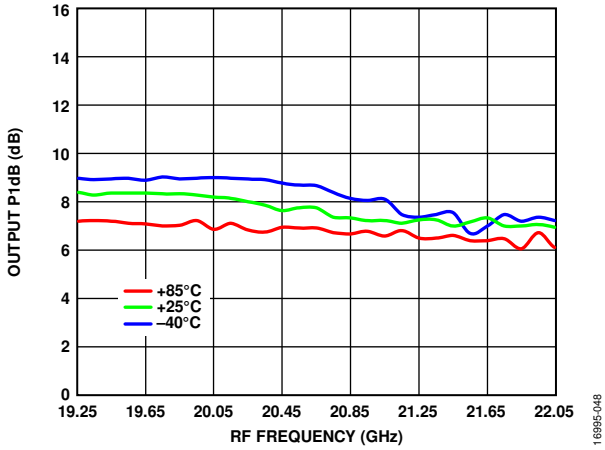


Figure 50. Output P1dB vs. RF Frequency at Various Temperatures

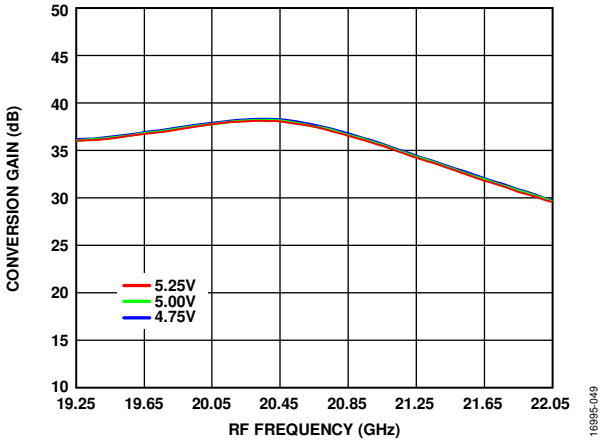


Figure 51. Conversion Gain vs. RF Frequency at Various Supply Voltages, T_A = 25°C

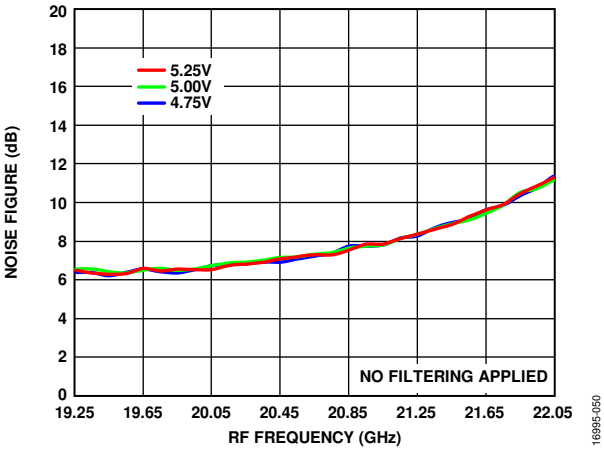


Figure 52. Noise Figure vs. RF Frequency at Various Supply Voltages, T_A = 25°C

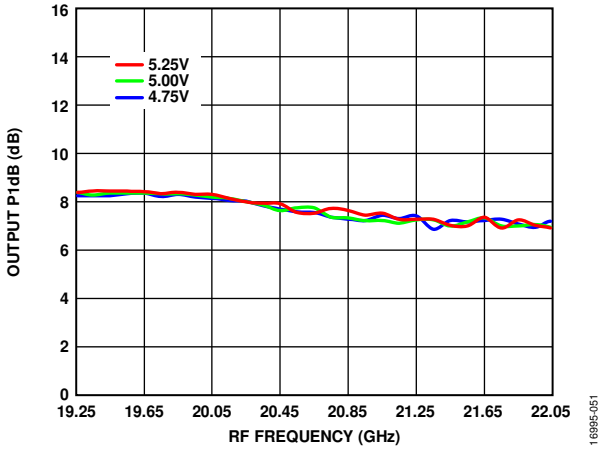


Figure 53. Output P1dB vs. RF Frequency at Various Supply Voltages, T_A = 25°C

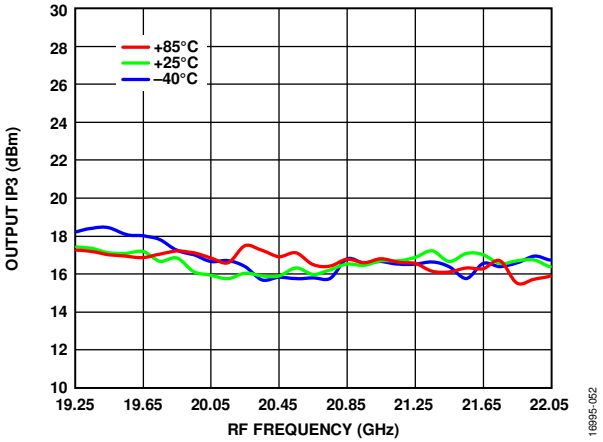


Figure 54. Output IP3 vs. RF Frequency at Various Temperatures

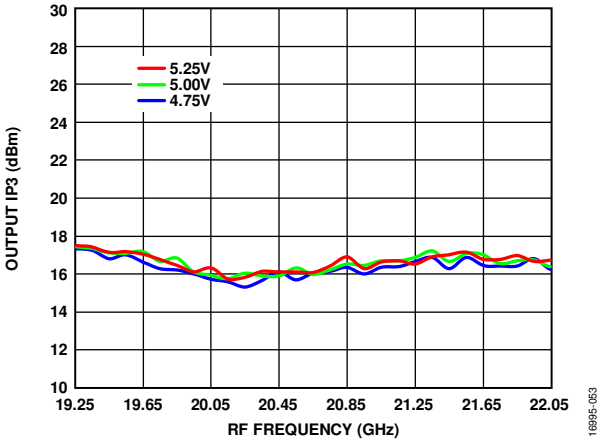


Figure 55. Output IP3 vs. RF Frequency at Various Supply Voltages, T_A = 25°C

IF = 2500 MHz, HIGH-SIDE INJECTION LO PERFORMANCE

The RF minimum frequency is limited at 16.95 GHz for optimal performance and the RF maximum frequency is limited at the maximum LO frequency (21.15 GHz).

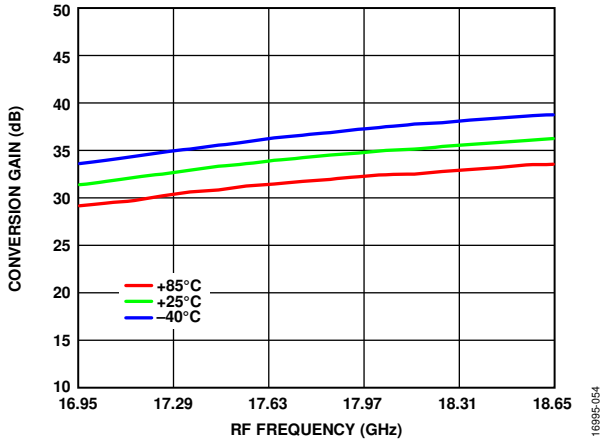


Figure 56. Conversion Gain vs. RF Frequency at Various Temperatures

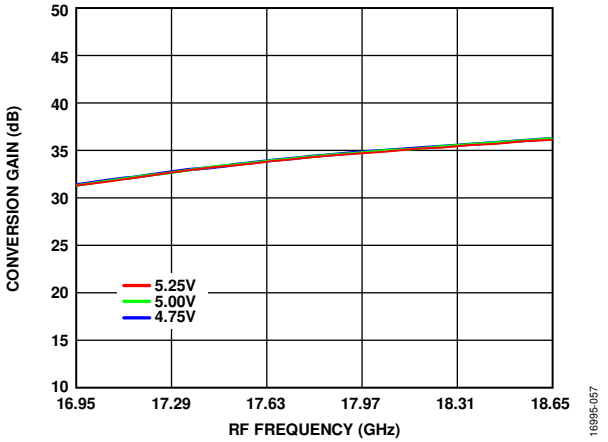


Figure 59. Conversion Gain vs. RF Frequency at Various Supply Voltages, T_A = 25°C

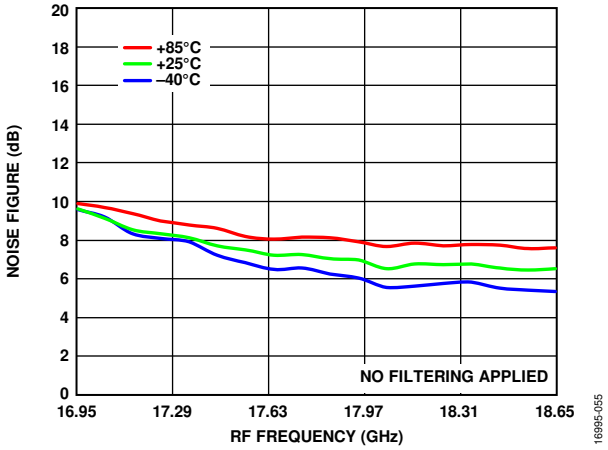


Figure 57. Noise Figure vs. RF Frequency at Various Temperatures

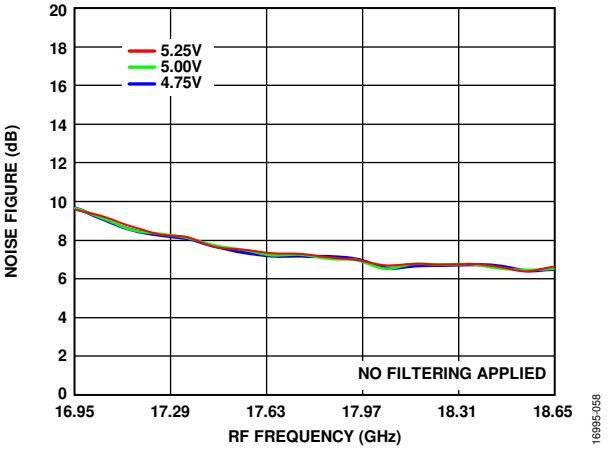


Figure 60. Noise Figure vs. RF Frequency at Various Supply Voltages, T_A = 25°C

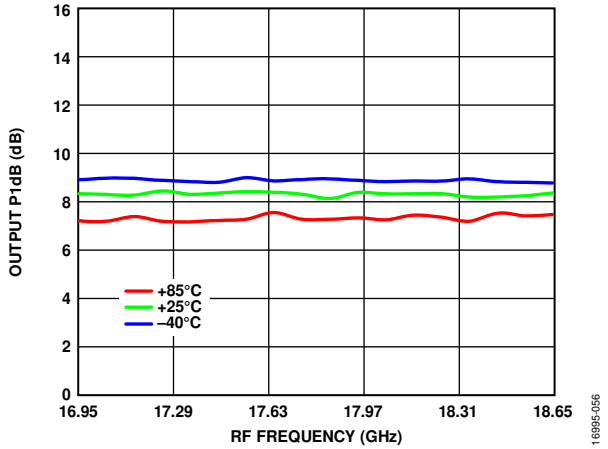


Figure 58. Output P1dB vs. RF Frequency at Various Temperatures

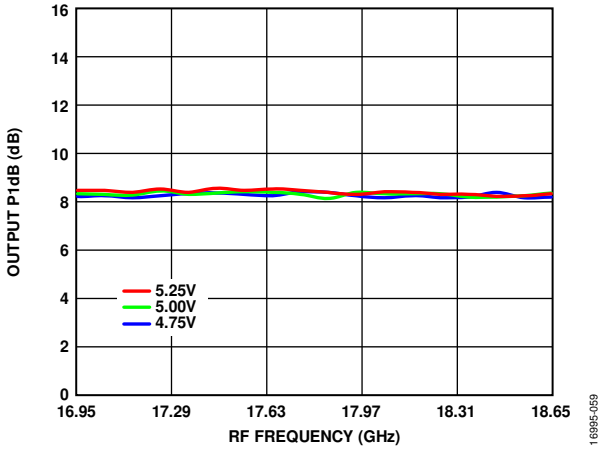


Figure 61. Output P1dB vs. RF Frequency at Various Supply Voltages, T_A = 25°C

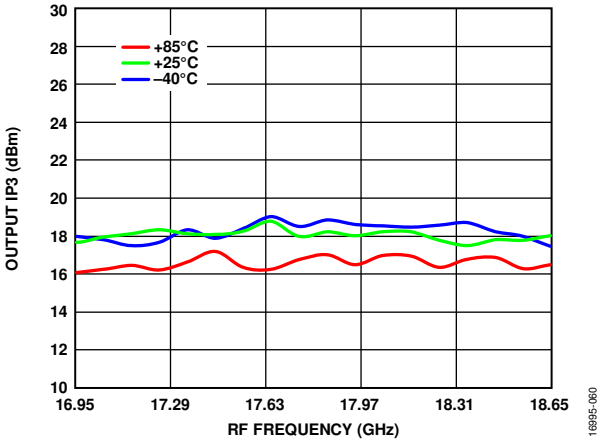


Figure 62. Output IP3 vs. RF Frequency at Various Temperatures

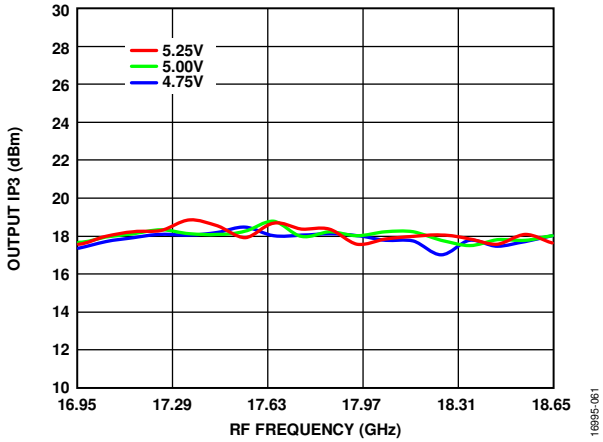


Figure 63. Output IP3 vs. RF Frequency at Various Supply Voltages, T_A = 25°C

LO = 16.75 GHz, LOW-SIDE INJECTION PERFORMANCE

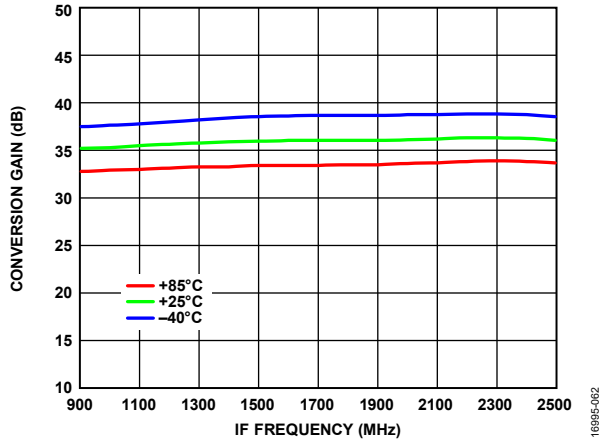


Figure 64. Conversion Gain vs. IF Frequency at Various Temperatures

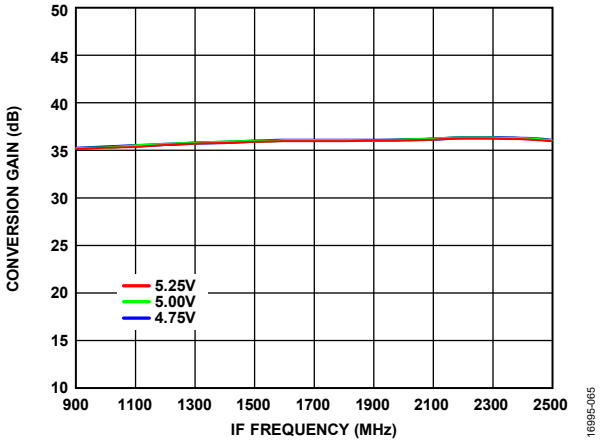


Figure 67. Conversion Gain vs. IF Frequency at Various Supply Voltages, $T_A = 25°C$

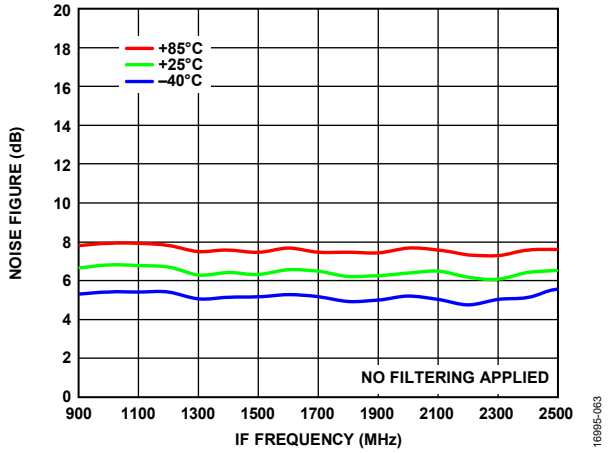


Figure 65. Noise Figure vs. IF Frequency at Various Temperatures

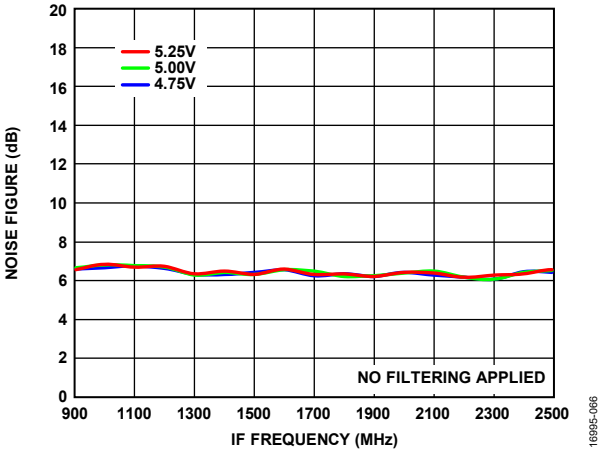


Figure 68. Noise Figure vs. IF Frequency at Various Supply Voltages, $T_A = 25°C$

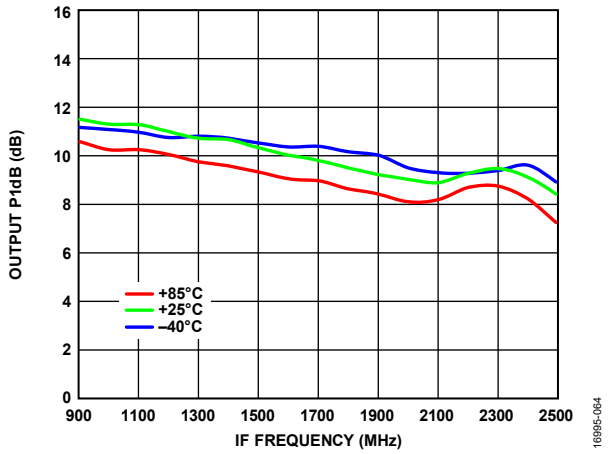


Figure 66. Output P1dB vs. IF Frequency at Various Temperatures

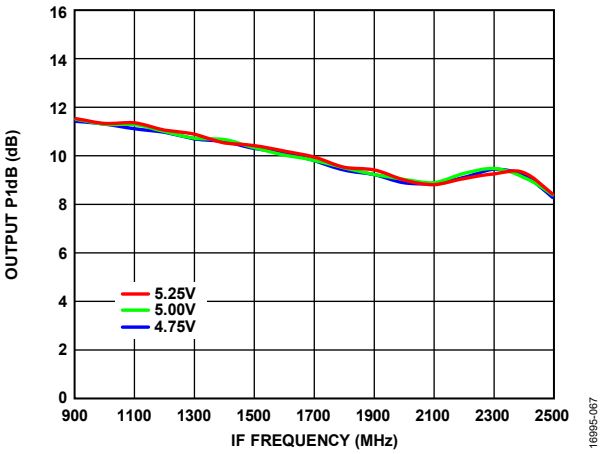


Figure 69. Output P1dB vs. IF Frequency at Various Supply Voltages, $T_A = 25°C$

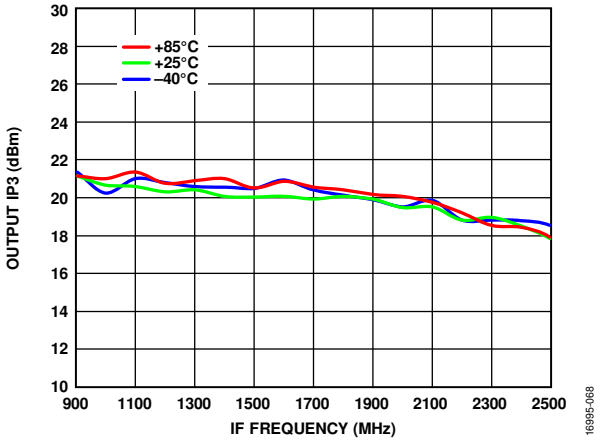


Figure 70. Output IP3 vs. IF Frequency at Various Temperatures

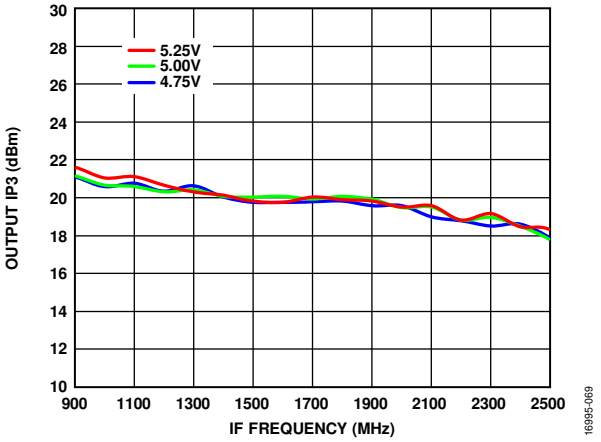


Figure 71. Output IP3 vs. IF Frequency at Various Supply Voltages, T_A = 25°C

LO = 16.75 GHz, HIGH-SIDE INJECTION PERFORMANCE

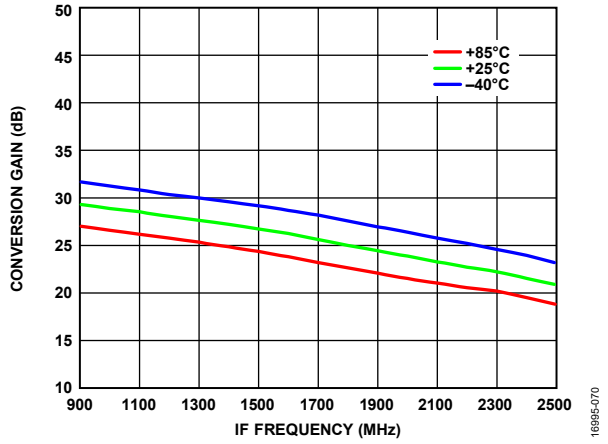


Figure 72. Conversion Gain vs. IF Frequency at Various Temperatures

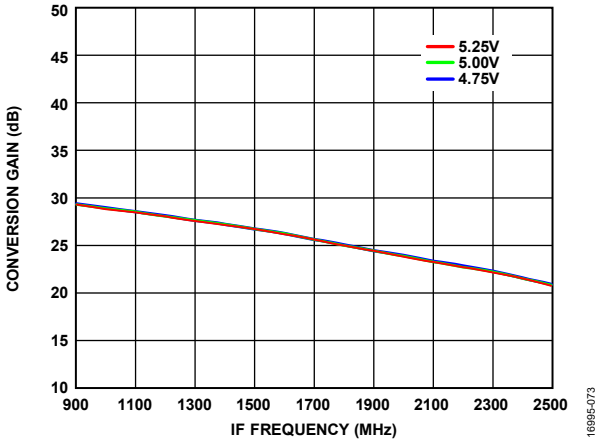


Figure 75. Conversion Gain vs. IF Frequency at Various Supply Voltages, $T_A = 25°C$

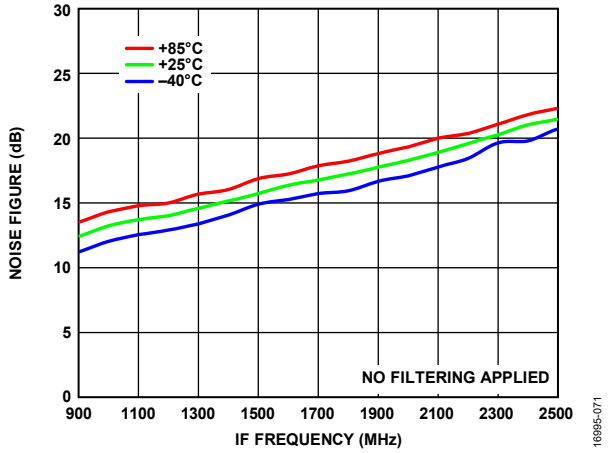


Figure 73. Noise Figure vs. IF Frequency at Various Temperatures

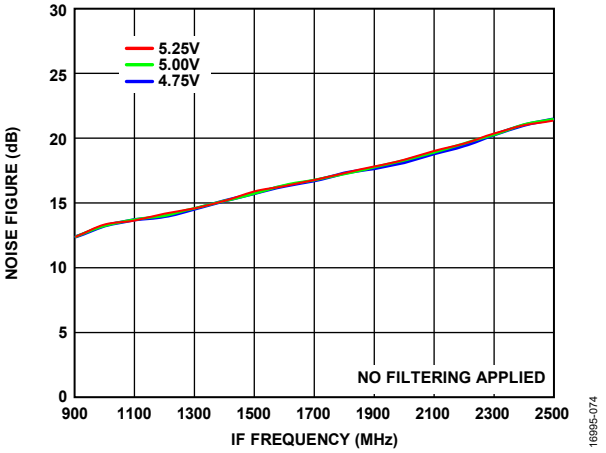


Figure 76. Noise Figure vs. IF Frequency at Various Supply Voltages, $T_A = 25°C$

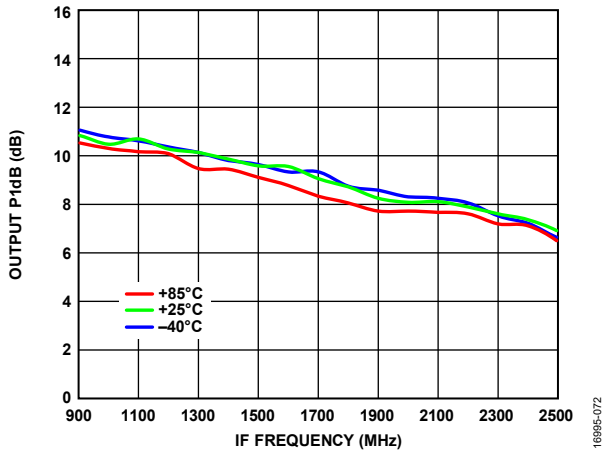


Figure 74. Output P1dB vs. IF Frequency at Various Temperatures

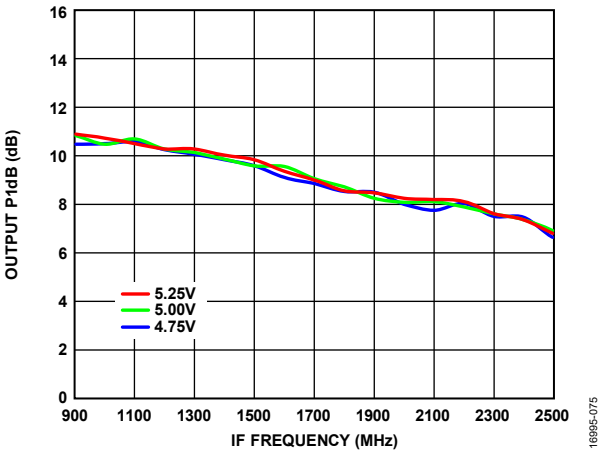


Figure 77. Output P1dB vs. IF Frequency at Various Supply Voltages, $T_A = 25°C$

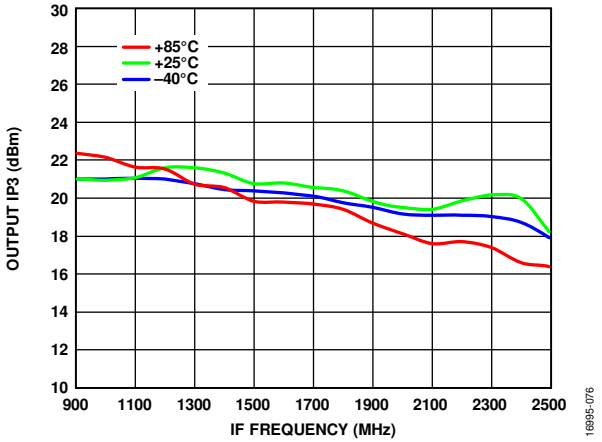


Figure 78. Output IP3 vs. IF Frequency at Various Temperatures

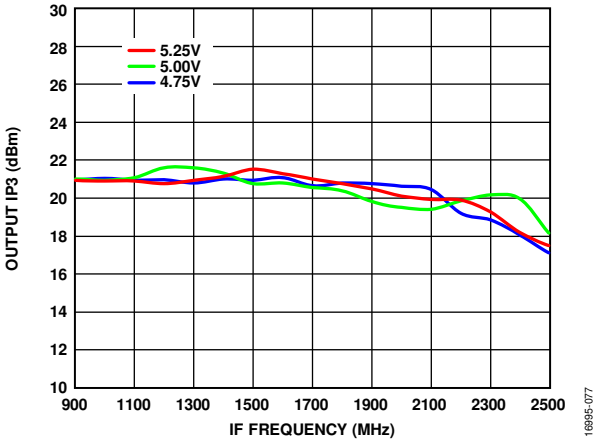


Figure 79. Output IP3 vs. IF Frequency at Various Supply Voltages, T_A = 25°C

LO = 18.95 GHz, LOW-SIDE INJECTION PERFORMANCE

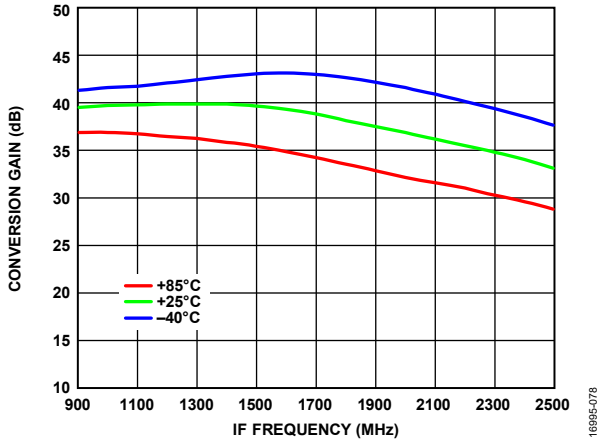


Figure 80. Conversion Gain vs. IF Frequency at Various Temperatures

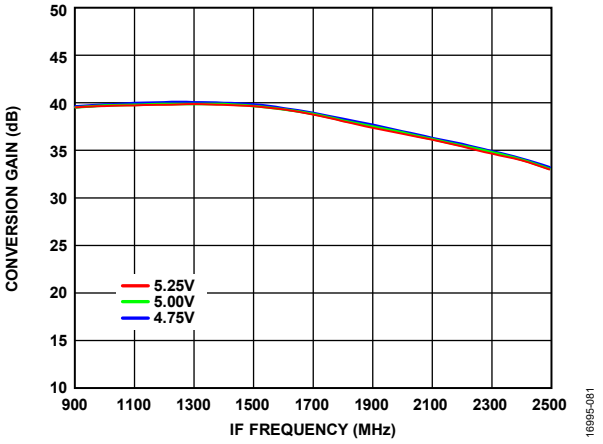


Figure 83. Conversion Gain vs. IF Frequency at Various Supply Voltages, $T_A = 25°C$

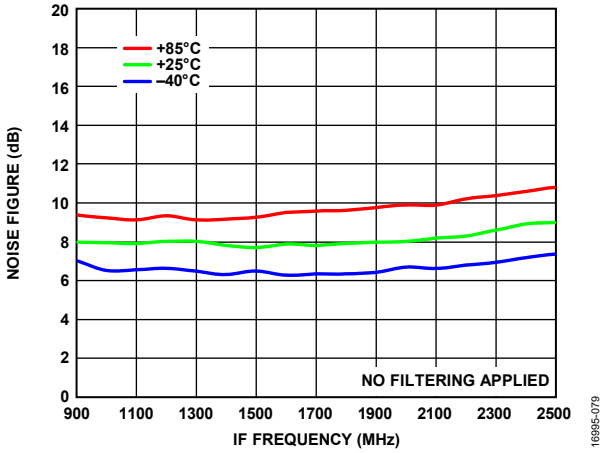


Figure 81. Noise Figure vs. IF Frequency at Various Temperatures

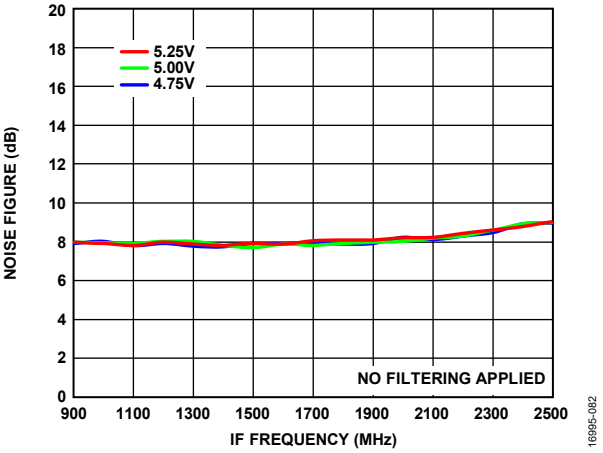


Figure 84. Noise Figure vs. IF Frequency at Various Supply Voltages, $T_A = 25°C$

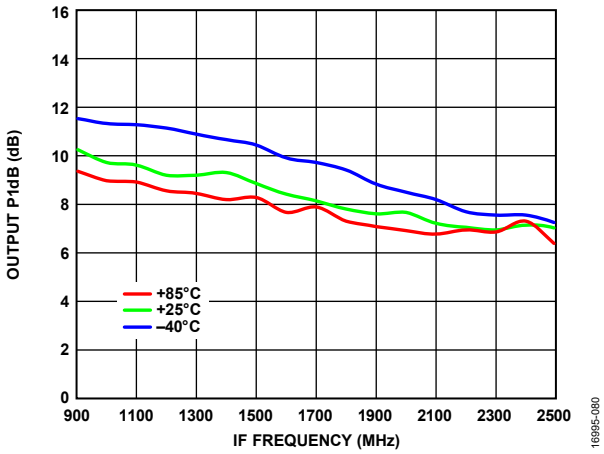


Figure 82. Output P1dB vs. IF Frequency at Various Temperatures

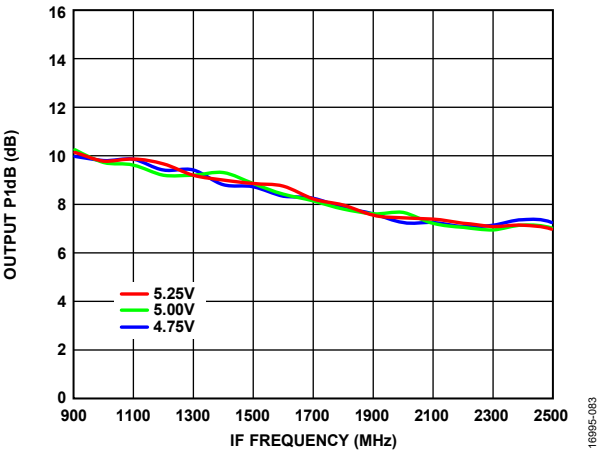


Figure 85. Output P1dB vs. IF Frequency at Various Supply Voltages, $T_A = 25°C$

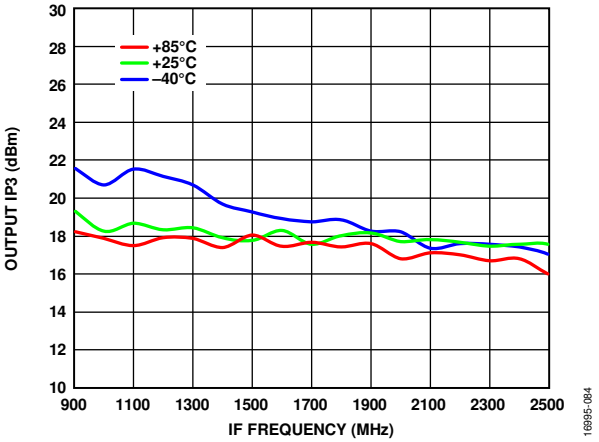


Figure 86. Output IP3 vs. IF Frequency at Various Temperatures

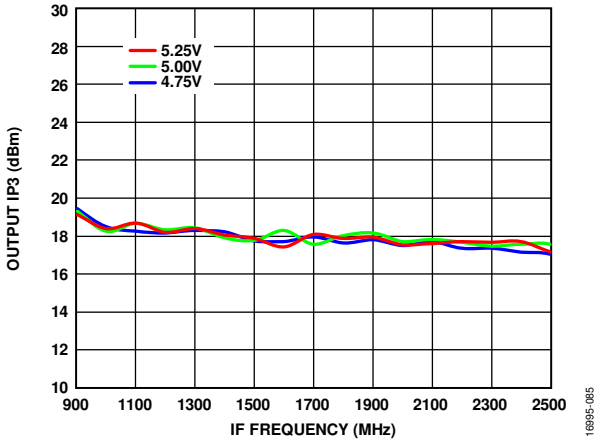


Figure 87. Output IP3 vs. IF Frequency at Various Supply Voltages, T_A = 25°C

LO = 18.95 GHz, HIGH-SIDE INJECTION PERFORMANCE

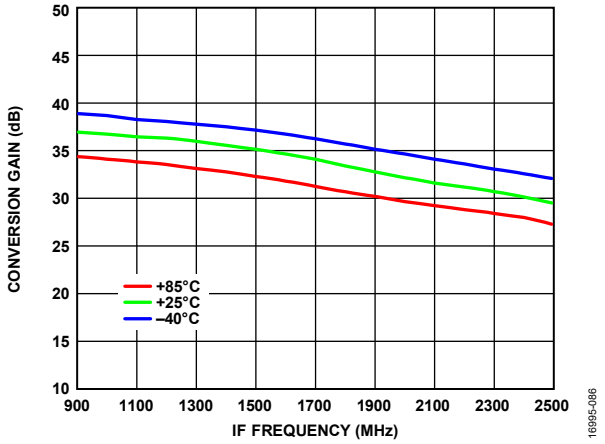


Figure 88. Conversion Gain vs. IF Frequency at Various Temperatures

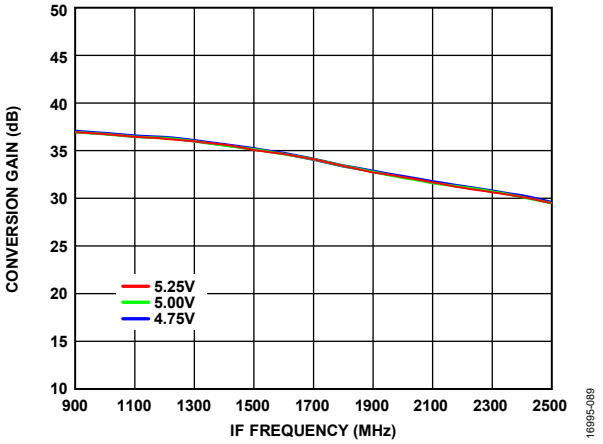


Figure 91. Conversion Gain vs. IF Frequency at Various Supply Voltages, T_A = 25°C

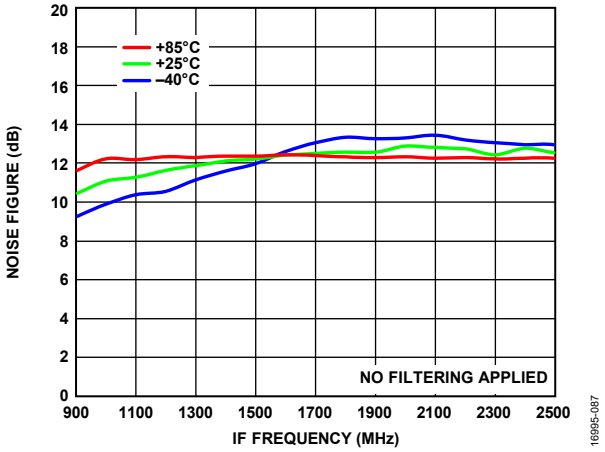


Figure 89. Noise Figure vs. IF Frequency at Various Temperatures

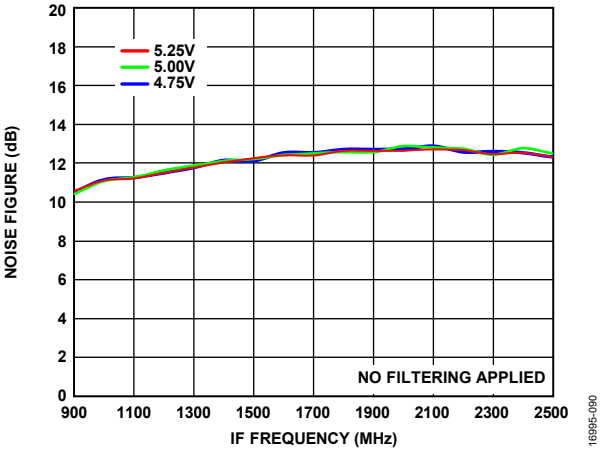


Figure 92. Noise Figure vs. IF Frequency at Various Supply Voltages, T_A = 25°C

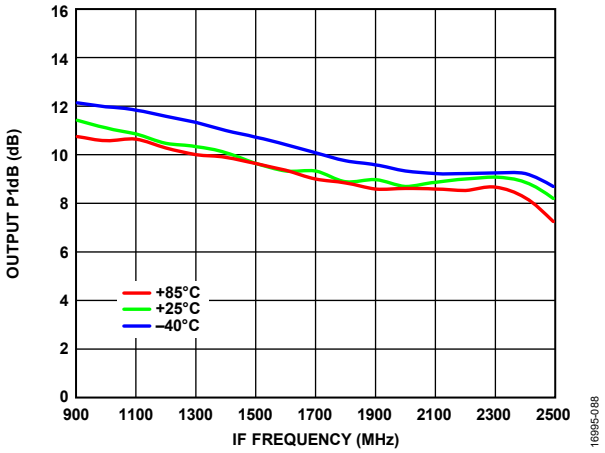


Figure 90. Output P1dB vs. IF Frequency at Various Temperatures

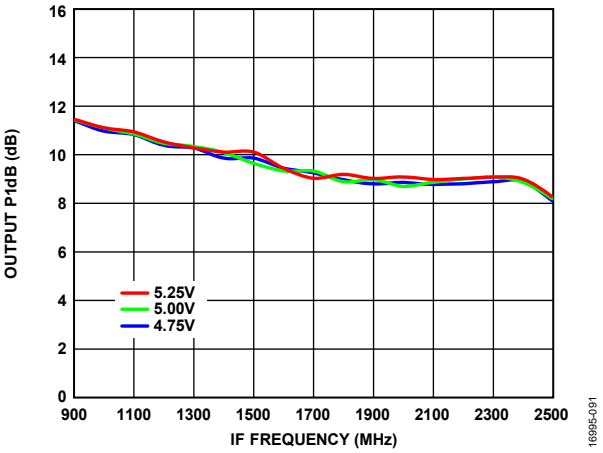


Figure 93. Output P1dB vs. IF Frequency at Various Supply Voltages, T_A = 25°C

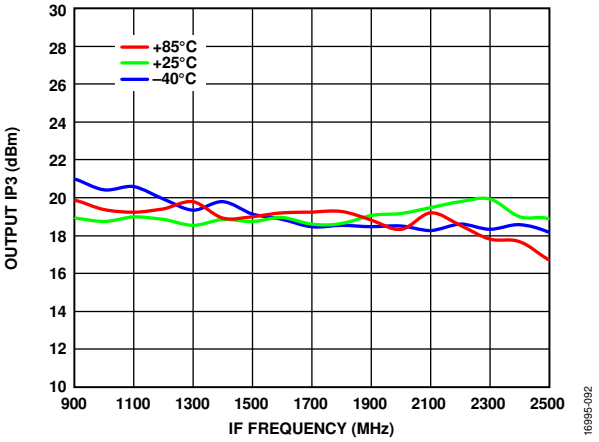


Figure 94. Output IP3 vs. IF Frequency at Various Temperatures

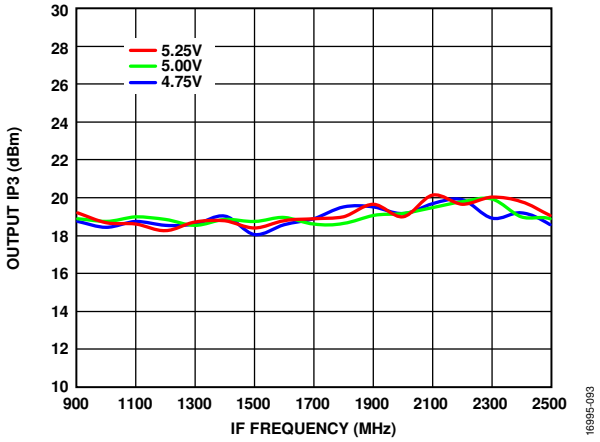


Figure 95. Output IP3 vs. IF Frequency at Various Supply Voltages, T_A = 25°C

LO = 21.15 GHz, LOW-SIDE INJECTION PERFORMANCE

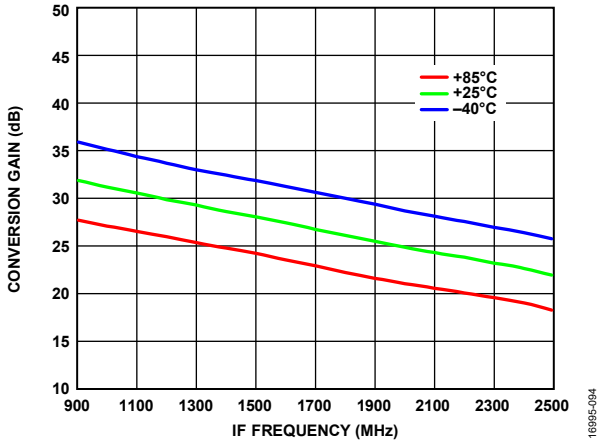


Figure 96. Conversion Gain vs. IF Frequency at Various Temperatures

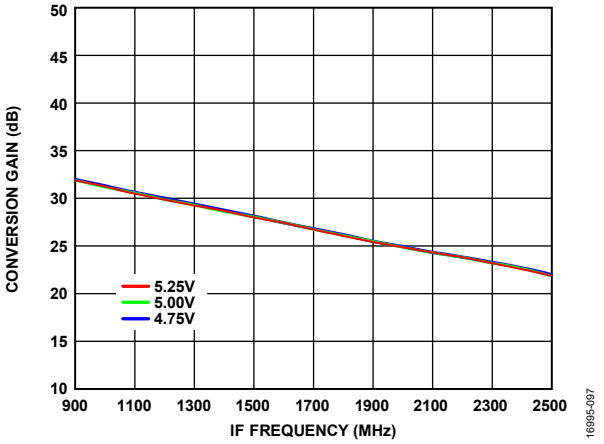


Figure 99. Conversion Gain vs. IF Frequency at Various Supply Voltages, T_A = 25°C

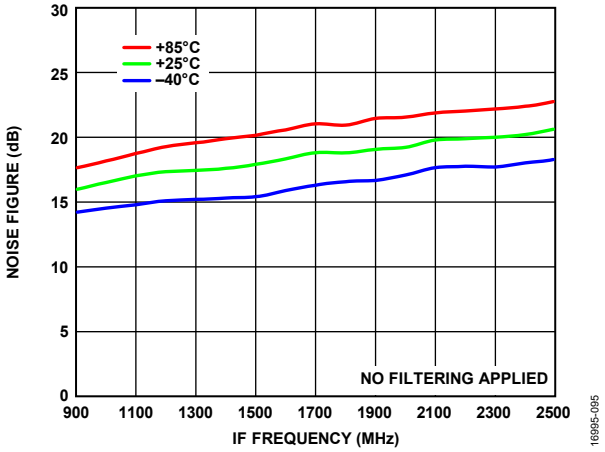


Figure 97. Noise Figure vs. IF Frequency at Various Temperatures

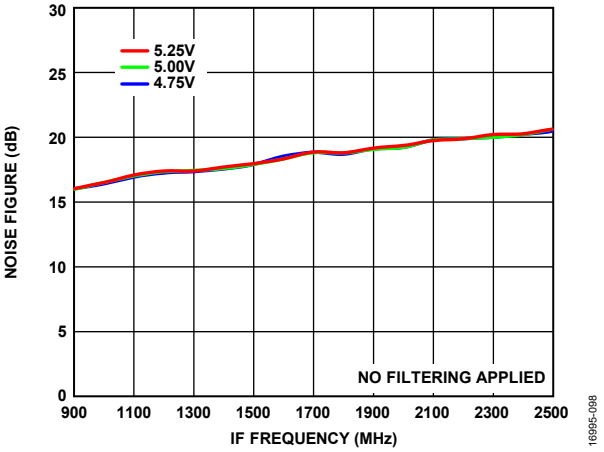


Figure 100. Noise Figure vs. IF Frequency at Various Supply Voltages, T_A = 25°C

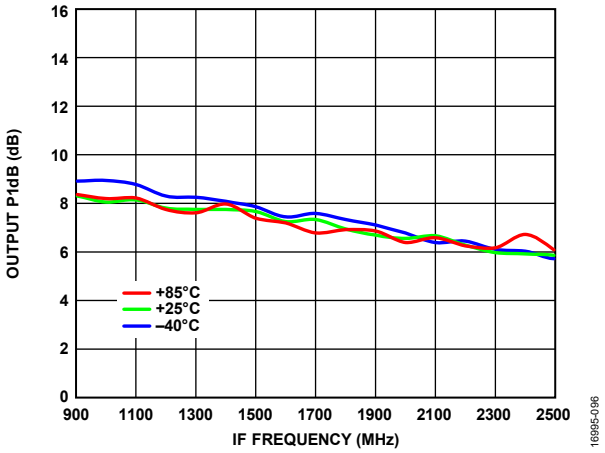


Figure 98. Output P1dB vs. IF Frequency at Various Temperatures

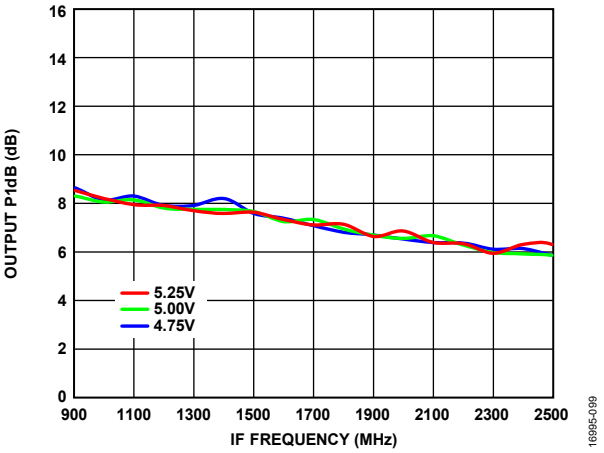


Figure 101. Output P1dB vs. IF Frequency at Various Supply Voltages, T_A = 25°C

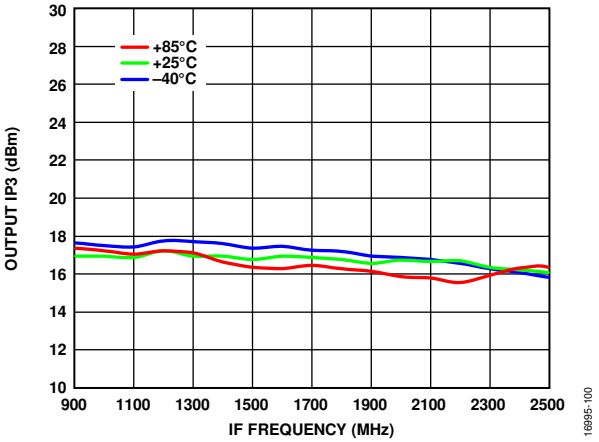


Figure 102. Output IP3 vs. IF Frequency at Various Temperatures

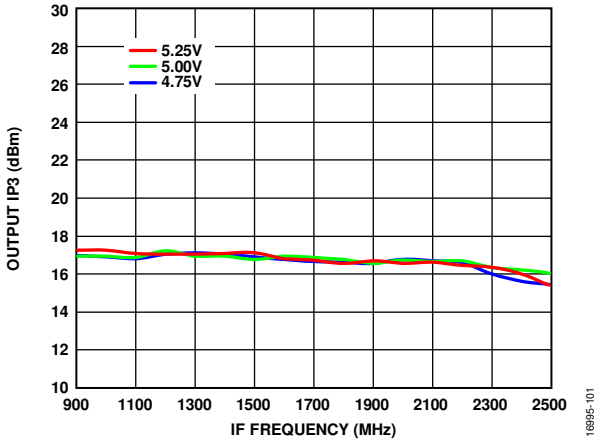


Figure 103. Output IP3 vs. IF Frequency at Various Supply Voltages, T_A = 25°C

LO = 21.15 GHz, HIGH-SIDE INJECTION PERFORMANCE

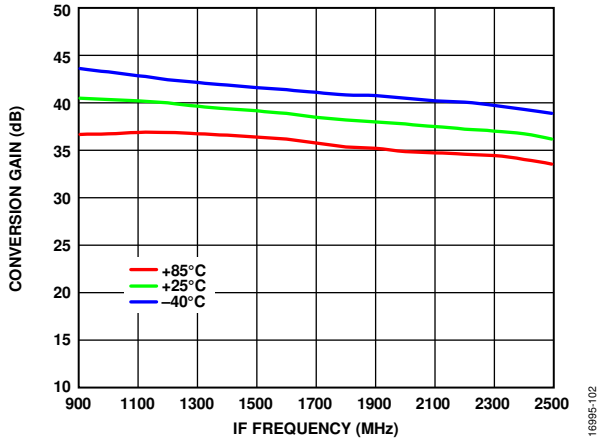


Figure 104. Conversion Gain vs. IF Frequency at Various Temperatures

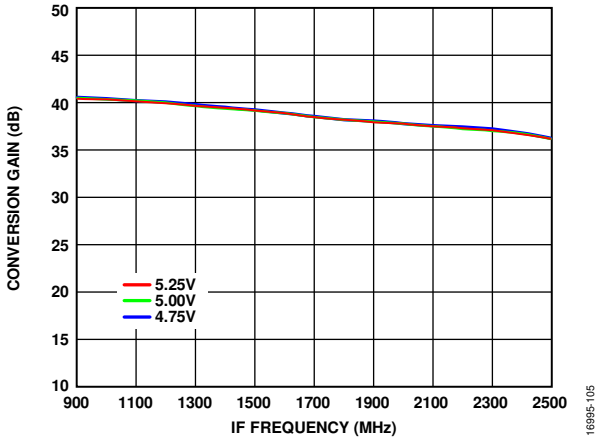


Figure 107. Conversion Gain vs. IF Frequency at Various Supply Voltages, T_A = 25°C

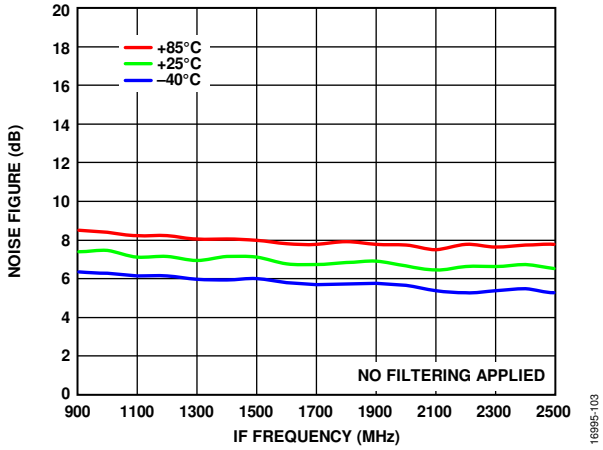


Figure 105. Noise Figure vs. IF Frequency at Various Temperatures

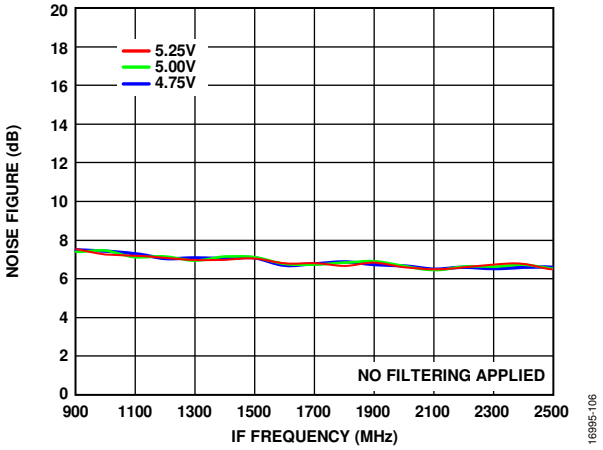


Figure 108. Noise Figure vs. IF Frequency at Various Supply Voltages, T_A = 25°C

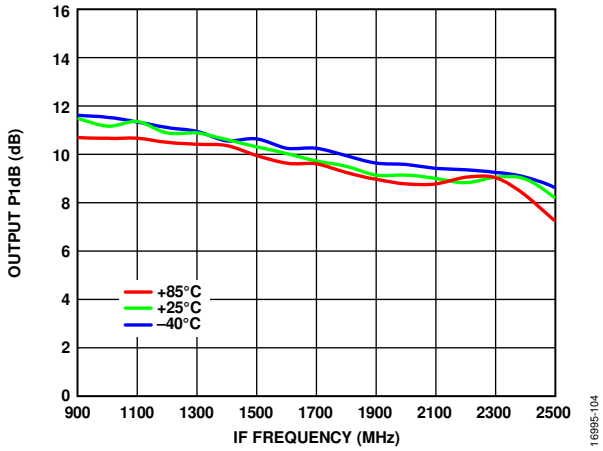


Figure 106. Output P1dB vs. IF Frequency at Various Temperatures

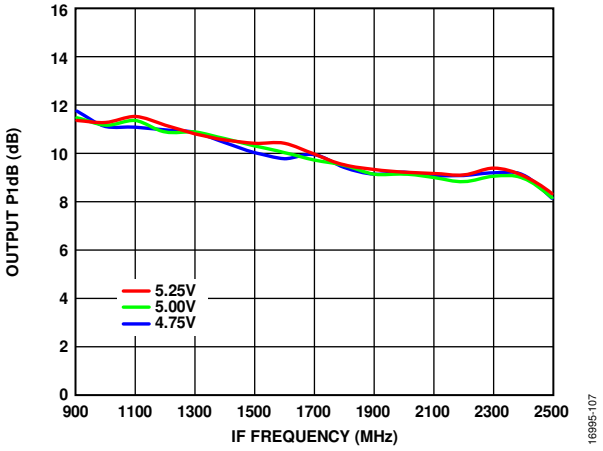


Figure 109. Output P1dB vs. IF Frequency at Various Supply Voltages, T_A = 25°C

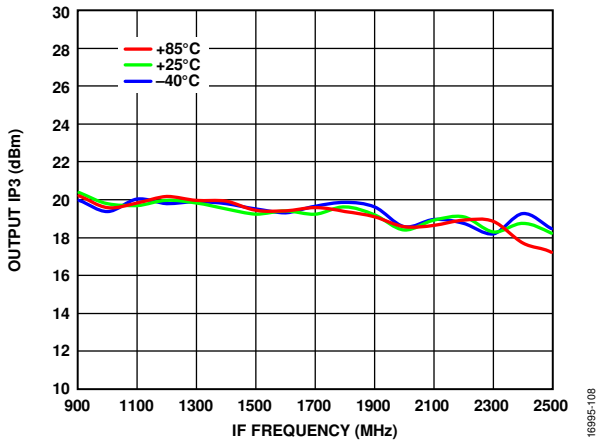


Figure 110. Output IP3 vs. IF Frequency at Various Temperatures

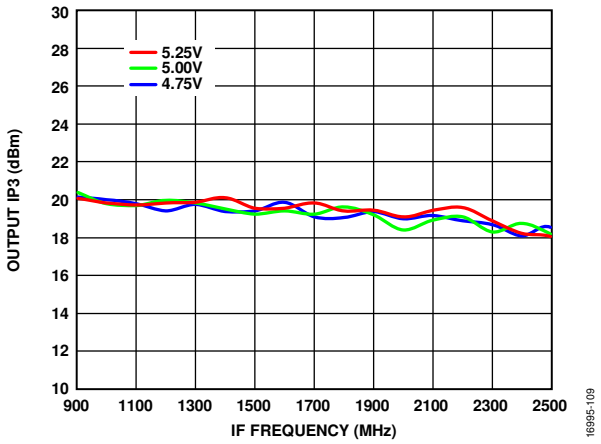


Figure 111. Output IP3 vs. IF Frequency at Various Supply Voltages, $T_A = 25°C$

PHASE NOISE PERFORMANCE

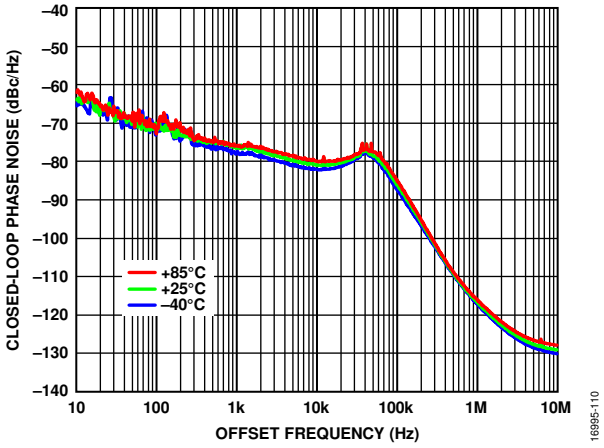


Figure 112. Closed-Loop Phase Noise vs. Offset Frequency at Various Temperatures, IF = 900 MHz, Low-Side Injection LO = 18.95 GHz

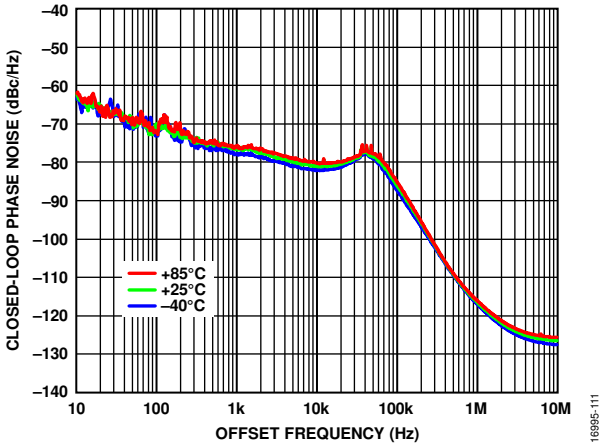


Figure 113. Closed-Loop Phase Noise vs. Offset Frequency at Various Temperatures, IF = 900 MHz, High-Side Injection LO = 18.95 GHz

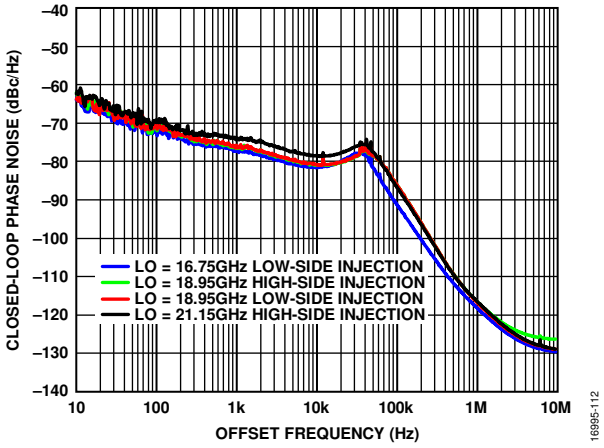


Figure 114. Closed-Loop Phase Noise vs. Offset Frequency at Various LO Frequencies, T_A = 25°C GHz

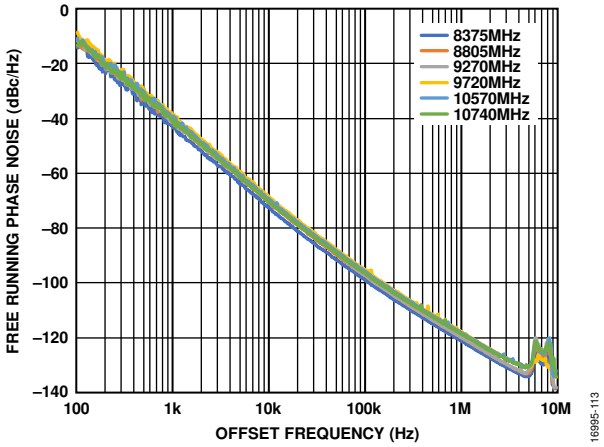


Figure 115. Free Running Phase Noise vs. Offset Frequency at Various VCO Frequencies, T_A = 25°C

RETURN LOSS AND ISOLATION

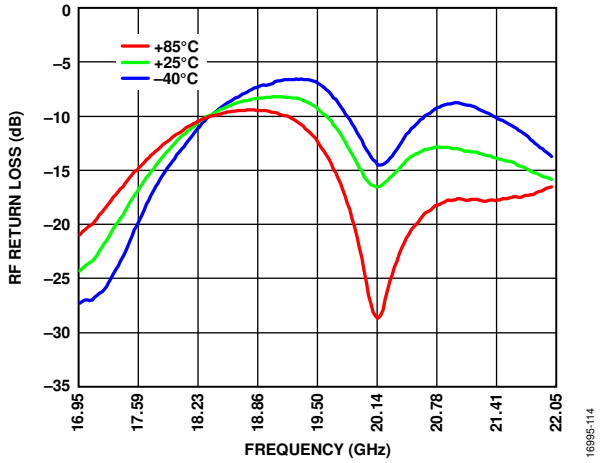


Figure 116. RF Return Loss vs. Frequency at Various Temperatures, LO = 18.95 GHz

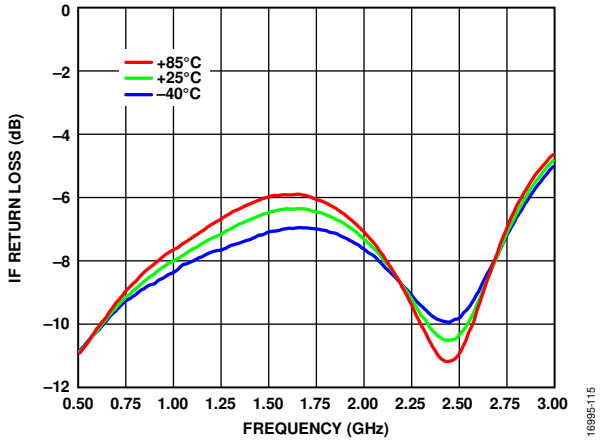


Figure 117. IF Return Loss vs. Frequency at Various Temperatures, LO = 18.95 GHz, Based on 75 Ω Output System

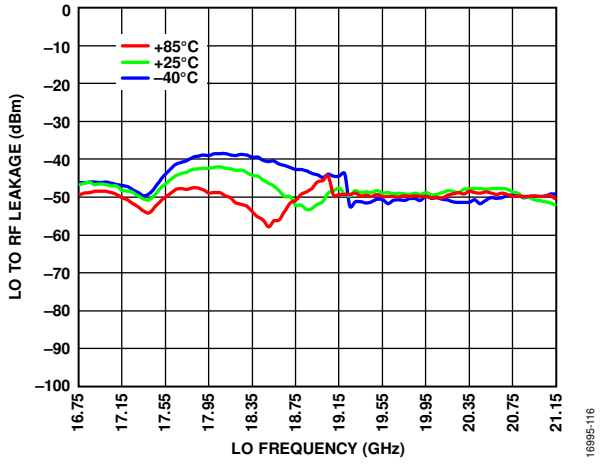


Figure 118. LO to RF Leakage vs. LO Frequency at Various Temperatures for Low-Side Injection LO, IF = 900 MHz

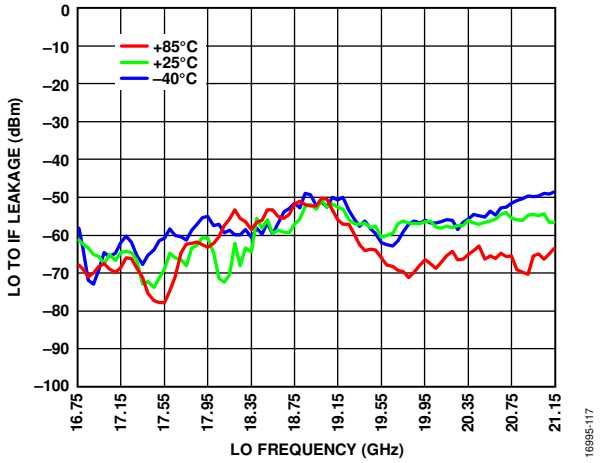


Figure 119. LO to IF Leakage vs. LO Frequency at Various Temperatures for Low-Side Injection LO, IF = 900 MHz

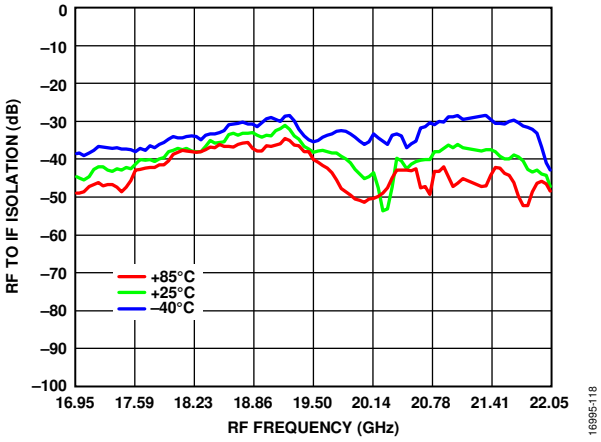


Figure 120. RF to IF Leakage vs. RF Frequency at Various Temperatures for LO = 21.15 GHz

SPURIOUS AND HARMONICS PERFORMANCE

LO Harmonics

All values are in dBm and are measured at the IF output. Trace and connector losses are de-embedded.

Table 5. LO Harmonics at IF Output

	LO Harmonics (dBm)				
LO Frequency (GHz)	**0.25**	**0.5**	**1**	**1.5**	**2**
16.75	−110	−49	−58	−71	−66
18.95	−113	−41	−45	−63	−62
21.15	−111	−34	−58	−85	−69

Reference Input (REFIN) Harmonics

All values are in dBm and measured at the IF output. Trace and connector losses are de-embedded. Reference frequency is at 50 MHz.

Table 6. REFIN Harmonics at the IF Output

REFIN Frequency (MHz)	**REFIN Harmonics (dBm)**							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
50	−78	−46	−60	−47	−57	−56	−61	−59

IF Harmonics

All values are in dBm and are measured at the IF output. Trace and connector losses are de-embedded. The downconverted IF frequency is at 900 MHz.

Table 7. IF Harmonics at the IF Output

	IF Harmonics (dBm)				
IF Frequency (MHz)	**1**	**2**	**3**	**4**	**5**
900	−7	−42	−58	−89	−90

Downconverter Spurious Outputs

Mixer spurious products are measured in dBc from the IF output power level, unless otherwise specified. Trace and connector losses are de-embedded. N/A means not applicable.

RF = 19.85 GHz, LO = 18.95 GHz, IF = 0.9 GHz, RF power = −40 dBm. Spur frequencies are the absolute value of (M × RF) + (N × LO/2)

		N × LO				
		0	**1**	**2**	**3**	**4**
M × RF	**−2**	−95	−99	−101	−91	−37
	−1	−78	−77	0	−81	−90
	0	N/A	−46	−50	−65	−56
	+1	−78	−98	−80	−88	N/A
	+2	−95	−88	N/A	N/A	N/A

RF = 18.05 GHz, LO = 18.95 GHz, IF = 0.9 GHz, RF power = −40 dBm. Spur frequencies are the absolute value of (M × RF) + (N × LO/2).

		N × LO				
		0	**1**	**2**	**3**	**4**
M × RF	**−2**	−77	−70	0	−82	−87
	−1	−95	−98	−103	−96	−41
	0	N/A	−45	−49	−64	−55
	+1	−77	−98	−93	−89	N/A
	+2	−95	−89	N/A	N/A	N/A

THEORY OF OPERATION

REFERENCE INPUT STAGE

The reference input stage is shown in Figure 121 and employs a differentially excited, 50 MHz crystal oscillator. Alternatively, the reference input can be driven by an external singled-ended 50 MHz source. Use the REF_IN_MODE bit (Register 0x20E, Bit 1) to select the input configuration. To select crystal oscillator mode, set this bit to 0 to close the SW1 switch and open the SW2 switch. To select single-ended mode, set this bit to 1 to close the SW2 switch and open the SW1 switch.

The selection of a crystal oscillator must be such that the electrical series resistance (ESR) and the load capacitance are well defined. For worst case demonstration purposes, the crystal oscillator selected for the evaluation board uses a maximum ESR of 100 Ω. To ensure the crystal oscillation startup over all temperature and process variations, a maximum ESR of 40 Ω is recommended. The nominal crystal load capacitance (C_{LOAD}) = 10 pF, which is computed from series combination of the C5 and C6 capacitors. It is recommended to keep C_{LOAD} between 8 pF and 12 pF. Additionally, ensure that C21 is not installed for crystal oscillator mode, as this can impact capacitive loading on the crystal, which can in turn prevent the oscillation from starting up.

REFERENCE DOUBLER, R COUNTER, AND RDIV2

Following the reference input stage as shown in Figure 121, there is an internal reference multiply by 2 block (×2 doubler) that allows generation of higher phase frequency detector frequencies (f_{PFD}). A higher f_{PFD} is useful for improving overall system phase noise performance. Typically, doubling the f_{PFD} improves the inband phase noise performance by up to 3 dBc/Hz. Use the EN_REF_X2 bit (Register 0x20E, Bit 2) to enable the reference doubler, which toggles the SW3 switch, as shown in Figure 121.

Following the reference doubler block, there are two frequency dividers: a 10-bit R counter (1 to 1023 allowed) and a divide by 2 block. These dividers allow the input reference frequency (f_{REF}) to be divided down to produce lower f_{PFD}, which helps to minimize fractional-N integer boundary spurs at the output.

The R counter is set using the R_DIV bits in Register 0x20C and Register 0x20D. If the R_DIV = 1, the SW4 switch is in the position shown in Figure 121. Otherwise, the SW4 switch toggles to use the R counter.

The reference divide by 2 block is enabled by using the RDIV2_SEL bit (Register 0x20E, Bit 0), which toggles the SW5 switch, as shown in Figure 121.

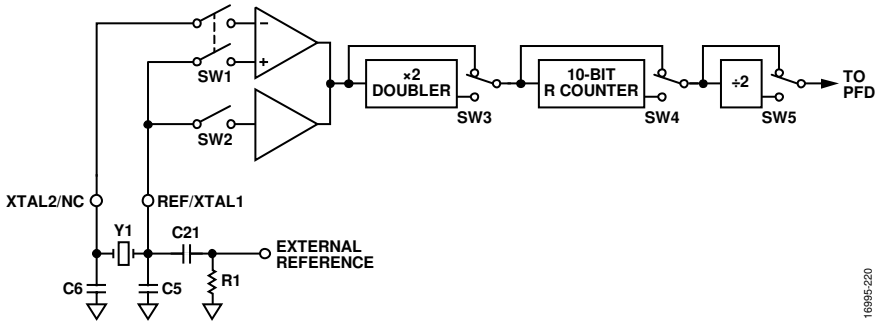


Figure 121. Reference Input Path Block Diagram

N COUNTER

The N counter allows a division ratio in the PLL feedback path from the VCO. Note that the VCO signal is multiplied by 2 to achieve the LO frequency at the double balanced mixer. The division ratio is determined using the integer-N (INT), fractional-N (FRAC), and modulus (MOD) values that this counter comprises. The applicable registers for setting the INT, FRAC, and MOD values are Register 0x200 to Register 0x20A.

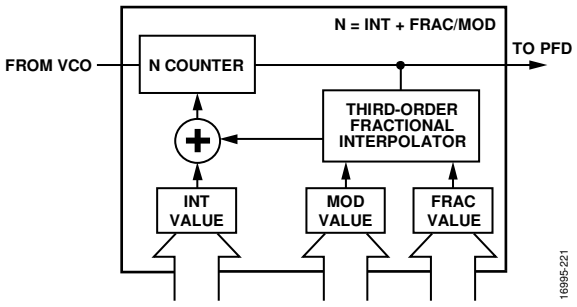


Figure 122. N Counter Functional Diagram

INT, FRAC, MOD, AND REFERENCE PATH RELATIONSHIP

The INT, FRAC, and MOD values, in conjunction with the reference path, make it possible to generate VCO frequencies spaced by fractions of the f_{PFD}.

The f_{PFD} can be calculated from the reference frequency (f_{REF}) and the reference path configuration parameters,

$$f_{PFD} = f_{REF} \times \frac{1 + D}{R \times (1 + T)} \quad (1)$$

where:
D is the reference doubler bit (0 or 1).
R is the reference divide ratio of the binary, 10-bit programmable counter (1 to 1023).
T is the reference divide by 2 bit (0 or 1).

The VCO frequency (f_{VCO}) is calculated with the following equation:

$$f_{VCO} = \frac{f_{LO}}{2} = f_{PFD} \times N \quad (2)$$

where:
f_{LO} is the frequency of the LO driving the mixer.
N is the desired value of the N counter.

The N counter value is defined as:

$$N = INT + \frac{FRAC}{MOD} = \frac{f_{LO}}{2f_{PFD}} = \frac{f_{VCO}}{f_{PFD}} \quad (3)$$

where:
INT is the 16-bit integer value (75 to 65,535).
FRAC is the numerator of the 24-bit primary modulus value (0 to 16,777,215).
MOD is the denominator of the 24-bit primary modulus value (1 to 16,777,215).

To obtain the INT portion of the N counter value, round down using the mathematical floor function,

$$INT = \text{FLOOR}(N) \quad (4)$$

where FLOOR is the mathematical floor function.

To determine the value of the MOD parameter, a channel spacing step size (f_{CHSP}) and the f_{PFD} must be selected first.

The MOD parameter is then computed with the f_{PFD} and the greatest common denominator (GCD),

$$MOD = \frac{f_{PFD}}{GCD(f_{CHSP}, f_{PFD})} \quad (5)$$

The FRAC value can be computed for a given an N counter value, INT value, and MOD value,

$$FRAC = \text{FLOOR}(MOD \times (N - INT)) \quad (6)$$

INTEGER-N MODE

When the FRAC value is equal to zero, the synthesizer operates in integer-N mode.

PHASE FREQUENCY DETECTOR AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter to produce an output that is proportional to the phase and frequency differences between them. This proportional information is then output to a charge pump (CP) circuit that generates current to drive an external loop filter, which is then used to appropriately increase or decrease the VTUNE tuning voltage.

Figure 123 shows a simplified schematic of the PFD and CP. Note that the PFD includes a fixed delay element, which is used to ensure there is no dead zone in the PFD transfer function for consistent reference spur levels.

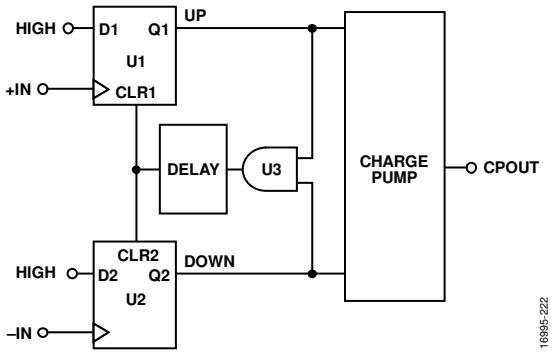


Figure 123. PFD and CP Simplified Schematic

LOOP FILTER

Defining a loop filter for a PLL is dependent on several dynamics, such as the PFD frequency, the N counter value, the tuning sensitivity characteristics (k_{VCO}) of the VCO, and the selected CP current. A higher f_{PFD} has the advantage of lowering inband phase noise performance at the expense of integer boundary spur levels when operating in fractional-N mode. Consequently, a lower f_{PFD} can allow the PLL to operate in integer-N mode, which can eliminate integer boundary spurs at the expense of higher inband phase noise performance. Given the trade-offs, care must be taken with frequency planning and f_{PFD} selection to ensure the appropriate inband phase noise performance is met with acceptable spur levels for the end application.

The loop filter, as implemented in the ADMV4420-EVALZ evaluation board, is a third-order passive filter, as shown in Figure 124. The filter is designed with the following simulation input parameters: f_{PFD} = 50 MHz, k_{VCO} = 80 MHz/V, f_{VCO} = 9.4 GHz and I_{CP} = 1.25 mA. The resulting loop filter bandwidth and phase margin are 60 kHz and 45°, respectively.

For additional guidance with loop filter simulations on the ADMV4420, contact Analog Devices, Inc., for technical support.

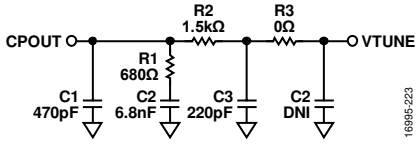


Figure 124. Recommended Loop Filter Schematic

CP CURRENT SETUP

For a specifically designed loop filter, the CP current (I_{CP}) must be set by adjusting the CP_CURRENT value in Register 0x22E.

The CP current follows the equation,

$$I_{CP} = (CP\_CURRENT + 1) \times 312.5\ \mu A \quad (7)$$

where *CP_CURRENT* is an integer value (0 to 15).

Note that the default value of CP_CURRENT is 3, which yields a current of 1.25 mA. The applicable range is 312.5 µA to 5 mA, with 312.5 µA steps.

To change the f_{PFD}, if no change has been made to the existing loop filter components, it is recommended to scale the I_{CP} using the following equation:

$$I_{CP(NEW)} = \frac{I_{CP(DEFAULT)} \times f_{PFD(DEFAULT)}}{f_{PFD(NEW)}} = \frac{1.25\ \text{mA} \times 50\ \text{MHz}}{f_{PFD(NEW)}} \quad (8)$$

where:
$I_{CP(NEW)}$ is the new desired I_{CP}.
$I_{CP(DEFAULT)}$ is the default I_{CP}.
$f_{PFD(DEFAULT)}$ is the default f_{PFD}.
$f_{PFD(NEW)}$ is the new desired f_{PFD}.

When $I_{CP(NEW)}$ is obtained, the CP_CURRENT value in Register 0x22E can be updated using the round function,

$$CP\_CURRENT = \text{ROUND}\left(\frac{I_{CP(NEW)}}{312.5\ \mu A}\right) - 1 \quad (9)$$

where ROUND is the mathematical round function.

BLEED CURRENT (CP_BLEED) SETUP

The charge pump includes a binary scaled bleed current (I_{BLEED}), which is set by using the CP_BLEED value in Register 0x22F. The bleed current introduces a slight phase offset in the PFD to improve integer boundary spurs when operating in fractional-N mode.

Generally, the bleed current follows Equation 10 and provides a value that can be applicable for most applications, but there can be additional spur level improvement by empirically determining the appropriate bleed current value from actual measurements for the intended application. The applicable range is 0 µA to 956.25 µA, with 3.75 µA steps.

$$I_{BLEED} = CP\_BLEED \times 3.75\ \mu A = \frac{4 \times I_{CP}}{N} \quad (10)$$

where *CP_BLEED* is an integer value (0 to 255).

When I_{BLEED} is obtained, the CP_BLEED value in Register 0x22F can be updated using the round function,

$$CP\_BLEED = \text{ROUND}\left(\frac{I_{BLEED}}{3.75\ \mu A}\right) \quad (11)$$

where I_{BLEED} is the desired charge pump bleed current.

MUXOUT

The on-chip multiplexer output (MUXOUT) allows access to various internal signals, in addition to providing a digital lock detect function. A representative diagram is shown in Figure 125. The state of the MUXOUT pin is determined from the PLL_MUX_SEL value in Register 0x213. See Table 31 for full details.

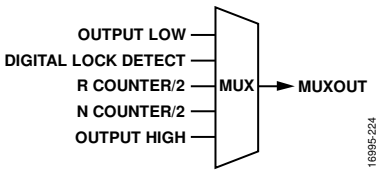


Figure 125. Multiplexer Output Diagram

DIGITAL LOCK DETECT

The digital lock detect function that is output on the MUXOUT pin has two adjustable settings in Register 0x214. LD_BIAS adjusts an internal precision window and LD_COUNT adjusts the consecutive cycle count to declare PLL lock. It is recommended to keep the 20 µA and 8192 PFD cycle count factory settings. For special applications, contact Analog Devices technical support for guidance on adjusting these settings.

ENABLES

Register 0x103 has individual circuit block enables. Setting this register to 0 disables all circuit blocks, resulting in approximately 80 mW of power dissipation. For nominal operation, keep all enables in this register set to 1 (register value of 0x6F). Note that Bit 4 and Bit 7 are reserved and must be set to 0.

IF OUTPUT—EXTERNAL INDUCTOR/BIASING

The IF amplifier output is an open-collector configuration and requires an external biasing inductor pulled up to the VPOS4_IF supply. The recommended value of the inductor is approximately 50 nH, which requires a current carrying capability of at least 150 mA. Because this configuration is dc-coupled, it is necessary to place a series capacitor between the IF output and the next stage in the end application. A recommended minimum value for the series capacitor is 1 nF.

SPI CONFIGURATION

The SPI of the ADMV4420 allows configuration of the device for specific functions or operations via the 4-pin SPI port. This interface provides users with added flexibility and customization. The SPI consists of four control lines: SCLK, SDI, SDO, and $\overline{\text{CS}}$. The ADMV4420 protocol consists of a write/read bit followed by 15 register address bits and 8 data bits. The address field and data field are organized MSB first and end with the LSB.

For a write operation, set the MSB to 0, and for a read operation, set the MSB to 1. The write cycle sampling must be done on the rising edge of SCLK. The 24 bits of the serial write address and data are shifted in on the SDI control line, MSB to LSB. The ADMV4420 input logic level for the write cycle supports a 3.3 V interface.

For a read cycle, the R/W bit and the 15 bits of address shift in on the rising edge of SCLK on the SDI control line. Then, 8 bits of serial read data shift out on the SDO control line, MSB first, on the falling edge of SCLK. The output logic level for a read cycle is 3.3 V. The output drivers of the SDO are enabled after the last rising edge of SCLK of the instruction cycle and remain active until the end of the read cycle. In a read operation, when $\overline{\text{CS}}$ is deasserted, SDO returns to high impedance until the next read transaction. The $\overline{\text{CS}}$ is active low and must be deasserted at the end of the write or read sequence.

An active low input on $\overline{\text{CS}}$ starts and gates a communication cycle. The $\overline{\text{CS}}$ pin allows more than one device to be used on the same serial communications lines. The SDO pin goes to a high impedance state when the $\overline{\text{CS}}$ input is high. During the communication cycle, the chip select must stay low.

The SPI communications protocol follows the Analog Devices SPI standard. For more information, see the ADI-SPI Serial Control Interface Standard (Rev 1.0).

VCO AUTOCALIBRATION AND AUTOMATIC LEVEL CONTROL

The multicore VCO uses an internal autocalibration (AUTOCAL) and automatic level control (ALC) routine that optimizes the VCO settings for a particular frequency and allows the PLL to lock in approximately 400 µs after the lower portion of the N counter integer value (INT_L) has been programmed. For nominal applications, maintain the AUTOCAL and ALC default values in the register map (see Table 8).

PROGRAMMING SEQUENCE

A number of double buffered registers that take effect only after a write to the lower portion of the N counter integer value (INT_L). The INT_L register applies any changes to these double registers and initiate the autocalibration routine. Additionally, it is recommended to allow 16 SPI clock cycles after writing to the INT_L register.

The following describes the recommended programming sequence:

1. Program the CP_CURRENT register (Register 0x22E).
2. Program the FRAC_H register (Register 0x204).
3. Program the FRAC_M register (Register 0x203).
4. Program the FRAC_L register (Register 0x202).
5. Program the MOD_H register (Register 0x20A).
6. Program the MOD_M register (Register 0x209).
7. Program the MOD_L register (Register 0x208).
8. Program the INT_H register (Register 0x201).
9. Program the INT_L register (Register 0x200).
10. Program 16 SPI clock cycles.

CONTROL REGISTERS

Table 8. Control Register Map

Register Address	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x000	ADI_SPI_CONFIG_1	[7:0]	SOFTRESET_	LSB_FIRST_	ENDIAN_	SDOACTIVE_	SDOACTIVE	ENDIAN	LSB_FIRST	SOFTRESET	0x00	R/W
0x001	ADI_SPI_CONFIG_2	[7:0]	SINGLE_INSTRUCTION	CSB_STALL	MASTER_SLAVE_RB	RESERVED				MASTER_SLAVE_TRANSFER	0x00	R/W
0x003	CHIPTYPE	[7:0]	CHIPTYPE								0x01	R
0x004	PRODUCT_ID_L	[7:0]	PRODUCT_ID_L								0x03	R
0x005	PRODUCT_ID_H	[7:0]	PRODUCT_ID_H								0x00	R
0x00A	SCRATCHPAD	[7:0]	SCRATCHPAD								0x00	R/W
0x00B	SPI_REV	[7:0]	SPI_REV								0x00	R
0x103	ENABLES	[7:0]	RESERVED	EN_PLL	EN_LO	RESERVED	EN_VCO	EN_IFAMP	EN_MIXER	EN_LNA	0x6F	R/W
0x108	SDO_LEVEL	[7:0]	RESERVED					SDO_LEVEL	RESERVED		0x05	R/W
0x200	INT_L	[7:0]	INT[7:0]								0xA7	R/W
0x201	INT_H	[7:0]	INT[15:8]								0x00	R/W
0x202	FRAC_L	[7:0]	FRAC[7:0]								0x02	R/W
0x203	FRAC_M	[7:0]	FRAC[15:8]								0x00	R/W
0x204	FRAC_H	[7:0]	FRAC[23:16]								0x00	R/W
0x208	MOD_L	[7:0]	MOD[7:0]								0x04	R/W
0x209	MOD_M	[7:0]	MOD[15:8]								0x00	R/W
0x20A	MOD_H	[7:0]	MOD[23:16]								0x00	R/W
0x20C	R_DIV_L	[7:0]	R_DIV[7:0]								0x01	R/W
0x20D	R_DIV_H	[7:0]	RESERVED						R_DIV[9:8]		0x00	R/W
0x20E	REFERENCE	[7:0]	RESERVED					END_REF_X2	REF_IN_MODE	RDIV2_SEL	0x00	R/W
0x211	VCO_DATA_READBACK1	[7:0]	VCO_DATA_READBACK[7:0]								0x00	R
0x212	VCO_DATA_READBACK2	[7:0]	RESERVED					VCO_DATA_READBACK[10:8]			0x00	R
0x213	PLL_MUX_SEL	[7:0]	PLL_MUX_SEL								0x01	R/W
0x214	LOCK_DETECT	[7:0]	LD_BIAS		LD_COUNT			RESERVED			0x98	R/W
0x215	VCO_BAND_SELECT	[7:0]	VCO_BAND_SELECT								0x00	R/W
0x216	VCO_ALC_TIMEOUT	[7:0]	RESERVED				VCO_ALC_TIMEOUT				0x00	R/W
0x217	VCO_MANUAL	[7:0]	RESERVED		VCO_CORE_SELECT		VCO_BIAS_ADJUST				0x01	R/W
0x219	ALC	[7:0]	RESERVED			EN_ALC	RESERVED				0x13	R/W
0x21C	VCO_TIMEOUT1	[7:0]	VCO_TIMEOUT[7:0]								0x90	R/W
0x21D	VCO_TIMEOUT2	[7:0]	RESERVED						VCO_TIMEOUT[9:8]		0x01	R/W
0x21E	VCO_BAND_DIV	[7:0]	VCO_BAND_DIV								0x4B	R/W
0x21F	VCO_READBACK_SEL	[7:0]	RESERVED					VCO_READBACK_SEL			0x18	R/W
0x226	AUTOCAL	[7:0]	RESERVED						EN_AUTOCAL	RESERVED	0x02	R/W
0x22C	CP_STATE	[7:0]	RESERVED						CP_STATE		0x07	R/W
2x22D	CP_BLEED_EN	[7:0]	RESERVED							EN_BLEED	0x01	R/W
0x22E	CP_CURRENT	[7:0]	RESERVED				CP_CURRENT				0x03	R/W
0x22F	CP_BLEED	[7:0]	BICP								0x0C	R/W

REGISTER DETAILS

ADDRESS 0x000, RESET: 0x00, NAME: ADI_SPI_CONFIG_1

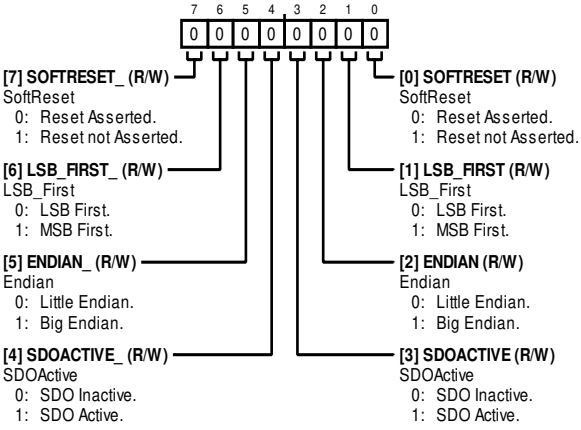


Table 9. ADI_SPI_CONFIG1 Bit Descriptions

Bit	Bit Name	Description	Reset	Access
7	SOFTRESET_	Soft reset bit 0: Reset asserted 1: Reset not asserted	0x0	R/W
6	LSB_FIRST_	LSB first bit 0: LSB first 1: MSB first	0x0	R/W
5	ENDIAN_	Endian bit 0: Little endian 1: Big endian	0x0	R/W
4	SDOACTIVE_	SDO active bit 0: SDO inactive 1: SDO active	0x0	R/W
3	SDOACTIVE	SDO active bit 0: SDO inactive 1: SDO active	0x0	R/W
2	ENDIAN	Endian bit 0: Little endian 1: Big endian	0x0	R/W
1	LSB_FIRST	LSB first bit 0: LSB first 1: MSB first	0x0	R/W
0	SOFTRESET	Soft reset 0: Reset asserted 1: Reset not asserted	0x0	R/W

ADDRESS 0x001, RESET: 0x00, NAME: ADI_SPI_CONFIG_2

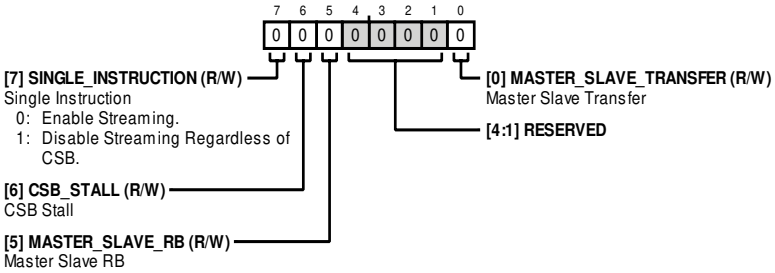


Table 10. ADI_SPI_CONFIG_2 Bit Descriptions

Bit	Bit Name	Description[1]	Reset	Access
7	SINGLE_INSTRUCTION	Single instruction bit 0: Enable streaming 1: Disable streaming regardless of CSB	0x0	R/W
6	CSB_STALL	CSB stall bit	0x0	R/W
5	MASTER_SLAVE_RB	Master slave readback bit	0x0	R/W
[4:1]	RESERVED	Reserved	0x0	R
0	MASTER_SLAVE_TRANSFER	Master slave transfer bit	0x0	R/W

[1] Note that $\overline{CS}$ corresponds to CSB.

ADDRESS 0x003, RESET: 0x01, NAME: CHIPTYPE

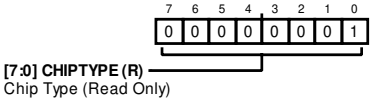


Table 11. CHIPTYPE Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	CHIPTYPE	Chip type bits, read only.	0x01	R

ADDRESS 0x004, RESET: 0x03, NAME: PRODUCT_ID_L

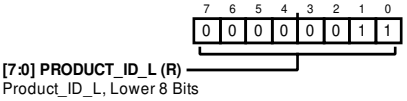


Table 12. PRODUCT_ID_L Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID_L	PRODUCT_ID_L bits, lower 8 bits.	0x03	R

ADDRESS 0x005, RESET: 0x00, NAME: PRODUCT_ID_H

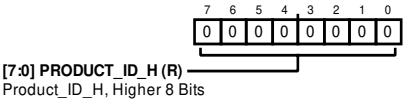


Table 13. PRODUCT_ID_H Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID_H	PRODUCT_ID_H bits, higher 8 bits.	0x00	R

ADDRESS 0x00A, RESET: 0x00, NAME: SCRATCHPAD

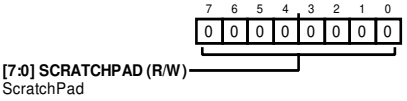


Table 14. SCRATCHPAD Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCHPAD	Scratch pad bits	0x00	R/W

ADDRESS 0x00B, RESET: 0x00, NAME: SPI_REV

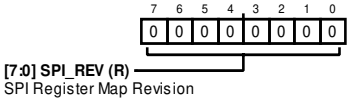


Table 15. SPI_REV Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	SPI_REV	SPI register map revision bits	0x00	R

ADDRESS 0x103, RESET: 0x6F, NAME: ENABLES

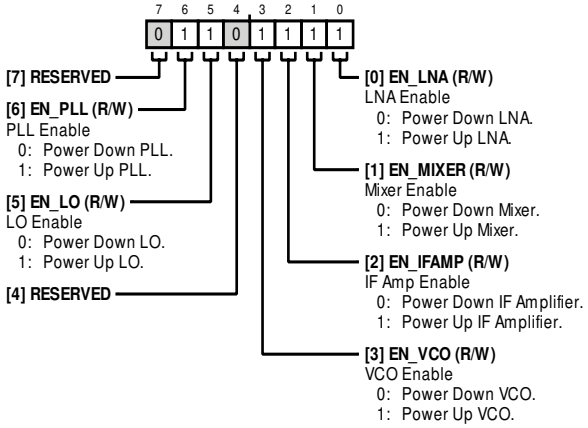


Table 16. ENABLES Bit Descriptions

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved	0x0	R
6	EN_PLL	PLL enable bit 0: Power down PLL 1: Power up PLL	0x1	R/W
5	EN_LO	LO enable bit 0: Power down LO 1: Power up LO	0x1	R/W
4	RESERVED	Reserved	0x0	R
3	EN_VCO	VCO enable bit 0: Power down VCO 1: Power up VCO	0x1	R/W
2	EN_IFAMP	IF amplifier enable bit 0: Power down IF amplifier 1: Power up IF amplifier	0x1	R/W
1	EN_MIXER	Mixer enable bit 0: Power down mixer 1: Power up mixer	0x1	R/W
0	EN_LNA	LNA enable bit 0: Power down LNA 1: Power up LNA	0x1	R/W

ADDRESS 0x108, RESET: 0x05, NAME: SDO_LEVEL

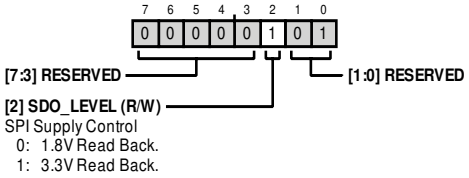


Table 17. SDO_LEVEL Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved	0x0	R
2	SDO_LEVEL	SPI supply control bit 0: 1.8 V readback 1: 3.3 V readback	0x1	R/W
[1:0]	RESERVED	Reserved	0x1	R/W

ADDRESS 0x200, RESET: 0xA7, NAME: INT_L

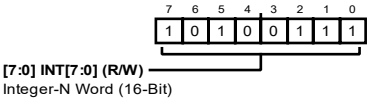


Table 18. INT_L Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	INT[7:0]	Integer-N word (16-bit)	0xA7	R/W

ADDRESS 0x201, RESET: 0x00, NAME: INT_H

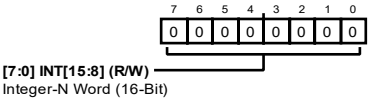


Table 19. INT_H Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	INT[15:8]	Integer-N word (16-bit)	0x0	R/W

ADDRESS 0x202, RESET: 0x02, NAME: FRAC_L

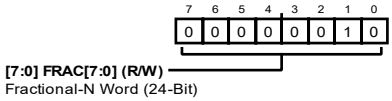


Table 20. FRAC_L Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC[7:0]	Fractional-N word (24-bit)	0x2	R/W

ADDRESS 0x203, RESET: 0x00, NAME: FRAC_M

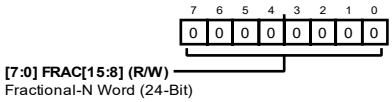


Table 21. FRAC_M Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC[15:8]	Fractional-N word (24-bit)	0x0	R/W

ADDRESS 0x204, RESET: 0x00, NAME: FRAC_H

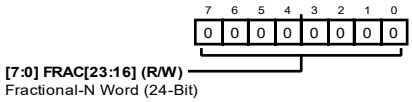


Table 22. FRAC_H Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC[23:16]	Fractional-N word (24-bit)	0x0	R/W

ADDRESS 0x208, RESET: 0x04, NAME: MOD_L

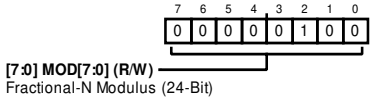


Table 23. MOD_L Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	MOD[7:0]	Fractional-N modulus (24-bit)	0x4	R/W

ADDRESS 0x209, RESET: 0x00, NAME: MOD_M

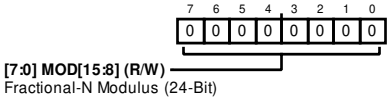


Table 24. MOD_M Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	MOD[15:8]	Fractional-N modulus (24-bit)	0x0	R/W

ADDRESS 0x20A, RESET: 0x00, NAME: MOD_H

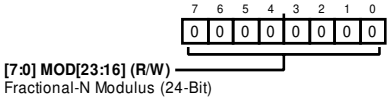


Table 25. MOD_H Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	MOD[23:16]	Fractional-N modulus (24-bit)	0x0	R/W

ADDRESS 0x20C, RESET: 0x01, NAME: R_DIV_L

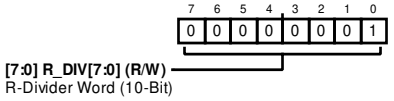


Table 26. R_DIV_L Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	R_DIV[7:0]	R divider word (10-bit)	0x1	R/W

ADDRESS 0x20D, RESET: 0x00, NAME: R_DIV_H

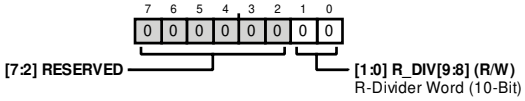


Table 27. R_DIV_H Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved	0x0	R
[1:0]	R_DIV[9:8]	R divider word (10-bit)	0x0	R/W

ADDRESS 0x20E, RESET: 0x00, NAME: REFERENCE

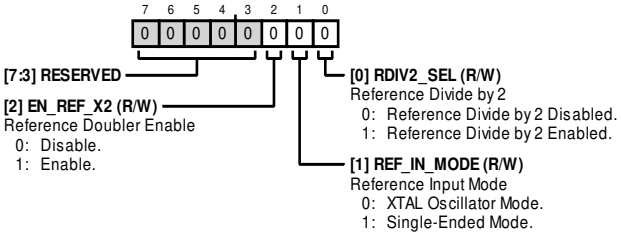


Table 28. REFERENCE Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved	0x0	R
2	EN_REF_X2	Reference doubler enable bit 0: Disable 1: Enable	0x0	R/W
1	REF_IN_MODE	Reference input mode bit 0: Crystal (XTAL) oscillator mode 1: Single-ended mode	0x0	R/W
0	RDIV2_SEL	Reference divide by 2 bit 0: Reference divide by 2 disabled 1: Reference divide by 2 enabled	0x0	R/W

ADDRESS 0x211, RESET: 0x00, NAME: VCO_DATA_READBACK1

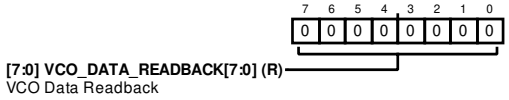


Table 29. VCO_DATA_READBACK1 Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_DATA_READBACK[7:0]	VCO data readback	0x0	R

ADDRESS 0x212, RESET: 0x00, NAME: VCO_DATA_READBACK2

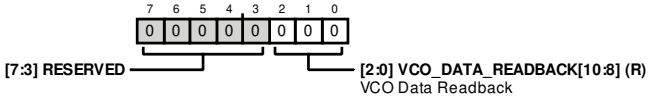


Table 30. VCO_DATA_READBACK2 Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved	0x0	R
[2:0]	VCO_DATA_READBACK[10:8]	VCO data readback bits	0x0	R

ADDRESS 0x213, RESET: 0x01, NAME: PLL_MUX_SEL

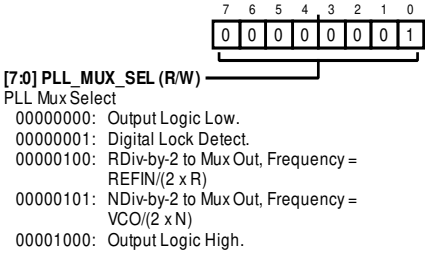


Table 31. PLL_MUX_SEL Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	PLL_MUX_SEL	PLL mux select bits 00000000: Output logic low 00000001: Digital lock detect 00000100: R divide by 2 to mux out, frequency = REFIN /2 × R) 00000101: N divide by 2 to mux out, frequency = VCO/(2 × N) 00001000: Output logic high	0x1	R/W

ADDRESS 0x214, RESET: 0x98, NAME: LOCK_DETECT

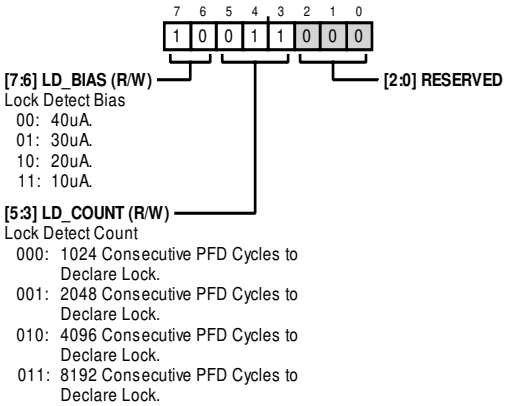


Table 32. LOCK_DETECT Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:6]	LD_BIAS	Lock detect bias bits 00: 40 µA 01: 30 µA 10: 20 µA 11: 10 µA	0x2	R/W
[5:3]	LD_COUNT	Lock detect count bits 000: 1024 consecutive PFD cycles to declare lock 001: 2048 consecutive PFD cycles to declare lock 010: 4096 consecutive PFD cycles to declare lock 011: 8192 consecutive PFD cycles to declare lock	0x3	R/W
[2:0]	RESERVED	Reserved	0x0	R/W

ADDRESS 0x215, RESET: 0x00, NAME: VCO_BAND_SELECT

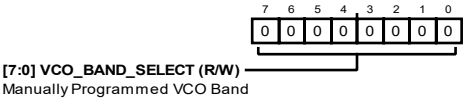


Table 33. VCO_BAND_SELECT Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_BAND_SELECT	Manually programmed VCO band	0x0	R/W

ADDRESS 0x216, RESET: 0x00, NAME: VCO_ALC_TIMEOUT

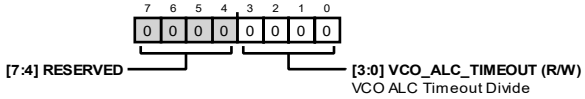


Table 34. VCO_ALC_TIMEOUT Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved	0x0	R
[3:0]	VCO_ALC_TIMEOUT	VCO ALC timeout divide	0x0	R/W

ADDRESS 0x217, RESET: 0x01, NAME: VCO_MANUAL

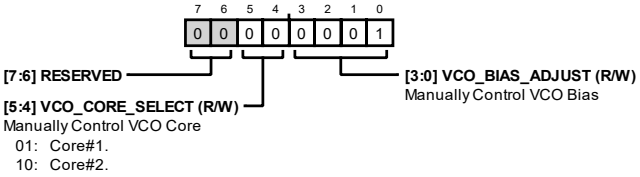


Table 35. VCO_MANUAL Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved	0x0	R
[5:4]	VCO_CORE_SELECT	Manual control of VCO core 01: Core 1 10: Core 2	0x0	R/W
[3:0]	VCO_BIAS_ADJUST	Manual control of VCO bias	0x1	R/W

ADDRESS 0x219, RESET: 0x13, NAME: ALC

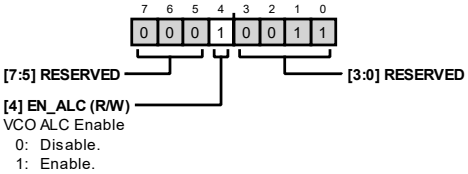


Table 36. ALC Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved	0x0	R
4	EN_ACL	VCO ALC enable bit 0: Disable 1: Enable	0x1	R/W
[3:0]	RESERVED	Reserved	0x3	R/W

ADDRESS 0x21C, RESET: 0x90, NAME: VCO_TIMEOUT1

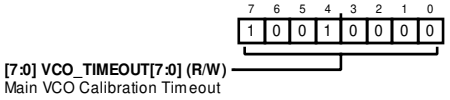


Table 37. VCO_TIMEOUT1 Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_TIMEOUT[7:0]	Main VCO calibration timeout	0x90	R/W

ADDRESS 0x21D, RESET: 0x01, NAME: VCO_TIMEOUT2

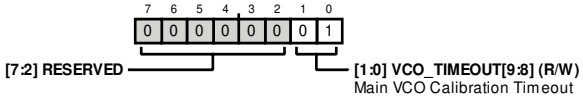


Table 38. VCO_TIMEOUT2 Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved	0x0	R
[1:0]	VCO_TIMEOUT[9:8]	Main VCO calibration timeout	0x1	R/W

ADDRESS 0x21E, RESET: 0x4B, NAME: VCO_BAND_DIV

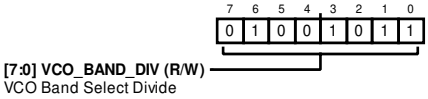


Table 39. VCO_BAND_DIV Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_BAND_DIV	VCO band select divide	0x4B	R/W

ADDRESS 0x21F, RESET: 0x18, NAME: VCO_READBACK_SEL

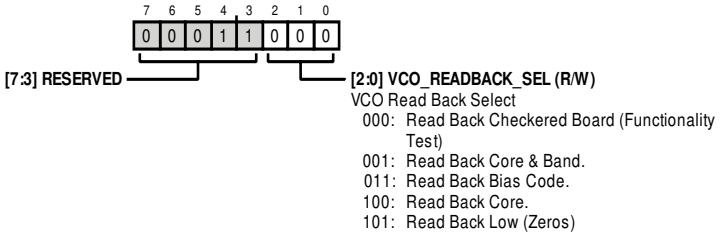


Table 40. VCO_READBACK_SEL Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved	0x3	R
[2:0]	VCO_READBACK_SEL	VCO read back select 000: Read back checkered board (functionality test) 001: Read back core and band 011: Read back bias code 100: Read back core 101: Read back low (zeros)	0x0	R/W

ADDRESS 0x226, RESET: 0x02, NAME: AUTOCAL

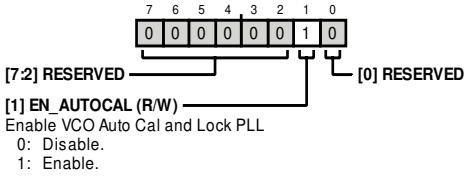


Table 41. AUTOCAL Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved	0x0	R
1	EN_AUTOCAL	Enable VCO autocalibration and lock PLL 0: Disable 1: Enable	0x1	R/W
0	RESERVED	Reserved	0x0	R

ADDRESS 0x22C, RESET: 0x07, NAME: CP_STATE

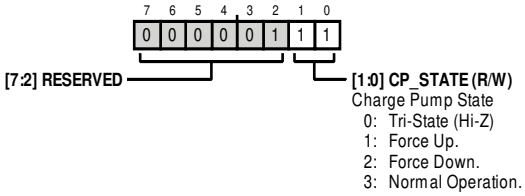


Table 42. CP_STATE Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved	0x1	R
[1:0]	CP_STATE	Charge pump state 0: Tristate (high-Z) 1: Force up 2: Force down 3: Normal operation	0x3	R/W

ADDRESS 0x22D, RESET: 0x01, NAME: CP_BLEED_EN

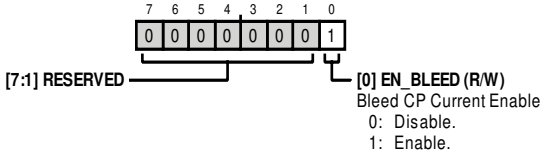


Table 43. CP_BLEED_EN Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved	0x0	R
0	EN_BLEED	Bleed CP current enable 0: Disable 1: Enable	0x1	R/W

ADDRESS 0x22E, RESET: 0x03, NAME: CP_CURRENT

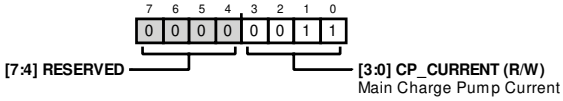


Table 44. CP_CURRENT Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved	0x0	R
[3:0]	CP_CURRENT	Main charge pump current bit	0x3	R/W

ADDRESS 0x22F, RESET: 0x0C, NAME: CP_BLEED

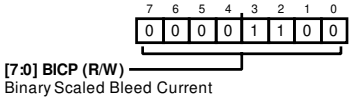


Table 45. CP_BLEED Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	BICP	Binary scaled bleed current	0xC	R/W

APPLICATIONS INFORMATION

EVALUATION BOARD

The ADMV4420-EVALZ evaluation board can be used to evaluate the performance of the ADMV4420. The top and cross sectional layout views of the ADMV4420-EVALZ evaluation board are shown in Figure 126 and Figure 127, respectively. The RF transmission lines were designed using a coplanar waveguide (CPWG) model with a line width (W) of 16 mil and 13 mil of ground spacing for a characteristic impedance of 50Ω for the RF input (RFIN) and the external reference input (REF/XTAL1). The line width and ground spacing for the IF output (IFOUT) are 9 mil and 15 mil, respectively. The PCB is made with Rogers 4350B dielectric material, which offers low loss performance, and isola 370HR dielectric material, which achieves the required thickness of the PCB.

The ADMV4420-EVALZ evaluation board layout consists of four layers. Layer 1 contains the charge pump, IF supplies (VPOS3_CP and VPOS4_IF), and the multiplexer output signal (MUXOUT) trace, which are routed together with the peripheral component placements. Layer 2 is arranged to provide the ground plane for the board. Layer 3 includes the VCO (VPOS1_VCO) supply, the PLL (VPOS2_PLL) supply, and digital SPI control signal ($\overline{CS}$, SDI, SDO, and SCLK) traces, and Layer 4 includes the chip enable (ENBL0 and ENBL1) traces on the bottom side of the board. Note that on the evaluation board, $\overline{CS}$ is indicated by CSB. Figure 128 to Figure 130 show the routing details of Layer 2 to Layer 4. For optimal RF and thermal grounding place as many plated through vias as possible around the RF transmission lines, underneath the exposed pad and throughout the entire PCB (See Figure 128).

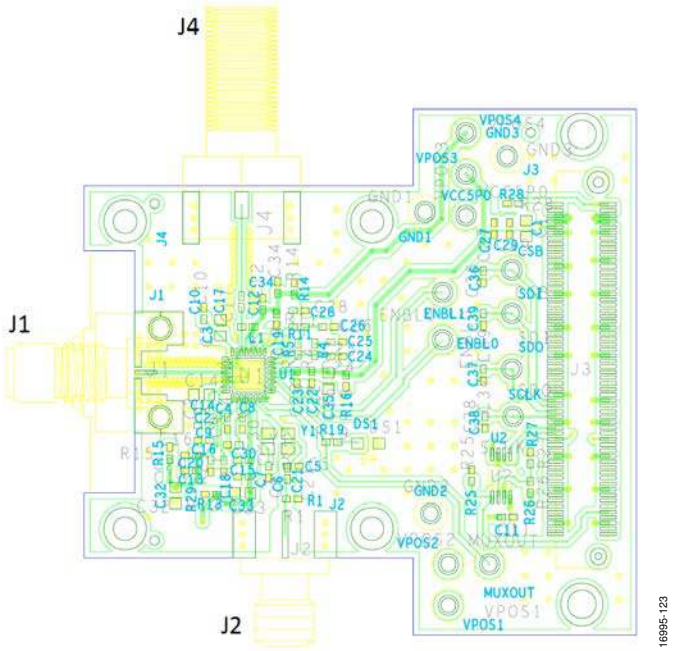


Figure 126. ADMV4420-EVALZ Evaluation Board Layout, Top View (Layer 1)

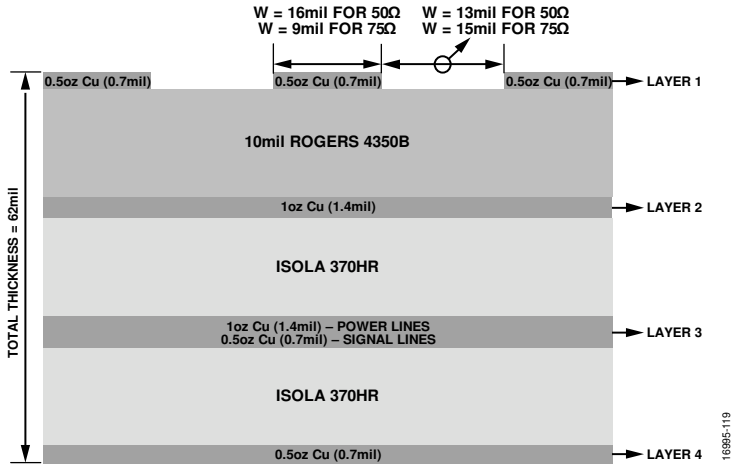


Figure 127. ADMV4420-EVALZ PCB, Cross Sectional View

Figure 128. ADMV4420-EVALZ Evaluation Board, Layer 2

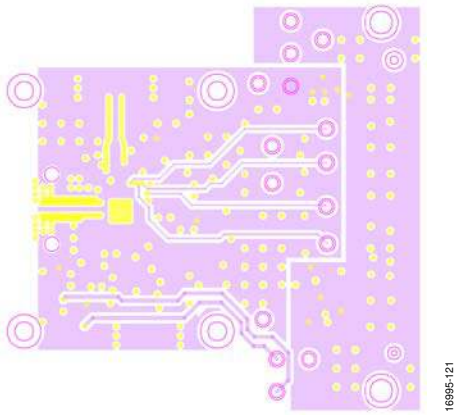


Figure 129. ADMV4420-EVALZ Evaluation Board, Layer 3

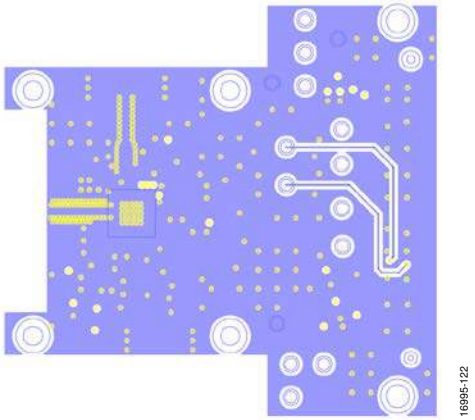


Figure 130. ADMV4420-EVALZ Evaluation Board, Layer 4 (Bottom Side)

Figure 126 shows the ADMV4420-EVALZ evaluation board with component placement. The decoupling capacitors on the LDO decoupling pin and power supply traces to minimize noise effects. The schematic and Pb-free reflow solder profile of the evaluation board are shown in and Figure 2 and Figure 132, respectively.

There are two options to power up the evaluation board. The first option is to apply a 5 V supply to the VPOS1, VPOS2, VPOS3, and VPOS4 test points for the VCO, PLL, CP, and IF blocks (VPOS1_VCO, VPOS2_PLL, VPOS3_CP, and VPOS4_IF pins) respectively, and connect a 0 V supply to one of the GND1, GND2, or GND3 ground test points. In this option, remove the R13, R14, R15, and R16 resistors from the evaluation board. This option allows the user to monitor the currents of each block separately.

The second option to power up the board requires the power supply to be applied through the VCC5P0 test point with the appropriate ground connection. Only the total current of the ADMV4420 can be monitored with this option. After powering up the evaluation board, program the required digital settings for the target configuration through the SDP-S controller board by using the Analysis, Control, Evaluation (ACE) software, which can be downloaded from the Analysis, Control, Evaluation (ACE) product page. See the ADMV4420-EVALZ user guide for details.

There are two different options to apply an external reference input to the ADMV4420, as shown in Figure 132. The required configurations for these options are described in Table 46. When using the Case 1 option, the external reference input is applied through the J2 connector with a signal generator. When using the Case 2 option, the external reference input is provided by the crystal (Y1).

A loop filter circuit generates the VCO control voltage (VTUNE) by applying the CP current output of the ADMV4420 from the charge pump output pin (CPOUT) to obtain the target LO frequency. Figure 131 shows the recommended schematic and Table 47 describes the loop filter components when the phase frequency detector frequency is 50 MHz. Table 48 describes the complete list of materials, which includes the loop filter components. For details about the evaluation board, see the ADMV4420-EVALZ user guide.

Table 46. External Reference Input Configurations

Option	Component Configuration
Case 1	Populate C21. Replace C6 with 1 nF capacitor. Remove C5 and Y1.
Case 2 (Default)	C5 = 20 pF, C6 = 20 pF. Do not populate C21.

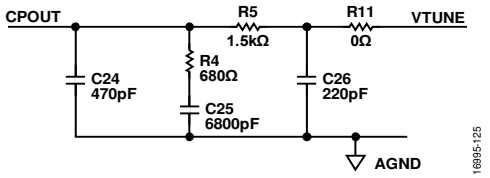


Figure 131. Recommended Integer Mode Loop Filter Schematic

Table 47. Recommended Integer Mode Loop Filter Components for Phase Frequency Detector = 50 MHz

Component	Value
C24	470 pF (0402)
C25	6800 pF (0402)
C26	220 pF (0402)
R4	680 Ω (0402)
R5	1.5 kΩ (0402)
R11	0 Ω (0402)

Table 48. Bill of Materials for ADMV4420-EVALZ

Reference Designator	Description
C1, C3, C14, C32, C33, C35	Power supply decoupling and LDO decoupling capacitor, 10 µF, 0603
C2, C10, C16, C18, C30	Power supply decoupling and LDO decoupling capacitor, 10 pF, 0402
C5, C6	Crystal loading capacitors
C7, C8, C11, C12, C13, C22, C27	Power supply decoupling and LDO decoupling capacitor, 0.1 µF, 0402
C15, C19, C20, C23, C29	Power supply decoupling and LDO decoupling capacitor, 100 pF, 0402)
C4, C34	Power supply decoupling and LDO decoupling capacitor, 10 µF, 0402
C9	Power supply decoupling and LDO decoupling capacitor, 4.7 µF, 0402
C17, C21	AC coupling capacitor, 0.01 µF, 0402
C24	Loop filter capacitor, 470 pF, 0402
C25	Loop filter capacitor, 6800 pF, 0402
C26	Loop filter capacitor, 220 pF, 0402
$\overline{CS}$, ENBL0, ENBL1, MUXOUT, SCLK, SDI, SDO	Test point, yellow
DS1	LED, green
GND1, GND2, GND3	Test point, black
J1	RF connector, SRI, K type, female
J2	RF connector, subminiature version a (SMA), female
J3	System demonstration platform (SDP) connector
J4	RF connector, F type, female
L1	Choke inductor, 51 nH, 0402
M1	Heat sink
R1	External reference input matching, 49.9 Ω, 0402
R11, R13, R14, R15, R16	Resistor, 0 Ω, 0402
R19, R29	Resistor, 1 kΩ, 0402
R25, R27	Resistor, pull-down, 100 kΩ, 0402
R4	Resistor, loop filter, 680 Ω, 0402
R5	Resistor, loop filter,1.5 kΩ, 0402
U1	K band downconverter with integrated fractional-N PLL and VCO, ADMV4420
U2	Serial EEPROM, 32-bit
VCC5P0, VPOS1, VPOS2, VPOS3, VPOS4	Test point, red
Y1	Crystal

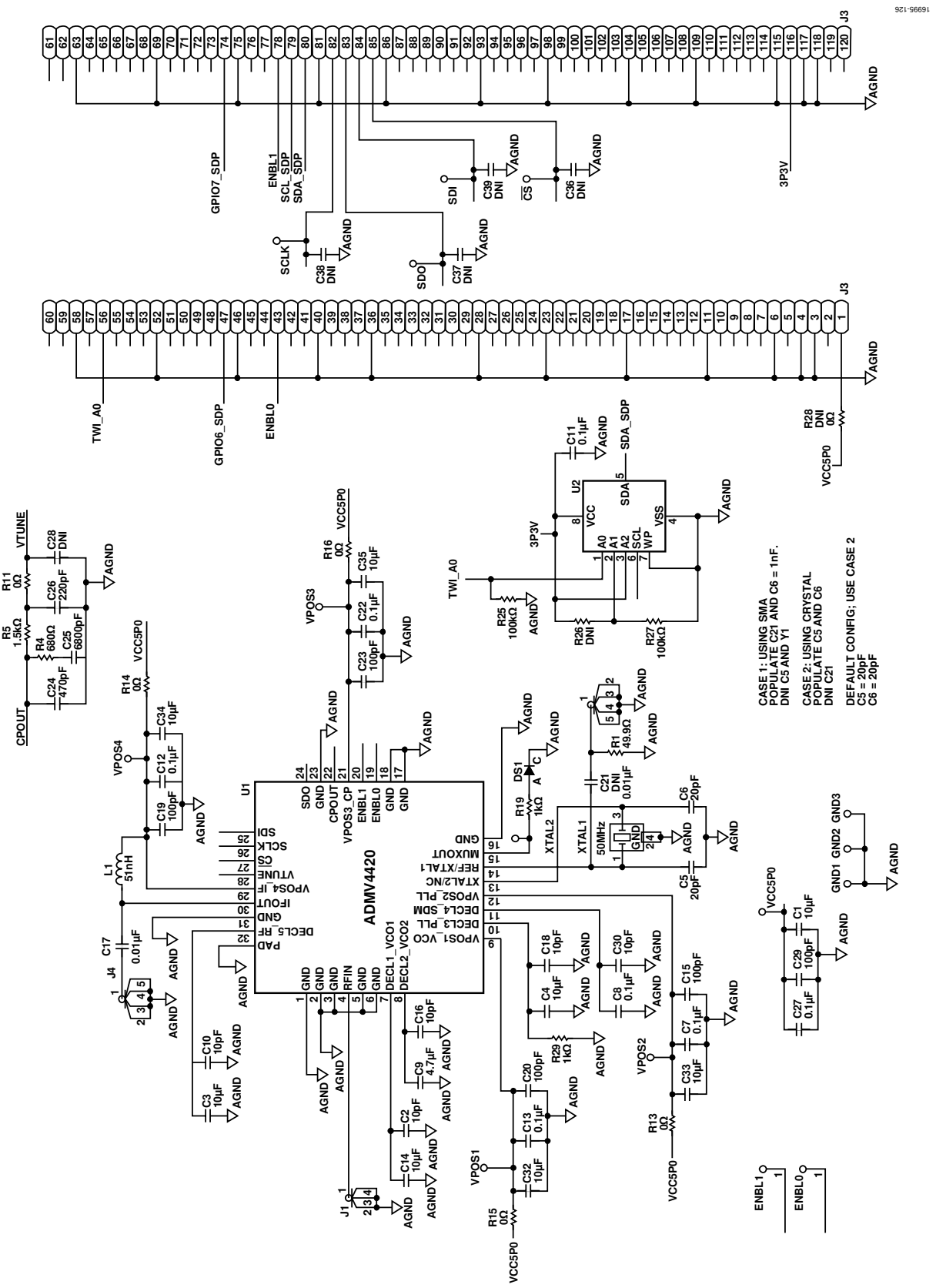
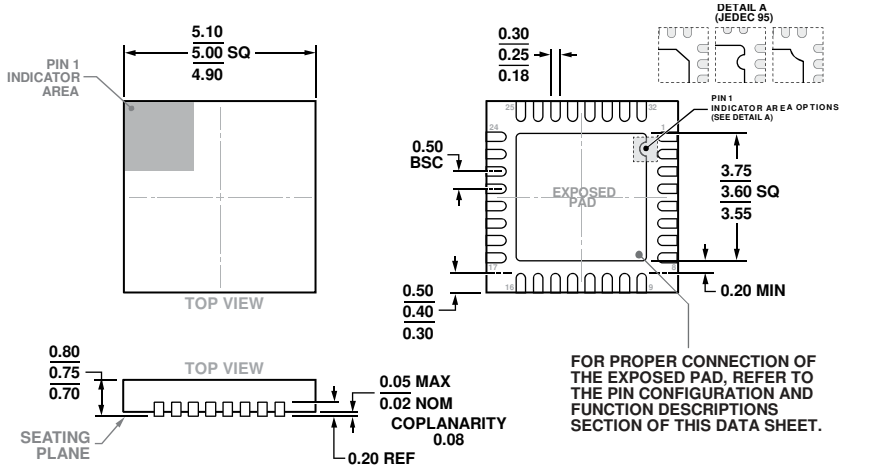


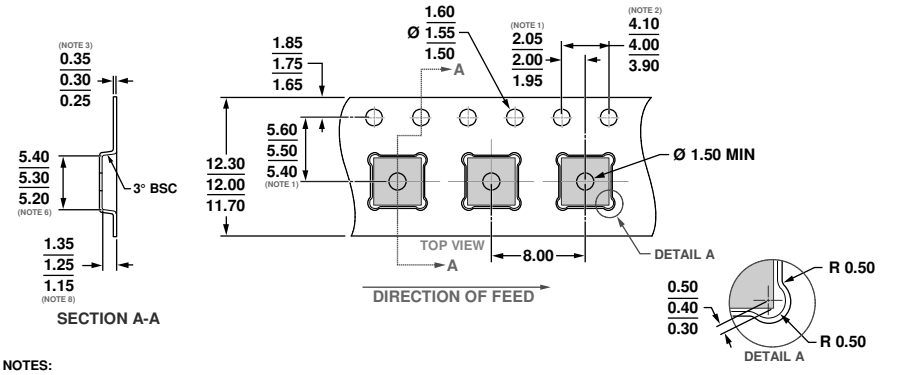
Figure 132. ADMV4420-EVALZ Evaluation Board Schematic

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5

Figure 133. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-12)
Dimensions shown in millimeters



NOTES:
1. MEASURED FROM THE CENTERLINE OF SPROCKET HOLE TO CENTERLINE OF THE POCKET HOLE
2. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE IS ± 0.20
3. THICKNESS IS APPLICABLE AS MEASURED AT EDGE OF TAPE
4. BLACK POLYSTYRENE MATERIAL
5. ALLOWABLE CAMBER TO BE 1 mm PER 100 mm IN LENGHT, NON-CUMULATIVE OVER 250 mm
6. MEASUREMENT POINT TO BE 0.3 mm FROM BOTTOM POCKET
7. SURFACE RESISTIVITY FROM 10^5 TO 10^{11} Ω/SQ
8. KO MEASUREMENT POINT SHOULD NOT BE REFERED ON POCKET RIDGE

Figure 134. 32-Lead Lead Frame Chip Scale Package [LFCSP] Tape and Reel Outline Dimensions
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Moisture Sensitivity Level (MSL) Rating[2]	Package Description	Package Option
ADMV4420ACPZ	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADMV4420ACPZ-R2	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADMV4420ACPZ-RL7	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADMV4420-EVALZ				

[1] Z = RoHS Compliant Part.
[2] See Table 2 and Figure 2 for the peak reflow temperature.

NOTES

D16995-0-4/19(A)