

5 V, 3 A Logic Controlled High-Side or Low-Side Load Switch

Data Sheet

FEATURES

Low RDS_{ON} of 10 m Ω in 6-ball WLCSP Wide input voltage range: 0 V to 5.5 V 3 A continuous operating current at 70°C Bias supply voltage range: 1.83 V to 5.5 V Low 26 μ A ground (quiescent) current, V_{IN} \leq 3.4 V Low 50 μ A quiescent current, V_{IN} = 5.5 V Overtemperature protection circuitry Low shutdown current: <3.5 μ A Ultrasmall 1.0 mm × 1.5 mm, 6-ball, 0.5 mm pitch WLCSP

APPLICATIONS

Communications and infrastructure

Thermoelectric cooler (TEC) controller reverse polarity for heating and cooling Fine line geometry core voltage inrush current control

Medical and healthcare Instrumentation

ADP1196

TYPICAL APPLICATIONS CIRCUITS

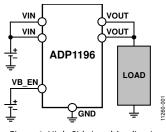
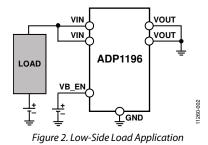


Figure 1. High-Side Load Application



GENERAL DESCRIPTION

The ADP1196 is a high-side or low-side load switch designed for VIN operation between 0 V and 5.5 V with a VB_EN supply of 1.83 V to 5.5 V. The device contains an internal charge pump that operates from either VIN or VB_EN, whichever is higher, and an ultralow on resistance, N-channel MOSFET. This N-channel MOSFET supports more than 2 A of continuous current at VIN close to 0 V, and, with its ultralow on resistance, minimizes power loss. In addition, the on resistance is constant, independent of the VIN or VB_EN voltage. The low 26 μ A quiescent current and ultralow shutdown current make the ADP1196 ideal for low power applications.

When the junction temperature exceeds 125°C, overtemperature protection circuitry is activated, thereby protecting the ADP1196 and downstream circuits from potential damage.

The ADP1196 occupies minimal printed circuit board (PCB) space, with an area of less than 1.5 mm² and a height of 0.60 mm.

The ADP1196 is available in an ultrasmall $1.0 \text{ mm} \times 1.5 \text{ mm}$, 6-ball, 0.5 mm pitch WLCSP.

Rev. B

Document Feedback

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A. Tel: 781.329.4700 ©2013–2014 Analog Devices, Inc. All rights reserved. Technical Support www.analog.com

TYPICAL PERFORMANCE CHARACTERISTICS

 V_{IN} = 1.8 V, V_{VB_EN} = 1.83 V, C_{IN} = C_{OUT} = 1 μ F, T_A = 25°C, unless otherwise noted.

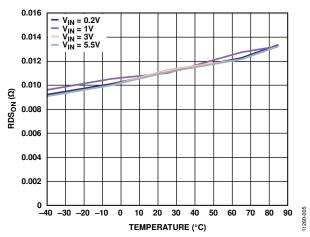


Figure 5. RDS_{ON} vs. Temperature, 50 mA, Different Input Voltages (V_{IN})

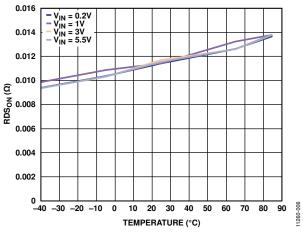


Figure 6. RDS_{ON} vs. Temperature, 3 A, Different Input Voltages (V_{IN})

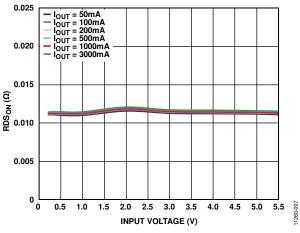


Figure 7. RDS_{ON} vs. Input Voltage (V_{IN}), Different Load Currents

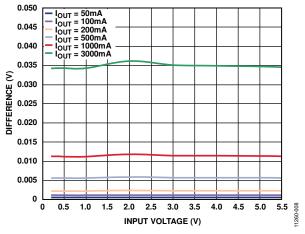


Figure 8. Voltage Drop vs. Input Voltage (V_{IN}), Different Load Currents

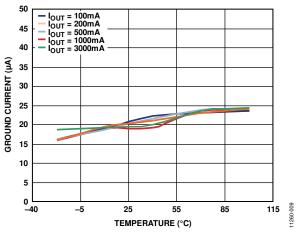


Figure 9. Ground Current vs. Temperature, Different Load Currents, $V_{IN} = 1.8 V$

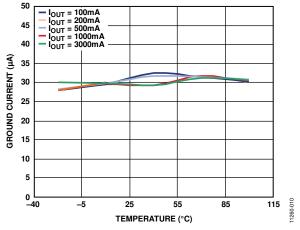


Figure 10. Ground Current vs. Temperature, Different Load Currents, $V_{IN} = 3.6 V$

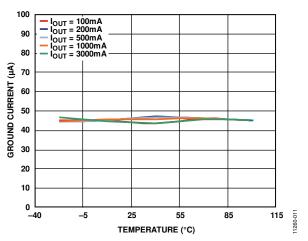
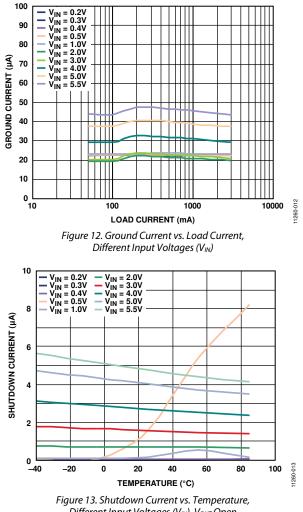
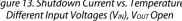
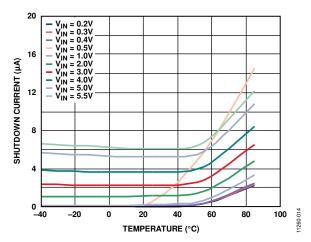
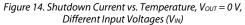


Figure 11. Ground Current vs. Temperature, Different Load Currents, $V_{IN} = 5 V$









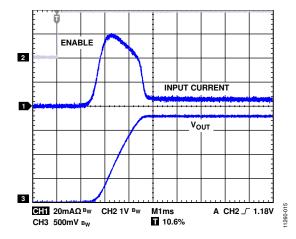


Figure 15. Typical Turn-On Time and Inrush Current, $V_{IN} = 1.8 V, C_{OUT} = 47 \mu F, 330 \Omega Load$

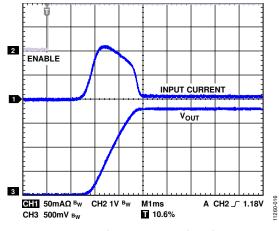
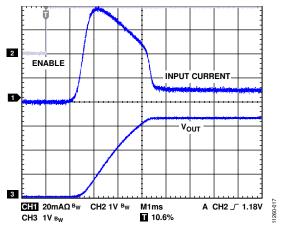
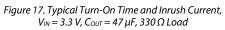
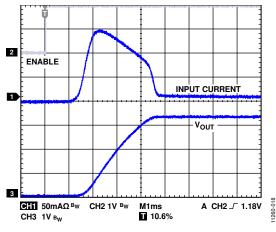
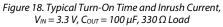


Figure 16. Typical Turn-On Time and Inrush Current, $V_{IN} = 1.8 V, C_{OUT} = 100 \mu F, 330 \Omega Load$









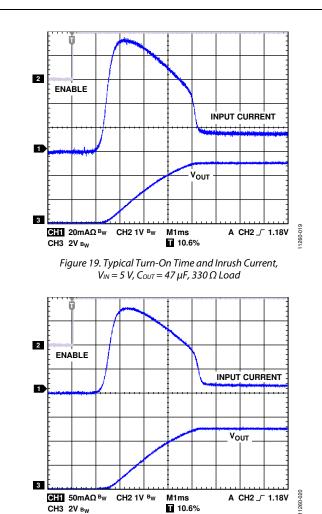


Figure 20. Typical Turn-On Time and Inrush Current, $V_{IN} = 5 V, C_{OUT} = 100 \,\mu F, 330 \,\Omega \,Load$

10.6%

CH3 2V BW

THEORY OF OPERATION

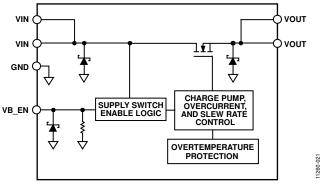


Figure 21. Functional Block Diagram

The ADP1196 is a high-side or low-side N-channel metal oxide semiconductor (NMOS) load switch that is controlled by an internal charge pump. The ADP1196 operates with voltages from 1.83 V to 5.5 V on either VIN or VB_EN.

Internal circuitry monitors the VIN and VB_EN pins, connecting the internal power supply to the higher of the two voltages. This operation allows the NMOS load switch to operate on the low side of a particular load.

An internal charge pump biases the NMOS switch to achieve a relatively constant, ultralow on resistance of 10 m Ω across the entire supply range. The use of the internal charge pump also allows for controlled turn-on times. Turning the NMOS switch on and off is controlled by the enable input, VB_EN, which can interface directly with 1.83 V logic signals when VIN is greater than 1.8 V.

The ADP1196 supports 3 A of continuous current as long as T_A is less than or equal to 70°C. At 85°C, the derated load current falls to ± 2.22 A.

The overtemperature protection circuit is activated if the load current causes the junction temperature to exceed 125°C. When this occurs, the overtemperature protection circuitry disables the output until the junction temperature falls below approximately 110°C, at which point the output is reenabled. If the fault condition persists, the output cycles off and on until the fault is removed.

ESD protection structures are shown in the block diagram as Zener diodes (see Figure 21).

The ADP1196 is a low quiescent current device with a nominal 4 M Ω pull-down resistor on its enable pin (VB_EN). The package is a space-saving 1.0 mm \times 1.5 mm, 6-ball WLCSP.

APPLICATIONS INFORMATION CAPACITOR SELECTION

Output Capacitor

The ADP1196 is designed for operation with small, spacesaving ceramic capacitors; however, it functions with most commonly used capacitors when the effective series resistance (ESR) value is carefully considered. The ESR of the output capacitor affects the response to load transients. Use a typical 1 μ F capacitor with an ESR of 0.1 Ω or less for good transient response. Using a larger value of output capacitance improves the transient response to large changes in load current.

Input Bypass Capacitor

Connecting at least 1 μ F of capacitance from VIN to GND reduces the circuit sensitivity to the PCB layout, especially when high source impedance or long input traces are encountered. When greater than 1 μ F of output capacitance is required, increase the input capacitor to match it.

GROUND CURRENT

The major source of ground current in the ADP1196 is the internal charge pump for the field effect transistor (FET) drive circuitry. Figure 22 shows the typical ground current when $V_{VB_EN} = 1.83$ V and V_{IN} varies from 0.2 V to 5.5 V.

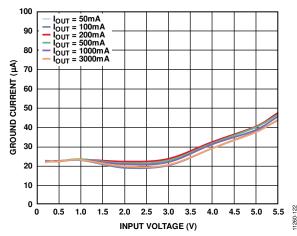
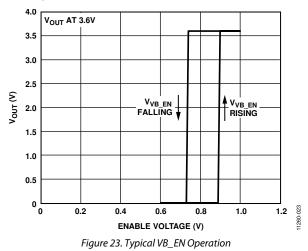


Figure 22. Ground Current vs. Input Voltage, Different Load Currents

ENABLE FEATURE

The ADP1196 uses the VB_EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 23, when a rising voltage (V_{VB_EN}) on the VB_EN pin crosses the active threshold, VOUT turns on. When a falling voltage (V_{VB_EN}) on the VB_EN pin crosses the inactive threshold, VOUT turns off.



As shown in Figure 23, the VB_EN pin has hysteresis built into it. This built-in hysteresis prevents on/off oscillations that can occur due to noise on the VB_EN pin as it passes through the threshold points.

The VB_EN pin active/inactive thresholds derive from the V_{IN} voltage; therefore, these thresholds vary with changing input voltages. Figure 24 shows the typical VB_EN active/inactive threshold when the input voltage varies from 1.83 V to 5.5 V.

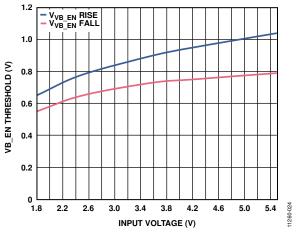


Figure 24. Typical VB_EN Threshold vs. Input Voltage (VIN)

TIMING

Turn-on delay is defined as the interval between the time that V_{VB_EN} exceeds the rising threshold voltage and when V_{OUT} rises to ~10% of its final value. The ADP1196 includes circuitry that has a typical 2 ms turn-on delay and a controlled rise time to limit the V_{IN} inrush current. As shown in Figure 25 and Figure 26, the turn-on delay is nearly independent of the input voltage.

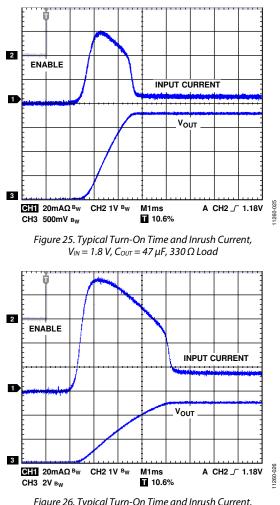


Figure 26. Typical Turn-On Time and Inrush Current, $V_{\rm IN} = 5 V$, $C_{\rm OUT} = 47 \mu$ F, 330 Ω Load

The rise time is defined as the time it takes the output voltage (V_{OUT}) to rise from 10% to 90% of its final value. The output voltage rise time is dependent on the rise time of the internal charge pump.

For very large values of output capacitance, the RC time constant (where C is the load capacitance (C_{LOAD}) and R is the RDS_{ON} ||R_{LOAD}) can become a factor in the rise time of the output voltage. Because RDS_{ON} is much smaller than R_{LOAD}, an adequate approximation for RC is RDS_{ON} × C_{LOAD}. An input or load capacitor is not required for the ADP1196, although capacitors can be used to suppress noise on the board.

The turn-off time is defined as the time it takes for the output voltage to fall from 90% to 10% of V_{OUT}. It is also dependent on the RC time constant of the output capacitance and load resistance. Figure 27 shows the typical turn-off times with V_{IN} = 1.8 V, V_{IN} = 3.3 V, and V_{IN} = 5.0 V, C_{OUT} = 47 μ F, and R_{LOAD} = 330 Ω .

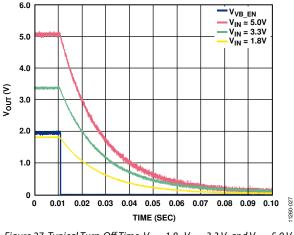


Figure 27. Typical Turn-Off Time, $V_{\rm IN}$ = 1.8 , $V_{\rm IN}$ = 3.3 V, and $V_{\rm IN}$ = 5.0 V, $C_{\rm OUT}$ = 47 μ F, $R_{\rm LOAD}$ = 330 Ω

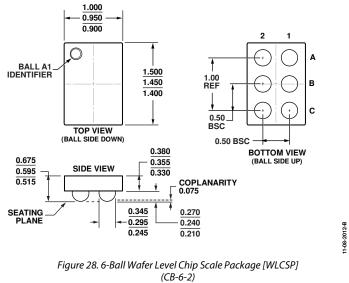
THERMAL OVERLOAD PROTECTION

Thermal overload protection is included, which limits the junction temperature to a maximum of 125°C (typical). Under extreme conditions (that is, high ambient temperature and/or high power dissipation), when the junction temperature starts to rise above 125°C, the output is turned off, reducing the output current to zero. When the junction temperature falls below 110°C, the output is turned on again, and output current is restored to its operating value.

If the self-heating of the junction is great enough to cause its temperature to rise above 125°C, thermal shutdown is activated, turning off the output and reducing the output current to zero. As the junction temperature cools and falls below 110°C, the output turns on and conducts current into the load, again causing the junction temperature to rise above 125°C. This thermal oscillation between 110°C and 125°C causes a current oscillation between the load current and 0 mA that continues as long as the load remains connected to the output.

The thermal limit protection is intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that the junction temperature does not exceed 125°C.

OTTLINE DIMENSIONS



Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADP1196ACBZ-02-R7	40 Cto +85 C	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	CK

¹Z = RoHSCompliant Part.

©2013–2014 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners. D11260-0-4/14(B)



www.analog.com