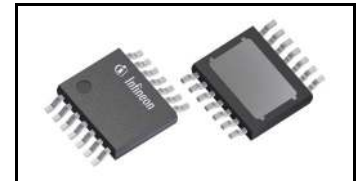


# TLE94103EP



## Features

- Three half bridge power outputs
- Very low power consumption in sleep mode
- 3.3V / 5V compatible inputs with hysteresis
- All outputs with overload and short circuit protection
- Independently diagnosable outputs (overcurrent, open load)
- Open load diagnostics in ON-state for all high-side and low-side
- 16-bit Standard SPI interface with daisy chain and in-frame response capability for control and diagnosis
- Fast diagnosis with the global error flag
- Overtemperature pre-warning and protection
- Over- and Undervoltage lockout
- Cross-current protection



## Potential applications

- HVAC Flap DC motors
- Monostable and bistable relays
- Side mirror x-y adjustment

## Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100

## Description

The TLE94103EP is a protected triple half-bridge driver designed especially for automotive motion control applications such as side mirror x-y adjustment. It is part of a larger family offering half-bridge drivers from three outputs to twelve outputs with direct interface or SPI interface.

The half bridge drivers are designed to drive DC motor loads in sequential or parallel operation. Operation modes forward (cw), reverse (ccw), brake and high impedance are controlled from a 16-bit SPI interface. It offers diagnosis features such as short circuit, open load, power supply failure and overtemperature detection. In combination with its low quiescent current, this device is attractive among others for automotive applications. The small fine pitch exposed pad package, PG-TSDSO-14, provides good thermal performance and reduces PCB-board space and costs.

Type	Package	Marking
TLE94103EP	PG-TSDSO-14	TLE94103

**Table 1 Product Summary**

Operating Voltage	$V_S$	5.5 ... 20 V
Logic Supply Voltage	$V_{DD}$	3.0 ... 5.5 V
Maximum Supply Voltage for Load Dump Protection	$V_{S(LD)}$	40 V
Minimum Overcurrent Threshold	$I_{SD}$	0.9 A
Maximum On-State Path Resistance at $T_j = 150^\circ\text{C}$	$R_{DSON(total)\_HSx+LSy}$	1.8 + 1.8 $\Omega$
Typical Quiescent Current at $T_j = 85^\circ\text{C}$	$I_{SQ}$	0.1 $\mu\text{A}$
Maximum SPI Access Frequency	$f_{SCLK}$	5 MHz

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## Pin Configuration

### 1 Pin Configuration

#### 1.1 Pin Assignment

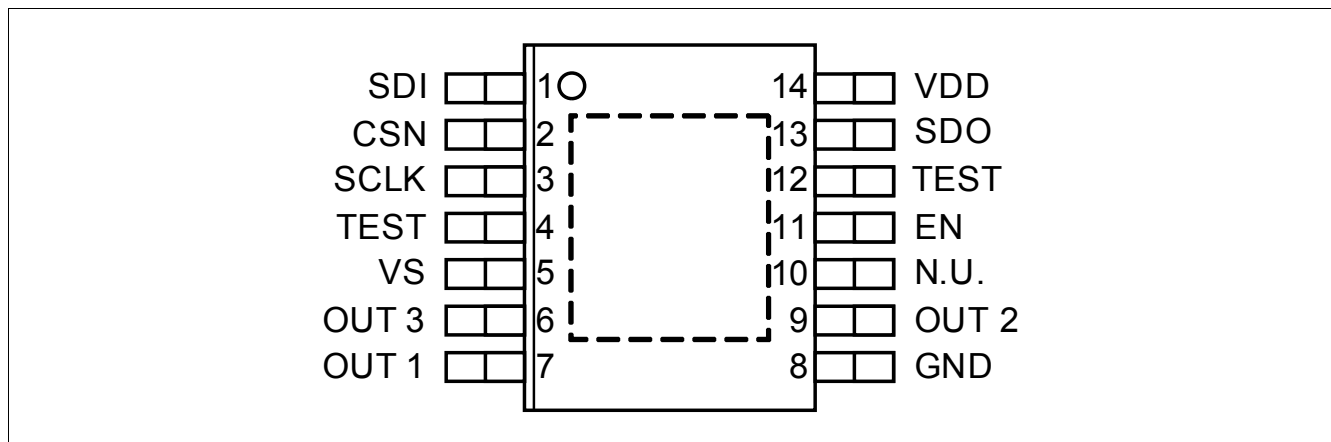


Figure 1 Pin Configuration TLE94103EP with SPI interface

#### 1.2 Pin Definitions and Functions

Pin	Symbol	Function
1	SDI	Serial data input with internal pull down
2	CSN	Chip select Not input with internal pull up
3	SCLK	Serial clock input with internal pull down
4	TEST	Test input. This pin can be left open or be terminated to ground.
5	VS	Main supply voltage for power half bridges.
6	OUT 3	Power half-bridge 3
7	OUT 1	Power half-bridge 1
8	GND	Ground
9	OUT 2	Power half-bridge 2
10	N.U.	Not used. This pin should be left open or terminated to GND.
11	EN	Enable with internal pull-down; Places device in standby mode by pulling the EN line Low
12	TEST	Test pin. This pin must be terminated to ground.
13	SDO	Serial data output
14	VDD	Logic supply voltage
EDP	-	Exposed Die Pad; For cooling and EMC purposes only - not usable as electrical ground. Electrical ground must be provided by pins 8. <sup>1)</sup>

1) The exposed die pad at the bottom of the package allows better heat dissipation from the device via the PCB. The exposed pad (EP) must be either left open or connected to GND. It is recommended to connect EP to GND for best EMC and thermal performance.

---

**Pin Configuration**

*Note: Not used (N.U.) pins and unused outputs are recommended to be left unconnected (open) on the application board. If N.U. pins or unused output pins are routed to an external connector which leaves the PCB, then these outputs should have provision for a zero ohm jumper (depopulated if unused) or ESD protection. In other words, they should be treated like used pins.*

Block Diagram

2 Block Diagram

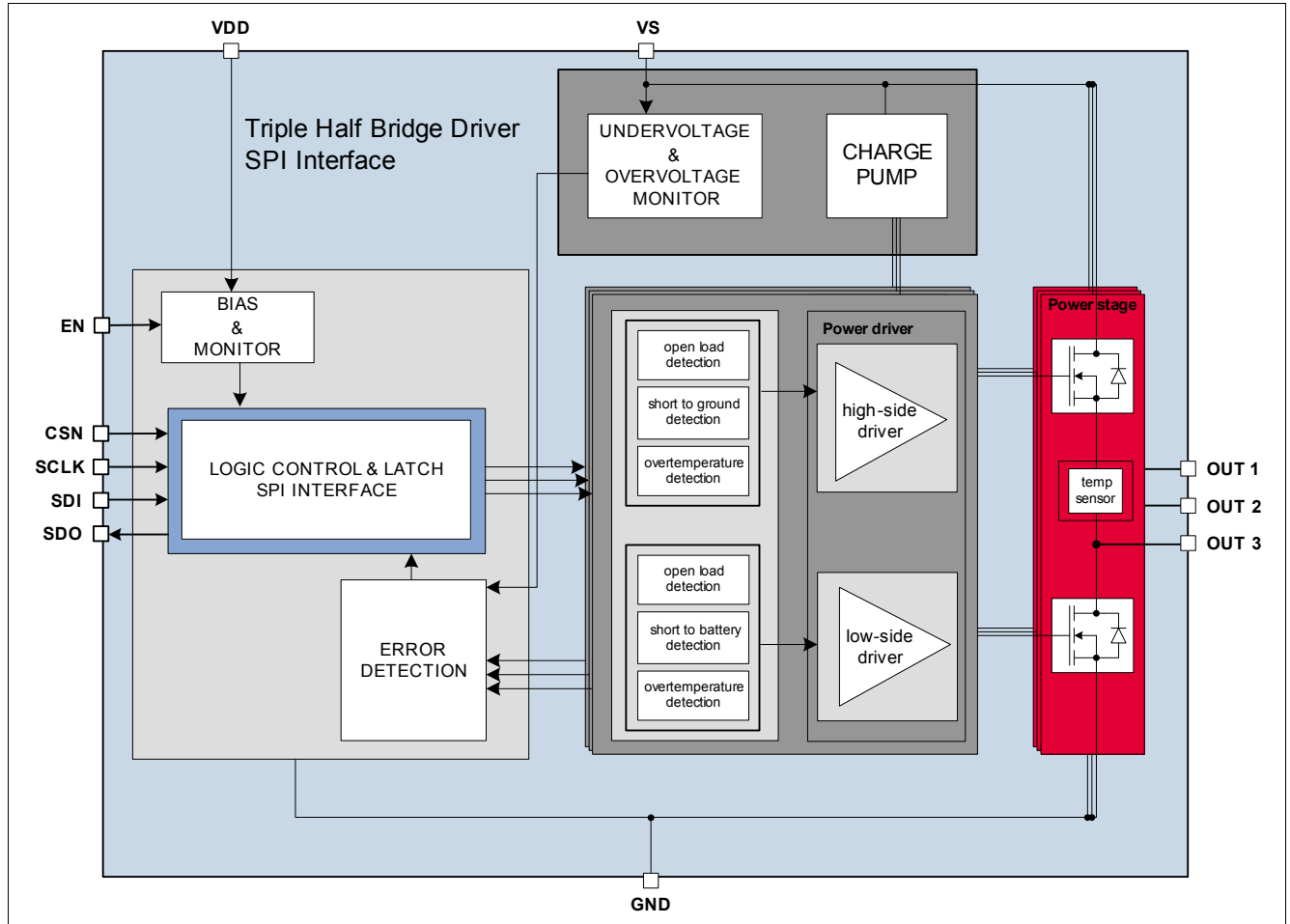


Figure 2 Block Diagram TLE94103EP (SPI Interface)

Block Diagram

2.1 Voltage and current definition

Figure 3 shows terms used in this datasheet, with associated convention for positive values.

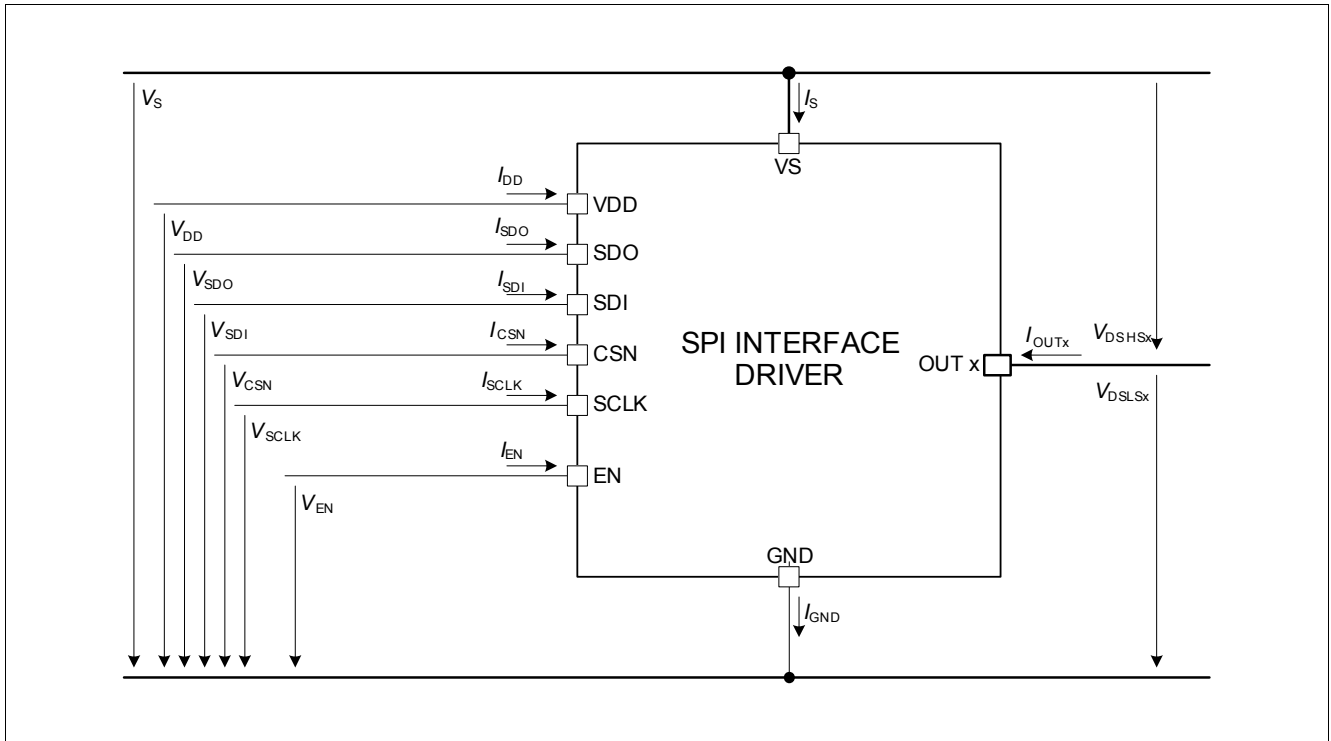


Figure 3 Voltage and Current Definition



## General Product Characteristics

### 3 General Product Characteristics

#### 3.1 Absolute Maximum Ratings

**Table 2 Absolute Maximum Ratings<sup>1)</sup>  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Voltages</b>							
Supply voltage	$V_S$	-0.3	–	40	V		P_4.1.1
Supply Voltage Slew Rate	$ dV_S/dt $	–	–	10	V/ $\mu\text{s}$	$V_S$ increasing and decreasing <sup>1)</sup>	P_4.2.2
Power half-bridge output voltage	$V_{\text{OUT}}$	-0.3	–	40	V	$0\text{ V} < V_{\text{OUT}} < V_S$ <sup>2)</sup>	P_4.1.2
Logic supply voltage	$V_{\text{DD}}$	-0.3	–	5.5	V	$0\text{ V} < V_S < 40\text{ V}$	P_4.1.3
Logic input voltages (SDI, SCLK, CSN, EN)	$V_{\text{SDI}}, V_{\text{SCLK}}, V_{\text{CSN}}, V_{\text{EN}}$	-0.3	–	VDD	V	$0\text{ V} < V_S < 40\text{ V}$ $0\text{ V} < V_{\text{DD}} < 5.5\text{ V}$	P_4.1.4
Logic output voltage (SDO)	$V_{\text{SDO}}$	-0.3	–	VDD	V	$0\text{ V} < V_S < 40\text{ V}$ $0\text{ V} < V_{\text{DD}} < 5.5\text{ V}$	P_4.1.5
Test pins	$V_{\text{TEST}}$	-0.3	–	VDD	V	$0\text{ V} < V_S < 40\text{ V}$ $0\text{ V} < V_{\text{DD}} < 5.5\text{ V}$	P_4.1.19
<b>Currents</b>							
Continuous Supply Current for $V_S$	$I_S$	0	–	1.5	A	–	P_4.1.20
Current per GND pin	$I_{\text{GND}}$	0	–	2.0	A	–	P_4.1.14
Output Currents	$I_{\text{OUT}}$	-2.0	–	2.0	A	–	P_4.1.15
<b>Temperatures</b>							
Junction temperature	$T_j$	-40	–	150	$^\circ\text{C}$	–	P_4.1.8
Storage temperature	$T_{\text{stg}}$	-50	–	150	$^\circ\text{C}$	–	P_4.1.9
<b>ESD Susceptibility</b>							
ESD susceptibility OUTn and VS pins versus GND. All other pins grounded.	$V_{\text{ESD}}$	-4	–	4	kV	JEDEC HBM <sup>1)3)</sup>	P_4.1.10
ESD susceptibility all pins	$V_{\text{ESD}}$	-2	–	2	kV	JEDEC HBM <sup>1)3)</sup>	P_4.1.11
ESD susceptibility all pins	$V_{\text{ESD}}$	-500	–	500	V	CDM <sup>1)4)</sup>	P_4.1.12
ESD susceptibility corner pins	$V_{\text{ESD}}$	-750	–	750	V	CDM <sup>1)4)</sup>	P_4.1.13

1) Not subject to production test, specified by design

2) Also applicable to not used (N.U.) pins

3) ESD susceptibility, "JEDEC HBM" according to ANSI/ ESDA/ JEDEC JS001 (1.5 k $\Omega$ , 100pF)

4) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101

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**General Product Characteristics****Notes**

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

---

**General Product Characteristics**
**3.2 Functional Range**
**Table 3 Functional Range**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation	$V_{S(nor)}$	5.5	–	20	V	–	P_4.2.1
Logic supply voltage range for normal operation	$V_{DD}$	3.0	–	5.5	V	–	P_4.2.3
Logic input voltages (SDI, SCLK, CSN, EN)	$V_{SDI}$ , $V_{SCLK}$ , $V_{CSN}$ , $V_{EN}$	-0.3	–	5.5	V	–	P_4.2.4
Junction temperature	$T_j$	-40	–	150	°C		P_4.2.5

*Note: Within the normal functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## General Product Characteristics

### 3.3 Thermal Resistance

**Table 4 Thermal Resistance TLE94103EP**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case, $T_A = -40^\circ\text{C}$	$R_{thjC\_cold}$	–	16	–	K/W	1)	
Junction to Case, $T_A = 85^\circ\text{C}$	$R_{thjC\_hot}$	–	19	–	K/W	1)	
Junction to ambient, $T_A = -40^\circ\text{C}$ (1s0p, minimal footprint)	$R_{thjA\_cold\_min}$	–	136	–	K/W	1) 2)	
Junction to ambient, $T_A = 85^\circ\text{C}$ (1s0p, minimal footprint)	$R_{thjA\_hot\_min}$	–	148	–	K/W	1) 2)	
Junction to ambient, $T_A = -40^\circ\text{C}$ (1s0p, 300mm <sup>2</sup> Cu)	$R_{thjA\_cold\_300}$	–	79	–	K/W	1) 3)	
Junction to ambient, $T_A = 85^\circ\text{C}$ (1s0p, 300mm <sup>2</sup> Cu)	$R_{thjA\_hot\_300}$	–	95	–	K/W	1) 3)	
Junction to ambient, $T_A = -40^\circ\text{C}$ (1s0p, 600mm <sup>2</sup> Cu)	$R_{thjA\_cold\_600}$	–	77	–	K/W	1) 4)	
Junction to ambient, $T_A = 85^\circ\text{C}$ (1s0p, 600mm <sup>2</sup> Cu)	$R_{thjA\_hot\_600}$	–	94	–	K/W	1) 4)	
Junction to ambient, $T_A = -40^\circ\text{C}$ (2s2p)	$R_{thjA\_cold\_2s2p}$	–	63	–	K/W	1) 5)	
Junction to ambient, $T_A = 85^\circ\text{C}$ (2s2p)	$R_{thjA\_hot\_2s2p}$	–	82	–	K/W	1) 5)	

1) Not subject to production test, specified by design.

2) Specified  $R_{thjA}$  value is according to JEDEC JESD51-2, -3 at natural convection on FR4 1s0p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with minimal footprint copper area and 35 $\mu\text{m}$  thickness.  $T_a = -40^\circ\text{C}$ , each channel dissipates 0.2W.  $T_a = 85^\circ\text{C}$ , each channel dissipates 0.135W.

3) Specified  $R_{thjA}$  value is according to JEDEC JESD51-2, -3 at natural convection on FR4 1s0p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with additional cooling of 300mm<sup>2</sup> copper area and 35 $\mu\text{m}$  thickness.  $T_a = -40^\circ\text{C}$ , each channel dissipates 0.2W.  $T_a = 85^\circ\text{C}$ , each channel dissipates 0.135W.

4) Specified  $R_{thjA}$  value is according to JEDEC JESD51-2, -3 at natural convection on FR4 1s0p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with additional cooling of 600mm<sup>2</sup> copper area and 35 $\mu\text{m}$  thickness.  $T_a = -40^\circ\text{C}$ , each channel dissipates 0.2W.  $T_a = 85^\circ\text{C}$ , each channel dissipates 0.135W.

5) Specified  $R_{thjA}$  value is according to JEDEC JESD51-2, -3 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with two inner copper layers ( 4 x 35 $\mu\text{m}$  Cu).  $T_a = -40^\circ\text{C}$ , each channel dissipates 0.2W.  $T_a = 85^\circ\text{C}$ , each channel dissipates 0.135W.

## General Product Characteristics

### 3.4 Electrical Characteristics

**Table 5** Electrical Characteristics,  $V_S=5.5\text{ V to }20\text{ V}$ ,  $V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $T_j = -40^\circ\text{C to }+150^\circ\text{C}$ , EN= HIGH,  $I_{OUTn} = 0\text{ A}$ ; Typical values refer to  $V_{DD} = 5.0\text{ V}$ ,  $V_S = 13.5\text{ V}$  and  $T_j = 25^\circ\text{C}$  unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Current Consumption, EN = GND</b>							
Supply Quiescent current	$I_{SQ}$	–	0.1	2	$\mu\text{A}$	$-40^\circ\text{C} \leq T_j \leq 85^\circ\text{C}$	P_4.4.1
Logic supply quiescent current	$I_{DD\_Q}$	–	0.1	1	$\mu\text{A}$	$-40^\circ\text{C} \leq T_j \leq 85^\circ\text{C}$	P_4.4.2
Total quiescent current	$I_{SQ} + I_{DD\_Q}$	–	0.6	3	$\mu\text{A}$	$-40^\circ\text{C} \leq T_j \leq 85^\circ\text{C}$	P_4.4.3
<b>Current Consumption, EN=HIGH</b>							
Supply current	$I_S$	–	0.13	0.5	mA	Power drivers and power stages are off	P_4.4.4
Supply current	$I_{S\_HSON}$	–	1.5	3	mA	All high-sides ON <sup>1)2)</sup>	P_4.4.101
Logic supply current	$I_{DD}$	–	0.6	2.5	mA	SPI not active	P_4.4.5
Logic supply current	$I_{DD\_RUN}$	–	2.5	–	mA	SPI 5MHz <sup>2)</sup>	P_4.4.6
Total supply current	$I_S + I_{DD\_RUN}$	–	2.7	–	mA	SPI 5MHz <sup>2)</sup>	P_4.4.7
<b>Over- and Undervoltage Lockout</b>							
Undervoltage Switch ON voltage threshold	$V_{UV\_ON}$	4.4	4.90	5.3	V	$V_S$ increasing	P_4.4.8
Undervoltage Switch OFF voltage threshold	$V_{UV\_OFF}$	4	4.50	4.9	V	$V_S$ decreasing	P_4.4.9
Undervoltage Switch ON/OFF hysteresis	$V_{UV\_HY}$	–	0.40	–	V	$V_{UV\_ON} - V_{UV\_OFF}$ <sup>2)</sup>	P_4.4.10
Oversvoltage Switch OFF voltage threshold	$V_{OV\_OFF}$	21	23	25	V	$V_S$ increasing	P_4.4.11
Oversvoltage Switch ON voltage threshold	$V_{OV\_ON}$	20	22	24	V	$V_S$ decreasing	P_4.4.12
Oversvoltage Switch ON/OFF hysteresis	$V_{OV\_HY}$	–	1	–	V	$V_{OV\_OFF} - V_{OV\_ON}$ <sup>2)</sup>	P_4.4.13
$V_{DD}$ Power-On-Reset	$V_{DD\_POR}$	2.40	2.63	2.90	V	$V_{DD}$ increasing	P_4.4.14
$V_{DD}$ Power-Off-Reset	$V_{DD\_POFFR}$	2.35	2.57	2.85	V	$V_{DD}$ decreasing	P_4.4.15
$V_{DD}$ Power ON/OFF hysteresis	$V_{DD\_POR\_HY}$	–	0.06	–	V	$V_{DD\_POR} - V_{DD\_POFFR}$ <sup>2)</sup>	P_4.4.98
<b>Static Drain-source ON-Resistance (High-Side or Low-Side)</b>							
High-Side or Low-Side $R_{DSON}$ (all outputs)	$R_{DSON\_HB\_25C}$	–	825	1200	m $\Omega$	$I_{OUT} = \pm 0.5\text{ A}$ ; $T_j = 25^\circ\text{C}$	P_4.4.16
High-Side or Low-Side $R_{DSON}$ (all outputs)	$R_{DSON\_HB\_150C}$	–	1350	1800	m $\Omega$	$I_{OUT} = \pm 0.5\text{ A}$ ; $T_j = 150^\circ\text{C}$	P_4.4.17

## General Product Characteristics

**Table 5** Electrical Characteristics,  $V_S = 5.5\text{ V to }20\text{ V}$ ,  $V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $T_j = -40^\circ\text{C to }+150^\circ\text{C}$ ,  $EN = \text{HIGH}$ ,  $I_{OUTn} = 0\text{ A}$ ; Typical values refer to  $V_{DD} = 5.0\text{ V}$ ,  $V_S = 13.5\text{ V}$  and  $T_j = 25^\circ\text{C}$  unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Output Protection and Diagnosis of high-side (HS) channels of half-bridge output</b>							
HS Overcurrent Shutdown Threshold	$I_{SD\_HS}$	-1.5	-1.2	-0.9	A	See <a href="#">Figure 5</a>	P_4.4.20
Difference between shutdown and limit current	$I_{LIM\_HS} - I_{SD\_HS}$	-1.2	-0.6	0	A	<sup>2)</sup> $ I_{LIM\_HS}  \geq  I_{SD\_HS} $ See <a href="#">Figure 5</a>	P_4.4.21
Overcurrent Shutdown filter time	$t_{dSD\_HS}$	15	19	23	$\mu\text{s}$	<sup>2)</sup>	P_4.4.22
Open Load Detection Current	$I_{OLD1\_HS}$	-15	-8	-3	mA	-	P_4.4.23
Open Load Detection filter time	$t_{OLD1\_HS}$	2000	3000	4000	$\mu\text{s}$	<sup>2)</sup>	P_4.4.24
<b>Output Protection and Diagnosis of low-side (LS) channels of half-bridge output</b>							
LS Overcurrent Shutdown Threshold	$I_{SD\_LS}$	0.9	1.2	1.5	A	See <a href="#">Figure 6</a>	P_4.4.27
Difference between shutdown and limit current	$I_{LIM\_LS} - I_{SD\_LS}$	0	0.6	1.2	A	<sup>2)</sup> $I_{LIM\_LS} \geq I_{SD\_LS}$ <a href="#">Figure 6</a>	P_4.4.28
Overcurrent Shutdown filter time	$t_{dSD\_LS}$	15	19	23	$\mu\text{s}$	<sup>2)</sup>	P_4.4.29
Open Load Detection Current	$I_{OLD\_LS}$	3	8	15	mA	-	P_4.4.30
Open Load Detection filter time	$t_{OLD\_LS}$	2000	3000	4000	$\mu\text{s}$	<sup>2)</sup>	P_4.4.31
<b>Outputs OUT(1...n) leakage current</b>							
HS leakage current in off state	$I_{QLHn\_NOR}$	-2	-0.5	-	$\mu\text{A}$	$V_{OUTn} = 0\text{ V}$ ; $EN = \text{High}$	P_4.4.32
HS leakage current in off state	$I_{QLHn\_SLE}$	-2	-0.5	-	$\mu\text{A}$	$V_{OUTn} = 0\text{ V}$ ; $EN = \text{GND}$	P_4.4.33
LS Leakage current in off state	$I_{QLLn\_NOR}$	-	0.5	2	$\mu\text{A}$	$V_{OUTn} = V_S$ ; $EN = \text{High}$	P_4.4.34
LS Leakage current in off state	$I_{QLLn\_SLE}$	-	0.5	2	$\mu\text{A}$	$V_{OUTn} = V_S$ ; $EN = \text{GND}$	P_4.4.35
<b>Output Switching Times. See <a href="#">Figure 7</a> and <a href="#">Figure 8</a>.</b>							
Slew rate of high-side and low-side outputs	$d_{VOUT}/dt$	0.1	0.45	0.75	$\text{V}/\mu\text{s}$	Resistive load = $100\Omega$ ; $V_S = 13.5\text{ V}$ <sup>3)</sup>	P_4.4.36
Output delay time high side driver on	$t_{dONH}$	5	20	35	$\mu\text{s}$	Resistive load = $100\Omega$ to GND	P_4.4.37
Output delay time high side driver off	$t_{dOFFH}$	15	45	75	$\mu\text{s}$	Resistive load = $100\Omega$ to GND	P_4.4.38
Output delay time low side driver on	$t_{dONL}$	5	20	35	$\mu\text{s}$	Resistive load = $100\Omega$ to VS	P_4.4.39
Output delay time low side driver off	$t_{dOFFL}$	15	45	75	$\mu\text{s}$	Resistive load = $100\Omega$ to VS	P_4.4.40
Cross current protection time, high to low	$t_{DHL}$	100	130	160	$\mu\text{s}$	Resistive load = $100\Omega$ <sup>2)</sup>	P_4.4.41

## General Product Characteristics

**Table 5** Electrical Characteristics,  $V_S = 5.5\text{ V to }20\text{ V}$ ,  $V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $T_j = -40^\circ\text{C to }+150^\circ\text{C}$ ,  $EN = \text{HIGH}$ ,  $I_{OUTn} = 0\text{ A}$ ; Typical values refer to  $V_{DD} = 5.0\text{ V}$ ,  $V_S = 13.5\text{ V}$  and  $T_j = 25^\circ\text{C}$  unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Cross current protection time, low to high	$t_{DLH}$	100	130	160	$\mu\text{s}$	Resistive load = $100\Omega^2$	P_4.4.42
<b>Input Interface: Logic Input EN</b>							
High-input voltage	$V_{ENH}$	$0.7 \cdot V_{DD}^*$	–	$V_{DD}$	V	–	P_4.4.43
Low-input voltage	$V_{ENL}$	0	–	$0.3 \cdot V_{DD}^*$	V	–	P_4.4.44
Hysteresis of input voltage	$V_{ENHY}$	–	500	–	mV	<sup>2)</sup>	P_4.4.45
Pull down resistor	$R_{PD\_EN}$	20	40	70	k $\Omega$	$V_{EN} = 0.2 \times V_{DD}$	P_4.4.46
<b>SPI frequency</b>							
Maximum SPI frequency	$f_{SPI,max}$	–	–	5.0	MHz	<sup>2) 4)</sup>	P_4.4.47
<b>SPI INTERFACE: Delay Time from EN rising edge to first Data in</b>							
Setup time	$t_{set}$	–	–	150	$\mu\text{s}$	<sup>2)</sup> See <a href="#">Figure 12</a>	P_4.4.48
<b>SPI INTERFACE: Input Interface, Logic Inputs SDI, SCLK, CSN</b>							
H-input voltage threshold	$V_{IH}$	$0.7 \cdot V_{DD}^*$	–	$V_{DD}$	V	–	P_4.4.50
L-input voltage threshold	$V_{IL}$	0	–	$0.3 \cdot V_{DD}^*$	V	–	P_4.4.51
Hysteresis of input voltage	$V_{IHY}$	–	500	–	mV	<sup>2)</sup>	P_4.4.52
Pull up resistor at pin CSN	$R_{PU\_CSN}$	20	40	70	k $\Omega$	$V_{CSN} = 0.7 \times V_{DD}$	P_4.4.53
Pull down resistor at pin SDI, SCLK	$R_{PD\_SDI}$ , $R_{PD\_SCLK}$	20	40	70	k $\Omega$	$V_{SDI}, V_{SCLK} = 0.2 \times V_{DD}$	P_4.4.54
Input capacitance at pin CSN, SDI or SCLK	$C_I$	–	10	15	pF	$0\text{V} < V_{DD} < 5.25\text{V}^2$	P_4.4.55
<b>Input Interface, Logic Output SDO</b>							
H-output voltage level	$V_{SDOH}$	$V_{DD} - 0.4$	$V_{DD} - 0.2$	$V_{DD}$	V	$I_{SDOH} = -1.6\text{ mA}$	P_4.4.56
L-output voltage level	$V_{SDOL}$	0	0.2	0.4	V	$I_{SDOL} = 1.6\text{ mA}$	P_4.4.57
Tri-state Leakage Current	$I_{SDOLK}$	-1	–	1	$\mu\text{A}$	$V_{CSN} = V_{DD}$ ; $0\text{V} < V_{SDO} < V_{DD}$	P_4.4.58
Tri-state input capacitance	$C_{SDO}$	–	10	15	pF	<sup>2)</sup>	P_4.4.59
<b>Data Input Timing. See <a href="#">Figure 13</a> and <a href="#">Figure 15</a>.</b>							
SCLK Period	$t_{pCLK}$	200	–	–	ns	<sup>2)</sup>	P_4.4.60
SCLK High Time	$t_{SCLKH}$	$0.45 \cdot t_{pCLK}^*$	–	$0.55 \cdot t_{pCLK}^*$	ns	<sup>2)</sup>	P_4.4.61
SCLK Low Time	$t_{SCLKL}$	$0.45 \cdot t_{pCLK}^*$	–	$0.55 \cdot t_{pCLK}^*$	ns	<sup>2)</sup>	P_4.4.62

## General Product Characteristics

**Table 5** Electrical Characteristics,  $V_S = 5.5\text{ V to }20\text{ V}$ ,  $V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $T_j = -40^\circ\text{C to }+150^\circ\text{C}$ ,  $EN = \text{HIGH}$ ,  $I_{OUTn} = 0\text{ A}$ ; Typical values refer to  $V_{DD} = 5.0\text{ V}$ ,  $V_S = 13.5\text{ V}$  and  $T_j = 25^\circ\text{C}$  unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SCLK Low before CSN Low	$t_{BEF}$	125	–	–	ns	2)	P_4.4.63
CSN Setup Time	$t_{lead}$	250	–	–	ns	2)	P_4.4.64
SCLK Setup Time	$t_{lag}$	250	–	–	ns	2)	P_4.4.65
SCLK Low after CSN High	$t_{BEH}$	125	–	–	ns	2)	P_4.4.66
SDI Setup Time	$t_{SDI\_setup}$	30	–	–	ns	2)	P_4.4.67
SDI Hold Time	$t_{SDI\_hold}$	30	–	–	ns	2)	P_4.4.68
Input Signal Rise Time at pin SDI, SCLK, CSN	$t_{rIN}$	–	–	50	ns	2)	P_4.4.69
Input Signal Fall Time at pin SDI, SCLK, CSN	$t_{fIN}$	–	–	50	ns	2)	P_4.4.70
Delay time from EN falling edge to standby mode	$t_{DMODE}$	–	–	8	$\mu\text{s}$	2)	P_4.4.71
Minimum CSN High Time	$t_{CSNH}$	5	–	–	$\mu\text{s}$	2)	P_4.4.72

### Data Output Timing. See Figure 13.

SDO Rise Time	$t_{rSDO}$	–	30	80	ns	$C_{load} = 40\text{pF}^{2)}$	P_4.4.73
SDO Fall Time	$t_{fSDO}$	–	30	80	ns	$C_{load} = 40\text{pF}^{2)}$	P_4.4.74
SDO Enable Time after CSN falling edge	$t_{ENSDO}$	–	–	75	ns	Low Impedance <sup>2)</sup>	P_4.4.75
SDO Disable Time after CSN rising edge	$t_{DISSDO}$	–	–	75	ns	High Impedance <sup>2)</sup>	P_4.4.76
Duty cycle of incoming clock at SCLK	$duty_{SCLK}$	45	–	55	%	2)	P_4.4.77
SDO Valid Time for $V_{DD} = 3.3\text{ V}$	$t_{VASDO3}$	–	70	95	ns	$V_{SDO} < 0.2 \times V_{DD}$ $V_{SDO} > 0.8 \times V_{DD}$ $C_{load} = 40\text{pF}^{2)}$	P_4.4.78
SDO Valid Time for $V_{DD} = 5\text{ V}$	$t_{VASDO5}$	–	50	65	ns	$V_{SDO} < 0.2 \times V_{DD}$ $V_{SDO} > 0.8 \times V_{DD}$ $C_{load} = 40\text{pF}^{2)}$	P_4.4.79

### Thermal warning & Shutdown

Thermal warning junction temperature	$T_{jW}$	120	135	150	$^\circ\text{C}$	See Figure 9 <sup>2)</sup>	P_4.4.80
Thermal shutdown junction temperature	$T_{jSD}$	160	175	190	$^\circ\text{C}$	See Figure 9 <sup>2)</sup>	P_4.4.81
Thermal comparator hysteresis	$T_{jHYS}$	–	4	–	$^\circ\text{C}$	2)	P_4.4.82
Difference between $T_{jSD} - T_{jW}$	$T_{jSD} - T_{jW}$	–	40	–	$^\circ\text{C}$	2)	P_4.4.120

1)  $I_{S\_HSON}$  does not include the load current

2) Not subject to production test, specified by design



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## General Product Characteristics

- 3) Measured for 20% - 80% of  $V_S$ .
- 4) Not applicable in daisy chain configuration

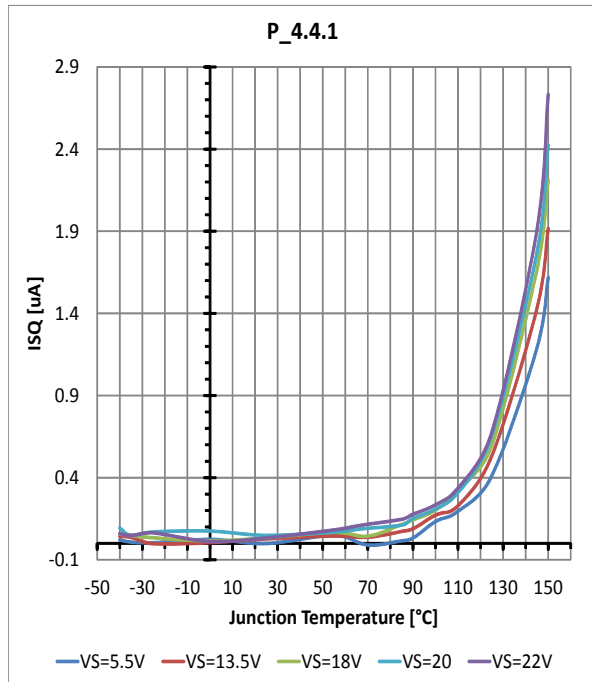
Characterization results

## 4 Characterization results

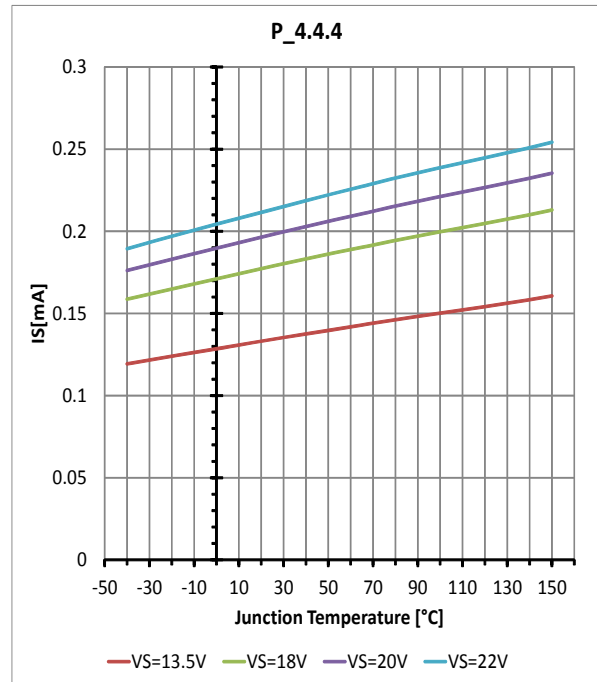
Performed on 5 devices, over operating temperature and nominal/extended supply range.

### Typical performance characteristics

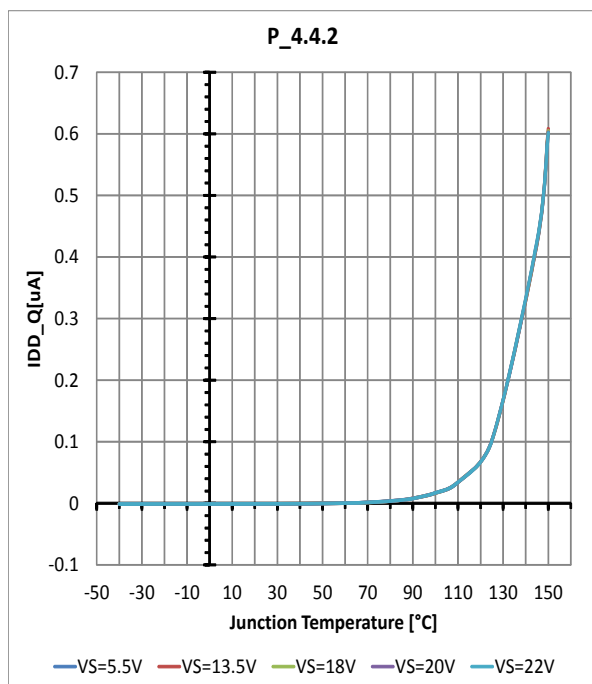
#### Supply quiescent current



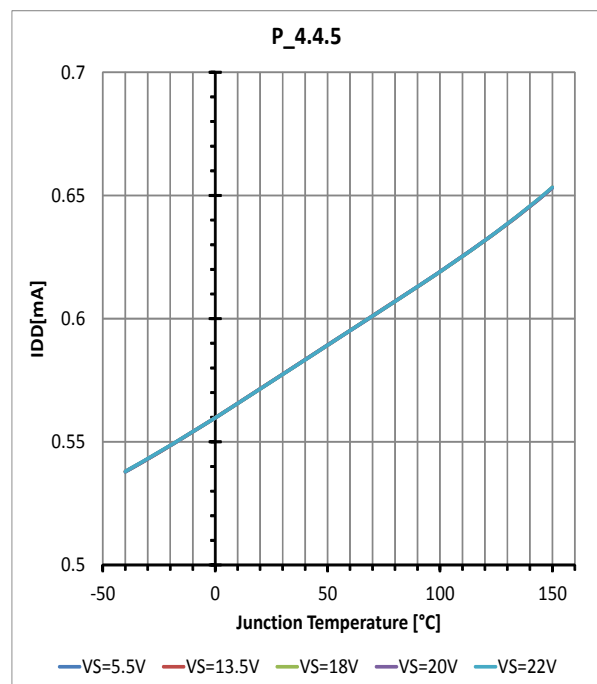
#### Supply current



#### Logic supply quiescent current

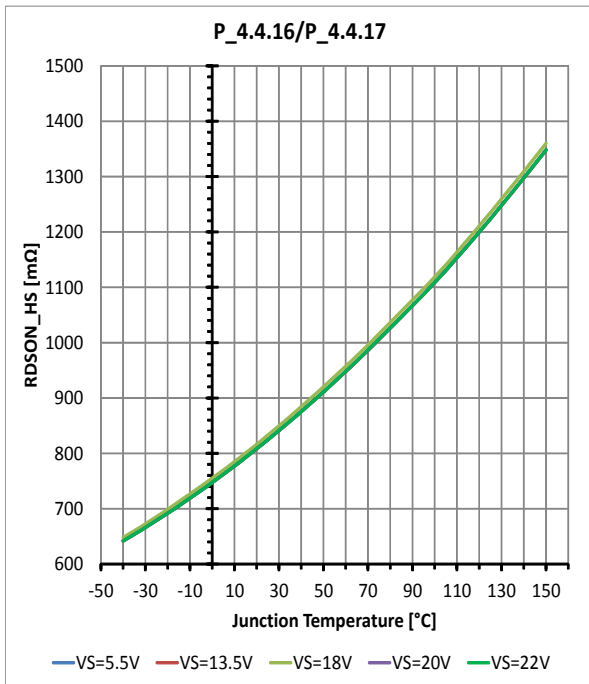


#### Logic supply current

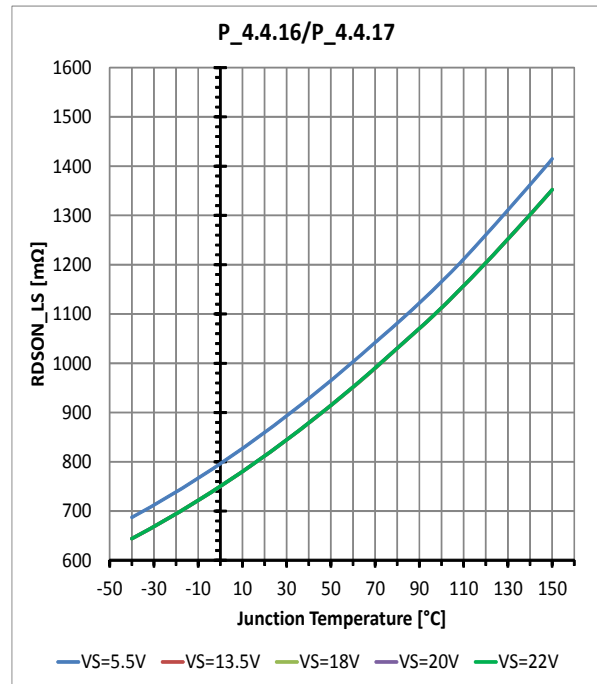


Characterization results

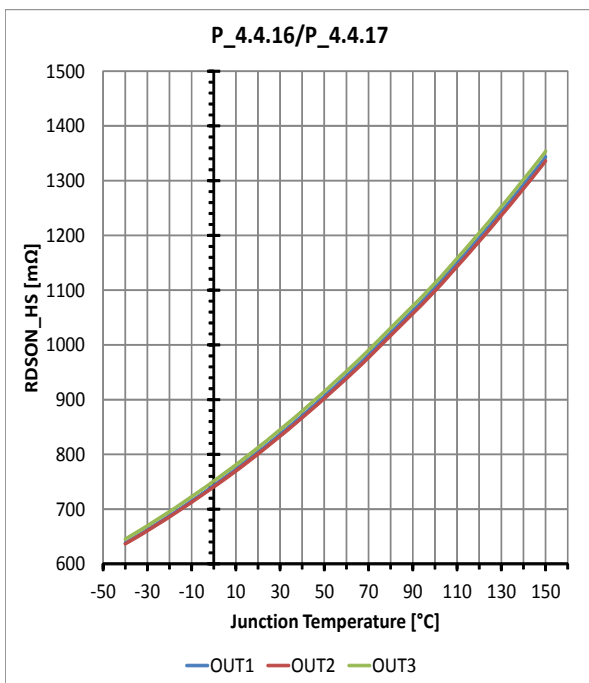
HS static Drain-source ON-resistance



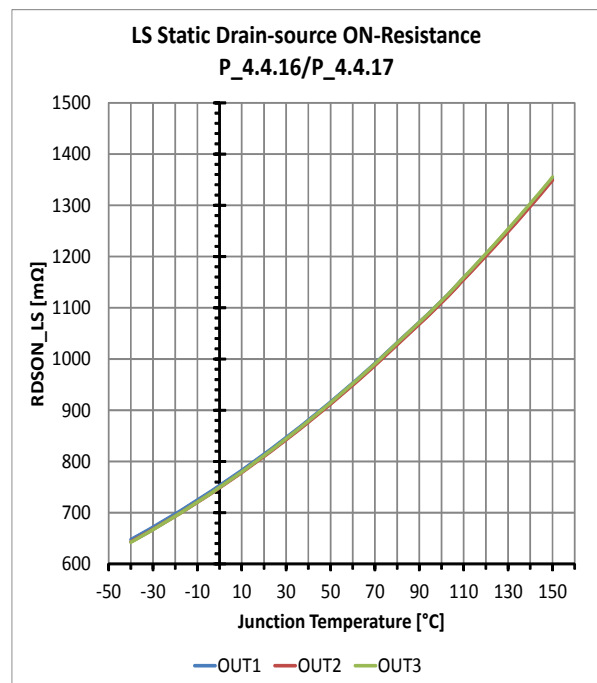
LS static Drain-source ON-resistance



HS static drain-source ON-resistance  
VS = 13.5V and VDD = 5V

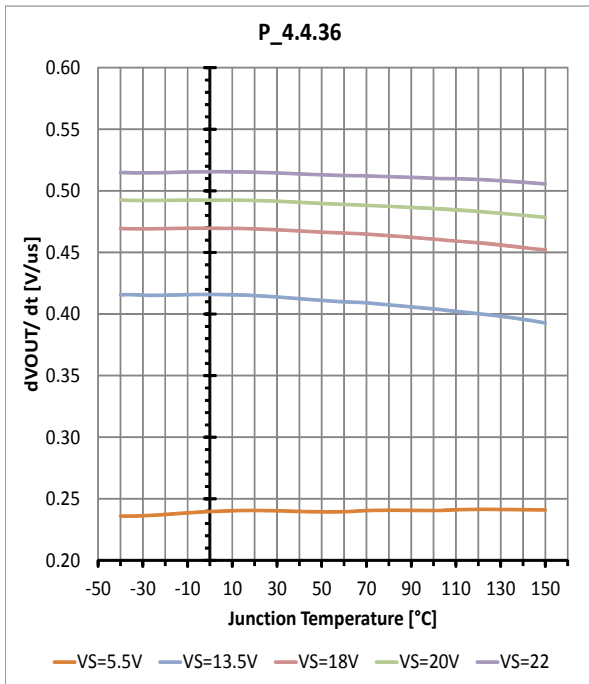


LS static drain-source ON-resistance  
VS = 13.5V and VDD = 5V

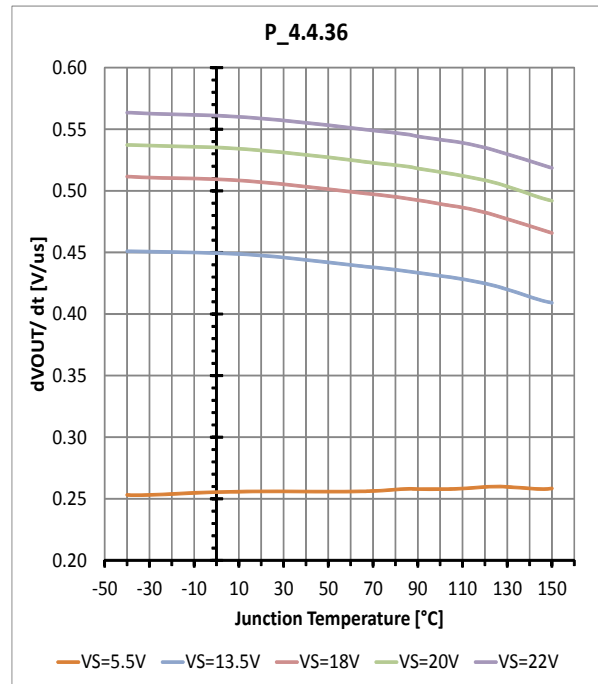


Characterization results

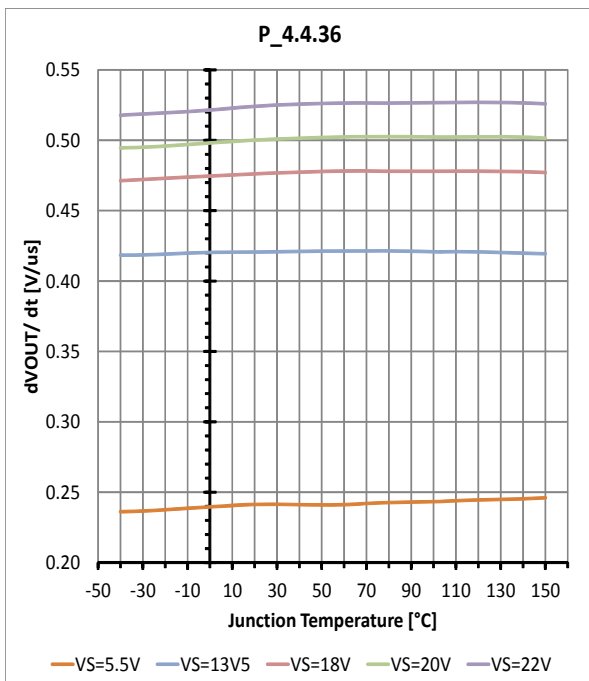
Slew rate ON of high-side outputs



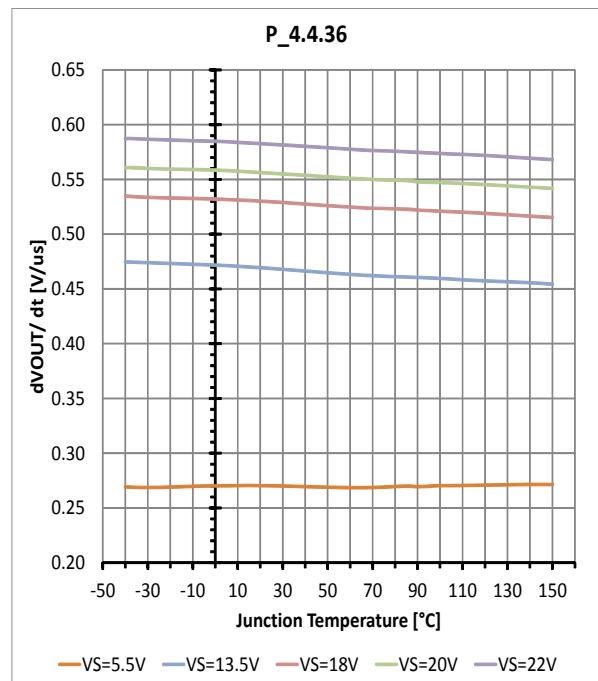
Slew rate ON of low-side outputs



Slew rate OFF of high-side outputs

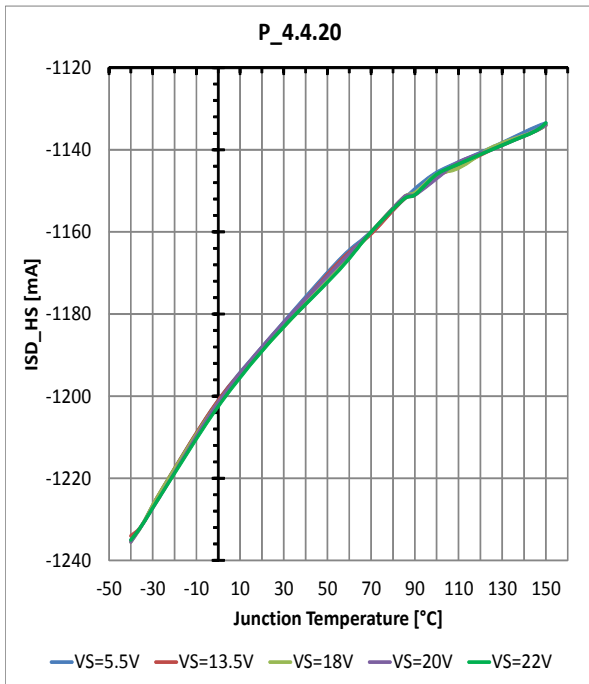


Slew rate OFF of low-side outputs

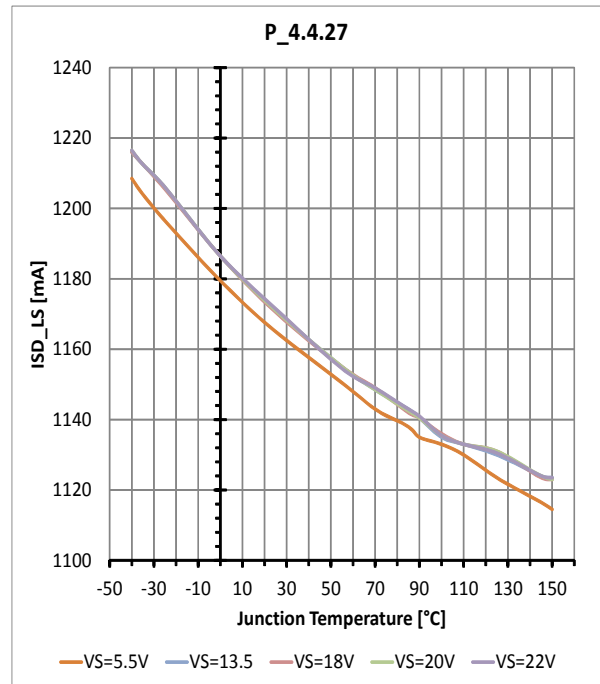


Characterization results

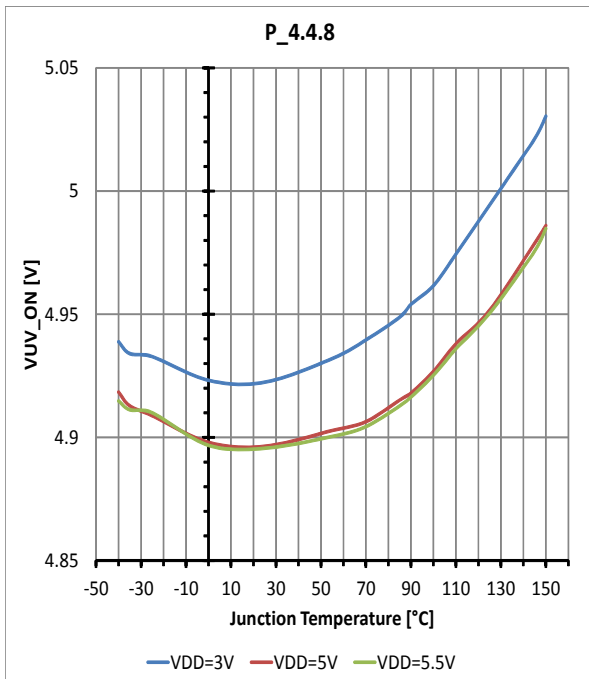
HS overcurrent shutdown threshold



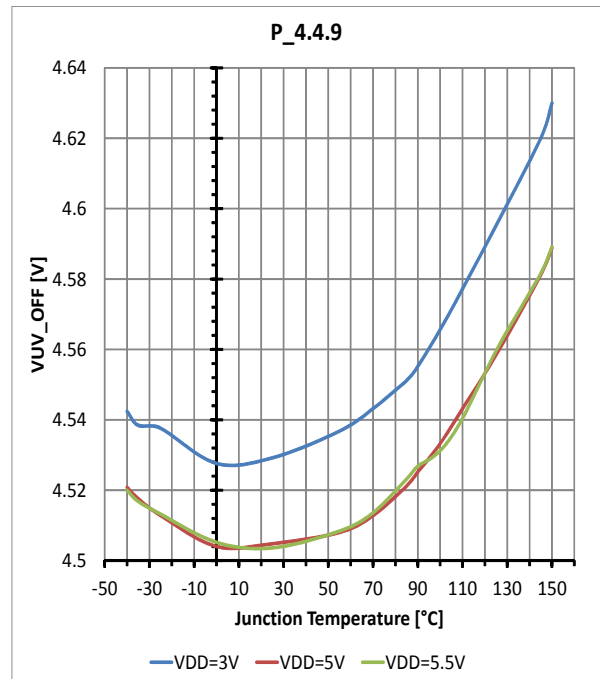
LS overcurrent shutdown threshold



Undervoltage switch ON voltage threshold

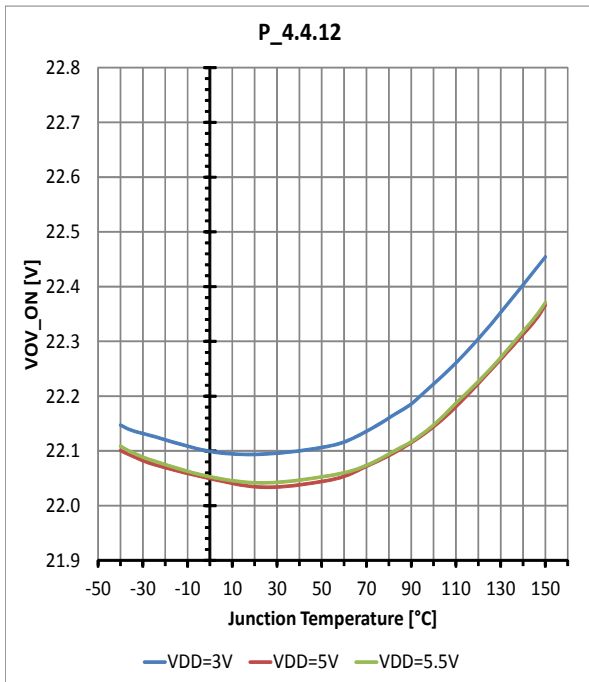


Undervoltage switch OFF voltage threshold

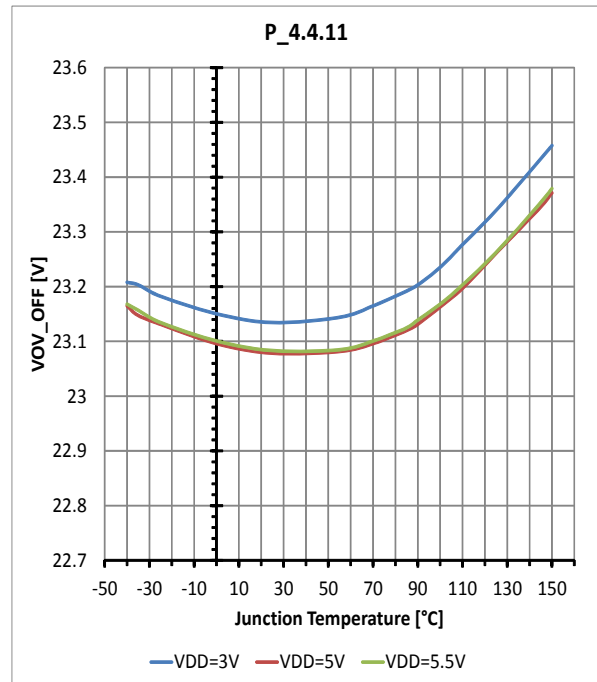


Characterization results

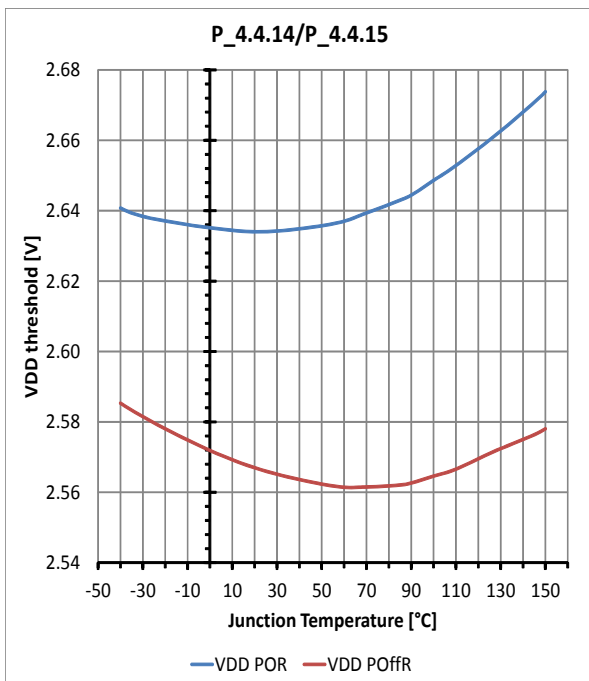
Overvoltage switch ON voltage threshold



Overvoltage switch OFF voltage threshold



VDD Power-on-reset and VDD Power-off-reset



## General Description

# 5 General Description

## 5.1 Power Supply

The TLE94103EP has two power supply inputs,  $V_S$  and  $V_{DD}$ . The half bridge outputs are supplied by  $V_S$ , which is connected to the 12V automotive supply rail.  $V_{DD}$  is used to supply the I/O buffers and internal voltage regulator of the device.

$V_S$  and  $V_{DD}$  supplies are separated so that information stored in the logic block remains intact in the event of voltage drop outs or disturbances on  $V_S$ . The system can therefore continue to operate once  $V_S$  has recovered, without having to resend commands to the device.

A rising edge on  $V_{DD}$  crossing  $V_{DD\_POR}$  triggers an internal Power-On Reset (POR) to initialize the IC at power-on. All data stored internally is deleted, and the outputs are switched off (high impedance).

An electrolytic and 100nF ceramic capacitors are recommended to be placed as close as possible to the  $V_S$  supply pin of the device for improved EMC performance in the high and low frequency band. The electrolytic capacitor must be dimensioned to prevent the  $V_S$  voltage from exceeding the absolute maximum rating. In addition, decoupling capacitors are recommended on the  $V_{DD}$  supply pin.

## 5.2 Operation modes

### 5.2.1 Normal mode

The TLE94103EP enters normal mode by setting the EN input High. In normal mode, the charge pump is active and all output transistors can be configured via SPI.

### 5.2.2 Sleep mode

The TLE94103EP enters sleep mode by setting the EN input Low. The EN input has an internal pull-down resistor.

In sleep mode, all output transistors are turned off and the SPI register banks are reset. The current consumption is reduced to  $I_{SQ} + I_{DD\_Q}$ .

## 5.3 Reset Behaviour

The following reset triggers have been implemented in the TLE94103EP:

### $V_{DD}$ Undervoltage Reset:

The SPI Interface shall not function if  $V_{DD}$  is below the undervoltage threshold,  $V_{DD\_POFFR}$ . The digital block will be deactivated, the logic contents cleared and the output stages are switched off. The digital block is initialized once  $V_{DD}$  voltage levels is above the undervoltage threshold,  $V_{DD\_POR}$ . Then the NPOR bit is reset (NPOR = 0 in **SYS\_DIAG1** and Global Status Register).

### Reset on EN pin:

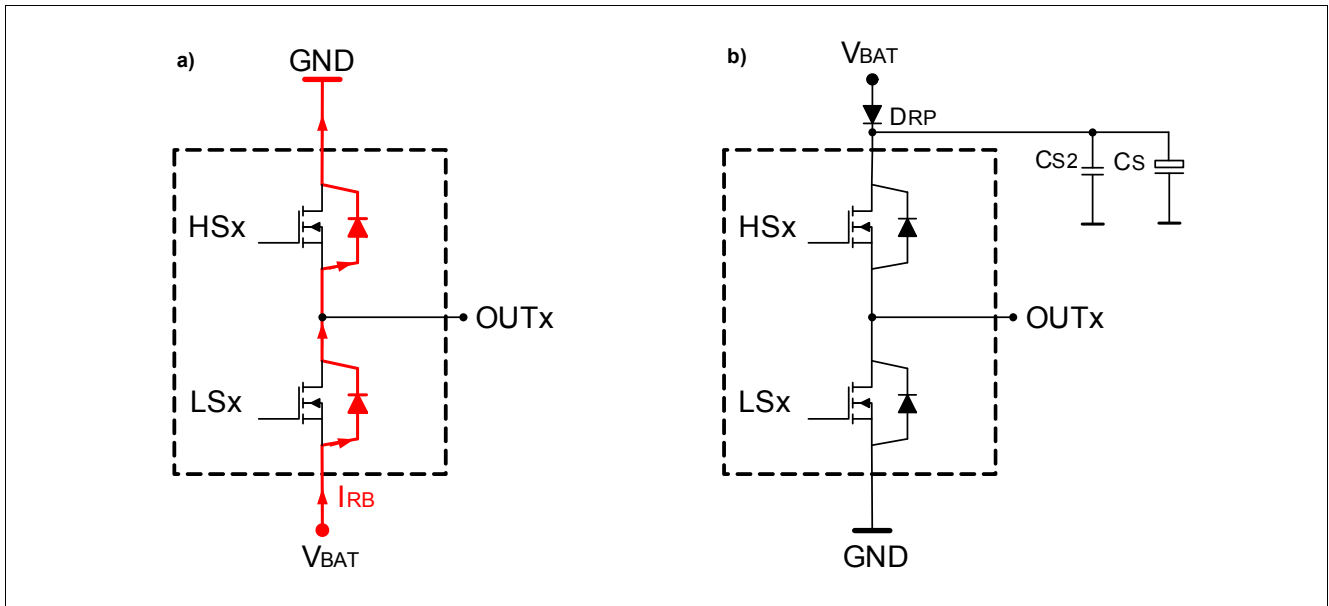
If the EN pin is pulled Low, the logic content is reset and the device enters sleep mode.

The reset event is reported by the NPOR bit (NPOR = 0) once the TLE94103EP is in normal mode (EN = High;  $V_{DD} > V_{DD\_POR}$ ).

## General Description

### 5.4 Reverse Polarity Protection

The TLE94103EP requires an external reverse polarity protection. During reverse polarity, the free-wheeling diodes across the half bridge output will begin to conduct, causing an undesired current flow ( $I_{RB}$ ) from ground potential to battery and excessive power dissipation across the diodes. As such, a reverse polarity protection diode is recommended (see [Figure 4](#)).



**Figure 4** Reverse Polarity Protection



## **6 Half-Bridge Outputs**

### **6.1 Functional Description**

The half-bridge outputs of the TLE94103EP are intended to drive motor loads.

If the outputs are driven continuously via SPI, for example HS1 and LS2 used to drive a motor, then the following suggested SPI commands shall be sent:

- Activate HS1: Bit HB1\_HS\_EN in HB\_ACT\_1\_CTRL register
- Activate LS2: Bit HB2\_LS\_EN in HB\_ACT\_1\_CTRL register

## Half-Bridge Outputs

### 6.2 Protection & Diagnosis

The TLE94103EP is equipped with an SPI interface to control and diagnose the state of the half-bridge drivers. This device has embedded protective functions which are designed to prevent IC destruction under fault conditions described in the following sections. Fault conditions are treated as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

The following table provides a summary of fault conditions, protection mechanisms and recovery states embedded in the TLE94103EP device.

**Table 6 Summary of diagnosis and monitoring of outputs**

Fault condition	Error Flag (EF) behaviour	Error bit: Status Register	Output Protection mechanism	Output error state	Output and error flag (EF) recovery
Overcurrent	Latch	1. Load Error bit, LE (bit 6) in SYS_DIAG 1: Global Status 1 Register 2. Localized error for each HS and LS channel of half-bridge, HBn_HS_OC and HBn_LS_OC bits in SYS_DIAG_2 status register.	Error output shutdown and latched	High-Z	Half-bridge control bits remain set despite error, however the output stage is shutdown. Clear EF to reactivate output stage.
Open load	Latch	1. Load Error bit, LE (bit 6) in SYS_DIAG 1: Global Status 1 Register 2. Localized error for each HS and LS channel of half-bridge, HBn_HS_OL and HBn_LS_OL bits in SYS_DIAG3 status register.	None	No state change	An open load detection does not change the state of the output. EF to be cleared.
Temperature pre-warning	Latch	Global error bit 1, TPW in SYS_DIAG_1: Global Status 1 register	None	No state change	Not applicable
Temperature shutdown	Latch	Global error bit 2, TSD in SYS_DIAG_1: Global Status 1 register	All outputs shutdown and latched.	High-Z	Half-bridge control bits remain set despite error, however the output stage is shutdown. Clear EF to reactivate output stage.

## Half-Bridge Outputs

**Table 6** Summary of diagnosis and monitoring of outputs (cont'd)

Fault condition	Error Flag (EF) behaviour	Error bit: Status Register	Output Protection mechanism	Output error state	Output and error flag (EF) recovery
Powersupply failure due to undervoltage	Latch	Global error bit 5, VS_UV in SYS_DIAG_1: Global Status 1 register	All outputs shutdown and automatically recovers.	High-Z	Half-bridge control bits remain set despite error, however the output stage is shutdown. They will automatically be reactivated once the power supply recovers. EF to be cleared.
Powersupply failure due to overvoltage	Latch	Global error bit 4, VS_OV in SYS_DIAG_1: Global Status 1 register	All outputs shutdown and automatically recover.	High-Z	Half-bridge control bits remain set despite error, however the output stage is shutdown. They will automatically be reactivated once the power supply recovers. EF to be cleared.

Half-Bridge Outputs

6.2.1 Short Circuit of Output to Supply or Ground

The high-side switches are protected against short to ground whereas the low-side switches are protected against short to supply.

The high-side and low-side power switches will enter into an over-current condition if the current within the switch exceeds the overcurrent shutdown detection threshold,  $I_{SD}$ . Upon detection of the  $I_{SD}$  threshold, an overcurrent shutdown filter,  $t_{dSD}$  is begun. As the current rises beyond the threshold  $I_{SD}$ , it will be limited by the current limit threshold,  $I_{LIM}$ . Upon expiry of the overcurrent shutdown filter time, the affected power switch is latched off and the corresponding error bit, HBn\_HS\_OC or HBn\_LS\_OC is set and latched. See **Figure 5** and **Figure 6** for more detail. A global load error bit, LE, contained in the global status register, SYS\_DIAG\_1, is also set for ease of error scanning by the application software. The power switch remains deactivated as long as the error bit is set.

To resume normal functionality of the power switch (in the event the overcurrent condition disappears or to verify if the failure still exists) the microcontroller shall clear the error bit in the respective status register to reactivate the desired power switch.

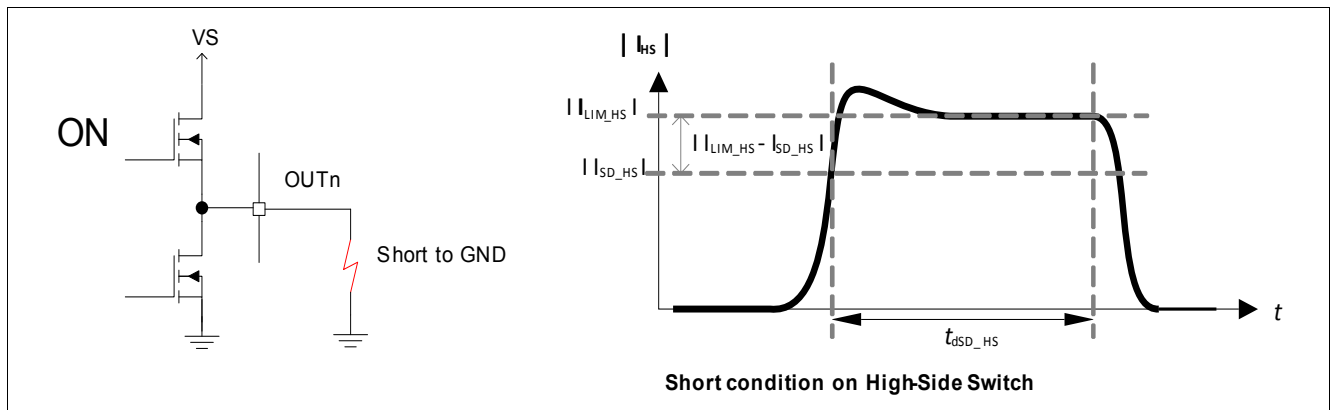


Figure 5 High-Side Switch - Short Circuit and Overcurrent Protection

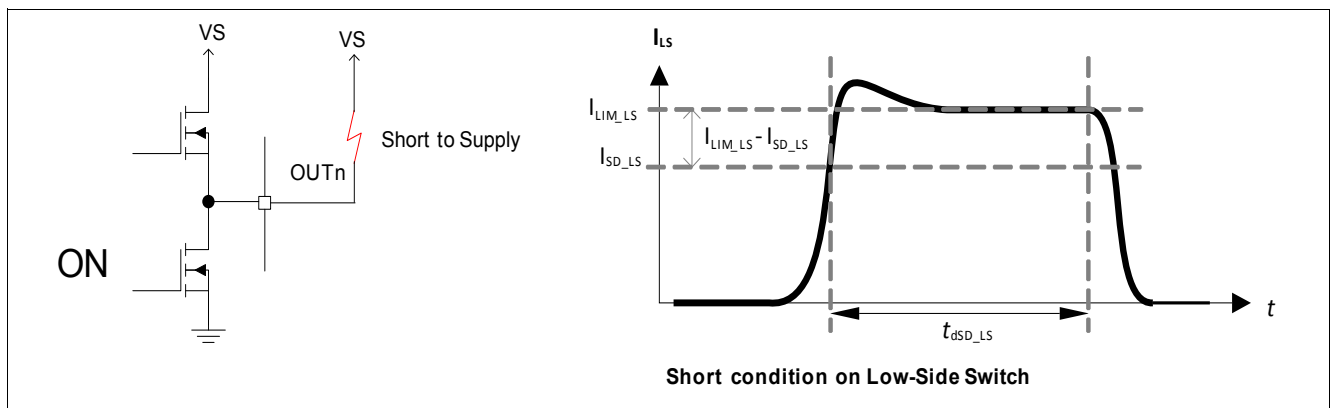


Figure 6 Low-Side Switch - Short Circuit and Overcurrent Protection

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**Half-Bridge Outputs**
**Table 7 Control and Status register bit state in the event of an overcurrent condition for an activated power switch**

REGISTER TYPE	REGISTER NAME	Bit	BEFORE OVERCURRENT	DURING OVERCURRENT	AFTER OVERCURRENT
			Bit State	Bit State	Bit State
Control	HB_ACT_CTRL_n	HBn_HS_EN HBn_LS_EN	1	1	1 (corresponding half-bridge deactivated)
Status	SYS_DIAG_1: Global Status 1	LE	0	0	1
Status	SYS_DIAG_x where x=2	HBn_HS_OC HBn_LS_OC	0	0	1

Half-Bridge Outputs

6.2.2 Cross-Current

In bridge configurations the high-side and low-side power transistors are ensured never to be simultaneously “ON” to avoid cross currents. This is achieved by integrating delays in the driver stage of the power outputs to create a dead-time between switching off of one power transistor and switching on of the adjacent power transistor within the half-bridge. The dead times,  $t_{DHL}$  and  $t_{DLH}$ , as shown in **Figure 7** case 3 and **Figure 8** case 3, have been specified to ensure that the switching slopes do not overlap with each other. This prevents a cross conduction event.

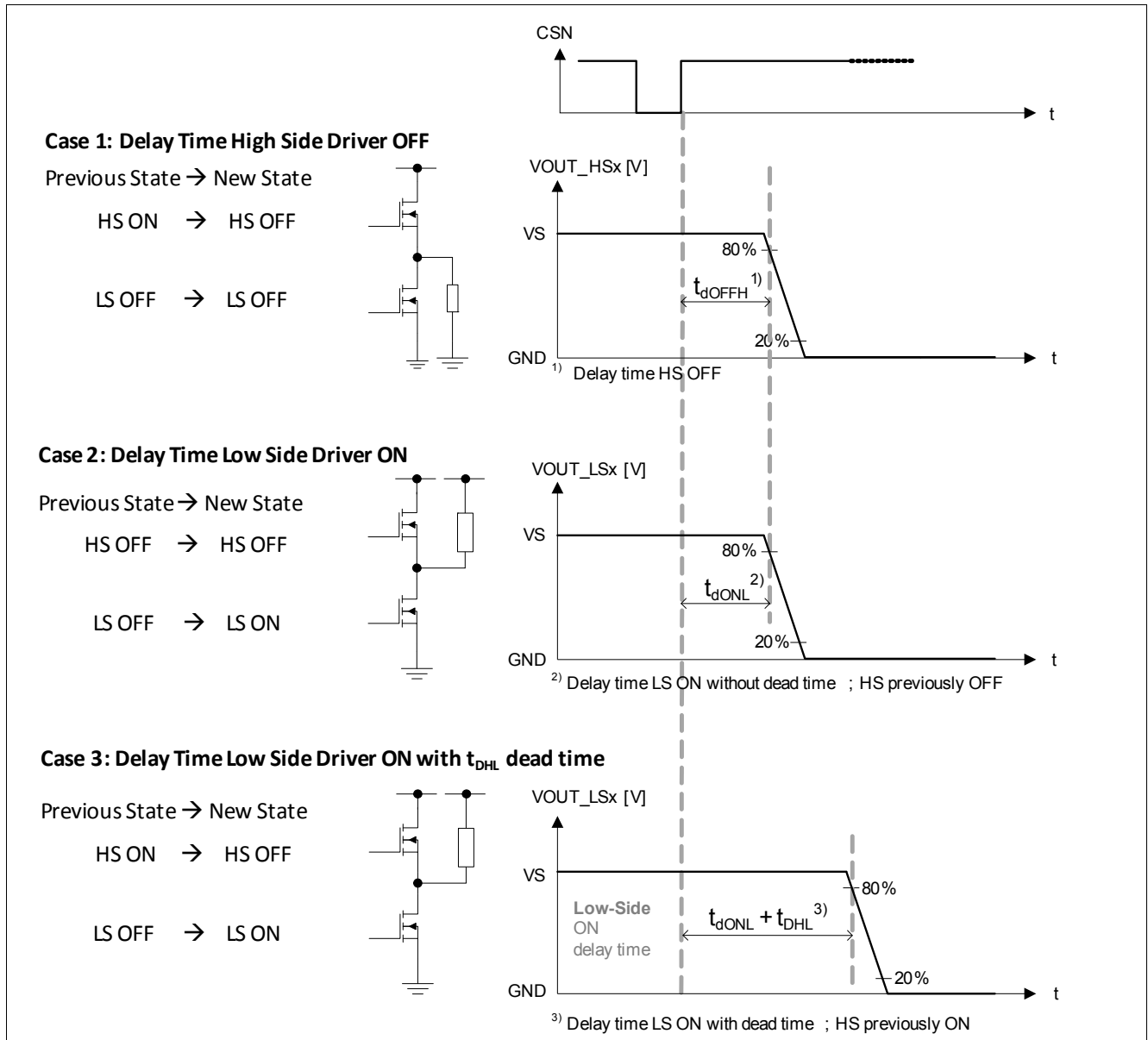


Figure 7 Half bridge outputs switching times - high-side to low-side transition

Half-Bridge Outputs

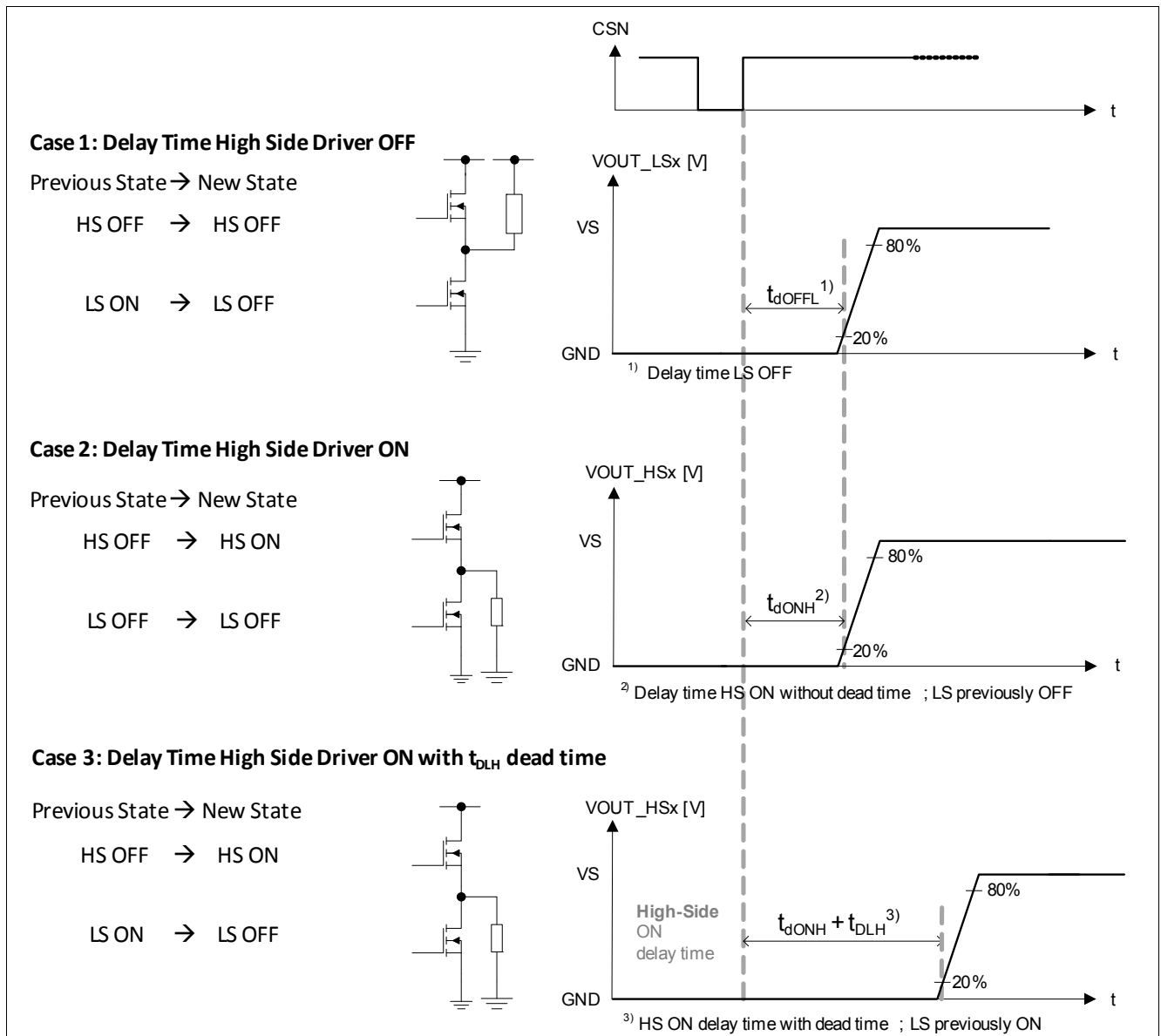


Figure 8 Half bridge outputs switching times- low-side to high-side transition

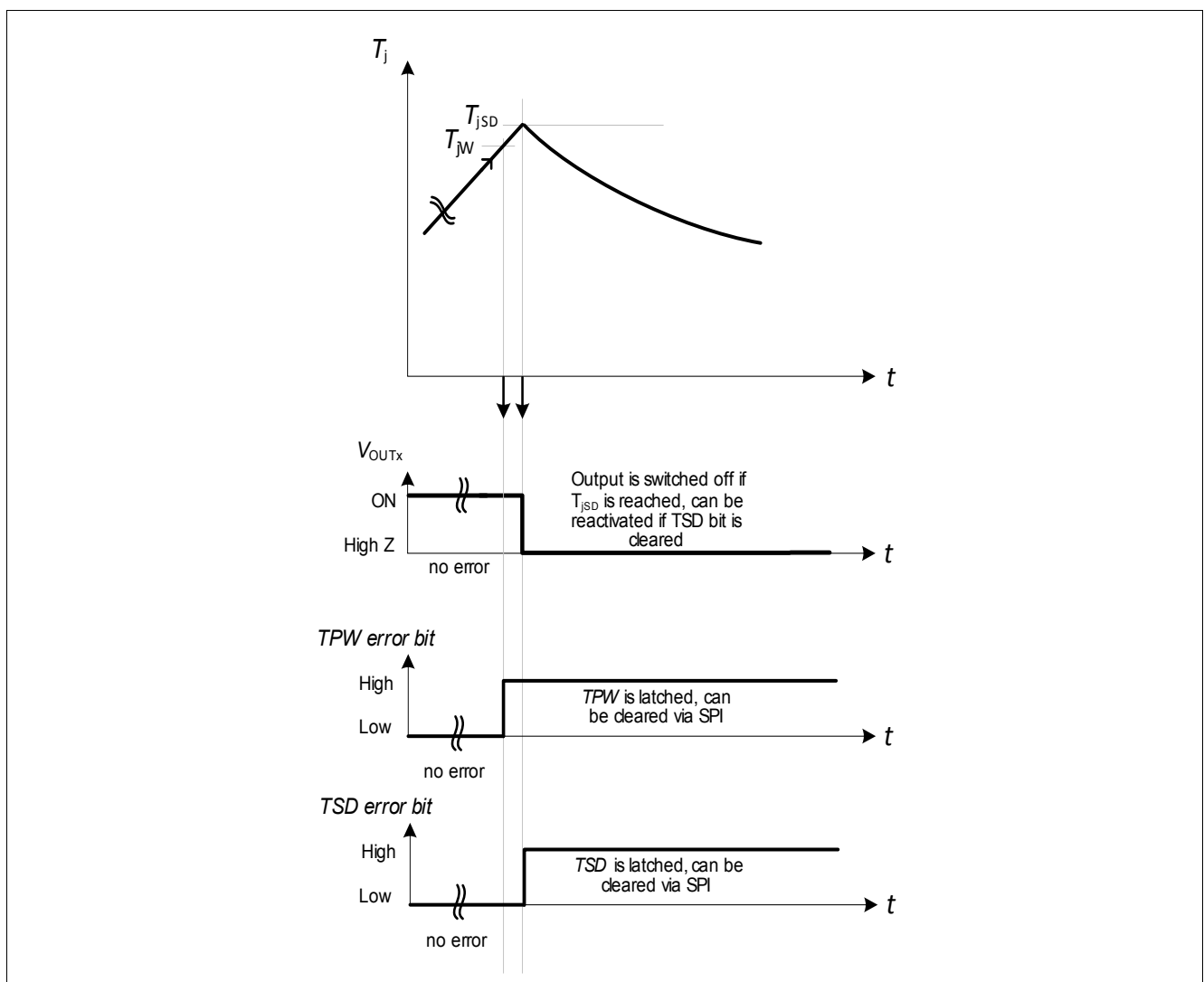
## Half-Bridge Outputs

### 6.2.3 Temperature Monitoring

Temperature sensors are integrated in the power stages. The temperature monitoring circuit compares the measured temperature to the warning and shutdown thresholds. If one or more temperature sensors reach the warning temperature, the temperature pre-warning bit, TPW is set. This bit is latched and can only be cleared via SPI. The outputs stages however remain activated.

If one or more temperature sensors reach the shut-down temperature threshold, **all outputs are latched off**. The TSD bit in SYS\_DIAG\_1: Global Status 1 is set. All outputs remain deactivated until the TSD bit is cleared. See [Figure 9](#).

To resume normal functionality of the power switch (in the event the overtemperature condition disappears, or to verify if the failure still exists) the microcontroller shall clear the TSD error bit in the status register to reactivate the respective power switch.



**Figure 9** Overtemperature Behavior



## Half-Bridge Outputs

**Table 8 Control and Status register bit state in the event of an overtemperature condition for an activated power switch**

REGISTER TYPE	REGISTER NAME	Bit	$T_j < T_{jW}$	$T_j > T_{jW}$	$T_j > T_{jSD}$	$T_j < T_{jSD} - T_{jHYS}$
			Bit State	Bit State	Bit State	Bit State
Control	HB_ACT_CTRL_n	HBn_HS_EN HBn_LS_EN	1	1	1 (all outputs are latched off)	'1' (outputs are latched off unless error is cleared)
Status	SYS_DIAG_1: Global status 1	TPW	0	1 (latched)	1 (latched)	'0' if error is cleared and $T_j < T_{jW}$ , else '1'
Status	SYS_DIAG_1: Global status 1	TSD	0	0	1 (latched)	'0' if error is cleared, else '1'

### 6.2.4 Overvoltage and undervoltage shutdown

The power supply rails  $V_S$  and  $V_{DD}$  are monitored for supply fluctuations. The  $V_S$  supply is monitored for under- and over-voltage conditions whereas the  $V_{DD}$  supply is monitored for under-voltage conditions.

#### 6.2.4.1 $V_S$ Undervoltage

In the event the supply voltage  $V_S$  drops below the switch off voltage  $V_{UV\ OFF}$ , all output stages are switched off, however, the logic information remains intact and uncorrupted. The  $V_S$  under-voltage error bit, VS\_UV, located in SYS\_DIAG\_1: Global Status 1 status register, will be set and latched. If  $V_S$  rises again and reaches the switch on voltage  $V_{UV\ ON}$  threshold, the power stages will automatically be activated. The VS\_UV error bit should be cleared to verify if the supply disruption is still present. See [Figure 10](#).

#### 6.2.4.2 $V_S$ Overvoltage

In the event the supply voltage  $V_S$  rises above the switch off voltage  $V_{OV\ OFF}$ , all output stages are switched off. The  $V_S$  over-voltage error bit, VS\_OV, located in SYS\_DIAG\_1: Global Status 1 status register, will be set and latched. If  $V_S$  falls again and reaches the switch on voltage  $V_{OV\ ON}$  threshold, the power stages will automatically be activated. The VS\_OV error bit should be cleared to verify if the overvoltage condition is still present. See [Figure 10](#).

#### 6.2.4.3 $V_{DD}$ Undervoltage

In the event the VDD logic supply decreases below the undervoltage threshold,  $V_{DD\ PoffR}$ , the SPI interface shall no longer be functional and the TLE94103EP will enter reset.

The digital block will be initialized and the output stages are switched off to High impedance. The undervoltage reset is released once  $V_{DD}$  voltage levels are above the undervoltage threshold,  $V_{DD\ POR}$ .

The reset event is reported in SYS\_DIAG1 by the NPOR bit (NPOR = 0) once the TLE94103EP is in normal mode (EN = High ;  $V_{DD} > V_{DD\ POR}$ ).

Half-Bridge Outputs

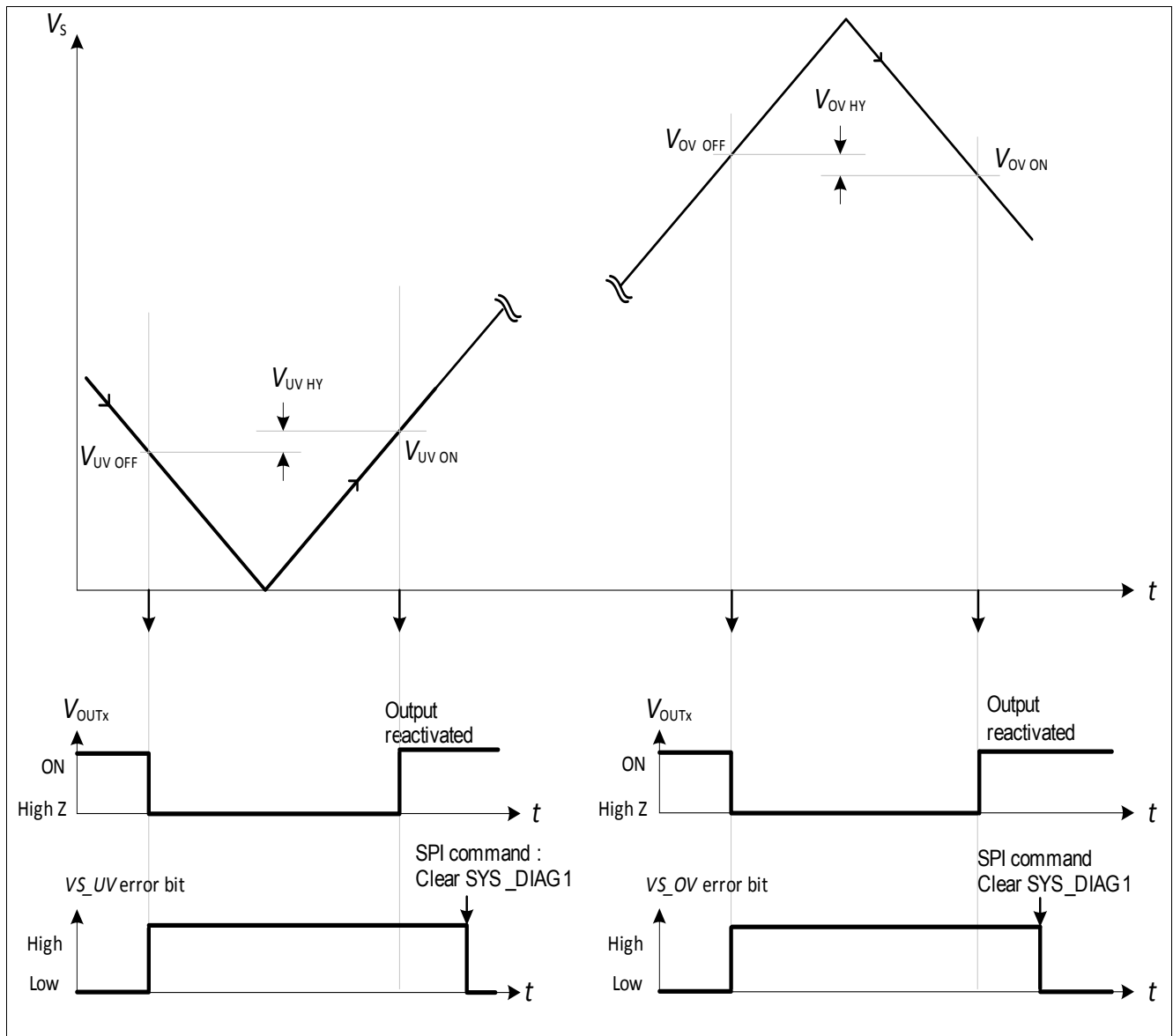


Figure 10 Output behavior during under- and overvoltage  $V_s$  condition

6.2.5 Open Load

Both high-side and low-side switches of the half-bridge power outputs are capable of detecting an open load in their activated state. If a load current lower than the open load detection threshold,  $I_{OLD}$  for at least  $t_{dOLD}$  is detected at the activated switch, the corresponding error bit, HBn\_HS\_OL or HBn\_LS\_OL is set and latched. A global load error bit, LE, in the global status register, SYS\_DIAG\_1: Global Status 1, is also set for ease of error scanning by the application software. The half-bridge output however, remains activated.

The microcontroller must clear the error bit in the respective status register to determine if the open load is still present or disappeared.

Serial Peripheral Interface (SPI)

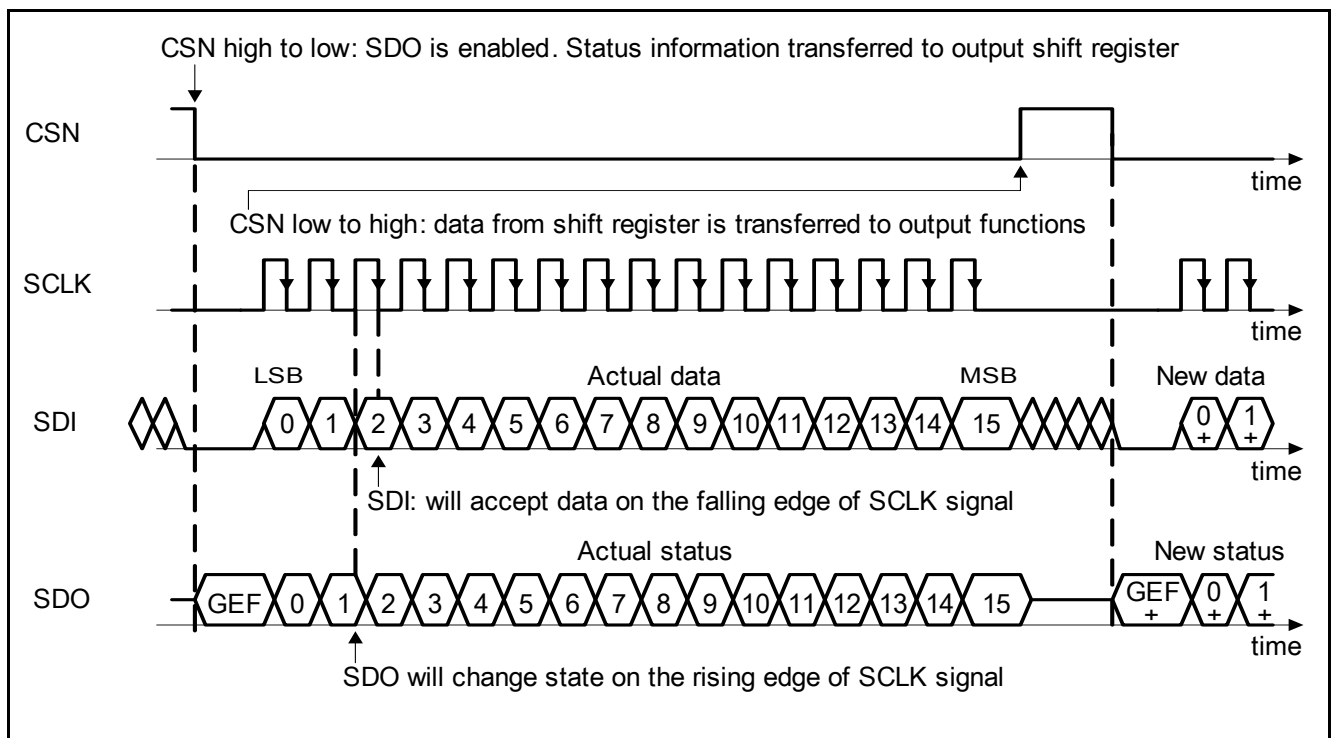
## 7 Serial Peripheral Interface (SPI)

The TLE94103EP has a 16-bit SPI interface for output control and diagnostics. This section describes the SPI protocol, the control and status registers.

### 7.1 SPI Description

The 16-bit wide Control Input Word is read via the data input SDI, which is synchronized with the clock input SCLK provided by the microcontroller. SCLK must be Low during CSN falling edge (Clock Polarity = 0). The SPI incorporates an in-frame response: the content of the addressed register is shifted out at SDO within the same SPI frame (see [Figure 17](#) and [Figure 19](#)). The transmission cycle begins when the chip is selected by the input CSN (Chip Select Not), Low active. After the CSN input returns from Low to High, the word that has been read is interpreted according to the content. The SDO output switches to tri-state status (High impedance) at this point, thereby releasing the SDO bus for other use. The state of SDI is shifted into the input register with every falling edge on SCLK. The state of SDO is shifted out of the output register at every rising edge on SCLK (Clock Phase = 1). The SPI protocol of the TLE94103EP is compatible with independent slave configuration and with daisy chain. Daisy chaining is applicable to SPI devices with the same protocol.

Writing, clearing and reading is done byte wise. The SPI configuration and status bits are not cleared automatically by the device and therefore must be cleared by the microcontroller, e.g. if the TSD bit was set due to over temperature (refer to the respective register description for detailed information).



**Figure 11 SPI Data Transfer Timing (note the reversed order of LSB and MSB as shown in this figure compared to the register description)**

SPI messages are only recognized if a minimum set time,  $t_{SET}$ , is observed upon rising edge of the EN pin ([Figure 12](#)).

Serial Peripheral Interface (SPI)

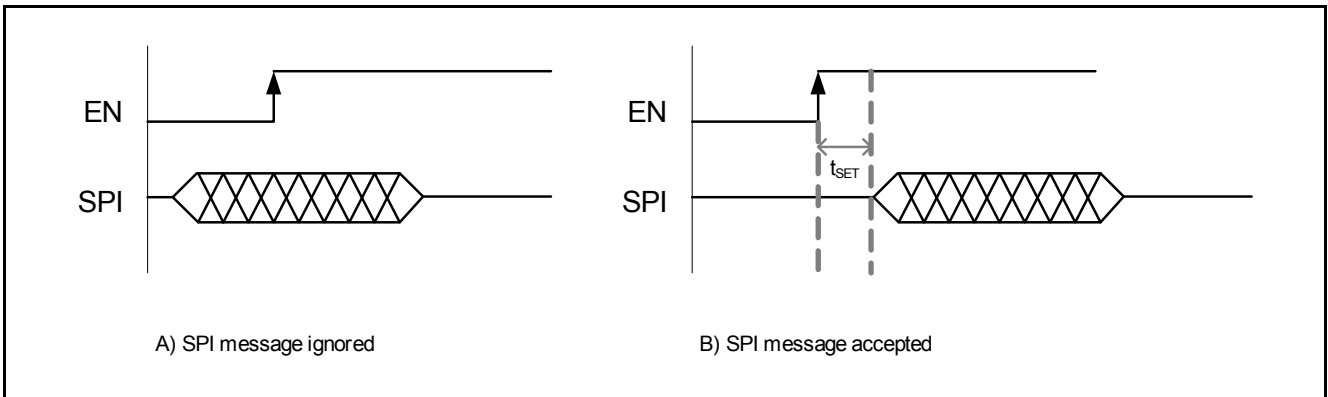


Figure 12 Setup time from EN rising edge to first SPI communication

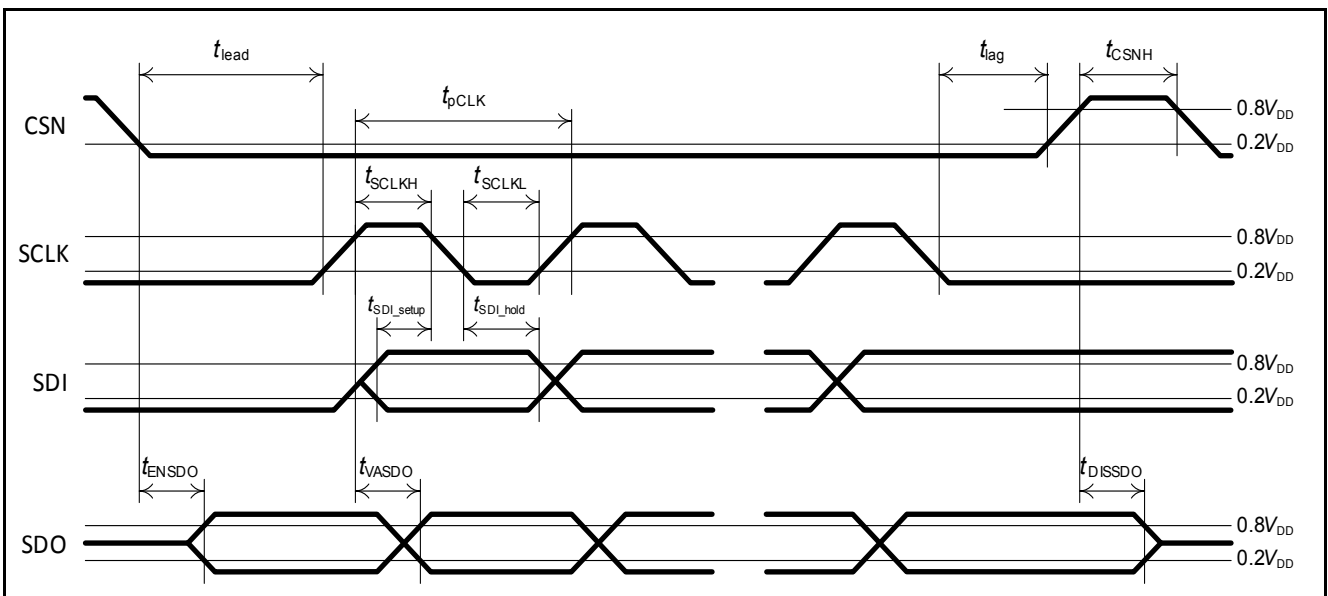


Figure 13 SPI Data Timing

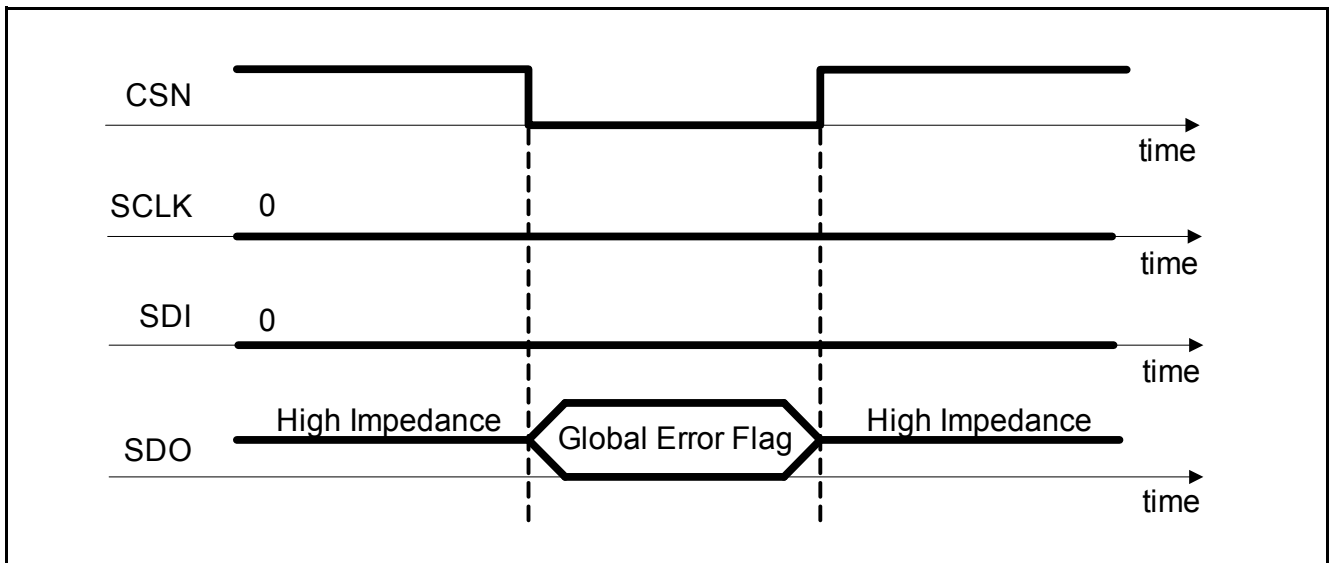
7.1.1 Global Error Flag

A logic OR combination between Global Error Flag (GEF) and the signal present on SDI is reported on SDO between a CSN falling edge and the first SCLK rising edge (Figure 11). GEF is set if a fault condition is detected or if the device comes from a Power On Reset (POR).

Note: The SDI pin of all devices in daisy chain or non daisy chain mode must be Low at the beginning of the SPI frame (between the CSN falling edge and the first SCLK rising edge).

It is possible to check if the TLE94103EP has detected a fault by reading the GEF without SPI clock pulse (Figure 14).

## Serial Peripheral Interface (SPI)



**Figure 14** SDO behaviour with 0-clock cycle

### 7.1.2 Global Status Register

The SDO shifts out during the first eight SCLK cycles the Global Status Register. This register provides an overview of the device status. All failures conditions are reported in this byte:

- SPI protocol error (SPI\_ERR)
- Load Error (LE bit): logical OR between Open Load (OL) and Overcurrent (OC) failures
- VS Undervoltage (VS\_UV bit)
- VS Overvoltage (VS\_OV bit)
- Negated Power ON Reset (NPOR bit)
- Temperature Shutdown (TSD bit)
- Temperature Pre-Warning (TPW bit)

See [Chapter 7.7.1](#) for details.

*Note:* The Global Error Flag is a logic OR combination of every bit of the Global Status Register with the exception of NPOR:  $GEF = (SPI\_ERR) \text{ OR } (LE) \text{ OR } (VS\_UV) \text{ OR } (VS\_OV) \text{ OR } (NOT(NPOR)) \text{ OR } (TSD) \text{ OR } (TPW)$ . It is possible to mask open load failures from the Global Error Flag by setting the OL\_BLANK bit (refer to [Chapter 7.6](#)).

The following table shows how failures are reported in the Global Status Register and by the Global Error Flag.

**Table 9** Failure reported in the Global Status Register and Global Error Flag

Type of Error	Failure reported in the Global Status Register	Global Error Flag
SPI protocol error	SPI_ERR = 1	1
Open load or Overcurrent	LE = 1	1 <sup>1)</sup>
VS Undervoltage	VS_UV = 1	1
VS Overvoltage	VS_OV = 1	1
Power ON Reset	<b>NPOR = 0</b>	1
Thermal Shutdown	TSD = 1	1

## Serial Peripheral Interface (SPI)

**Table 9 Failure reported in the Global Status Register and Global Error Flag**

Type of Error	Failure reported in the Global Status Register	Global Error Flag
Thermal Warning	TPW = 1	1
No Error and no Power ON Reset	SPI_ERR = 0 LE = 0 VS_UV = 0 VS_OV = 0 <b>NPOR = 1</b> TSD = 0 TPW = 0	0

1) Open load errors are reported in the Global Error Flag only if OL\_BLANK bit is set to 0.

*Note:* The default value (after Power ON Reset) of NPOR is 0, therefore the default value of GEF is 1.

### 7.1.3 SPI protocol error detection

The SPI incorporates an error flag in the Global Status Register (SPI\_ERR, Bit7) to supervise and preserve the data integrity. If an SPI protocol error is detected during a given frame, the SPI\_ERR bit is set in the next SPI communication.

The SPI\_ERR bit is set in the following error conditions:

- the number of SCLK clock pulses received when CSN is Low is not 0, or is not a multiple of 8 and at least 16
- the microcontroller sends an SPI command to an unused address. In particular, SDI stuck to High is reported in the SPI\_ERR bit
- the LSB of an address byte is not set to 1. In particular, SDI stuck to Low is reported in the SPI\_ERR bit
- the Last Address Bit Token (LABT, bit 1 of the address byte, see [Chapter 7.2](#)) in independent slave configuration is not set to 1
- the LABT bit of the last address byte in daisy chain configuration is not set to 1 (see [Chapter 7.3](#))
- a clock polarity error is detected (see [Figure 15](#) Case 2 and Case 3): the incoming clock signal was High during CSN rising or falling edges.

For a correct SPI communication:

- SCLK must be Low for a minimum  $t_{BEF}$  before CSN falling edge and  $t_{lead}$  after CSN falling edge
- SCLK must be Low for a minimum  $t_{lag}$  before CSN rising edge and  $t_{BEH}$  after CSN rising edge

Serial Peripheral Interface (SPI)

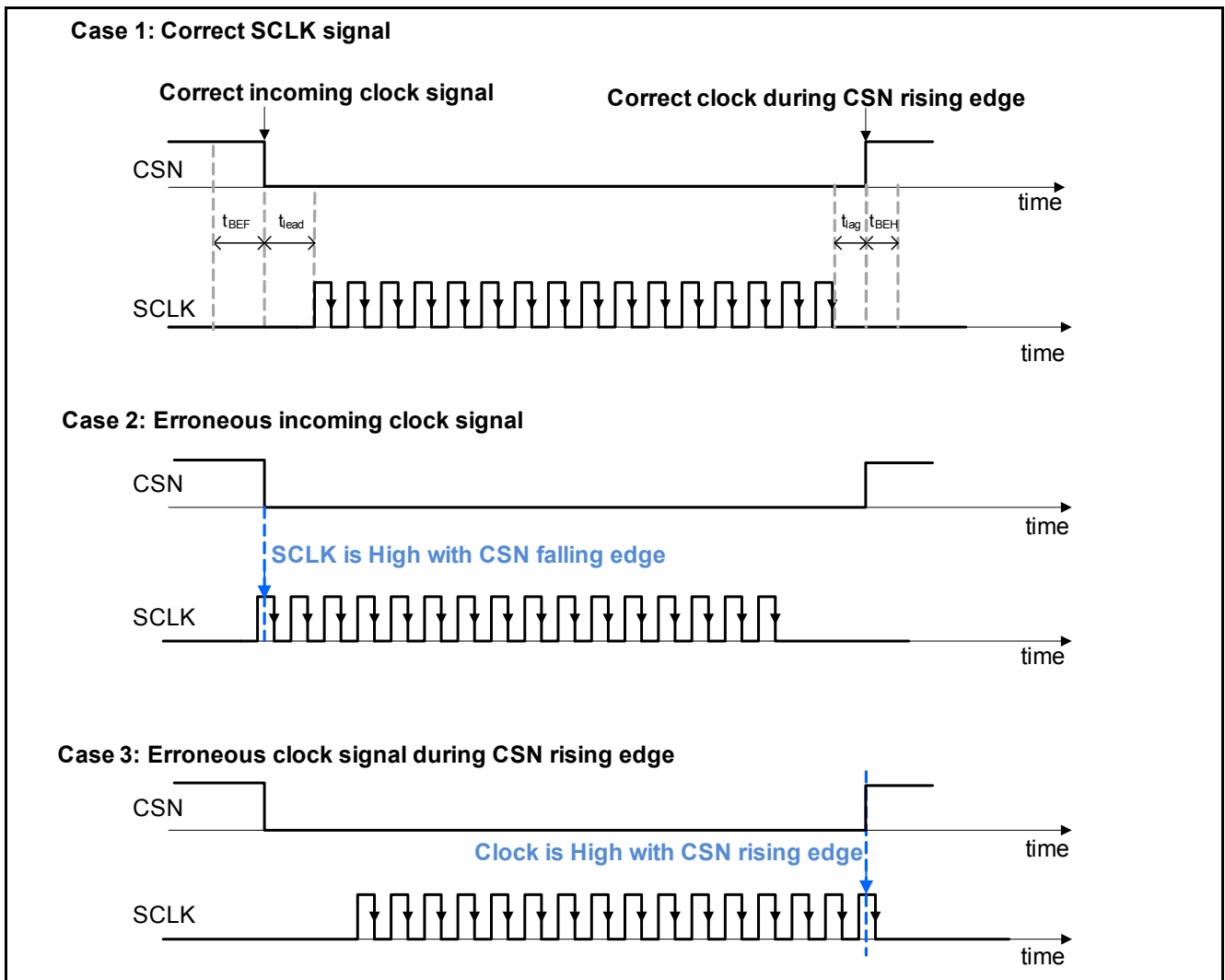
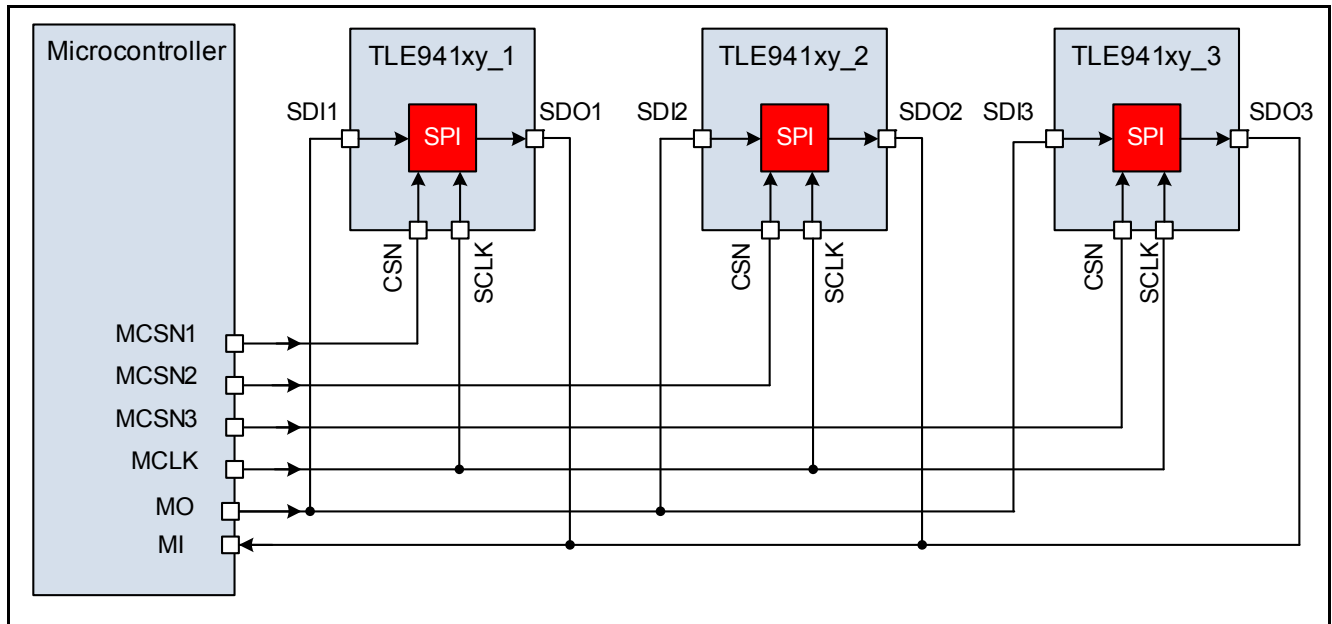


Figure 15 Clock Polarity Error

## Serial Peripheral Interface (SPI)

### 7.2 SPI with independent slave configuration

In an independent slave configuration, the microcontroller controls the CSN of each slave individually ([Figure 16](#)).



**Figure 16** SPI with independent slave configuration

Each SPI communication starts with one address byte followed by one data byte ([Figure 17](#)). The LSB of the data byte must be set to '1'. The address bytes specifies:

- the type of operation: READ ONLY (OP bit = 0) or READ/ WRITE (OP bit = 1) of the configuration bits, and READ ONLY (OP bit = 0) or READ & CLEAR (OP bit = 1) of the status bits.
- The target register address (A[6:2])

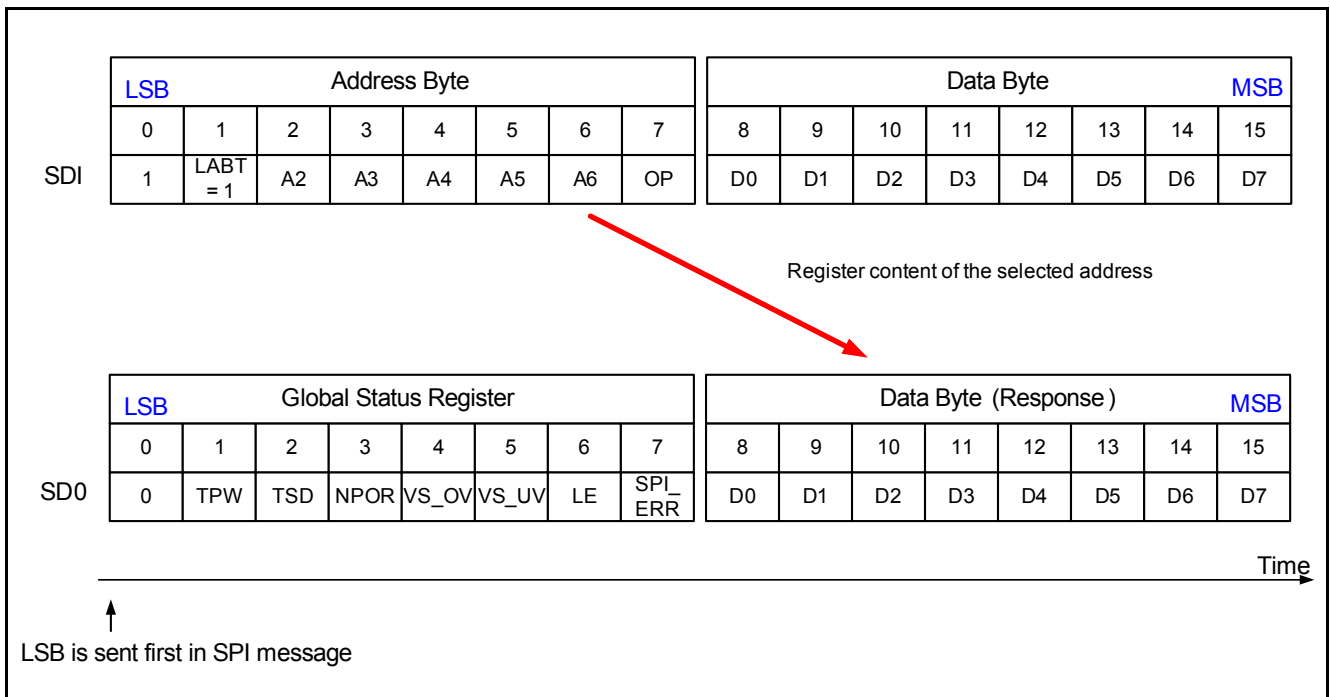
The Last Address Byte Token bit (LABT, Bit1 of the address byte) must be set to 1, as no daisy chain configuration is used.

While the microcontroller sends the address byte on SDI, SDO shifts out GEF and the Global Status Register.

A further data byte (Bit15...8) is allocated to either configure the half-bridges or retrieve status information of the TLE94103EP.



Serial Peripheral Interface (SPI)



**Figure 17 SPI Operation Mode with independent slave configuration**

The in-frame response characteristic enables the microcontroller to read the contents of the addressed register within the SPI command. See [Figure 17](#).

## Serial Peripheral Interface (SPI)

### 7.3 Daisy chain operation

The TLE94103EP supports daisy chain operation with devices with the same SPI protocol. This section describes the daisy chain hardware configuration with three devices from the TLE941xy family (See [Figure 18](#)).

The master output (noted MO) is connected to a slave SDI and the first slave SDO is connected to the next slave SDI to form a chain. The SDO of the final slave in the chain will be connected to the master input (MI) to close the loop of the SPI communication frame. In daisy chain configuration, a single chip select, CSN, and clock signal, SCLK, connected in parallel to each slave device, are used by the microcontroller to control or access the SPI devices.

In this configuration, the Master Output must send the address bytes and data bytes in the following order:

- All address bytes must be sent first:
  - Address Byte 1 (for TLE941xy\_1) is sent first, followed by Address Byte 2 (for TLE941xy\_2) etc,...
  - The LABT bit of the last address byte must be 1, while the LABT bit of all the other address bytes must be 0
- The data bytes are sent all together once all address bytes have been transmitted: Data Byte 1 (for TLE941xy\_1) is sent first, followed by Data Byte 2 (for TLE941xy\_2) etc,...

*Note: The signal on the SDI pin of the first IC in daisy chain (and in non-daisy chain mode), must be Low at the beginning of the SPI frame (between CSN falling edge and the first SCLK rising edge). This is because each Global Error Flag in daisy chain operation is implemented in OR logic.*

The Master Input (MI), which is connected to the SDO of the last device in the daisy chain receives:

- A logic OR combination of all Global Error Flags (GEF), at the beginning of the SPI frame, between CSN falling edge and the first SCLK rising edge
- The logic OR combination of the GEFs is followed by the Global Status Registers in reverse order. In other words MI receives first the Global Status Register of the last device of the daisy chain
- Once all Global Status Registers are received, MI receives the response bytes corresponding to the respective address and data bytes in reverse order. For example, if the daisy chain consists of three devices with SDO or TLE941xy\_3 connected to MI, the master receives first the Response Byte 3 of TLE941xy\_3 (corresponding to Address Byte 3 and Data Byte 3) followed by the Response Byte 2 of TLE941xy\_2 and finally the Response Byte 1 of TLE941xy\_1.

An example of an SPI frame with three devices from the TLE941xy family is shown in [Figure 19](#).

Serial Peripheral Interface (SPI)

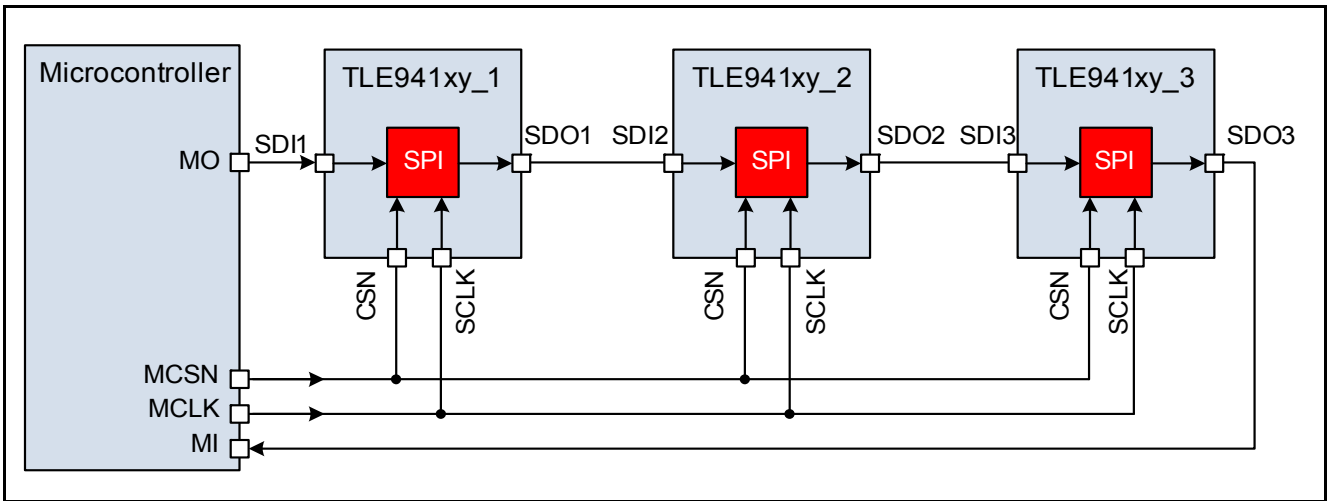


Figure 18 Example of daisy chain hardware configuration with devices from the TLE941xy family

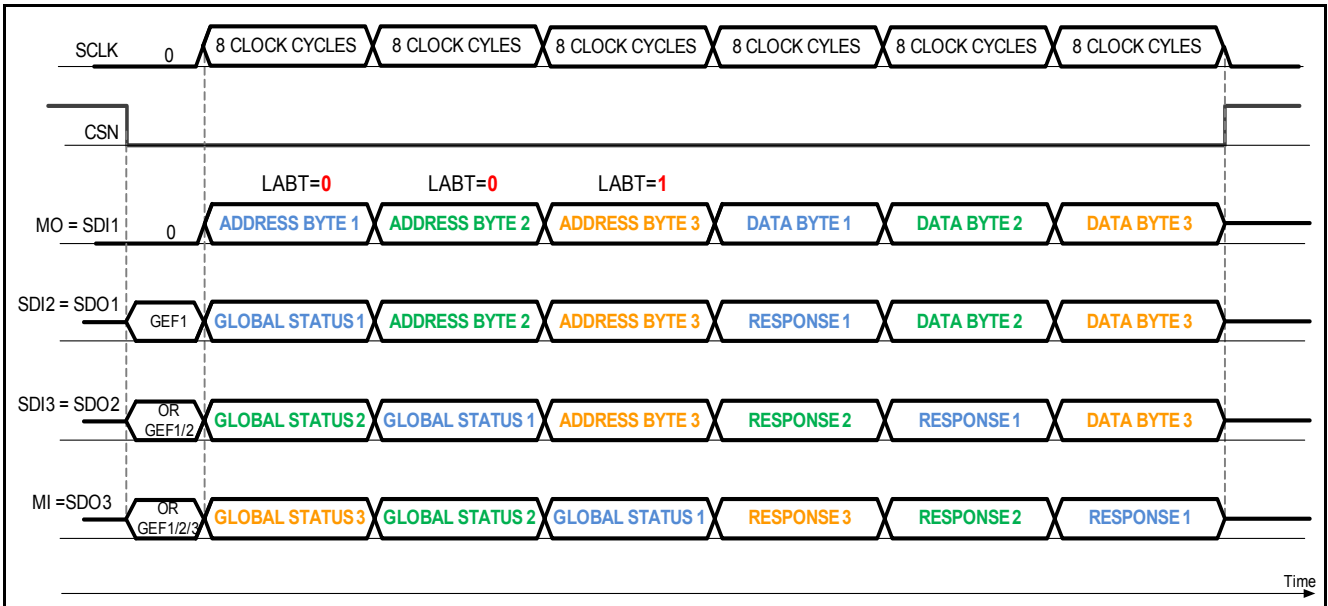
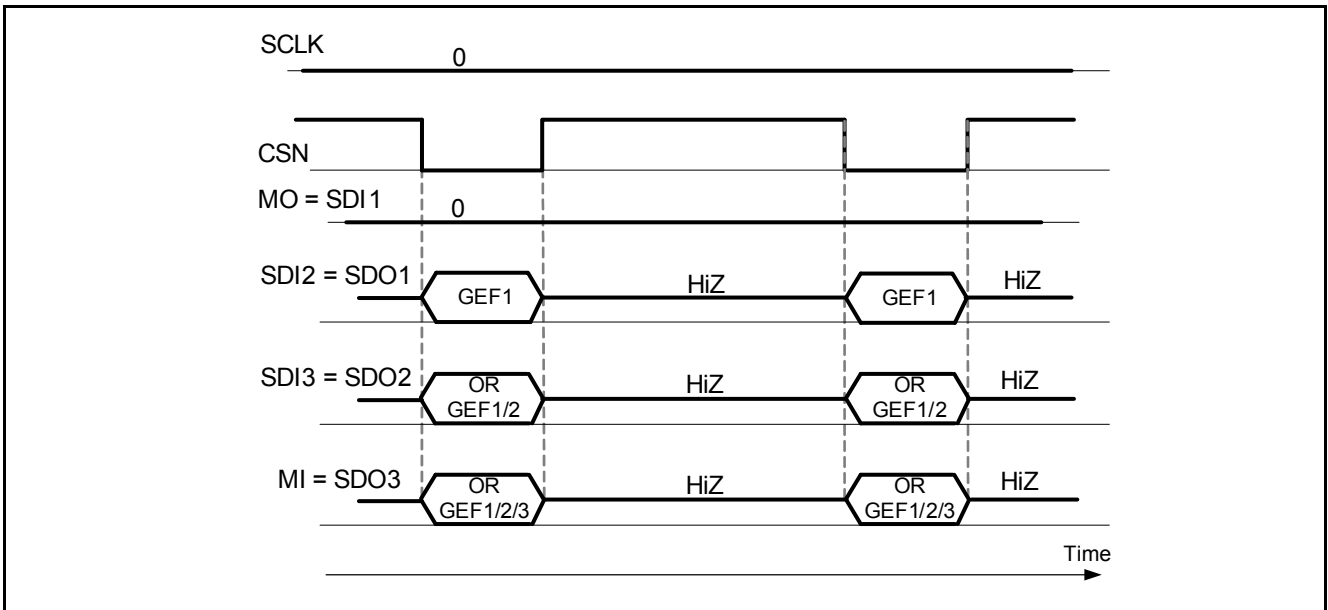


Figure 19 SPI frame with three devices of the TLE941xy family

Like in the individual slave configuration, it is possible to check if one or several TLE941xy have detected a fault condition by reading the logic OR combination of all the Global Error Flags when CSN goes Low without any clock cycle (Figure 20).

Serial Peripheral Interface (SPI)

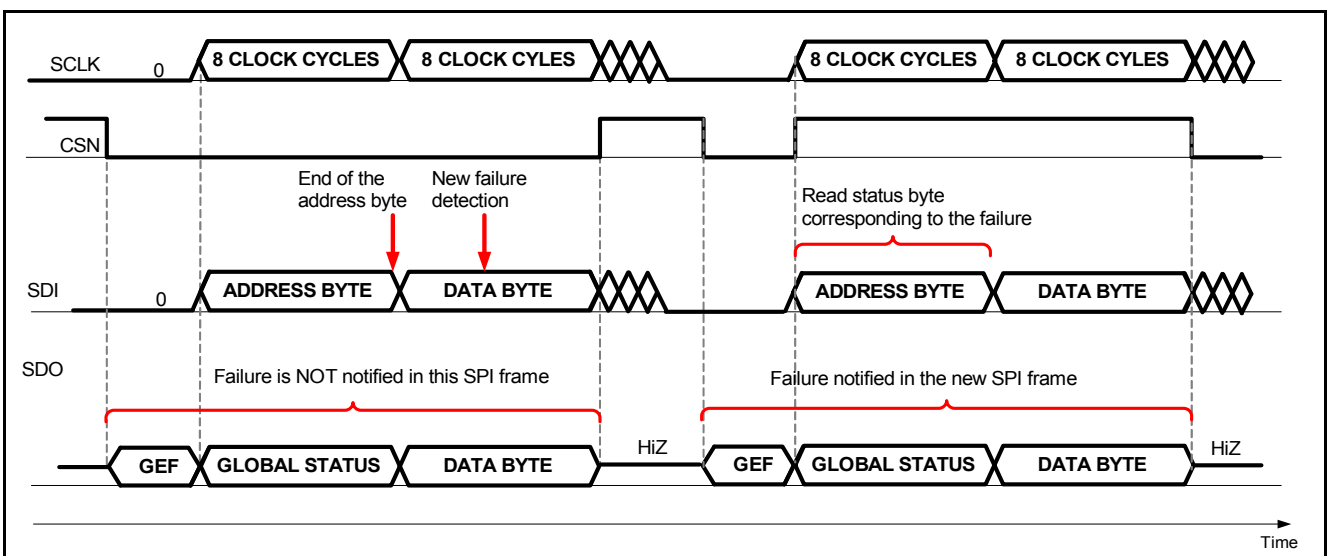


**Figure 20** Global Error Flag with zero SCLK clock cycle in daisy chain consisting only of TLE941xy devices

*Note:* Some SPI protocol errors such as the LSB of an address byte is wrongly equal to 0, may be reported in the SPI\_ERR bit of another device in the daisy chain (refer to [Chapter 7.1.3](#) and [Chapter 7.7](#) for more details on SPI\_ERR). In this case some devices might accept wrong data during the corrupted SPI frame. Therefore if one of the devices in the daisy chain reports an SPI error, it is recommended to verify the content of the registers of all devices.

**7.4 Status register change during SPI communication**

If a new failure occurs after the transfer of the data byte(s), i.e. between the end of the last address byte and the CSN rising edge, this failure will be reported in the next SPI frame (see example in [Figure 21](#)).



**Figure 21** Status register change during transfer of data byte - Example in independent slave configuration

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## Serial Peripheral Interface (SPI)

No information is lost, even if a status register is changed during a SPI frame, in particular during a Read and Clear command. For example:

- the microcontroller sends a Read and Clear command to a status register
- the TLE94103EP detects during the transfer the data byte(s) a new fault condition, which is normally reported in the target status register

The incoming Clear command will be ignored, so that the microcontroller can read the new failure in the subsequent SPI frames.

Data inconsistency between the Global Status Register (see [Chapter 7.7](#)) and the data byte (status register) within the same SPI frame is possible if:

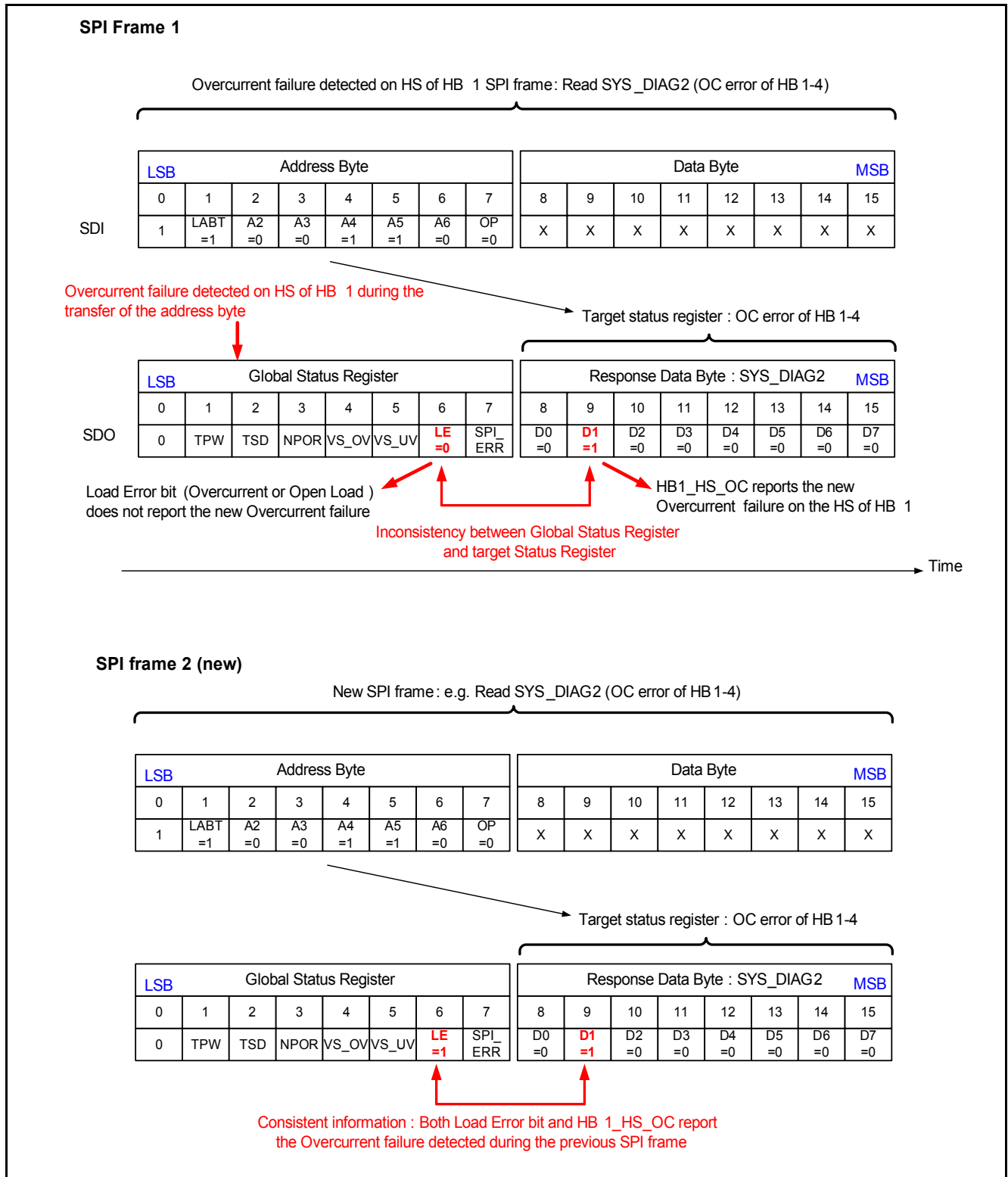
- an open load or overcurrent error is detected during the transfer of the data byte
- the target status register corresponds to the new detected failure

In this case the new failure:

- is not reported in the Global Status Register of the current SPI frame but in the next one
- is reported in the data byte of the current SPI frame

Refer to [Figure 21](#).

Serial Peripheral Interface (SPI)



**Figure 22 Example of inconsistency between Global Error Flag and Status Register when a status bit is changed during the transfer of an address byte**

Serial Peripheral Interface (SPI)

7.5 SPI Bit Mapping

The SPI Registers have been mapped as shown in [Figure 23](#) and [Figure 24](#) respectively.

The control registers are READ/ WRITE registers. To set the control register to READ, bit 7 of the address byte (OP bit) must be programmed to '0', otherwise '1' for WRITE.

The status registers are READ/CLEAR registers. To CLEAR any Status Register, bit 7 of the address byte must be set to '1', otherwise '0' for READ.

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		8 Data Bits [D7...D0] for Configuration & Status Information								8 Address Bits [A7...0]								
										Access type								
CONTROL REGISTERS	HB_ACT_1_CTRL									read/write	0	0	0	0	0	LABT	1	
	FM_CLK_CTRL									read/write	0	1	1	0	0	LABT	1	
	OLBLK_CTRL									read/write	1	1	0	1	0	LABT	1	
	CONFIG_CTRL									read	1	1	0	0	1	LABT	1	
STATUS REGISTERS	SYS_DIAG_1 : Global status 1									read/clear	0	0	1	1	0	LABT	1	
	SYS_DIAG_2 : OP ERROR_1_STAT									read/clear	1	0	1	1	0	LABT	1	
	SYS_DIAG_3 : OP ERROR_2_STAT									read/clear	0	0	0	0	1	LABT	1	

Figure 23 TLE94103EP SPI Register mapping

Note: LABT: Last Address Bit Token, refer to [Chapter 7.2](#) and [Chapter 7.3](#).

Serial Peripheral Interface (SPI)

Register Name	Data Bits D7...D0							Address Bits A7...A0						
	D7	D6	D5	D4	D3	D2	D1	D0	7	6	5	4	3	2
<b>CONTROL REGISTERS</b>														
HB_ACT_1_CTRL	reserved	reserved	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN	reserved	read/write	0	0	0	0
FM_CLK_CTRL	FM_CLK_MOD1	FM_CLK_MOD0	reserved	reserved	reserved	reserved	reserved	reserved	reserved	read/write	0	1	1	0
OLBLK_CTRL	OLBLANK	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved	read/write	1	1	0	1
CONFIG_CTRL	reserved	reserved	reserved	reserved	reserved	DEV_ID2	DEV_ID1	DEV_ID0	reserved	read	1	1	0	1
<b>STATUS REGISTERS</b>														
SYS_DIAG_1 : Global status 1	SPI_ERR	LE	VS_UV	VS_OV	NPOR	TSD	TPW	0	reserved	read/clear	0	0	1	1
SYS_DIAG_2 : OP ERROR_1_STAT	reserved	reserved	HB3_HS_OC	HB3_LS_OC	HB2_HS_OC	HB2_LS_OC	HB1_HS_OC	HB1_LS_OC	reserved	read/clear	1	0	1	1
SYS_DIAG_3 : OP ERROR_2_STAT	reserved	reserved	HB3_HS_OL	HB3_LS_OL	HB2_HS_OL	HB2_LS_OL	HB1_HS_OL	HB1_LS_OL	reserved	read/clear	0	0	0	1

Figure 24 TLE94103EP Bit Mapping

Note: LABT: Last Address Bit Token, refer to [Chapter 7.2](#) and [Chapter 7.3](#).



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## Serial Peripheral Interface (SPI)

### 7.6 SPI Control Registers

The Control Registers have a READ/WRITE access (see [Chapter 7.5](#)):

- The 'POR' value is defined by the register content after a POR or device Reset
  - The default value of all control registers is 0000 0000<sub>B</sub> with the exception of CONFIG\_CTRL and FM\_CLK\_CTRL
  - The default value of the CONFIG\_CTRL register is 0000 0101<sub>B</sub>
  - The default value of the FM\_CTLR\_CTRL register is 1100 0000<sub>B</sub>
- One 16-bit SPI command consists of two bytes (see [Figure 23](#) and [Figure 24](#)), i.e.
  - an address byte
  - followed by a data byte
- The control bits are not cleared or changed automatically by the device. This must be done by the microcontroller via SPI programming.
- Reading a register is done byte wise by setting the SPI bit 7 to "0" (= READ ONLY).
- Writing to a register is done byte wise by setting the SPI bit 7 to "1".

---

Serial Peripheral Interface (SPI)

### 7.6.1 Control register definition

**HB\_ACT\_1\_CTRL**
**Half-bridge output control 1 (Address Byte [OP] 000 00[LABT]1<sub>B</sub>)**

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
reserved	D7	rw	<b>Reserved. Always reads as '0'</b>
reserved	D6	rw	<b>Reserved. Always reads as '0'</b>
HB3_HS_EN	D5	rw	<b>Half-bridge output 3 high side switch enable</b> 0 <sub>B</sub> HS3 OFF/ High-Z (default value) 1 <sub>B</sub> HS3 ON
HB3_LS_EN	D4	rw	<b>Half-bridge output 3 low side switch enable</b> 0 <sub>B</sub> LS3 OFF/ High-Z (default value) 1 <sub>B</sub> LS3 ON
HB2_HS_EN	D3	rw	<b>Half-bridge output 2 high side switch enable</b> 0 <sub>B</sub> HS2 OFF/ High-Z (default value) 1 <sub>B</sub> HS2 ON
HB2_LS_EN	D2	rw	<b>Half-bridge output 2 low side switch enable</b> 0 <sub>B</sub> LS2 OFF/ High-Z (default value) 1 <sub>B</sub> LS2 ON
HB1_HS_EN	D1	rw	<b>Half-bridge output 1 high side switch enable</b> 0 <sub>B</sub> HS1 OFF/ High-Z (default value) 1 <sub>B</sub> HS1 ON
HB1_LS_EN	D0	rw	<b>Half-bridge output 1 low side switch enable</b> 0 <sub>B</sub> LS1 OFF/ High-Z (default value) 1 <sub>B</sub> LS1 ON

*Note:* The simultaneous activation of both HS and LS switch within a half-bridge is prevented by the digital block to avoid cross current. If both LS\_EN and HS\_EN bits of a given half-bridge are set, the logic turns off this half-bridge.

---

**Serial Peripheral Interface (SPI)**
**FM\_CLK\_CTRL****Frequency modulation select (Address Byte [OP]011 00[LABT]1<sub>B</sub>)**

D7	D6	D5	D4	D3	D2	D1	D0
<b>FM_CLK_MOD1</b>	<b>FM_CLK_MOD0</b>	<b>Reserved</b>	<b>Reserved</b>	<b>Reserved</b>	<b>Reserved</b>	<b>Reserved</b>	<b>Reserved</b>
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>FM_MOD_EN</b>	D7:D6	rw	<b>FM Modulation Enable<sup>1)</sup></b> 00 <sub>B</sub> No modulation 01 <sub>B</sub> Modulation frequency 15.625kHz 10 <sub>B</sub> Modulation frequency 31.25kHz 11 <sub>B</sub> Modulation frequency 62.5kHz (default)
<b>reserved</b>	D5:D4	r	<b>Reserved. Always reads as '0'.</b>
<b>reserved</b>	D3:D2	r	<b>Reserved. Always reads as '0'.</b>
<b>reserved</b>	D1:D0	r	<b>Reserved. Always reads as '0'.</b>

1) Not subject to production test, guaranteed by design. Frequency may deviate by ±10%

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**Serial Peripheral Interface (SPI)**
**OLBLK\_CTRL****Open load blanking setting (Address Byte [OP]110 10[LABT]1)<sub>B</sub>**

D7	D6	D5	D4	D3	D2	D1	D0
<b>OL_BLANK</b>	<b>reserved</b>	<b>reserved</b>	<b>reserved</b>	<b>reserved</b>	<b>reserved</b>	<b>reserved</b>	<b>reserved</b>
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>OL_BLANK</b>	D7	rw	<b>Internal target:</b> 0 <sub>B</sub> (default) Open load failures are reported in the GEF 1 <sub>B</sub> Open load failures are not reported in the GEF
<b>reserved</b>	D6	rw	<b>To be programmed as '0'.</b>
<b>reserved</b>	D5	rw	<b>Reserved. Always reads as '0'.</b>
<b>reserved</b>	D4	rw	<b>Reserved. Always reads as '0'.</b>
<b>reserved</b>	D3	rw	<b>Reserved. Always reads as '0'.</b>
<b>reserved</b>	D2	rw	<b>Reserved. Always reads as '0'.</b>
<b>reserved</b>	D1	rw	<b>Reserved. Always reads as '0'.</b>
<b>reserved</b>	D0	rw	<b>Reserved. Always reads as '0'.</b>

Serial Peripheral Interface (SPI)

**CONFIG\_CTRL**

Device Configuration control (Address Byte [OP]110 01[LABT]1<sub>B</sub>)

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	DEV_ID2	DEV_ID1	DEV_ID0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
reserved	D7:D3	r	Always reads as '0'
DEV_IDn	D2:D0	r	<p><b>Device/ derivative identifier</b></p> <p><i>Note: These bits can be used to verify the silicon content of the device</i></p> <p>000<sub>B</sub> TLE94112EL chip                      001<sub>B</sub> TLE94110EL chip                      010<sub>B</sub> TLE94108EL chip                      011<sub>B</sub> TLE94106EL/ES chip                      100<sub>B</sub> TLE94104EP chip                      101<sub>B</sub> TLE94103EP chip                      110<sub>B</sub> reserved                      111<sub>B</sub> reserved</p>

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## Serial Peripheral Interface (SPI)

### 7.7 SPI Status Registers

The Control Registers have a READ/CLEAR access (see also [Chapter 7.5](#)):

- The 'POR Value' of the Status registers (content after a POR or device Reset) and is 0000 0000<sub>B</sub>.
- One 16-bit SPI command consists of two bytes (see [Figure 23](#) and [Figure 24](#)), i.e.
  - an address byte
  - followed by a data byte
- Reading a register is done byte wise by setting the SPI bit 7 of the address byte to "0" (= Read Only).
- Clearing a register is done byte wise by setting the SPI bit 7 of the address byte to "1".
- SPI status registers are not cleared automatically by the device. This must be done by the microcontroller via SPI command.

## Serial Peripheral Interface (SPI)

### 7.7.1 Status register definition

#### SYS\_DIAG1

Global status 1 (Address Byte [OP]001 10[LABT]1<sub>B</sub>)

D7	D6	D5	D4	D3	D2	D1	D0
SPI_ERR	LE	VS_UV	VS_OV	NPOR	TSD	TPW	reserved
rc	r	rc	rc	rc	rc	rc	r

Field	Bits	Type	Description
SPI_ERR	D7	rc	<b>SPI error detection</b> 0 <sub>B</sub> No SPI protocol error is detected (default value). 1 <sub>B</sub> An SPI protocol error is detected.
LE	D6	r	<b>Load error detection (logic OR combination of Open Load and Overcurrent)</b> 0 <sub>B</sub> No Open Load and no Overcurrent detected (default value) 1 <sub>B</sub> Open Load or Overcurrent detected in at least one of the power outputs. Error latched. Faulty output is latched off in case of Overcurrent
VS_UV	D5	rc	<b>VS Undervoltage error detection</b> 0 <sub>B</sub> No undervoltage on V <sub>S</sub> detected (default value) 1 <sub>B</sub> Undervoltage on V <sub>S</sub> detected. Error latched and all outputs disabled.
VS_OV	D4	rc	<b>VS Overvoltage error detection</b> 0 <sub>B</sub> No overvoltage on V <sub>S</sub> detected (default value) 1 <sub>B</sub> Overvoltage on V <sub>S</sub> detected. Error latched and all outputs disabled.
NPOR	D3	rc	<b>Not Power On Reset (NPOR) detection</b> 0 <sub>B</sub> POR on EN or VDD supply rail (default value) 1 <sub>B</sub> No POR
TSD	D2	rc	<b>Temperature shutdown error detection</b> 0 <sub>B</sub> Junction temperature below temperature shutdown threshold (default value) 1 <sub>B</sub> Junction temperature has reached temperature shutdown threshold. Error latched and all outputs disabled.
TPW	D1	rc	<b>Temperature pre-warning error detection</b> 0 <sub>B</sub> Junction temperature below temperature pre-warning threshold (default value) 1 <sub>B</sub> Junction temperature has reached temperature pre-warning threshold.
reserved	D0	r	<b>Bit reserved. Always reads '0'.</b>

*Note:* The LE bit in the Global Status register is read only. It reflects an OR combination of the respective open load and overcurrent errors of the half-bridge channels. If all OC/OL bits of the respective high-side and low-side channels are cleared to '0', the LE bit will be automatically updated to '0'.

## Serial Peripheral Interface (SPI)

## SYS\_DIAG\_2 : OP\_ERROR\_1\_STAT

Overcurrent error status of half-bridge outputs 1 - 4 (Address Byte [OP]101 10[LABT]1<sub>B</sub>)

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	HB3_HS_OC	HB3_LS_OC	HB2_HS_OC	HB2_LS_OC	HB1_HS_OC	HB1_LS_OC
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
reserved	D7	rc	<b>Reserved. Always reads as '0'.</b>
reserved	D6	rc	<b>Reserved. Always reads as '0'.</b>
HB3_HS_OC	D5	rc	<b>High-side (HS) switch of half-bridge 3 overcurrent detection</b> 0 <sub>B</sub> No error on HS3 switch (default value) 1 <sub>B</sub> Overcurrent detected on HS3 switch. Error latched and HS3 disabled.
HB3_LS_OC	D4	rc	<b>Low-side (LS) switch of half-bridge 3 overcurrent detection</b> 0 <sub>B</sub> No error on LS3 switch (default value) 1 <sub>B</sub> Overcurrent detected on LS3 switch. Error latched and LS3 disabled.
HB2_HS_OC	D3	rc	<b>High-side (HS) switch of half-bridge 2 overcurrent detection</b> 0 <sub>B</sub> No error on HS2 switch (default value) 1 <sub>B</sub> Overcurrent detected on HS2 switch. Error latched and HS2 disabled.
HB2_LS_OC	D2	rc	<b>Low-side (LS) switch of half-bridge 2 overcurrent detection</b> 0 <sub>B</sub> No error on LS2 switch (default value) 1 <sub>B</sub> Overcurrent detected on LS2 switch. Error latched and LS2 disabled.
HB1_HS_OC	D1	rc	<b>High-side (HS) switch of half-bridge 1 overcurrent detection</b> 0 <sub>B</sub> No error on HS1 switch (default value) 1 <sub>B</sub> Overcurrent detected on HS1 switch. Error latched and HS1 disabled.
HB1_LS_OC	D0	rc	<b>Low-side (LS) switch of half-bridge 1 overcurrent detection</b> 0 <sub>B</sub> No error on LS1 switch (default value) 1 <sub>B</sub> Overcurrent detected on LS1 switch. Error latched and LS1 disabled.



## Serial Peripheral Interface (SPI)

## SYS\_DIAG\_3 : OP\_ERROR\_2\_STAT

Open load error status of half-bridge outputs 1 - 4 (Address Byte [OP]000 01[LABT]1<sub>B</sub>)

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	HB3_HS_OL	HB3_LS_OL	HB2_HS_OL	HB2_LS_OL	HB1_HS_OL	HB1_LS_OL
rc	rc	rc	rc	rc	rc	rc	rc

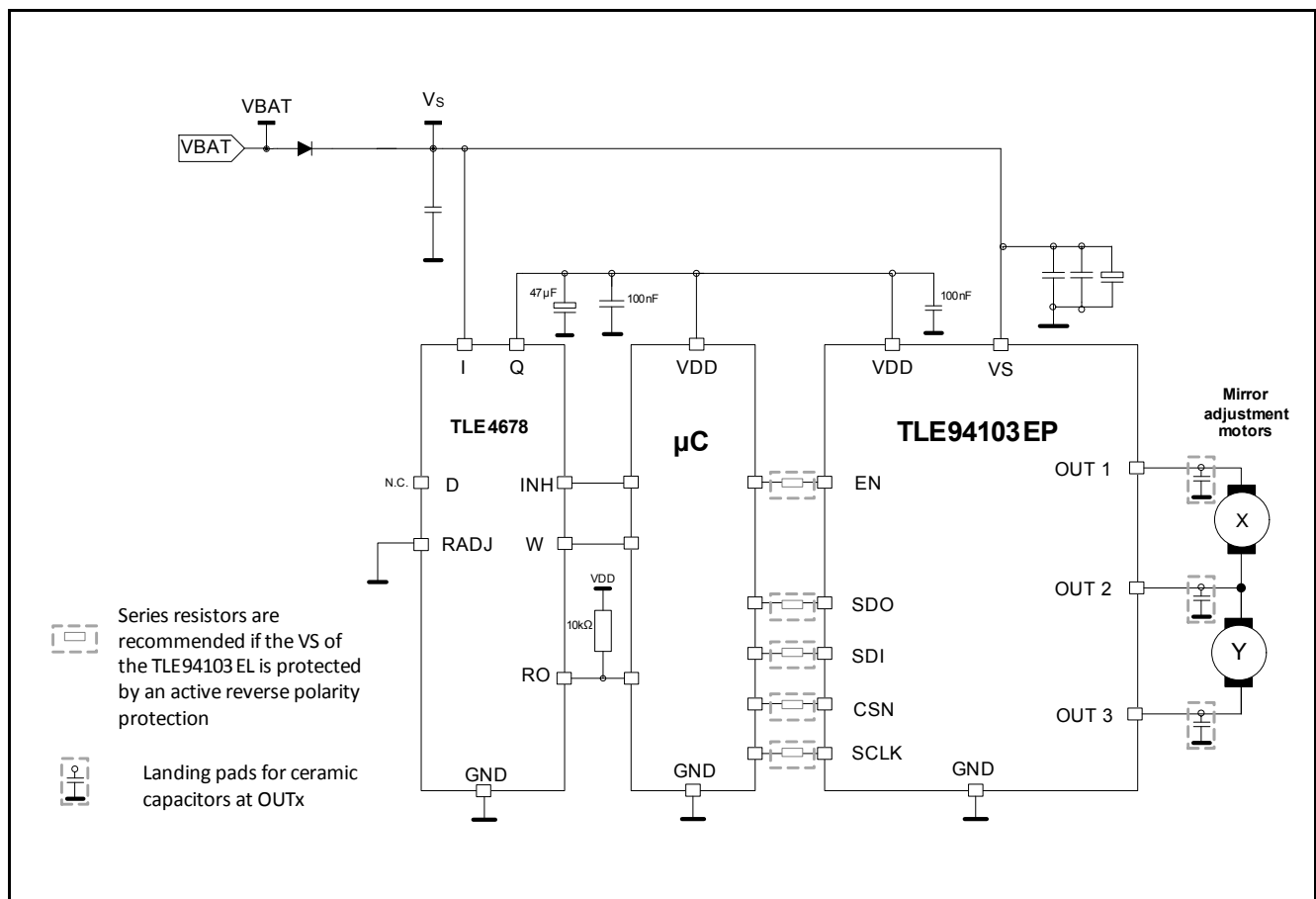
Field	Bits	Type	Description
reserved	D7	rc	<b>Reserved. Reads as '0'.</b>
reserved	D6	rc	<b>Reserved. Reads as '0'. Low-side (LS) switch of half-bridge 4 open load detection</b>
HB3_HS_OL	D5	rc	<b>High-side (HS) switch of half-bridge 3 open load detection</b> 0 <sub>B</sub> No error on HS3 switch (default value) 1 <sub>B</sub> Open load detected on HS3 switch. Error latched.
HB3_LS_OL	D4	rc	<b>Low-side (LS) switch of half-bridge 3 open load detection</b> 0 <sub>B</sub> No error on LS3 switch (default value) 1 <sub>B</sub> Open load detected on LS3 switch. Error latched.
HB2_HS_OL	D3	rc	<b>High-side (HS) switch of half-bridge 2 open load detection</b> 0 <sub>B</sub> No error on HS2 switch (default value) 1 <sub>B</sub> Open load detected on HS2 switch. Error latched.
HB2_LS_OL	D2	rc	<b>Low-side (LS) switch of half-bridge 2 open load detection</b> 0 <sub>B</sub> No error on LS2 switch (default value) 1 <sub>B</sub> Open load detected on LS2 switch. Error latched.
HB1_HS_OL	D1	rc	<b>High-side (HS) switch of half-bridge 1 open load detection</b> 0 <sub>B</sub> No error on HS1 switch (default value) 1 <sub>B</sub> Open load detected on HS1 switch. Error latched.
HB1_LS_OL	D0	rc	<b>Low-side (LS) switch of half-bridge 1 open load detection</b> 0 <sub>B</sub> No error on LS1 switch (default value) 1 <sub>B</sub> Open load detected on LS1 switch. Error latched.

## Application Information

### 8 Application Information

**Note:** The following simplified application examples are given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The function of the described circuits must be verified in the real application.

#### 8.1 Application Diagram



**Figure 25** Application Example for DC-motor loads

#### Notes on the application example

1. Series resistors between the microcontroller and the signal pins of the TLE94103EP are recommended if an active reverse polarity protection (MOSFET) is used to protect the VS pin. These resistors limit the current between the microcontroller and the device during negative transients on VBAT (e.g. ISO/TR 7637 pulse 1)
2. Landing pads for ceramic capacitors at the outputs of the TLE94103EP as close as possible to the connectors are recommended (the ceramic capacitors are not populated if unused). These ceramic capacitors can be mounted if a higher performance in term of ESD capability is required.
3. The electrolytic capacitor at the VS pin should be dimensioned in order to prevent the VS voltage from exceeding the absolute maximum rating. PWM operation with a too low capacitance can lead to a VS voltage overshoot, which results in a VS overvoltage detection.

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**Application Information**

4. *Not used (NU) pins and unused outputs are recommended to be left unconnected (open) in the application. If NU pins or unused output pins are routed to an external connector which leaves the PCB, then these outputs should have provision for a zero ohm jumper (depopulated if unused) or ESD protection. In other words, NU and unused pins should be treated like used pins.*
5. *Place bypass ceramic capacitors as close as possible to the VS pins, with shortest connections the GND pins and GND layer, for best EMC performance*

Application Information

8.2 Thermal application information

Ta = -40°C, Ch1 to Ch3 are dissipating a total of 0.6W (0.2W each).

Ta = 85°C, Ch1 to Ch3 are dissipating a total of 0.405W (0.135W each).

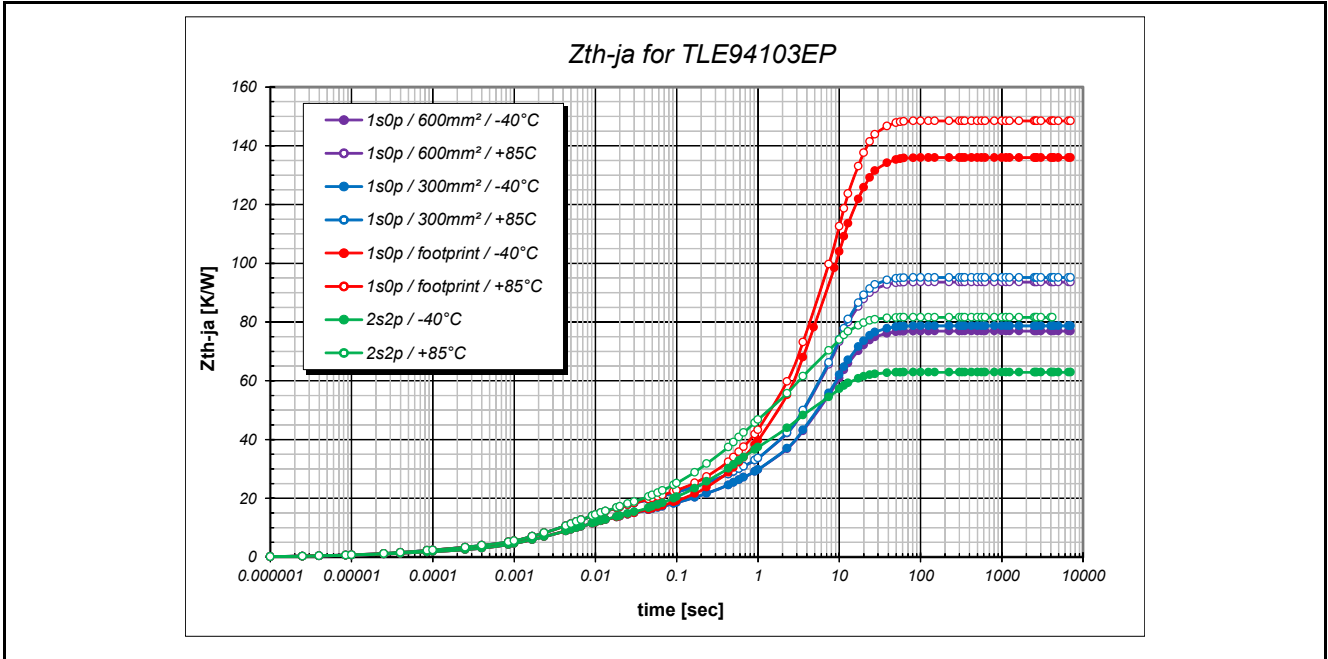


Figure 26 ZthJA Curve for different PCB setups

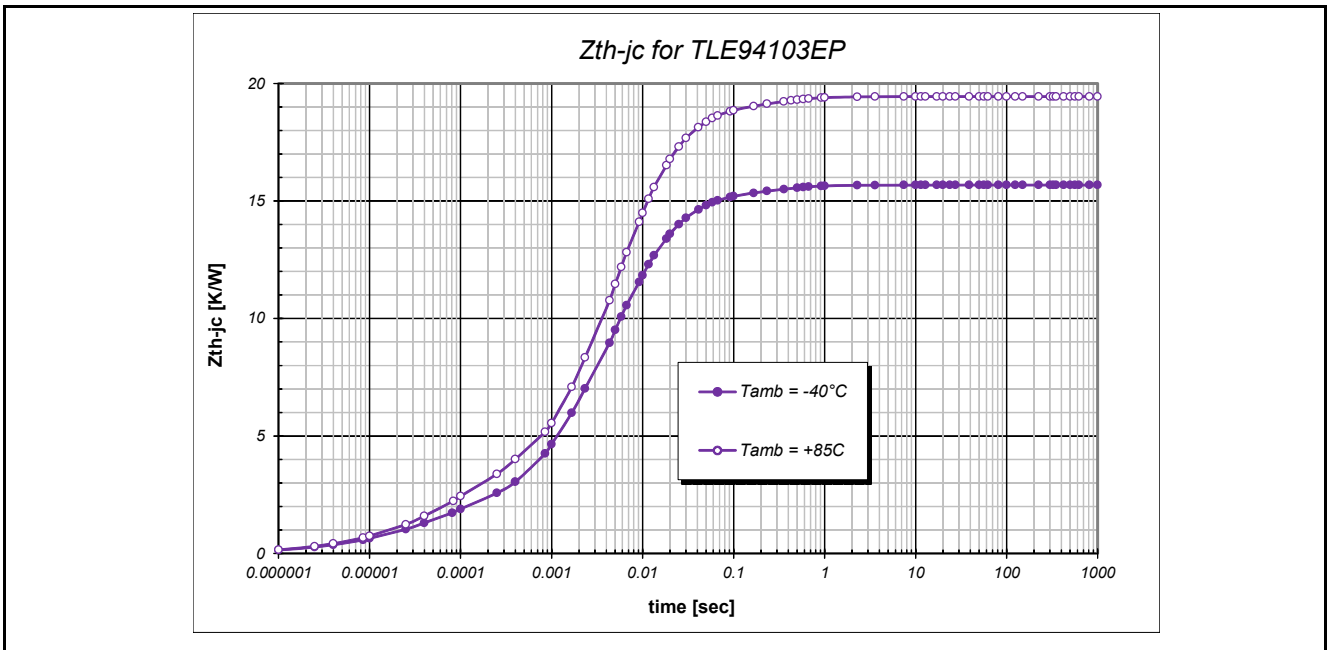


Figure 27 ZthJC Curve

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**Application Information****8.3 EMC Enhancement**

In the event the emissions of the device exceed the allowable limits, a modulation of the oscillator frequency is incorporated to reduce eventual harmonics of the 8MHz base clock. The frequencies can be selected based on the resolution bandwidth of the peak detector during EMC testing.

The selection is achieved by setting the FM\_CLK\_MODn bits in the FM\_CLK\_CTRL register as follows:

00<sub>B</sub>: OFF

01<sub>B</sub>: FM CLK=15.625 kHz

10<sub>B</sub>: FM CLK=31.25 kHz

11<sub>B</sub>: FM CLK=62.5 kHz

Package Outlines

9 Package Outlines

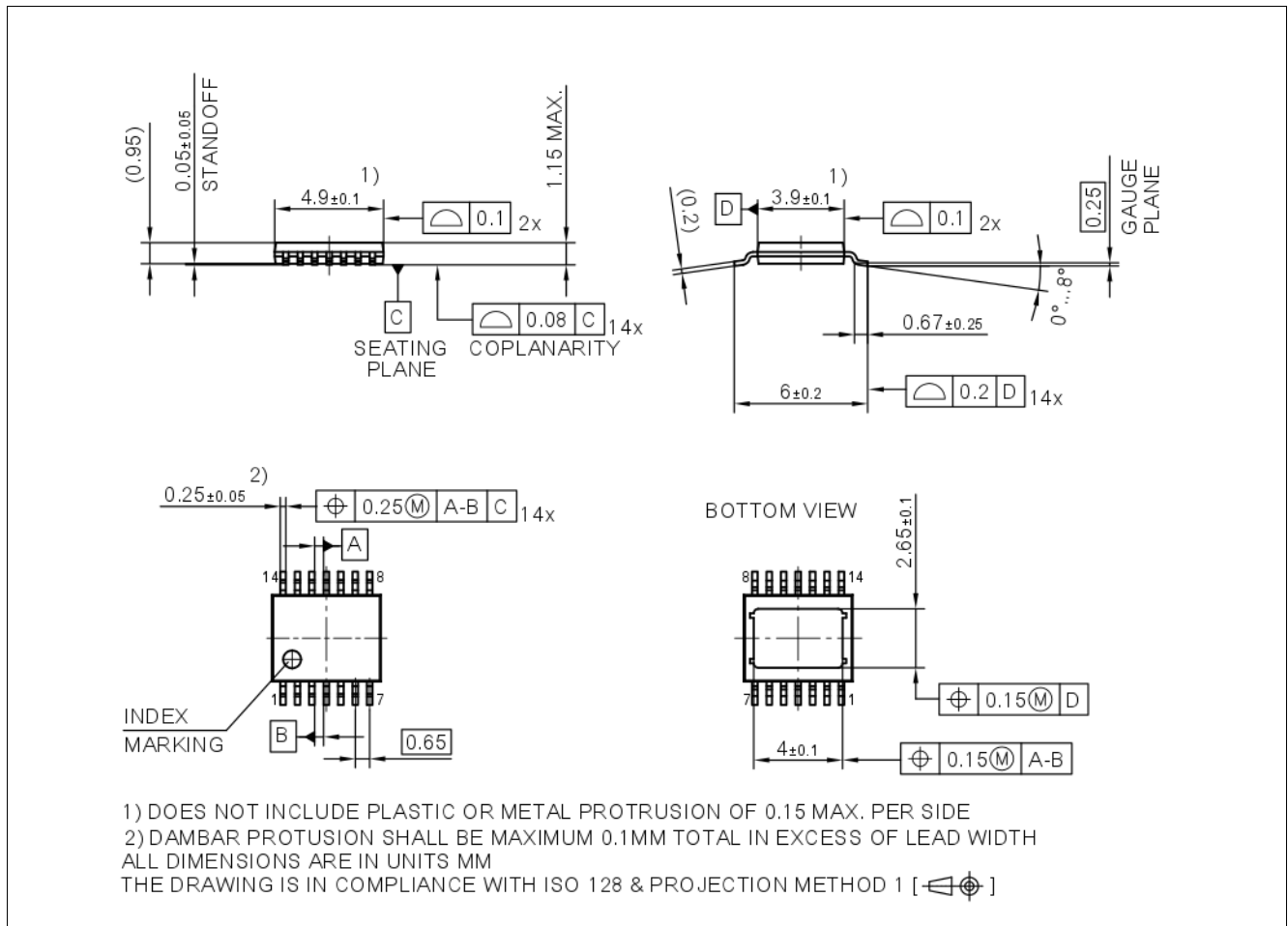


Figure 28 PG-TSDSO-14 (Plastic Green - Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e lead-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:  
<http://www.infineon.com/packages>.

Dimensions in mm

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**Revision History****10 Revision History**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.0	2017-12-07	Initial release

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