PL903xxx

Revision 1.0

General Description

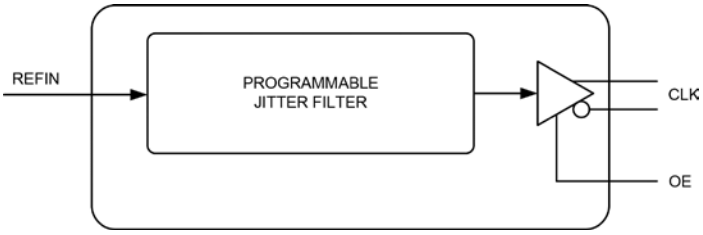
The PL903xxx series is a small form factor, high performance OTP-base device and a member of Micrel's JitterBlocker, factory programmable jitter attenuators. The JitterBlocker product family cleans deterministic jitter by attenuating spurious components in the phase noise, thereby improving the phase jitter and the overall phase noise. The PL903xxx is capable of reducing multiple pico seconds of phase jitter in a clock to a level below $1ps_{RMS}$, making that clock usable for many more applications.

The PL903xxx operates on a single 2.5V or 3.3V supply and is housed in a small QFN package for a broad range of applications.

Input clock frequencies up to 200MHz can be filtered and frequency translation allows for output clock frequencies up to 840MHz.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Block Diagram



Features

- Lowest-power, smallest programmable jitter attenuator
- Input frequency up to 200MHz
- Output frequency up to 840MHz
- Jitter attenuation 20dB at 3MHz spur frequency
- Additive phase jitter or phase jitter floor:
  - 55fs for 1.875MHz to 20MHz
  - 251fs for 12kHz to 20MHz
- Single ended CMOS input
- One differential or two single ended outputs. Output logic types supported are LVPECL, LVDS, HCSL and LVCMOS (single ended or differential).
- Operating temperature range from –40°C to +85°C
- Available in 24-pin QFN RoHS-compliant package.
- Related devices:
  - PL902xxx: LVCMOS, period jitter cleaning.
  - PL904xxx: Differential input, two differential outputs, phase noise cleaning

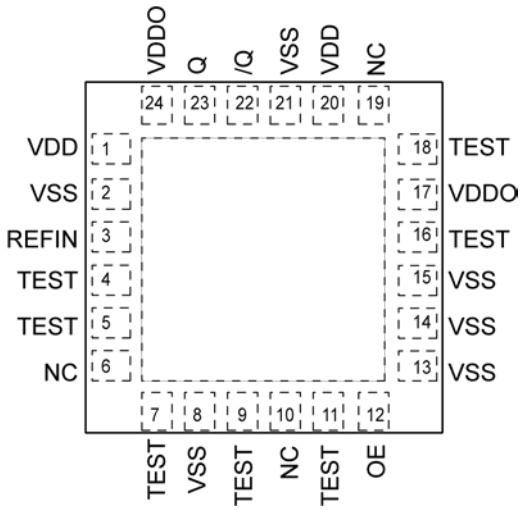
Applications

- 1/10/40/100 Gigabit Ethernet (GbE)
- SONET/SDH
- PCI Express
- CPRI/OBSAI wireless base stations
- Fibre Channel
- SAS/SATA
- DIMM

Ordering Information

Part Number	Marking	Shipping	Ambient Temp. Range	Package
PL903xxxUMG	PL903 XXX	Tray	–40° to +85°C	QFN-24L
PL903xxxUMG TR	PL903 XXX	Tape and Reel	–40° to +85°C	QFN-24L

Pin Configuration



24-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
22 23	Q /Q	O	Various	Clock output. Can be programmed to one of the following logic types:[1] LVPECL, LVDS, HCSL, or LVCMOS.
3	REFIN	I, (SE)	Various	Reference clock input. Can be programmed to either LVCMOS levels or smaller amplitude signals from other logic types.
12	OE	I	LVCMOS	Output enable control input with pull-up (45kΩ).
1, 20	VDD	PWR		Core power supply.
17, 24	VDDO	PWR		Output buffer power supply.
2, 8, 13, 14 15, 21	VSS	PWR		Power supply ground.
4, 5, 7, 9, 11 16, 18	TEST			Used for production test Do not connect anything to these pins.
6, 10, 19	NC			Not internally connected. No need to connect anything to these pins.
ePad	Exposed Pad	GND		The center pad must be connected to the ground plane both for electrical ground and thermal relief.

Note:

1. In case of LVCMOS, the output pair can provide two single-ended LVCMOS outputs.

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Functional Description

PL903xxx series is a very flexible, advanced programmable jitter filter design for high performance, small form-factor applications. The PL903xxx accepts a reference clock input between 12MHz and 200MHz and is capable of producing one differential output up to 840MHz or two single ended outputs up to 250MHz. The most common configuration will be with the same input and output frequency but this flexible design also allows frequency translation from one frequency to another frequency, as long as both frequencies are within the specified ranges for input and output**.**

Jitter Attenuation

Typically the jitter attenuation settings will be optimized for one particular input and output frequency. Customization of attenuation properties is possible.

The lowest possible output phase jitter, or phase jitter floor, is 251fs for the 12kHz to 20MHz integration range and 55fs for the Gigabit Ethernet integration range of 1.875MHz to 20MHz. The PL903xxx excels at attenuating deterministic jitter that presents itself as spurs in the phase noise plot above 1MHz.

Clock Output

The output pins Q and /Q make a differential output that can be programmed to several different logic types: LVPECL, LVDS, HCSL or LVCMOS. In the case of LVCMOS, there are three possible configurations:

1. One single-ended output with the complementary pin disabled to a high impedance.
2. Two single-ended, in-phase outputs.
3. A differential output with opposite phases at the two output pins

Output Frequency

The most common configuration is where the output frequency is the same as the input frequency. However, frequency translations are possible. The input frequency upper limit is 200MHz, but the output can go up to 840MHz.

Output Enable (OE)

The Output Enable feature allows the user to enable and disable the clock output(s) by toggling the OE pin. The OE pin incorporates a 45kΩ pull-up resistor giving a default condition of logic “1” that enables the output(s).

Reference (Noisy) Clock Input (REFIN)

The input requires a single-ended CMOS signal. The frequency range for the input is 12MHz to 200MHz.

Absolute Maximum Ratings[2]

Supply Voltage (V_{DD}, V_{DDO}) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.5V to V_{DD} + 0.5V
Lead Temperature (soldering, 20s) ..... 260°C
Case Temperature ..... 115°C
Storage Temperature (Ts) ..... –65°C to +150°C

Operating Ratings[3]

Supply Voltage (V_{DD}, V_{DDO}) ..... +2.375V to +3.465V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance[4]
(θ_{JA}), Still-Air ..... 50°C/W

DC Electrical Characteristics[5]

V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}	Power supply voltage		2.375		3.465	V
I_{DD}	Total supply current, V_{DD} + V_{DDO}	LVPECL, 312.5MHz Outputs open		100	120	mA
		HCSL (PCIe), 100MHz Outputs terminated with 50Ω to V_{SS}		80	100	mA
		2 × LVCMOS, 125MHz Outputs open		70	90	mA

LVCMOS Inputs (OE, REFIN) DC Electrical Characteristics[5]

V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		70% V_{DD}		V_{DD} + 0.3	V
V_{IN}	Input low voltage		V_{SS} – 0.3		30% V_{DD}	V
I_{IH}	Input high current	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input low current	V_{DD} = 3.465V, V_{IN} = 0V	–150			µA

Notes:

2. Exceeding the absolute maximum ratings may damage the device.
3. The device is not guaranteed to function outside its operating ratings.
4. Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
5. The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.

LVDS Output DC Electrical Characteristics[5]

V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C, R_L = 100Ω across Q and /Q.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OD}	Differential output voltage	Figure 6	275	350	475	mV
ΔV_{OD}	V_{OD} magnitude change				40	mV
V_{OS}	Offset voltage		1.15	1.25	1.50	V
ΔV_{OS}	V_{OS} magnitude change				50	mV

HCSL Output DC Electrical Characteristics[5]

V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C, R_L = 50Ω to V_{SS}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output high voltage	Figure 1, Figure 5	660	700	850	mV
V_{OL}	Output low voltage	Figure 1, Figure 5	–150	0	27	mV
V_{SWING}	Output voltage swing	Figure 1, Figure 5	630	700	1000	mV

LVPECL Output DC Electrical Characteristics[5]

V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C, R_L = 50Ω to V_{DD} – 2V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output high voltage	Figure 1, Figure 4	V_{DD} – 1.145	V_{DD} – 0.97	V_{DD} – 0.845	V
V_{OL}	Output low voltage	Figure 1, Figure 4	V_{DD} – 1.945	V_{DD} – 1.77	V_{DD} – 1.645	V
V_{SWING}	Output voltage swing	Figure 1, Figure 4	0.6	0.8	1.0	V

LVCMOS Output DC Electrical Characteristics[5]

V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C, R_L = 50Ω to V_{DD}/2

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output high voltage	Figure 1, Figure 7	V_{DD} – 0.7			V
V_{OL}	Output low voltage	Figure 1, Figure 7			0.6	V

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LVPECL AC Electrical Characteristics[5, 6, 7, 11]

V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output frequency		12		840	MHz
T_R/T_F	LVPECL output rise/fall time	20% – 80%	80	175	350	ps
ODC	Output duty cycle	< 350MHz	48	50	52	%
		≥ 350MHz	45	50	55	%
T_{LOCK}	PLL lock time				20	ms
$T_{jit}(\varnothing)$	RMS phase jitter @ 156.25MHz with clean input signal.	Integration range (12kHz to 20MHz)		251		fs
		Integration range (1.875MHz to 20MHz)		55		fs

Notes:

6. See Figures 4 through 7 for load test circuit examples.
7. All phase noise measurements were taken with an Agilent 5052B phase noise system.

LVDS AC Electrical Characteristics[5, 6, 7, 8]

V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output frequency		12		840	MHz
T_R/T_F	LVDS output rise/fall time	20% – 80%	100	160	400	ps
ODC	Output duty cycle	< 350MHz	48	50	52	%
		≥ 350MHz	45	50	55	%
T_{LOCK}	PLL lock time				20	ms
$T_{jit}(\varnothing)$	RMS phase jitter @ 156.25MHz	Integration range (1.875MHz to 20MHz)		60		fs

HCSL AC Electrical Characteristics[5, 6, 7, 9]

V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output frequency		12		840	MHz
T_R/T_F	Output rise/fall time	20% – 80%	150	300	450	ps
ODC	Output duty cycle	< 350MHz	48	50	52	%
		≥ 350MHz	45	50	55	%
T_{LOCK}	PLL lock time				20	ms
$T_{jit}(\varnothing)$	RMS phase jitter @ 100MHz	Integration range (12kHz to 20MHz)		250		fs

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LVCMOS AC Electrical Characteristics[5, 6, 7, 10]

V_{DD} = V_{DD} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output frequency		12		250	MHz
F_{REF}	REFIN frequency		12		200	MHz
V_{REF}	REFIN amplitude		40% V_{DD}		V_{DD} + 0.6	V_{PP}
T_R/T_F	Output rise/fall time	20% – 80%	100		500	ps
ODC	Output duty cycle		45	50	55	%
T_{LOCK}	PLL lock time				20	ms
$T_{jit}(\varnothing)$	RMS phase jitter @ 125MHz	Integration range: 1.875MHz to 20MHz		55		fs

Notes:

8. Outputs terminated 100Ω between Q and /Q. All unused outputs must be terminated.
9. Output load is 50Ω to V_{SS}.
10. Output load is 50Ω to $V_{DD}/2$.
11. Output load is 50Ω to V_{DD} – 2V

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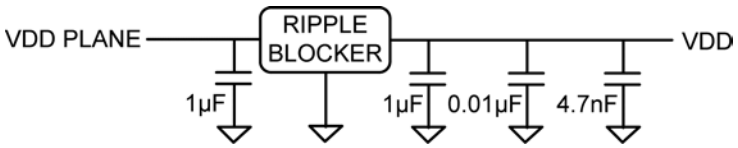
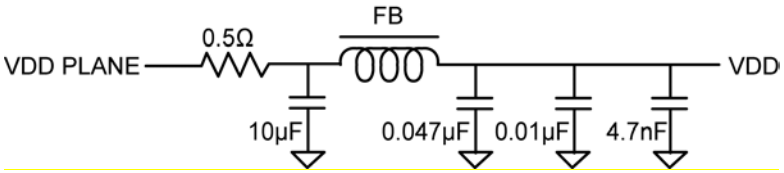
Power Supply Filtering Recommendations

Preferred filter, using Micrel's MIC94300 or MIC94310 Ripple Blocker™:



Alternative, traditional filter, using a ferrite bead:



Application Information

Power Supply Decoupling

Place the smallest value decoupling capacitor (4.7nF above) between the VDD and VSS pins, as close as possible to those pins and at the same side of the PCB as the IC. The shorter the physical path from VDD to capacitor and back from capacitor to VSS, the more effective the decoupling. Use one 4.7nF capacitor for each VDD pin on the PL903xxx.

The impedance value of the ferrite bead (FB) needs to be between 240Ω and 600Ω with a saturation current ≥150mA.

VDDO pins connect directly to the VDD plane. All VDD pins on the PL903xxx connect to VDD after the power supply filter.

Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30Ω resistor in series with the output, as close as possible to the output pin, and start a 50Ω trace on the other side of the resistor.

For differential traces, you can either use a differential design or two separate 50Ω traces. For EMI reasons, it is better to use a differential design.

LVDS can be AC-coupled or DC-coupled to its termination.

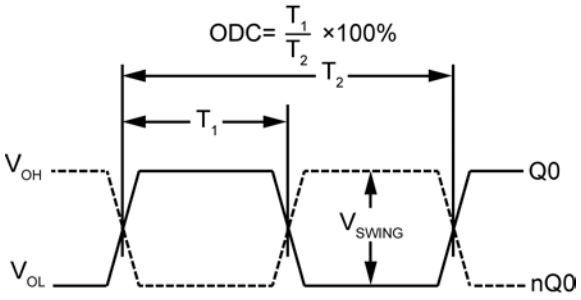


Figure 1. Duty Cycle Timing

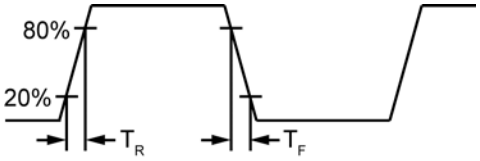


Figure 2. All Outputs Rise/Fall Time

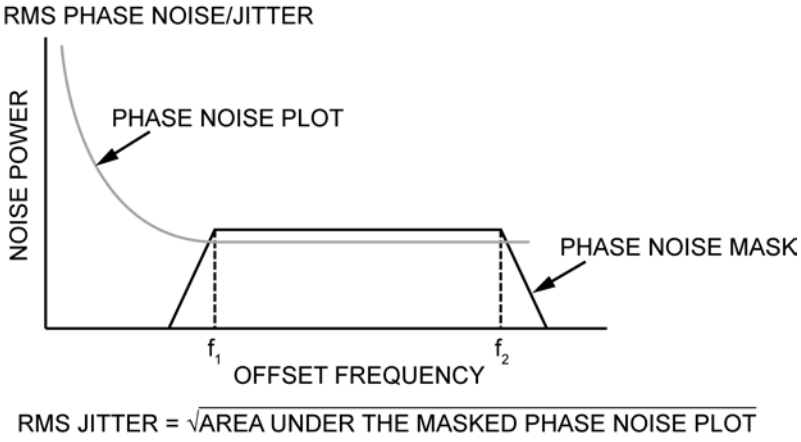


Figure 3. RMS Phase Noise Jitter

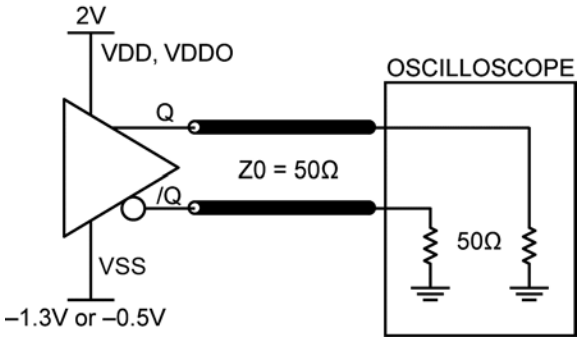


Figure 4. LVPECL Output Load and Test Circuit

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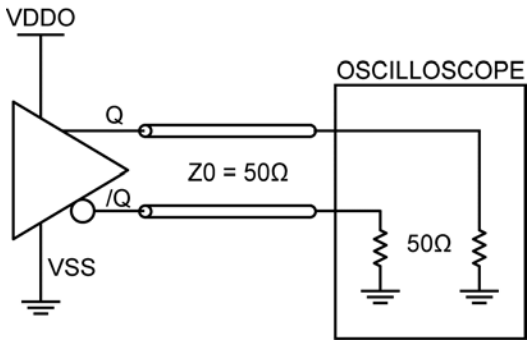


Figure 5. HCSL Output Load and Test Circuit

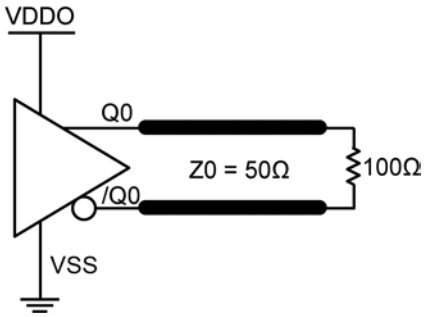


Figure 6. LVDS Output Load and Test Circuit

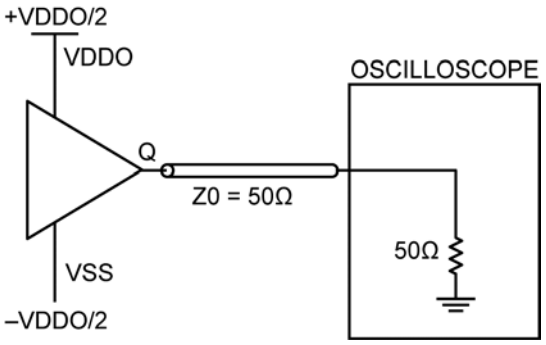
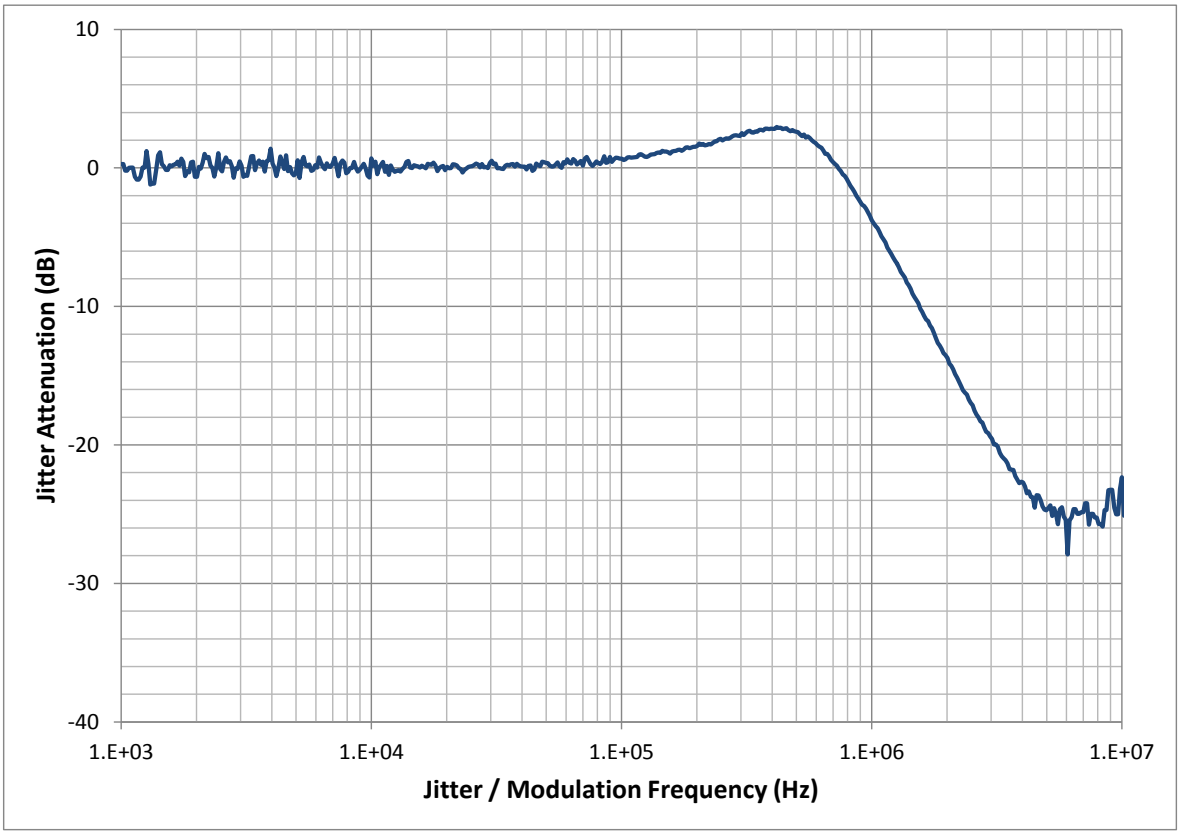


Figure 7. LVCMOS Output Load and Test Circuit

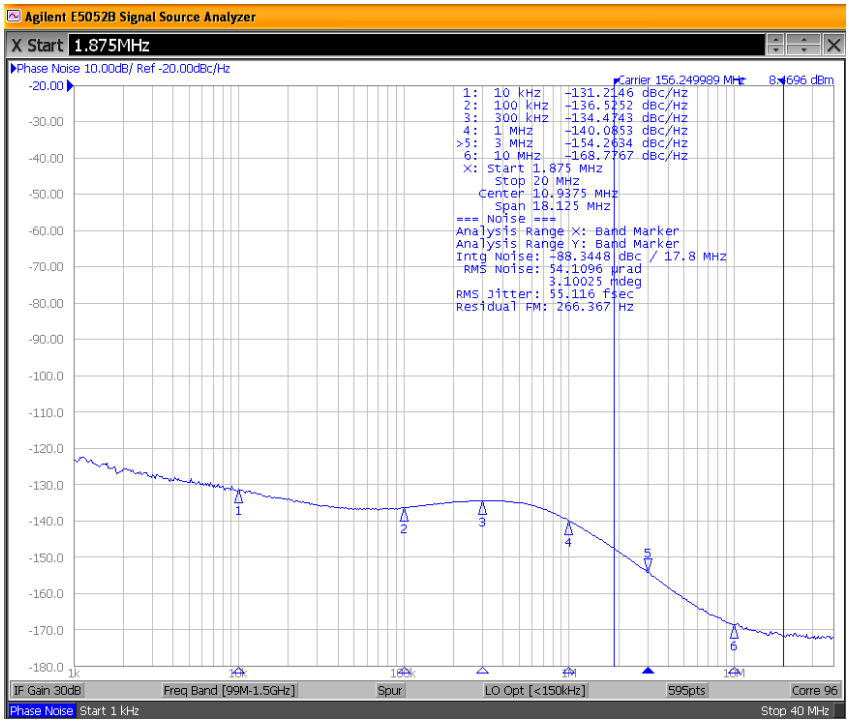
Jitter Attenuation Performance

The jitter attenuating frequency response was measured at 156.25MHz.

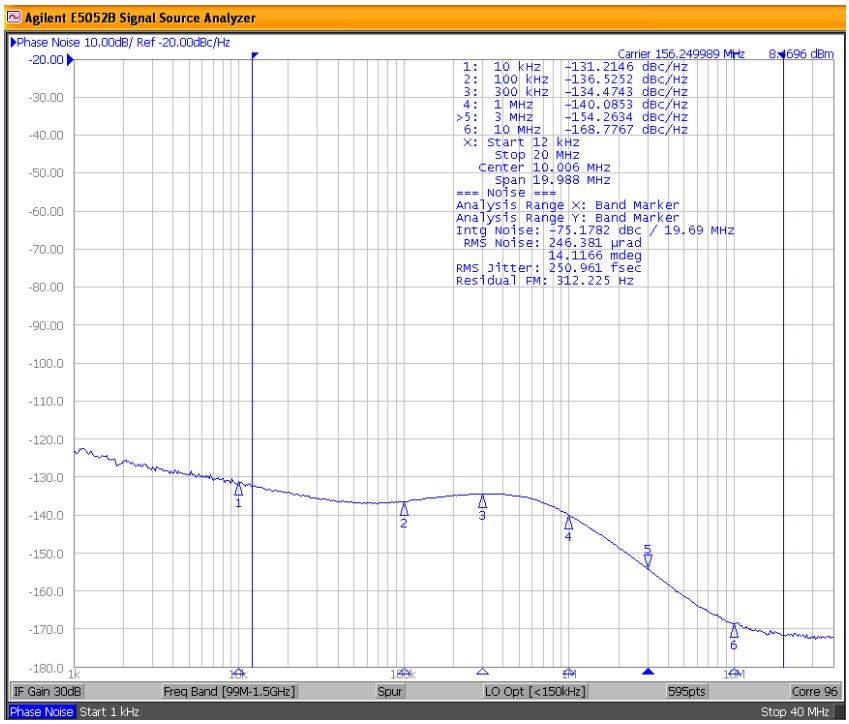


The jitter attenuation works like a low-pass filter for frequency modulated signals or noise. The bandwidth for this low-pass filter is 900kHz with a 12dB/octave slope above 900kHz. At about 6MHz the noise floor of this measurement is reached but in reality, the attenuation continues with the 12dB/octave slope.

Phase noise performance with a clean input clock.

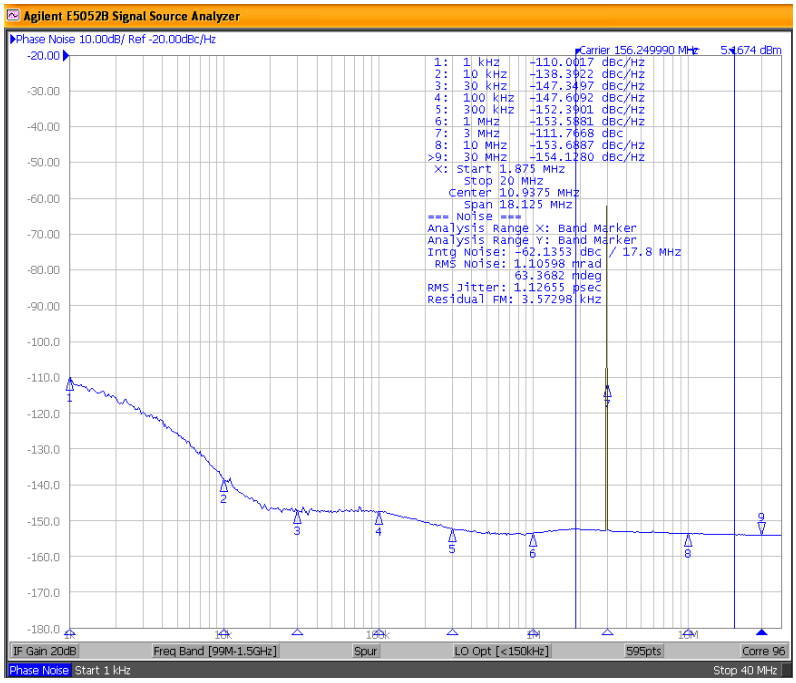


156.25MHz with 55fs$_{RMS}$ of phase jitter for 1.875MHz to 20MHz integration range



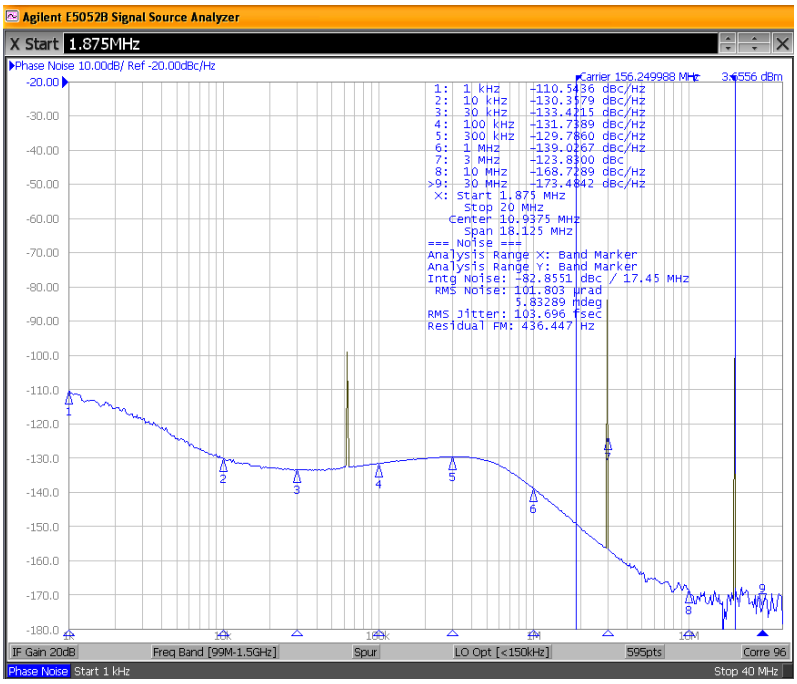
156.25MHz with 251fs$_{RMS}$ of phase jitter for 12kHz to 20MHz integration range

Example 156.25MHz input test clock with bad phase jitter caused by a 3MHz spur.



156.25MHz with 1.1ps$_{RMS}$ of phase jitter for 1.875MHz to 20MHz integration range

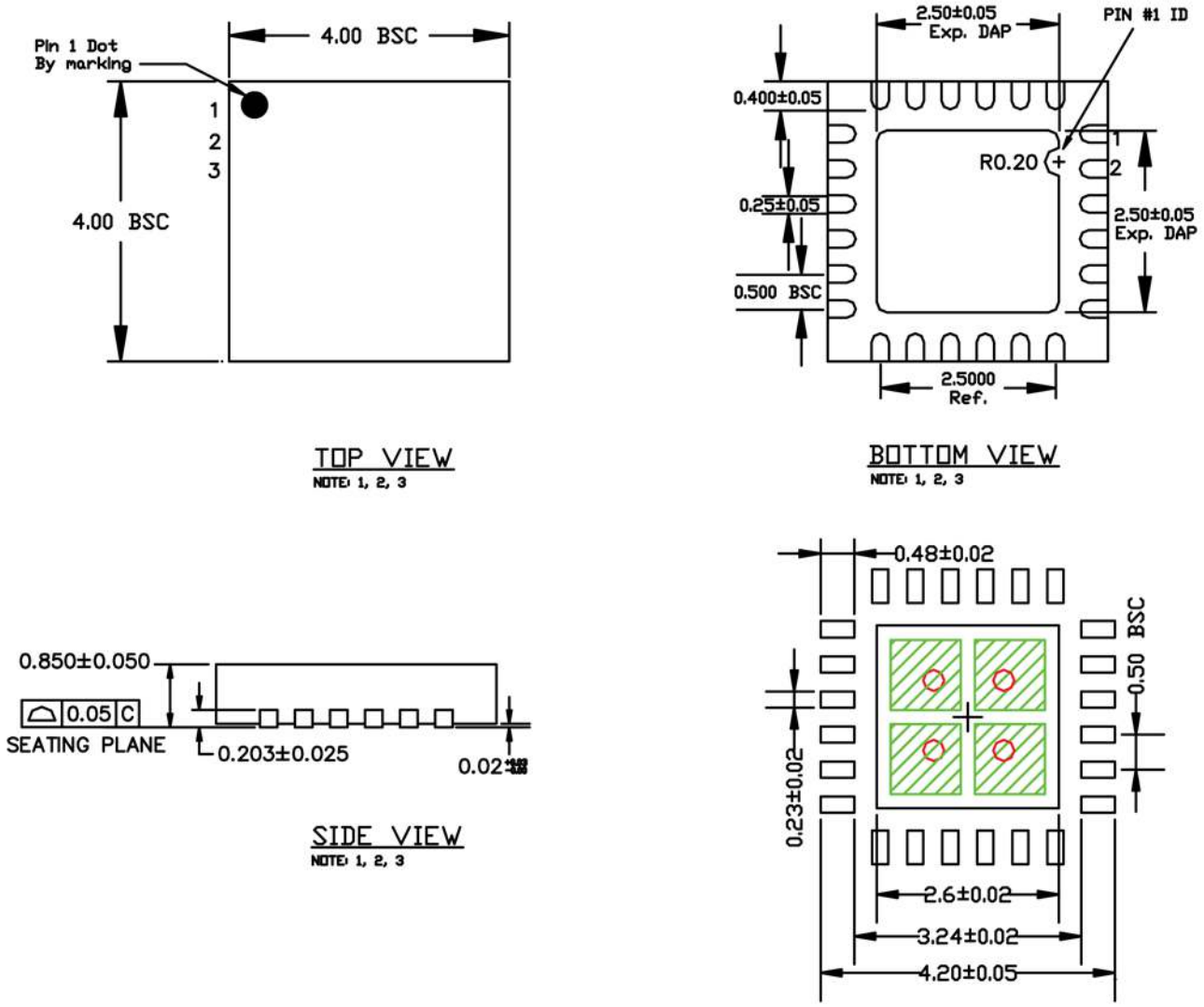
Output clock from PL903xxx.



156.25MHz with 104fs$_{RMS}$ of phase jitter for 1.875MHz to 20MHz integration range

The 3MHz spur is attenuated by 20dB, resulting in a phase jitter reduction from 1.1ps to 0.10ps.

Package Information[12]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) Indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 1.00x1.00 MM IN SIZE, 1.20 MM PITCH.

24-Pin QFN

Note:

12. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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