Description

The AUR9721 is a high efficiency step-down DC-DC voltage converter. The chip operation is optimized by peak-current mode architecture with built-in synchronous power MOS switchers. The oscillator and timing capacitors are all built-in providing an internal switching frequency of 1.5MHz that allows the use of small surface mount inductors and capacitors for portable product implementations.

Additional features including Soft Start (SS), Under Voltage Lock Out (UVLO), Thermal Shutdown Detection (TSD) and short circuit protection are integrated to provide reliable product applications.

The device is available in adjustable output voltage versions ranging from 0.8V to 0.9×V_{IN} when input voltage range is from 2.7V to 5.5V, and is able to deliver up to 2A.

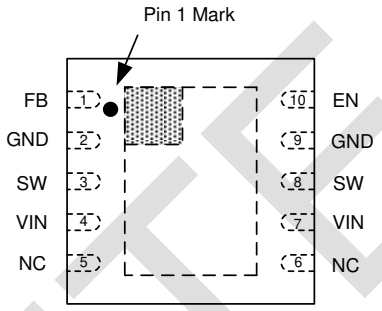
The AUR9721 is available in DFN-3×3-10 package.

Features

- High Efficiency Buck Power Converter
- Output Current: 2A
- Adjustable Output Voltage from 0.8V to 0.9×V_{IN}
- Wide Operating Voltage Range: 2.7V to 5.5V
- Built-in Power Switches for Synchronous Rectification with High Efficiency
- Feedback Voltage Allows Output: 800mV
- 1.5MHz Switching Frequency
- Thermal Shutdown Protection
- Low Drop-out Operation at 90% Duty Cycle
- No Schottky Diode Required
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Pin Assignments

(Top View)

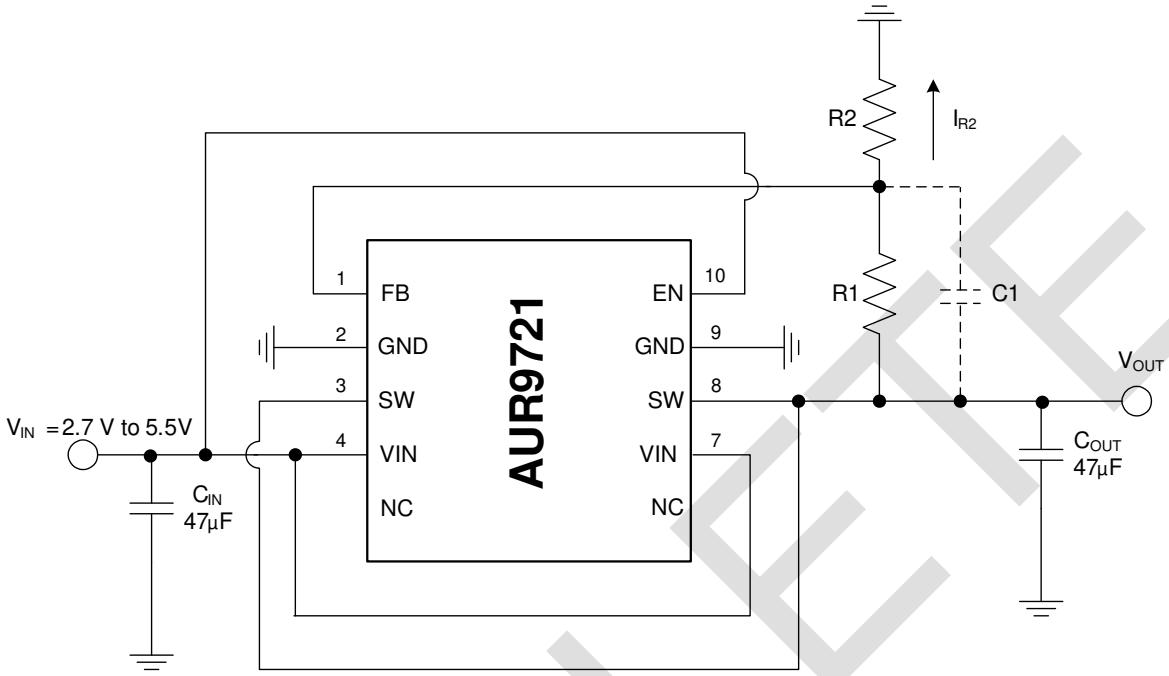


DFN-3×3-10

Applications

- LCD TV
- Set Top Box
- Post DC-DC Voltage Regulation
- PCI Card
- PDA and Notebook Computer

Typical Applications Circuit



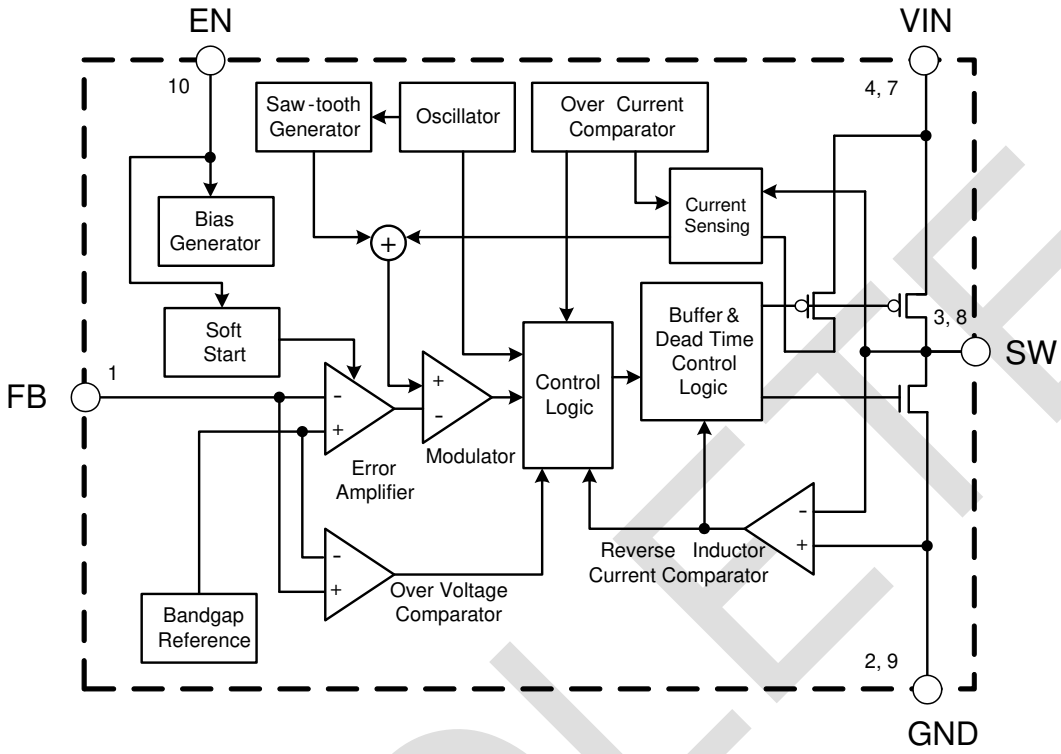
Note 1: $V_{OUT} = V_{FB} \times (1 + \frac{R_1}{R_2})$; V_{FB}=0.8V

When R2=400kΩ to 80kΩ, the I_{R2}=2µA to 10µA, and R1×C1 should be in the range between 3×10^{-6} and 6×10^{-6} for component selection.

Pin Descriptions

Pin Number	Pin Name	Function
1	FB	Feedback voltage from the output of the power supply
2, 9	GND	This pin is the GND reference for the NMOSFET power stage. It must be connected to the system ground
3, 8	SW	Connected to inductor
4, 7	VIN	Power supply input
5, 6	NC	No internal connection
10	EN	Enable signal input, active high

Functional Block Diagram



Absolute Maximum Ratings (Note 2)

Symbol	Parameter	Value	Unit
V_{IN}	Supply Input Voltage	0 to 6.0	V
V_{EN}	Enable Input Voltage	-0.3 to V_{IN}+0.3	V
V_{SW}	Switch Output Voltage	-0.3 to V_{IN}+0.3	V
P_D	Power Dissipation (On 4 Layer PCB, T_A=+25°C)	2.2	W
θ_{JA}	Thermal Resistance (Junction to Ambient, Simulation)	45	°C/W
T_J	Operating Junction Temperature	+150	°C
T_{OP}	Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
V_{HBM}	ESD (Human Body Model)	2000	V
V_{MM}	ESD (Machine Model)	200	V

Note 2: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Recommended Operating Conditions

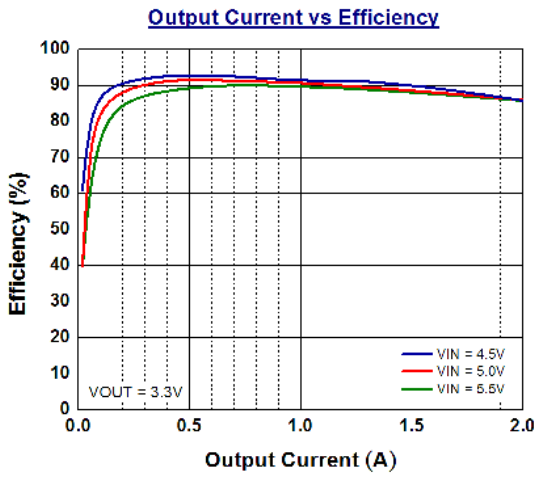
Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Input Voltage	2.7	5.5	V
T_J	Junction Temperature Range	-40	+125	°C
T_A	Ambient Temperature Range	-40	+80	°C

Electrical Characteristics (V_{IN}=V_{EN}=5V, V_{FB}=0.8V, L=1.2μH, C_{IN}=47μF, C_{OUT}=47μF, T_A=+25°C, unless otherwise specified.)

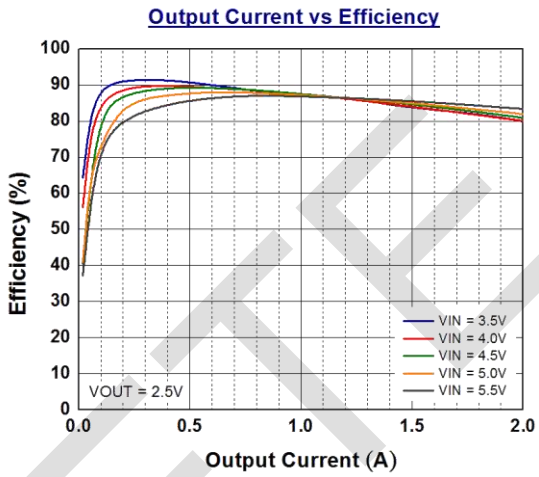
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	_	2.7	_	5.5	V
I_{OFF}	Shutdown Current	V_{EN}=0V	_	0.1	1	μA
I_{ON}	Active Current	V_{FB}=0.95V	_	460	_	μA
V_{FB}	Regulated Feedback Voltage	For Adjustable Output Voltage	0.784	0.8	0.816	V
$\Delta V_{OUT}/V_{OUT}$	Regulated Output Voltage Accuracy	V_{IN}=2.7V to 5.5V, I_{OUT}=10mA to 2A	-3	_	3	%
I_{PK}	Peak Inductor Current	_	2.2	3.2	_	A
f_{OSC}	Oscillator Frequency	_	1.2	1.5	1.8	MHz
$R_{ON(P)}$	PMOSFET R_{ON}	I_{SW}=0.75A	_	100	_	mΩ
$R_{ON(N)}$	NMOSFET R_{ON}	I_{SW}=0.75A	_	100	_	mΩ
I_{EN}	EN Input Current	_	_	2	_	μA
V_{EN_H}	EN High-threshold Input Voltage	_	1.5	_	_	V
V_{EN_L}	EN Low-threshold Input Voltage	_	_	_	0.4	V
t_{SS}	Soft Start Time	_	_	800	_	μs
D_{MAX}	Maximum Duty Cycle	_	90	_	_	%
V_{UVLO}	Under Voltage Lock Out Threshold	Rising	_	2.4	_	V
		Falling	_	2.3	_	
		Hysteresis	_	0.1	_	
T_{SD}	Thermal Shutdown	Hysteresis=+30°C	_	+150	_	°C

Performance Characteristics

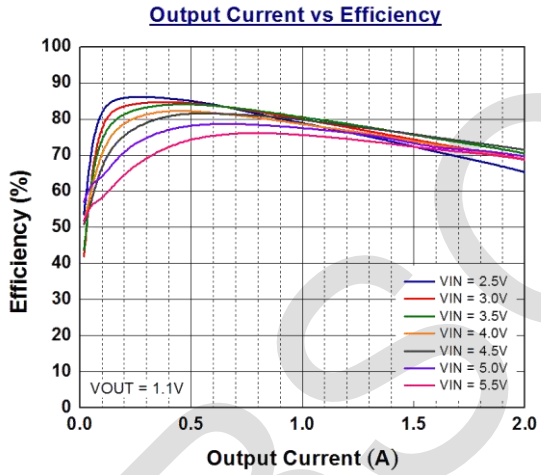
Output Current vs. Efficiency



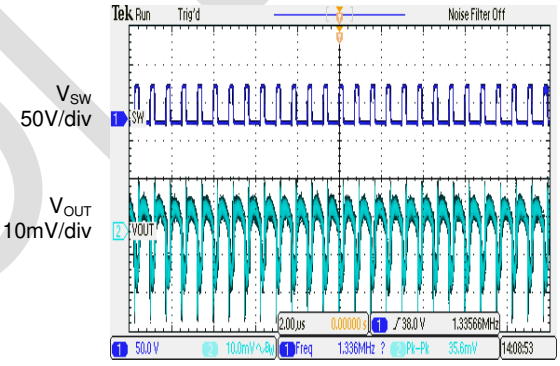
Output Current vs. Efficiency



Output Current vs. Efficiency

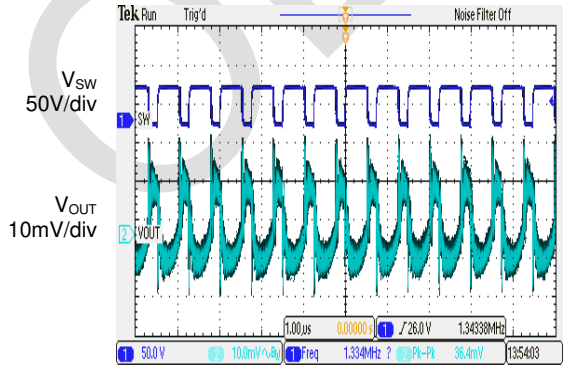


Output Ripple
(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=2A)



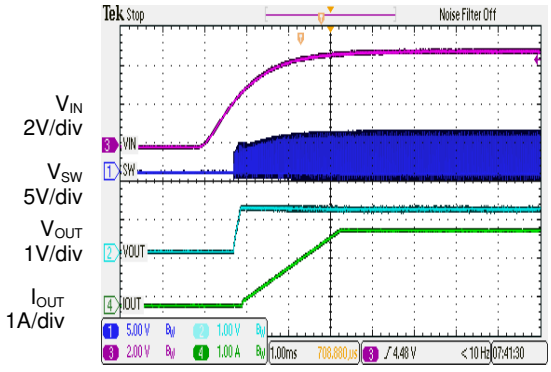
Time 2µs/div

Output Ripple
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=2A)



Time 1µs/div

Power On
(V_{IN}=5V, V_{OUT}=1.2V)



Time 1ms/div

Application Information

The basic AUR9721 application circuit is shown in Figure 11. External components selection is determined by the load current and is critical with the selection of inductor and capacitor values.

1. Inductor Selection

For most applications, the value of inductor is chosen based on the required ripple current with the range of 1.0μH to 6.8μH.

$$\Delta I_L = \frac{1}{f \times L} V_{OUT}(1 - \frac{V_{OUT}}{V_{IN}})$$

The largest ripple current occurs at the highest input voltage. Having a small ripple current reduces the ESR loss in the output capacitor and improves the efficiency. The highest efficiency is realized at low operating frequency with small ripple current. However, larger value inductors will be required. A reasonable starting point for ripple current setting is $\triangle I_L$=40%I_{MAX} . For a maximum ripple current stays below a specified value, the inductor should be chosen according to the following equation:

$$L = [\frac{V_{OUT}}{f \times \Delta I_L(MAX)}][1 - \frac{V_{OUT}}{V_{IN}(MAX)}]$$

The DC current rating of the inductor should be at least equal to the maximum output current plus half the highest ripple current to prevent inductor core saturation. For better efficiency, a lower DC-resistance inductor should be selected.

2. Capacitor Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} = I_{OMAX} \times \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{\frac{1}{2}}}{V_{IN}}$$

It indicates a maximum value at V_{IN}=2V_{OUT}, where I_{RMS}=I_{OUT}/2. This simple worse-case condition is commonly used for design because even significant deviations do not much relieve. The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize output voltage ripple and load step transients, as well as the amount of bulk capacitor that is necessary to ensure that the control loop is stable. The output ripple, $\triangle V_{OUT}$, is determined by:

$$\Delta V_{OUT} \le \Delta I_L[ESR + \frac{1}{8 \times f \times C_{OUT}}]$$

The output ripple is the highest at the maximum input voltage since $\triangle I_L$ increases with input voltage.

3. Load Transient

A switching regulator typically takes several cycles to respond to the load current step. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\triangle I_{LOAD}$×ESR, where ESR is the effective series resistance of output capacitor. $\triangle I_{LOAD}$ also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During the recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

4. Output Voltage Setting

The output voltage of AUR9721 can be adjusted by a resistive divider according to the following formula:

$$V_{OUT} = V_{FB} \times (1 + \frac{R_1}{R_2}) = 0.8V \times (1 + \frac{R_1}{R_2})$$

The resistive divider senses the fraction of the output voltage as shown in Figure 10.

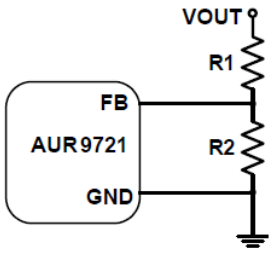


Figure 10. Setting the Output Voltage

Application Information (continued)

5. Short Circuit Protection

When the output node is shorted to GND, as V_{FB} drops under 0.4V, the chip will enter soft-start to protect itself; when short circuit is removed, and V_{FB} rises over 0.4V, AUR9721 will enter normal operation again. If the chip reaches OCP threshold while short circuited, it will enter soft-start cycle until the current drops under OCP threshold.

6. Efficiency Considerations

The efficiency of switching regulator is equal to the output power divided by the input power times 100%. It is usually useful to analyze the individual losses to determine what is limiting efficiency and which change could produce the largest improvement. Efficiency can be expressed as:

Efficiency=100%-L1-L2-…..

Where L1, L2, etc, are the individual losses as a percentage of input power.

Although all dissipative elements in the regulator produce losses, two major sources usually account for most of the power losses: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very light load currents and the I^2R loss dominates the efficiency loss at medium to heavy load currents.

6.1 The V_{IN} quiescent current loss comprises two parts: the DC bias current as given in the electrical characteristics and the internal MOSFET switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each cycle the gate is switched from high to low, then to high again, and the packet of charge, dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the internal DC bias current. In continuous mode,

$$I_{GATE} = f \times (Q_P + Q_N)$$

Where Q_P and Q_N are the gate charge of power PMOSFET and NMOSFET switches. Both the DC bias current and gate charge losses are proportional to the V_{IN} and this effect will be more serious at higher input voltages.

6.2 I^2R losses are calculated from internal switch resistance, R_{SW} and external inductor resistance R_L. In continuous mode, the average output current flowing through the inductor is chopped between power PMOSFET switch and NMOSFET switch. Then, the series resistance looking into the SW pin is a function of both PMOSFET $R_{DS(ON)P}$ and NMOSFET $R_{DS(ON)N}$ resistance and the duty cycle (D):

$$R_{SW} = R_{DS(ON)P} \times D + R_{DS(ON)N} \times (1 - D)$$

Therefore, to obtain the I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of total additional loss.

7. Thermal Characteristics

In most applications, the part does not dissipate much heat due to its high efficiency. However, in some conditions when the part is operating in high ambient temperature with high $R_{DS(ON)}$ resistance and high duty cycles, the heat dissipated may exceed the maximum junction temperature. To avoid the part from exceeding maximum junction temperature, the user should do some thermal analysis. The maximum power dissipation depends on the layout of PCB, the thermal resistance of IC package, the rate of surrounding airflow and the temperature difference between junction and ambient.

8. PC Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to optimize the performance of AUR9721.

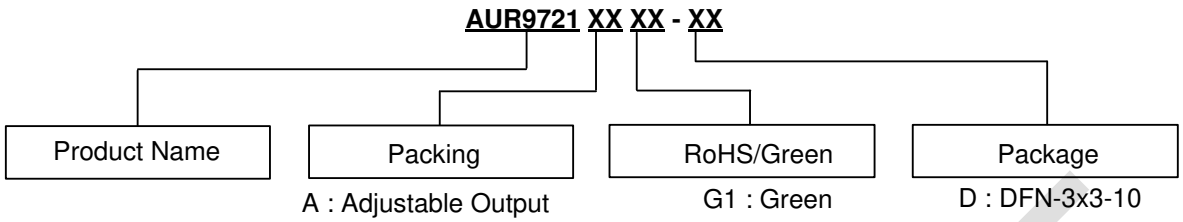
1. The power traces, including the GND trace, the SW trace and the VIN trace should be kept direct, short and wide.

2. Put the input capacitor as close as possible to the VIN and GND pins.

3. The FB pin should be connected directly to the feedback resistor divider.

4. Keep the switching node SW away from the sensitive FB pin and the node should be kept small area.

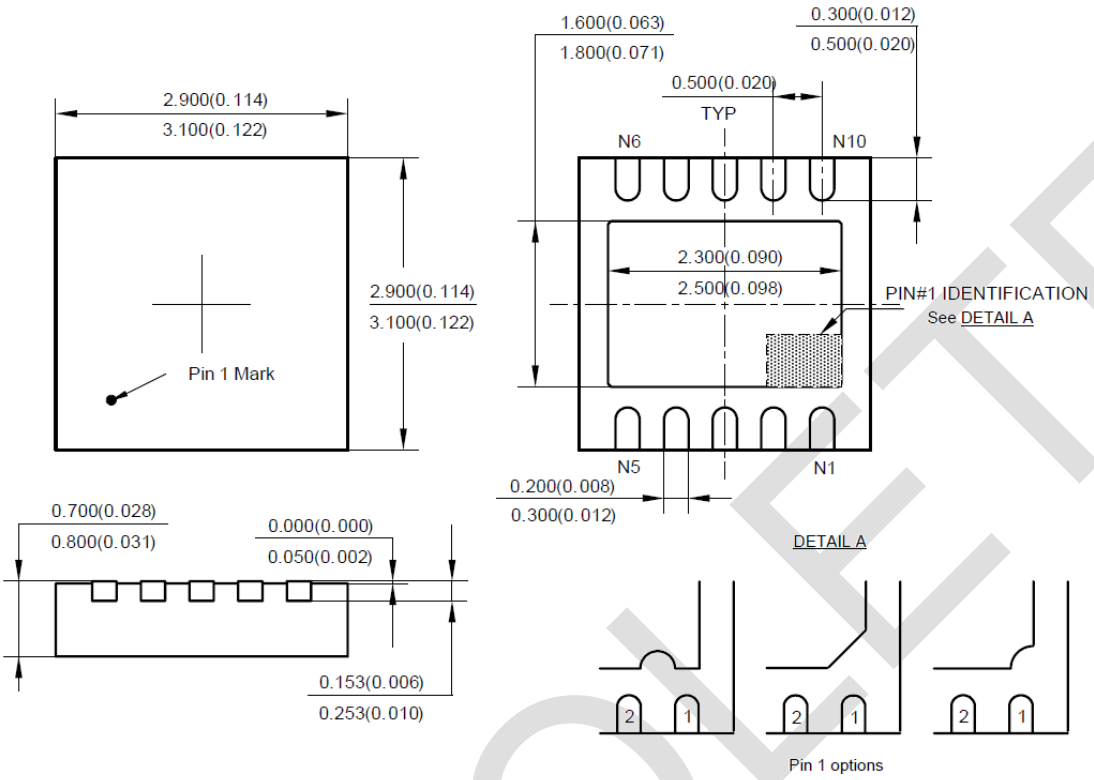
Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing
DFN-3×3-10	-40 to +80°C	AUR9721AGD	9721A	Tape & Reel

Package Outline Dimensions (All dimensions in mm(inch).)

(1) Package Type: DFN-3×3-10



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