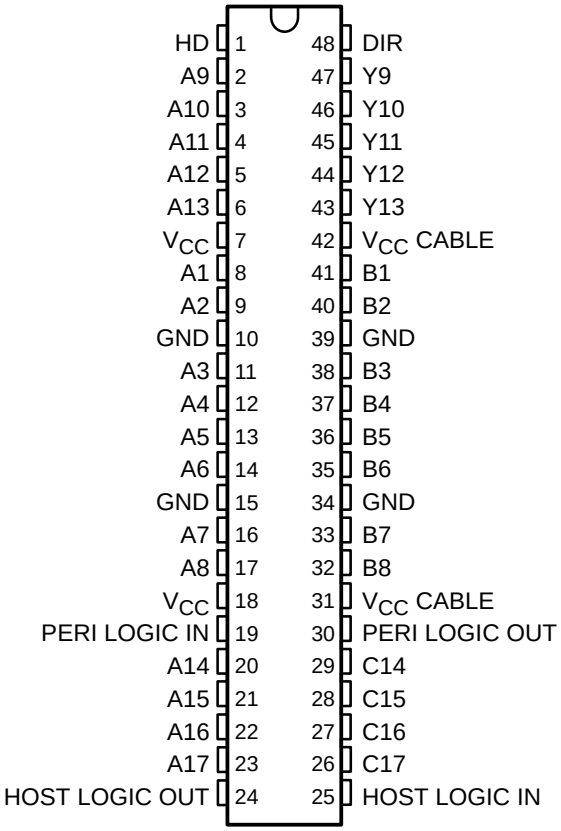
- **4.5-V to 5.5-V V_{CC} Operation**
- **1.4-kΩ Pullup Resistors Integrated on All Open-Drain Outputs Eliminate the Need for Discrete Resistors**
- **Designed for IEEE Std 1284-I (Level-1 Type) and IEEE Std 1284-II (Level-2 Type) Electrical Specifications**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC 17**
- **ESD Protection Exceeds JESD 22**
  - **4000-V Human-Body Model (A114-A)**
  - **300-V Machine Model (A115-A)**
  - **2000-V Charged-Device Model (C101)**

DGG OR DL PACKAGE
(TOP VIEW)



description/ordering information

The SN74LV161284 is designed for 4.5-V to 5.5-V V_{CC} operation. This device provides asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

This device has eight bidirectional bits; data can flow in the A-to-B direction when DIR is high, and in the B-to-A direction when DIR is low. This device also has five drivers, which drive the cable side, and four receivers. The SN74LV161284 has one receiver dedicated to the HOST LOGIC line and a driver to drive the PERI LOGIC line.

The output drive mode is determined by the high-drive (HD) control pin. When HD is high, the B, Y, and PERI LOGIC OUT outputs are in a totem-pole configuration, and in an open-drain configuration when HD is low. This meets the drive requirements as specified in the IEEE Std 1284-I (level-1 type) and IEEE Std 1284-II (level-2 type) parallel peripheral-interface specifications. Except for HOST LOGIC IN and PERI LOGIC OUT, all cable-side pins have a 1.4-kΩ integrated pullup resistor. The pullup resistor is switched off if the associated output driver is in the low state or if the output voltage is above V_{CC} CABLE. If V_{CC} CABLE is off, PERI LOGIC OUT is set to low.

The device has two supply voltages. V_{CC} is designed for 4.5-V to 5.5-V operation. V_{CC} CABLE supplies the output buffers of the cable side only and is designed for 4.5-V to 5.5-V operation.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74LV161284DL	LV161284
		Tape and reel	SN74LV161284DLR	
	TSSOP – DGG	Tape and reel	SN74LV161284DGGR	LV161284

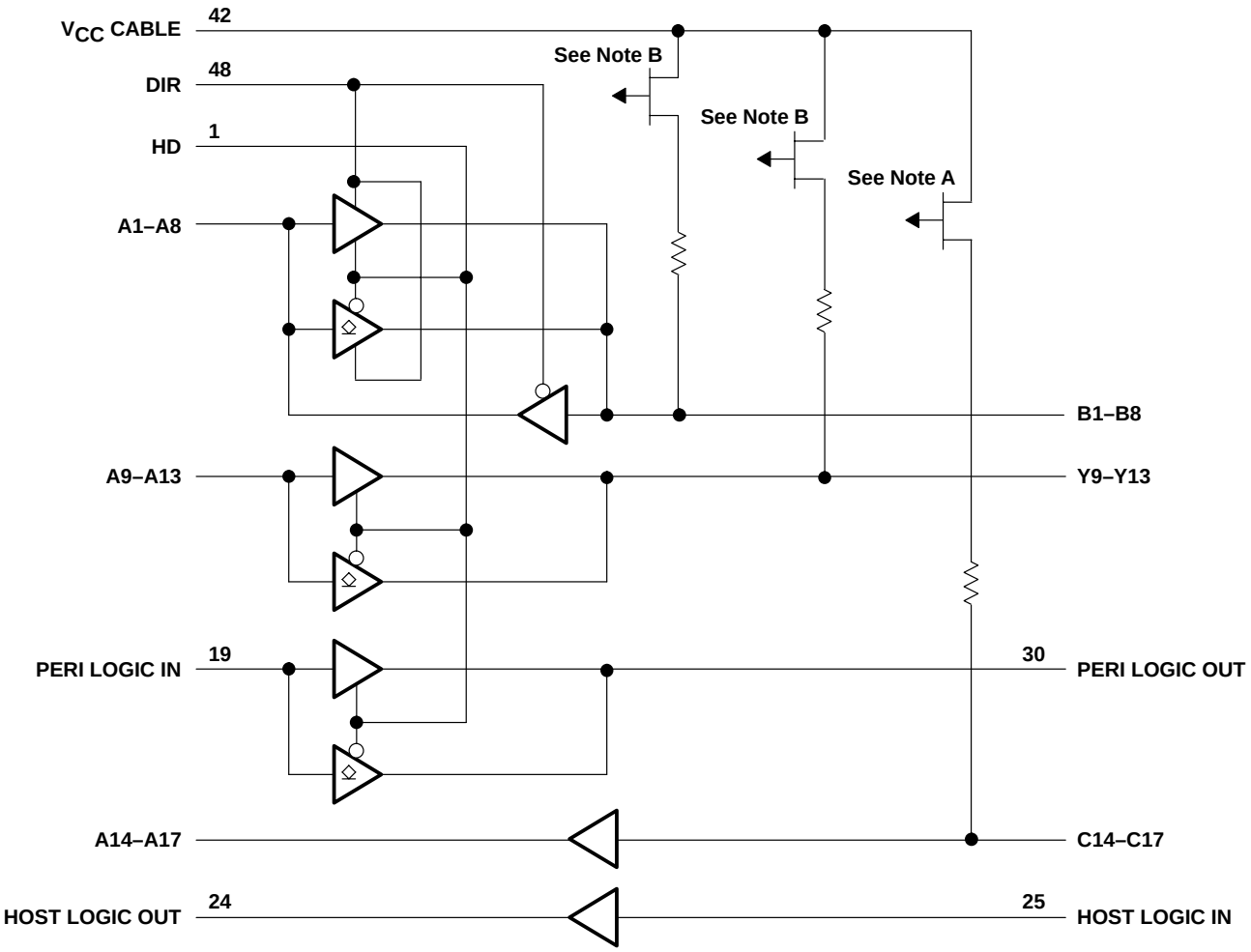
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLE

INPUTS		OUTPUT	MODE
DIR	HD		
L	L	Open drain	A9–A13 to Y9–Y13 and PERI LOGIC IN to PERI LOGIC OUT
		Totem pole	B1–B8 to A1–A8 and C14–C17 to A14–A17
L	H	Totem pole	B1–B8 to A1–A8, A9–A13 to Y9–Y13, PERI LOGIC IN to PERI LOGIC OUT, and C14–C17 to A14–A17
H	L	Open drain	A1–A8 to B1–B8, A9–A13 to Y9–Y13, and PERI LOGIC IN to PERI LOGIC OUT
		Totem pole	C14–C17 to A14–A17
H	H	Totem pole	A1–A8 to B1–B8, A9–A13 to Y9–Y13, C14–C17 to A14–A17, and PERI LOGIC IN to PERI LOGIC OUT

logic diagram (positive logic)



NOTES: A. The PMOS prevents backdriving current from the signal pins to V_{CC} CABLE when V_{CC} CABLE is open or at GND.
B. The PMOS prevents backdriving current from the signal pins to V_{CC} CABLE when V_{CC} CABLE is open or at GND. The PMOS is turned off when the associated driver is in the low state.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range: V_{CC} CABLE . . . . . –0.5 V to 7 V
V_{CC} . . . . . –0.5 V to 7 V
Input and output voltage range, V_I and V_O: Cable side (see Notes 1 and 2) . . . . . –2 V to 7 V
Peripheral side (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . . ±200 mA
Output high sink current, I_{SK} (V_O = 5.5 V and V_{CC} CABLE = 5.5 V) . . . . . 65 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . . 70°C/W
DL package . . . . . 63°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The ac input voltage pulse duration is limited to 40 ns if the amplitude is more negative than –0.5 V.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC} CABLE	Supply voltage for the cable side, V_{CC} CABLE ≥ V_{CC}		4.5	5.5	V
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage	A, DIR, HD, and PERI LOGIC IN	$V_{CC} \times 0.7$		V
		B	2		
		C14–C17	2.3		
		HOST LOGIC IN	2.6		
V_{IL}	Low-level input voltage	A, DIR, HD, and PERI LOGIC IN		$V_{CC} \times 0.3$	V
		B		0.8	
		C14–C17		0.8	
		HOST LOGIC IN		1.6	
V_I	Input voltage	Peripheral side	0	V_{CC}	V
		Cable side	0	5.5	
V_O	Open-drain output voltage	B, Y, and PERI LOGIC OUT (HD low)	0	5.5	V
I_{OH}	High-level output current	B and Y outputs (HD high)		–14	mA
		A outputs and HOST LOGIC OUT		–8	
		PERI LOGIC OUT		–0.5	
I_{OL}	Low-level output current	B and Y outputs		14	mA
		A outputs and HOST LOGIC OUT		8	
		PERI LOGIC OUT		84	
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range, V_{CC} CABLE = V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP†	MAX	UNIT
ΔV_t	Input hysteresis	$V_{thH} – V_{thL}$ for all inputs except the C inputs and HOST LOGIC IN	4.5 V to 5.5 V	0.4			V
		$V_{thH} – V_{thL}$ for the HOST LOGIC IN	5 V	0.3			
		$V_{thH} – V_{thL}$ for the C inputs		0.8			
V_{IK}	Input clamp diode voltage	I_I = –18 mA	3 V			–1.2	V
V_{OH}	B and Y outputs	I_{OH} = –14 mA (HD high)	4.5 V	3.73			V
	A outputs and HOST LOGIC OUT	I_{OH} = –8 mA (HD high)		3.8			
		I_{OH} = –50 μA		4.4			
	PERI LOGIC OUT	I_{OH} = –0.5 mA	4.5 V	4.45			
V_{OL}	B and Y outputs	I_{OL} = 14 mA	4.5 V			0.77	V
	A outputs and HOST LOGIC OUT	I_{OL} = 50 μA				0.1	
		I_{OL} = 8 mA				0.44	
	PERI LOGIC OUT	I_{OL} = 84 mA				0.7	
I_I	C inputs	$V_I = V_{CC}$	5.5 V			350	μA
		V_I = GND (pullup resistors)				–5	mA
	B and C inputs	V_I = 5.5 V or GND	0 to 5.5 V			±5	mA
	All inputs except the B or C inputs	$V_I = V_{CC}$ or GND	5.5 V			±1	μA
I_{OZ}	B outputs	$V_O = V_{CC}$	5.5 V			350	μA
		V_O = GND (pullup resistors)	5.5 V			–5	mA
	A1–A8	$V_O = V_{CC}$ or GND	5.5 V			±20	μA
	Open-drain Y outputs	V_O = GND (pullup resistors)	5.5 V			–5	mA
I_{OZPU}	B and Y outputs	V_O = 5.5 V	0 to 2 V			350	μA
		V_O = GND				–5	mA
I_{OZPD}	B and Y outputs	V_O = 5.5 V	2 V to 0			350	μA
		V_O = GND				–5	mA
I_{off}	Power-down output leakage, Outputs B1 – B8, Y9 – Y13, and PERI LOGIC OUT	V_O = 5.5 V	0			100	μA
	Power-down input leakage, Inputs C14 – C17 and HOST LOGIC IN	V_I = 5.5 V				100	
I_{CC}‡		$V_I = V_{CC}$, I_O = 0	5.5 V			0.8	mA
		V_I = GND (12 × pullup)				70	
C_i	All inputs	$V_I = V_{CC}$ or GND	5 V		5		pF
C_{io}	I/O ports	$V_O = V_{CC}$ or GND	5 V		9		pF
Z_O	Cable side	I_{OH} = –35 mA	5 V		45		Ω
R pullup	Cable side	V_O = 0 V (in Hi Z)	5 V	1.15		1.65	kΩ

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ A maximum current of 170 μA per pin is added to I_{CC} if the pullup resistor pin is above V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 and 2)

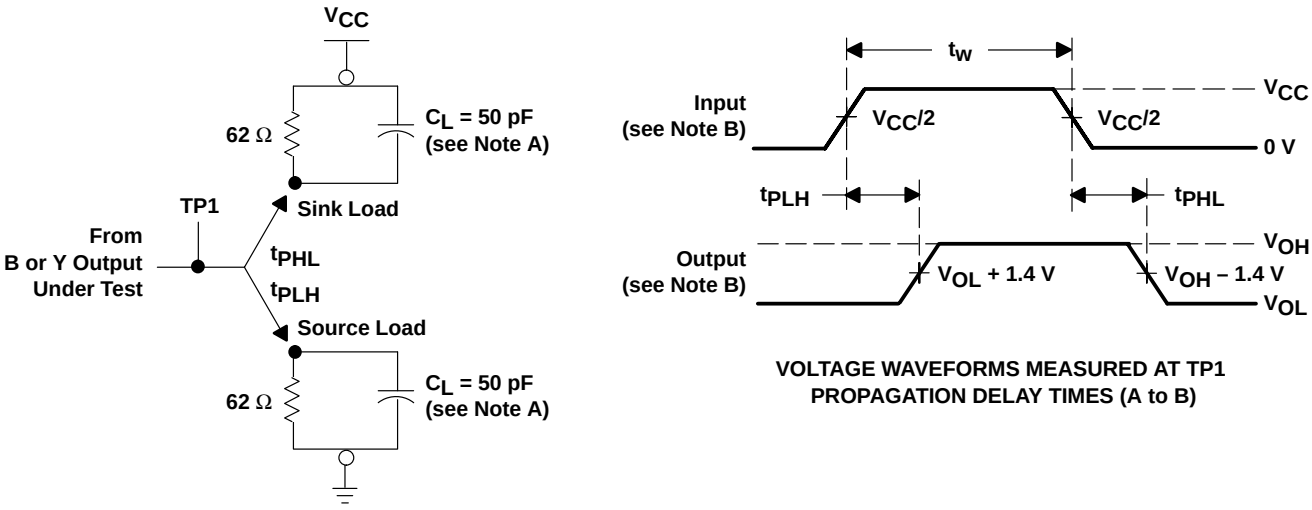
PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{PLH}	Totem pole	A or B	B or A	2		30	ns
t_{PHL}				2		30	
t_{PLH}	Totem pole	A	Y	2		30	ns
t_{PHL}				2		30	
t_{PLH}	Totem pole	C	A	2		30	ns
t_{PHL}				2		30	
t_{PLH}	Totem pole	PERI LOGIC IN	PERI LOGIC OUT	2		30	ns
t_{PHL}				2		30	
t_{PLH}	Totem pole	HOST LOGIC IN	HOST LOGIC OUT	2		30	ns
t_{PHL}				2		30	
t_{slew}	Totem pole	Cable-side outputs		0.05		0.95	V/ns
t_{en}	Totem pole	HD	B, Y, and PERI LOGIC OUT	2		25	ns
t_{dis}	Totem pole	HD	B, Y, and PERI LOGIC OUT	2		25	ns
t_{en}–t_{dis}						10	ns
t_{en}		DIR	A	2		25	ns
t_{dis}		DIR	A	2		15	ns
			B	2		25	
t_r, t_f	Open drain	A	B or Y			30	ns
$t_{sk(o)}$		A or B	B or A		1	6	ns

† Skew is measured at 1/2 (V_{OH} + V_{OL}) for signals switching in the same direction.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

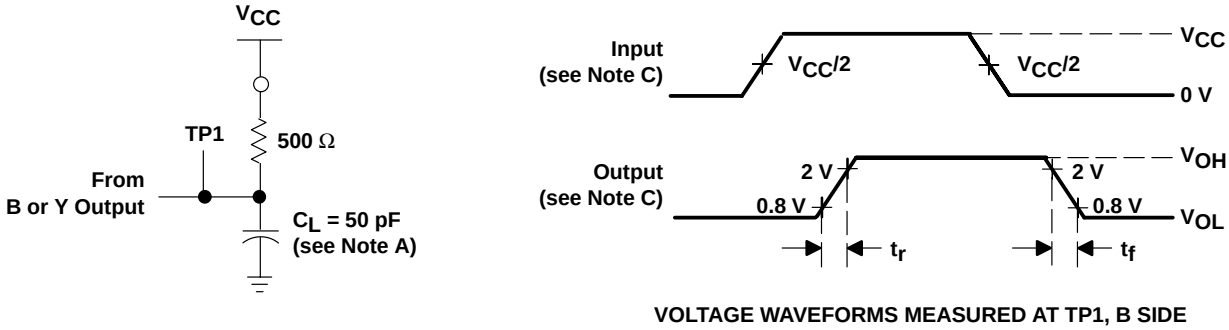
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 0, f = 10 MHz	25	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS MEASURED AT TP1
PROPAGATION DELAY TIMES (A to B)

SLEW RATE A-TO-B OR A-TO-Y LOAD (Totem Pole)



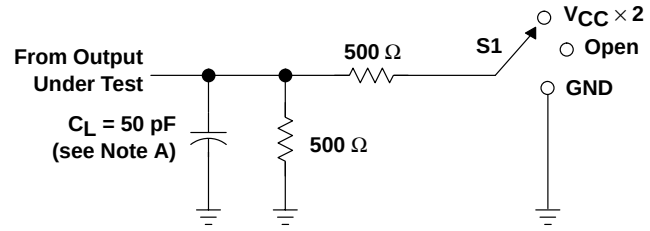
VOLTAGE WAVEFORMS MEASURED AT TP1, B SIDE

A-TO-B LOAD OR A-TO-Y LOAD (Open Drain)

NOTES: A. C_L includes probe and jig capacitance.
B. Input rise and fall times are 3 ns, 150 ns < pulse duration < 10 μs for both low-to-high and high-to-low transitions. Slew rate is measured between 0.4 V and 1.9 V for the rising edge and between 95% V_{CC} and 50% V_{CC} for the falling edge.
C. Input rise and fall times are 3 ns. Rise and fall times (open drain) < 120 ns.
D. The outputs are measured one at a time with one transition per measurement.

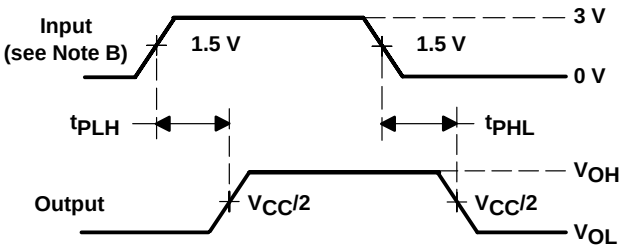
Figure 1. Load Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

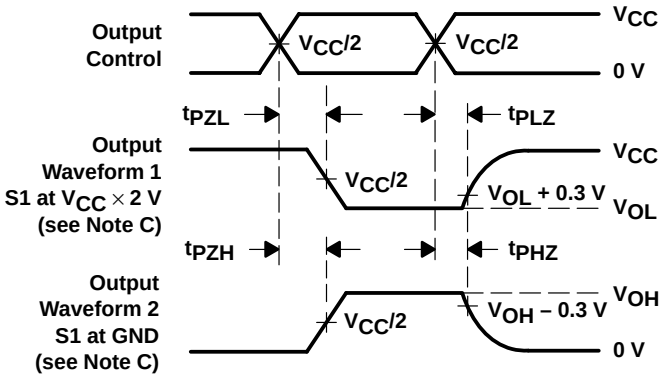


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$V_{CC} \times 2$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

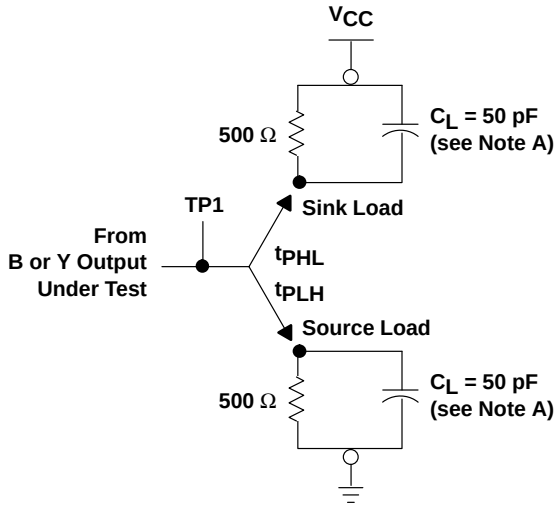


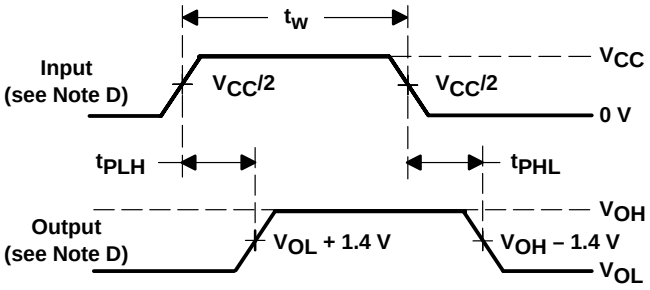
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

B-TO-A LOAD (Totem Pole)





VOLTAGE WAVEFORMS MEASURED AT TP1
PROPAGATION DELAY TIMES (A to B)

A-TO-B LOAD OR A-TO-Y LOAD (Totem Pole)

NOTES: A. C_L includes probe and jig capacitance.
B. Input rise and fall times are 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. Input rise and fall times are 3 ns, 150 ns < pulse duration < 10 μs for both low-to-high and high-to-low transitions.
E. The outputs are measured one at a time with one transition per measurement.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV161284DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161284	Samples
SN74LV161284DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161284	Samples
SN74LV161284DLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161284	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

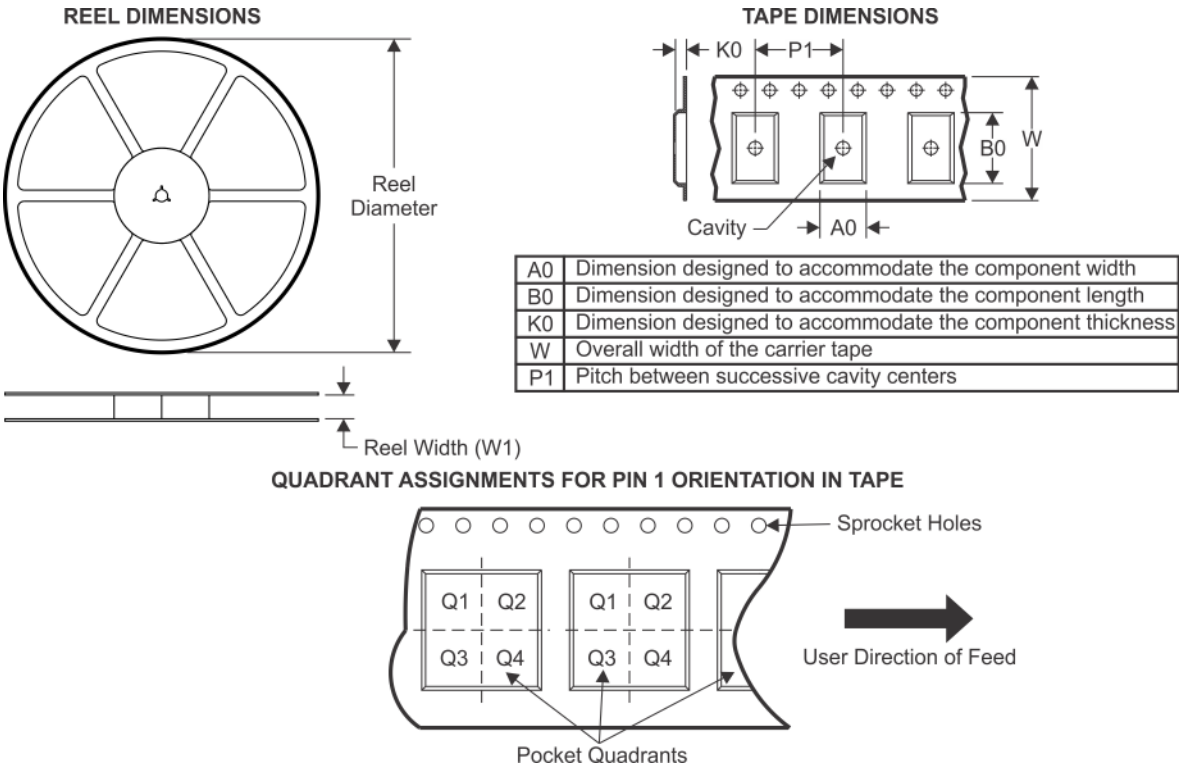
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

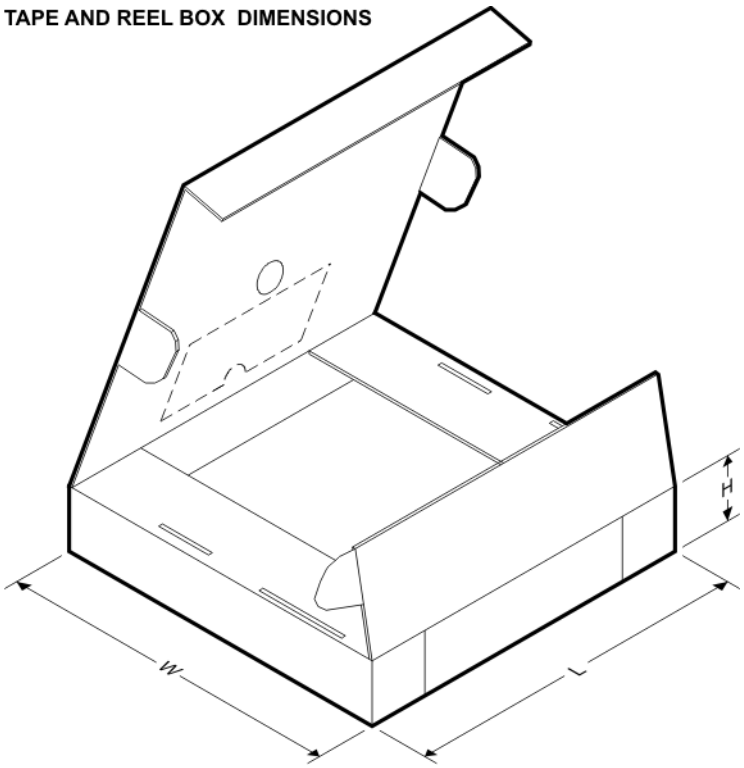


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV161284DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LV161284DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

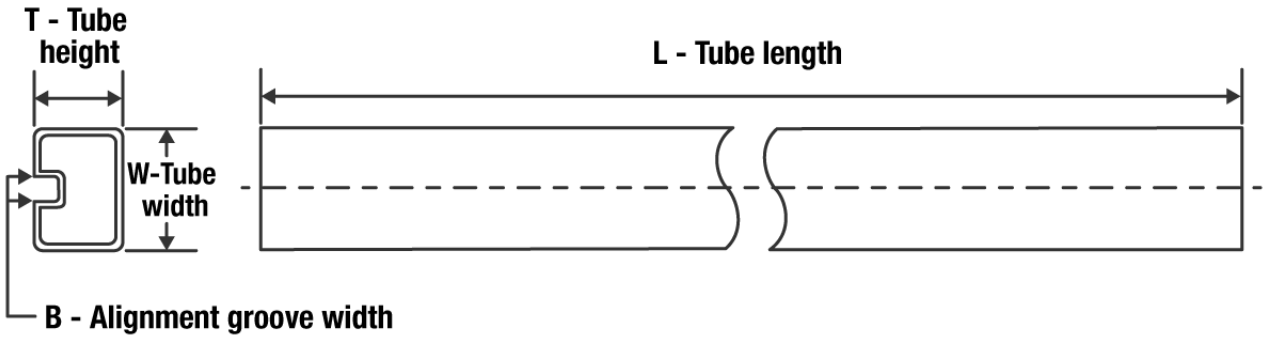
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV161284DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LV161284DLR	SSOP	DL	48	1000	367.0	367.0	55.0

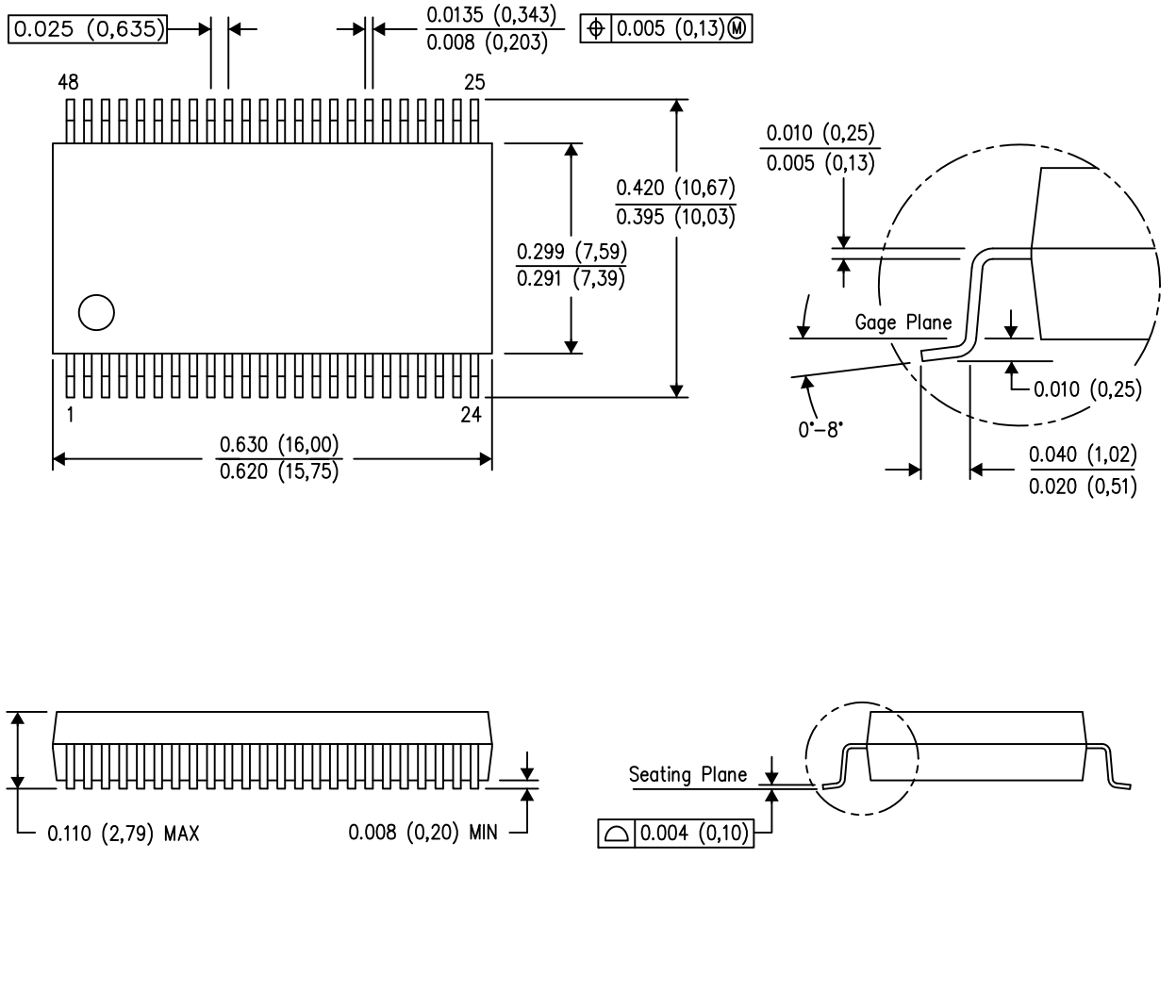
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LV161284DL	DL	SSOP	48	25	473.7	14.24	5110	7.87

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

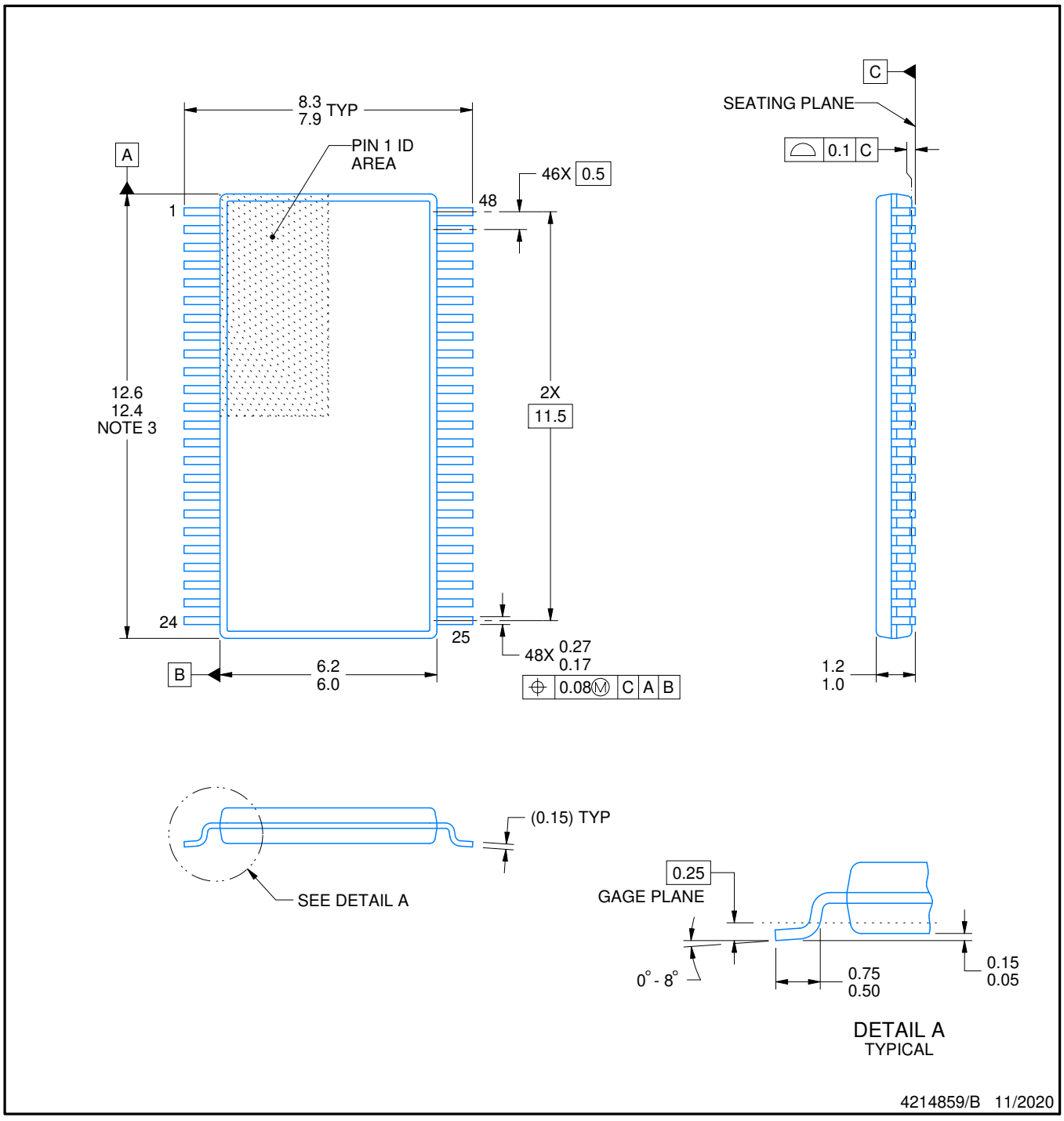
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DGG0048A

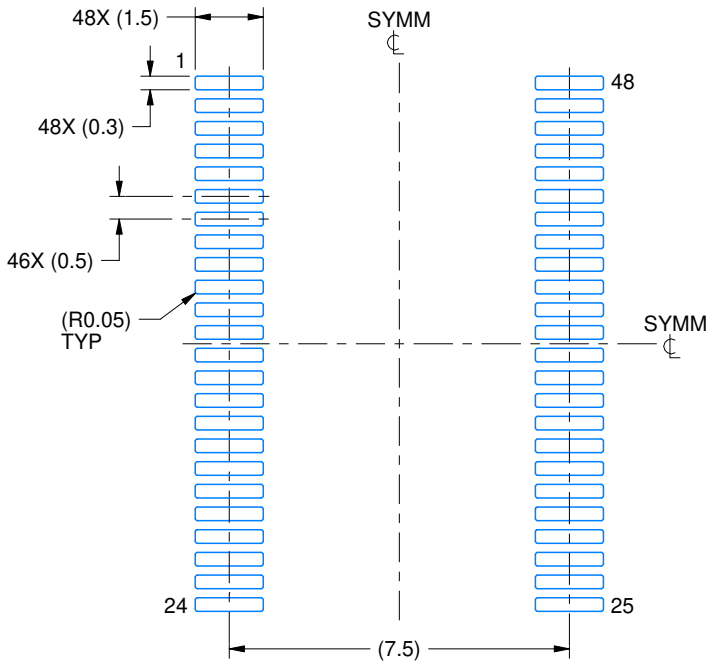
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

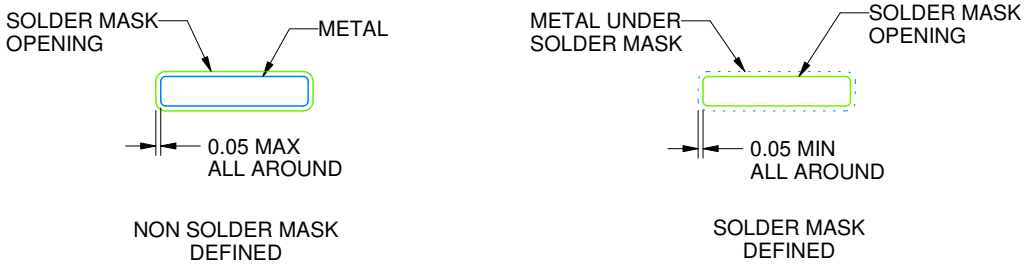


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

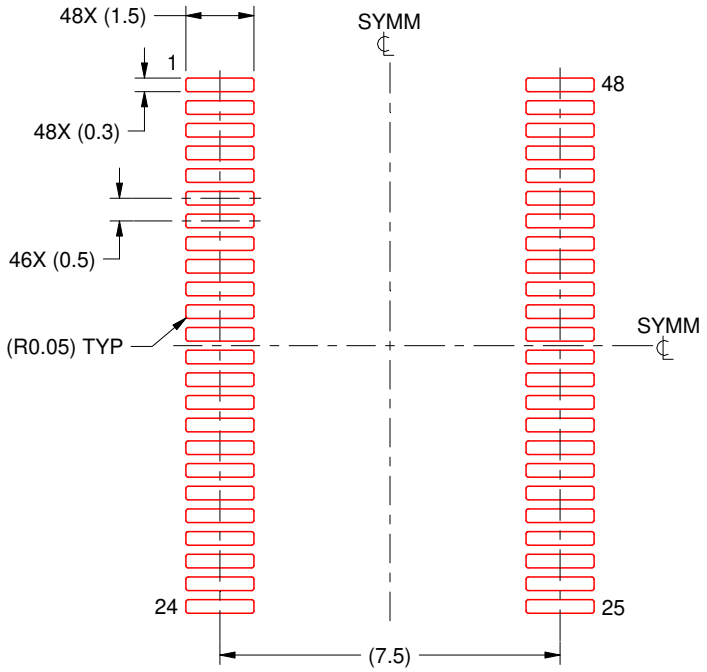


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

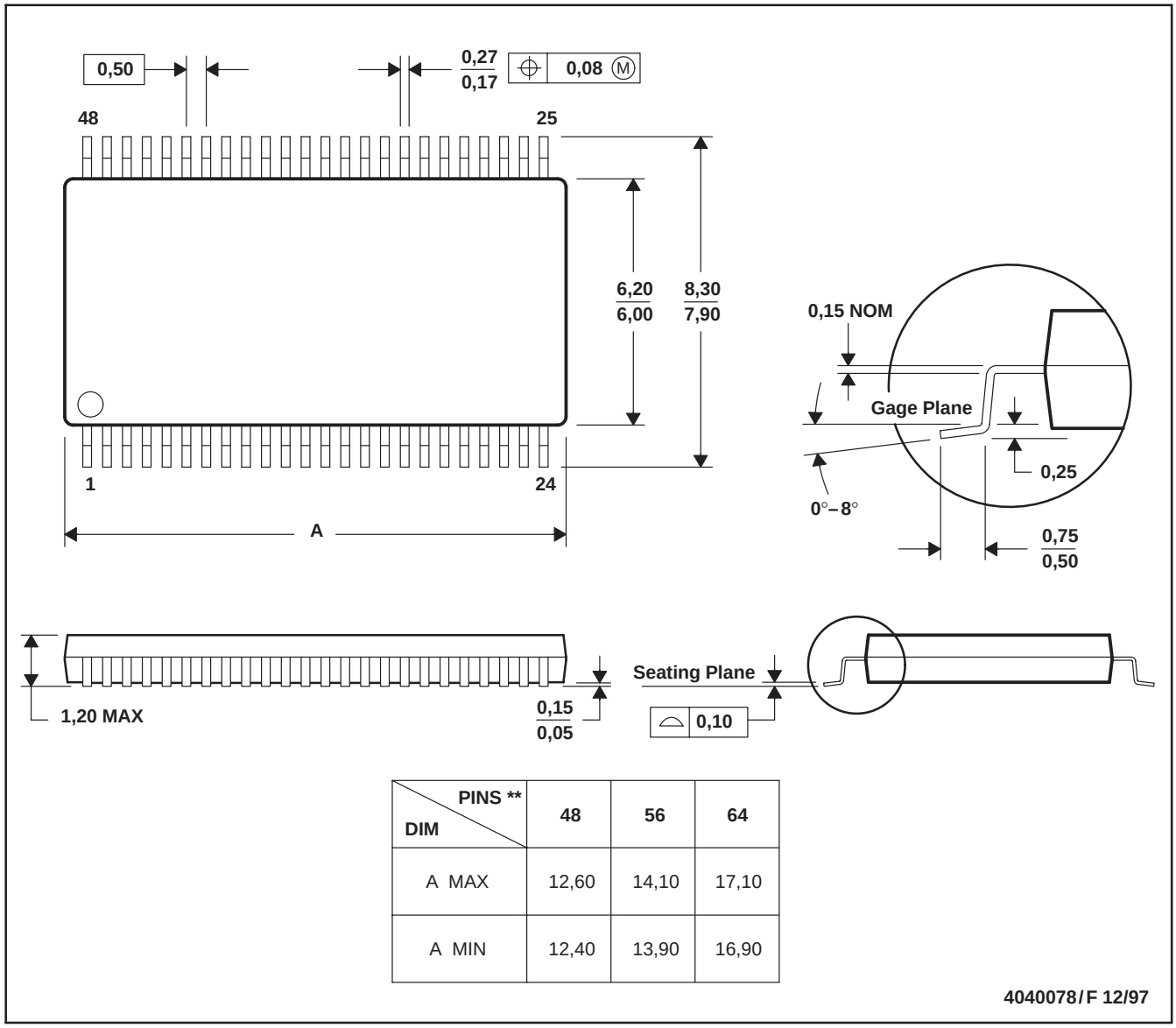
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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