

## Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

## Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

# SN74LS377

## Octal D Flip-Flop with Enable

The SN74LS377 is an 8-bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable.

- 8-Bit High Speed Parallel Registers
- Positive Edge-Triggered D-Type Flip Flops
- Fully Buffered Common Clock and Enable Inputs
- True and Complement Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

### GUARANTEED OPERATING RANGES

| Symbol          | Parameter                           | Min  | Typ | Max  | Unit |
|-----------------|-------------------------------------|------|-----|------|------|
| V <sub>CC</sub> | Supply Voltage                      | 4.75 | 5.0 | 5.25 | V    |
| T <sub>A</sub>  | Operating Ambient Temperature Range | 0    | 25  | 70   | °C   |
| I <sub>OH</sub> | Output Current - High               |      |     | -0.4 | mA   |
| I <sub>OL</sub> | Output Current - Low                |      |     | 8.0  | mA   |

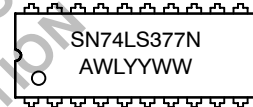
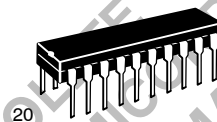


**ON Semiconductor**

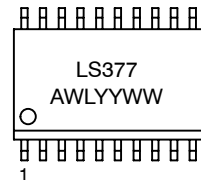
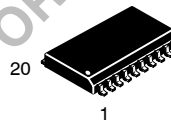
<http://onsemi.com>

**LOW  
POWER  
SCHOTTKY**

### MARKING DIAGRAMS



**PDIP-20  
N SUFFIX  
CASE 738**



**SOIC-20  
DW SUFFIX  
CASE 751D**

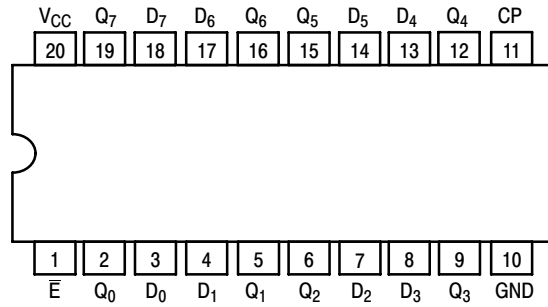
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

| Device        | Package   | Shipping         |
|---------------|-----------|------------------|
| SN74LS377N    | PDIP-20   | 1440 Units/Box   |
| SN74LS377DW   | SOIC-WIDE | 38 Units/Rail    |
| SN74LS377DWR2 | SOIC-WIDE | 2500/Tape & Reel |

# SN74LS377

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

|                         |                                      |
|-------------------------|--------------------------------------|
| $\bar{E}$               | Enable (Active LOW) Input            |
| $D_0 - D_3$             | Data Inputs                          |
| CP                      | Clock (Active HIGH Going Edge) Input |
| $Q_0 - Q_3$             | True Outputs                         |
| $\bar{Q}_0 - \bar{Q}_3$ | Complemented Outputs                 |

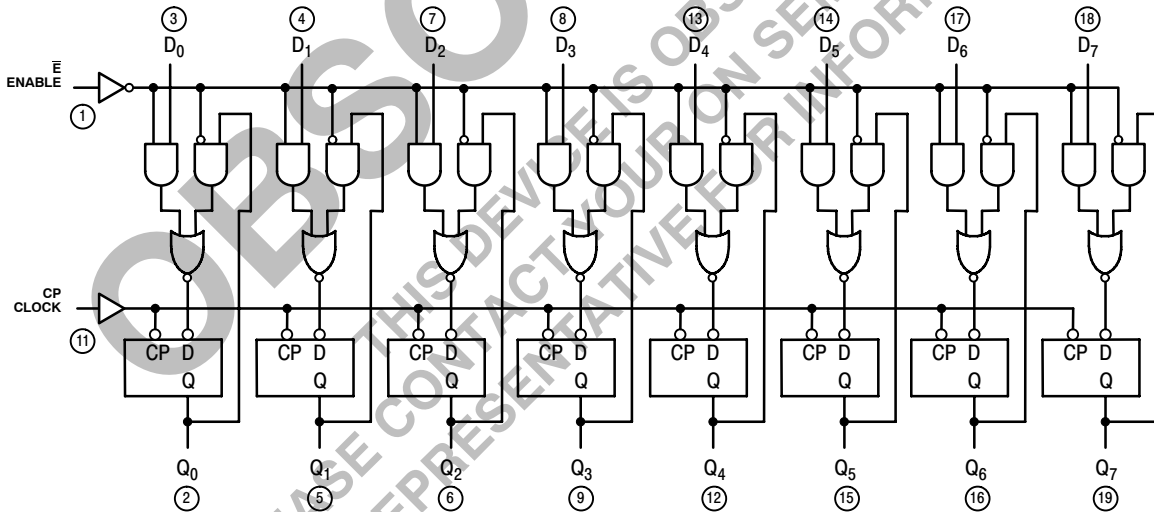
### LOADING (Note a)

|                         | HIGH     | LOW       |
|-------------------------|----------|-----------|
| $\bar{E}$               | 0.5 U.L. | 0.25 U.L. |
| $D_0 - D_3$             | 0.5 U.L. | 0.25 U.L. |
| CP                      | 0.5 U.L. | 0.25 U.L. |
| $Q_0 - Q_3$             | 10 U.L.  | 5 U.L.    |
| $\bar{Q}_0 - \bar{Q}_3$ | 10 U.L.  | 5 U.L.    |

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### LOGIC DIAGRAM



# SN74LS377

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol          | Parameter                      | Limits |       |      | Unit | Test Conditions   |
|-----------------|--------------------------------|--------|-------|------|------|---|
|                 |                                | Min    | Typ   | Max  |      |   |
| V <sub>IH</sub> | Input HIGH Voltage             | 2.0    |       |      | V    | Guaranteed Input HIGH Voltage for All Inputs  |
| V <sub>IL</sub> | Input LOW Voltage              |        |       | 0.8  | V    | Guaranteed Input LOW Voltage for All Inputs   |
| V <sub>IK</sub> | Input Clamp Diode Voltage      |        | -0.65 | -1.5 | V    | V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA   |
| V <sub>OH</sub> | Output HIGH Voltage            | 2.7    | 3.5   |      | V    | V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table                            |
| V <sub>OL</sub> | Output LOW Voltage             |        | 0.25  | 0.4  | V    | I <sub>OL</sub> = 4.0 mA<br>V <sub>CC</sub> = V <sub>CC</sub> MIN,<br>V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>per Truth Table |
|                 |                                |        | 0.35  | 0.5  | V    |   |
| I <sub>IH</sub> | Input HIGH Current             |        |       | 20   | μA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V  |
|                 |                                |        |       | 0.1  | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V  |
| I <sub>IL</sub> | Input LOW Current              |        |       | -0.4 | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V  |
| I <sub>OS</sub> | Short Circuit Current (Note 1) | -20    |       | -100 | mA   | V <sub>CC</sub> = MAX   |
| I <sub>CC</sub> | Power Supply Current           |        |       | 28   | mA   | V <sub>CC</sub> = MAX, NOTE 1   |

NOTE: With all inputs open and GND applied to all data and enable inputs, I<sub>CC</sub> is measured after a momentary GND, then 4.5 V is applied to clock.  
1. Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

| Symbol                               | Parameter                             | Limits |          |          | Unit | Test Conditions                                   |
|--------------------------------------|---------------------------------------|--------|----------|----------|------|---|
|                                      |                                       | Min    | Typ      | Max      |      |   |
| f <sub>MAX</sub>                     | Maximum Clock Frequency               | 30     | 40       |          | MHz  | V <sub>CC</sub> = 5.0 V<br>C <sub>L</sub> = 15 pF |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay,<br>Clock to Output |        | 17<br>18 | 27<br>27 | ns   |   |

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

| Symbol         | Parameter         | Limits           |     |     | Unit | Test Conditions         |
|----------------|-------------------|------------------|-----|-----|------|-------------------------|
|                |                   | Min              | Typ | Max |      |                         |
| t <sub>w</sub> | Any Pulse Width   | 20               |     |     | ns   | V <sub>CC</sub> = 5.0 V |
| t <sub>s</sub> | Data Setup Time   | 20               |     |     | ns   |                         |
| t <sub>s</sub> | Enable Setup Time | Inactive — State | 10  |     | ns   |                         |
|                |                   | Active — State   | 25  |     | ns   |                         |
| t <sub>h</sub> | Any Hold Time     | 5.0              |     |     | ns   |                         |

## DEFINITION OF TERMS




**SETUP TIME (t<sub>s</sub>)** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME (t<sub>h</sub>)** — is defined as the minimum time following the clock transition from LOW-to-HIGH that the

logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

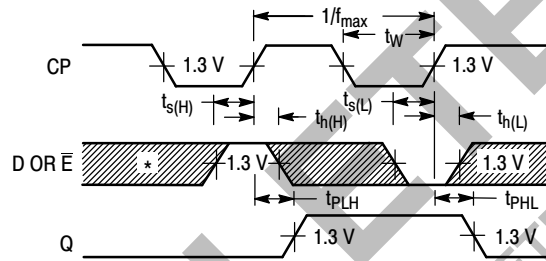
# SN74LS377

## TRUTH TABLE

| $\bar{E}$ | CP  | $D_n$ | $Q_n$     | $\bar{Q}_n$ |
|-----------|---|-------|-----------|-------------|
| H         |  | X     | No Change | No Change   |
| L         |  | H     | H         | L           |
| L         |  | L     | L         | H           |

L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Immaterial

## AC WAVEFORM

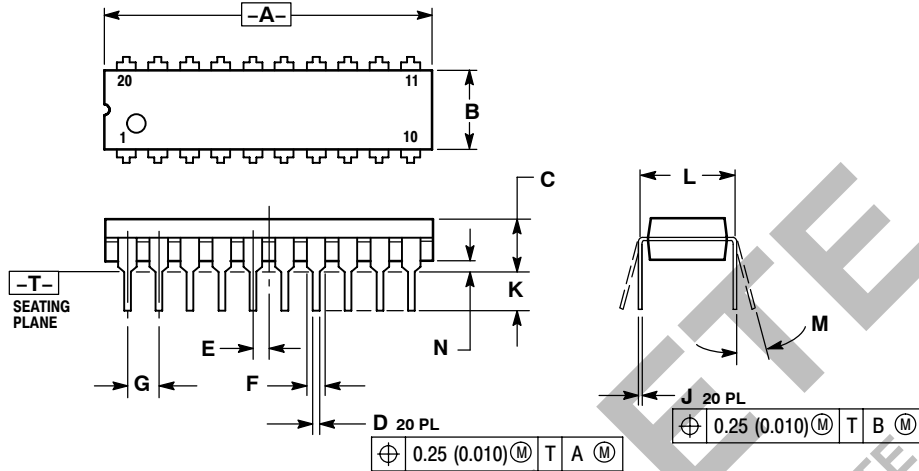


\*The shaded areas indicate when the input is permitted to change for predictable output performance.

# SN74LS377

## PACKAGE DIMENSIONS

**N SUFFIX**  
**PLASTIC PACKAGE**  
**CASE 738-03**  
**ISSUE E**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 1.010     | 1.070 | 25.66       | 27.17 |
| B   | 0.240     | 0.260 | 6.10        | 6.60  |
| C   | 0.150     | 0.180 | 3.81        | 4.57  |
| D   | 0.015     | 0.022 | 0.39        | 0.55  |
| E   | 0.050 BSC |       | 1.27 BSC    |       |
| F   | 0.050     | 0.070 | 1.27        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.140 | 2.80        | 3.55  |
| L   | 0.300 BSC |       | 7.62 BSC    |       |
| M   | 0°        | 15°   | 0°          | 15°   |
| N   | 0.020     | 0.040 | 0.51        | 1.01  |

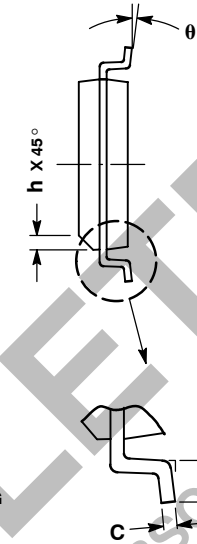
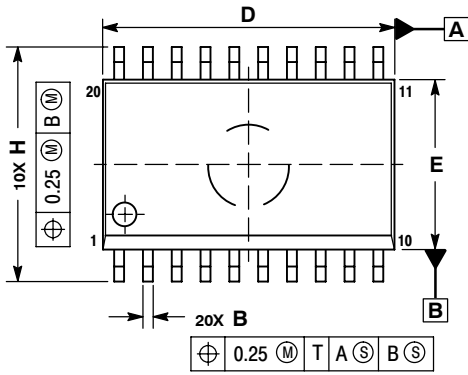
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# SN74LS377

## PACKAGE DIMENSIONS

DW SUFFIX  
 PLASTIC SOIC PACKAGE  
 CASE 751D-05  
 ISSUE F



- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       |
|-----|-------------|-------|
|     | MIN         | MAX   |
| A   | 2.35        | 2.65  |
| A1  | 0.10        | 0.25  |
| B   | 0.35        | 0.49  |
| C   | 0.23        | 0.32  |
| D   | 12.65       | 12.95 |
| E   | 7.40        | 7.60  |
| e   | 1.27 BSC    |       |
| H   | 10.05       | 10.55 |
| h   | 0.25        | 0.75  |
| L   | 0.50        | 0.90  |
| θ   | 0°          | 7°    |

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