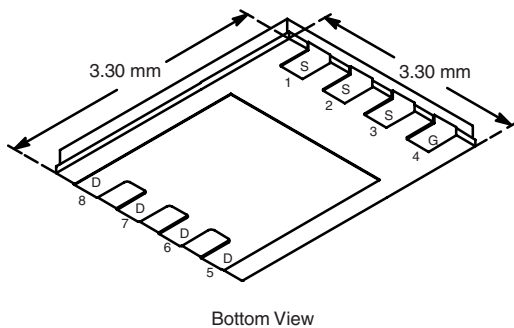


P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
- 20	0.0108 at V _{GS} = - 4.5 V	- 15.3
	0.015 at V _{GS} = - 2.5 V	- 13.0
	0.020 at V _{GS} = - 1.8 V	- 11.2

PowerPAK 1212-8



Bottom View

Ordering Information: Si7107DN-T1-E3 (Lead (Pb)-free)
Si7107DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

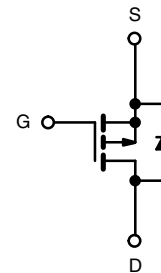
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET: 1.8 V Rated
- Ultra Low On-Resistance for Increased Battery Life
- New PowerPAK[®] Package
 - Low Thermal Resistance, R_{thJC}
 - Low 1.07 mm Profile
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Load/Power Switching in Portable Devices



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage	V _{DS}	- 20		V	
Gate-Source Voltage	V _{GS}	± 8			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	- 15.3	- 9.8	A
		T _A = 70 °C	- 12.2	- 7.8	
Pulsed Drain Current	I _{DM}	- 40			
Continuous Source Current (Diode Conduction) ^a	I _S	- 3.2	- 1.3		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	3.8	1.5	W
		T _A = 70 °C	2.4	1.0	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 s	24	33	°C/W
		Steady State	65	81	
Maximum Junction-to-Case	R _{thJC}	1.9	2.4		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

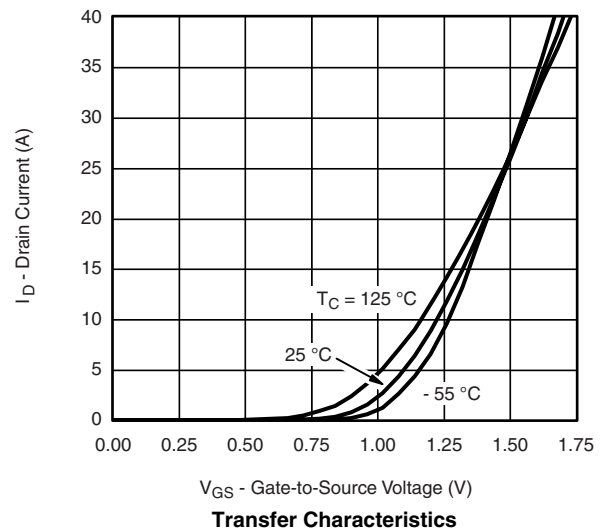
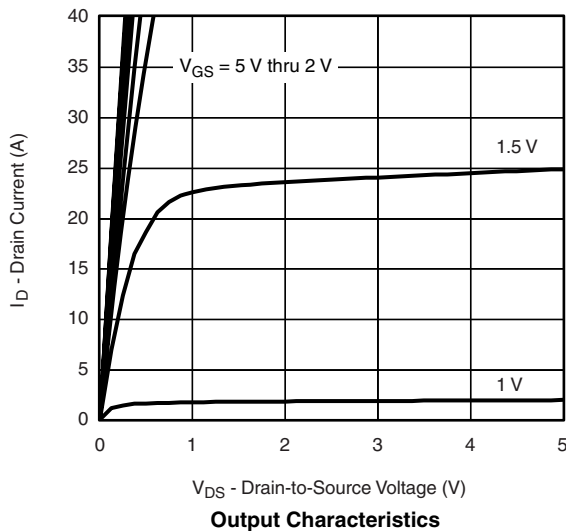
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -450\ \mu\text{A}$	-0.4		-1.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-40			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = -15.3\ \text{A}$		0.0090	0.0108	Ω
		$V_{GS} = -2.5\ \text{V}, I_D = -13\ \text{A}$		0.0125	0.015	
		$V_{GS} = -1.8\ \text{V}, I_D = -5\ \text{A}$		0.0167	0.020	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}, I_D = -15.3\ \text{A}$		58		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -3.2\ \text{A}, V_{GS} = 0\ \text{V}$		-0.7	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -15.3\ \text{A}$		34	44	nC
Gate-Source Charge	Q_{gs}		4.6			
Gate-Drain Charge	Q_{gd}		9.2			
Gate Resistance	R_g	$f = 1\ \text{MHz}$		8		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}, R_L = 10\ \Omega$ $I_D = -1\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_g = 6\ \Omega$		27	40	ns
Rise Time	t_r		55	85		
Turn-Off Delay Time	$t_{d(off)}$		270	400		
Fall Time	t_f		160	240		
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -3.2\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		110	165	

Notes:

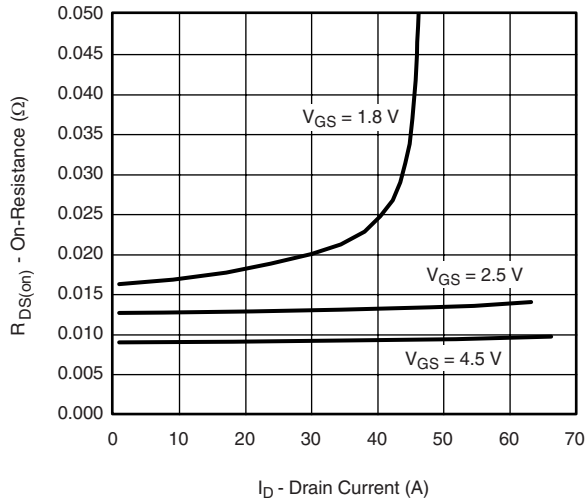
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

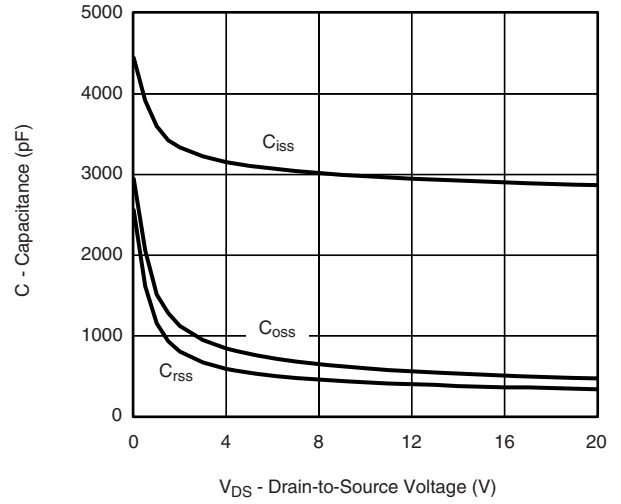
TYPICAL CHARACTERISTICS 25°C , unless otherwise noted



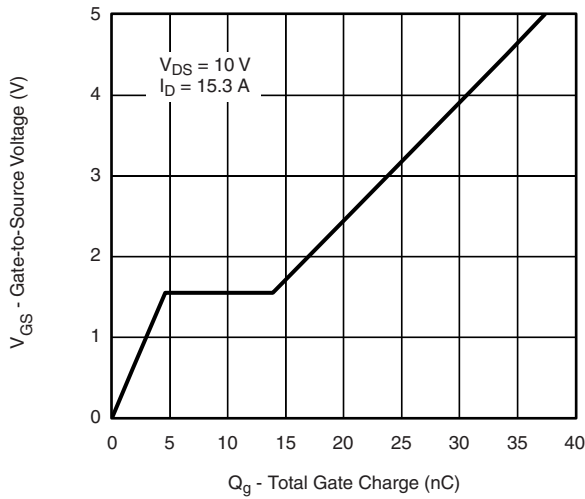
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



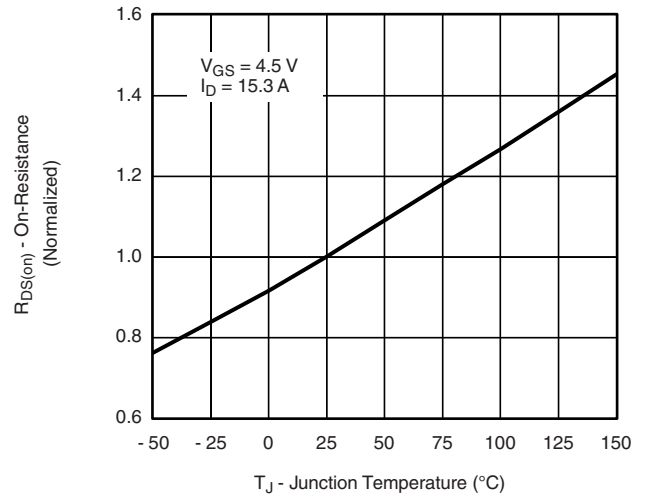
On-Resistance vs. Drain Current



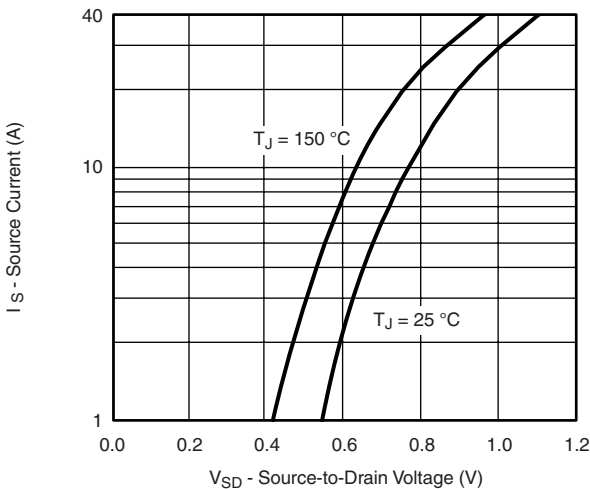
Capacitance



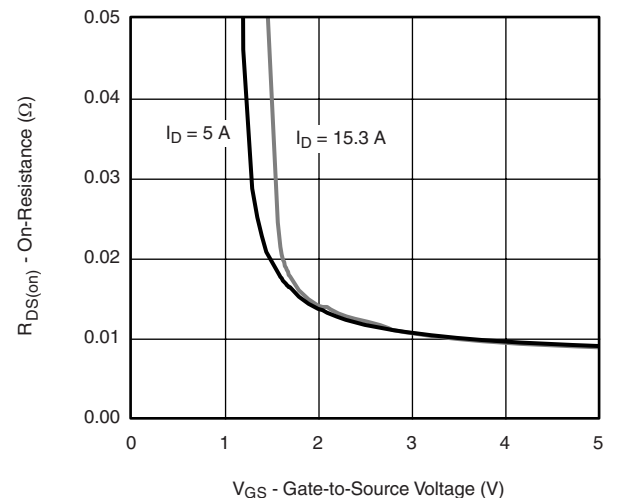
Gate Charge



On-Resistance vs. Junction Temperature

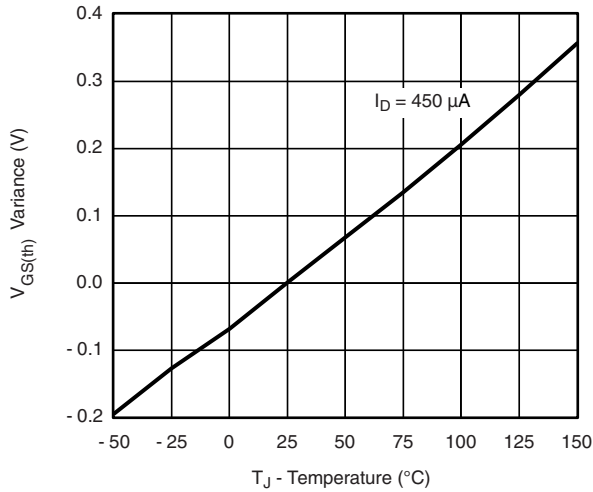


Source-Drain Diode Forward Voltage

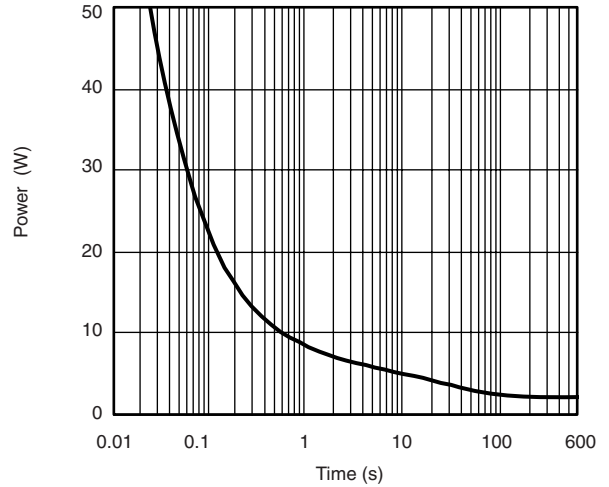


On-Resistance vs. Gate-to-Source Voltage

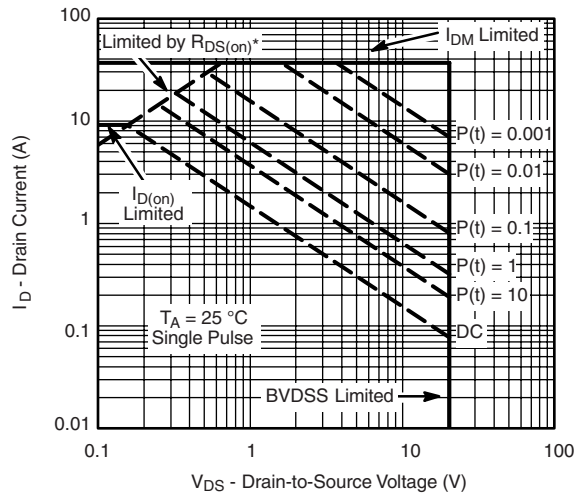
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Threshold Voltage



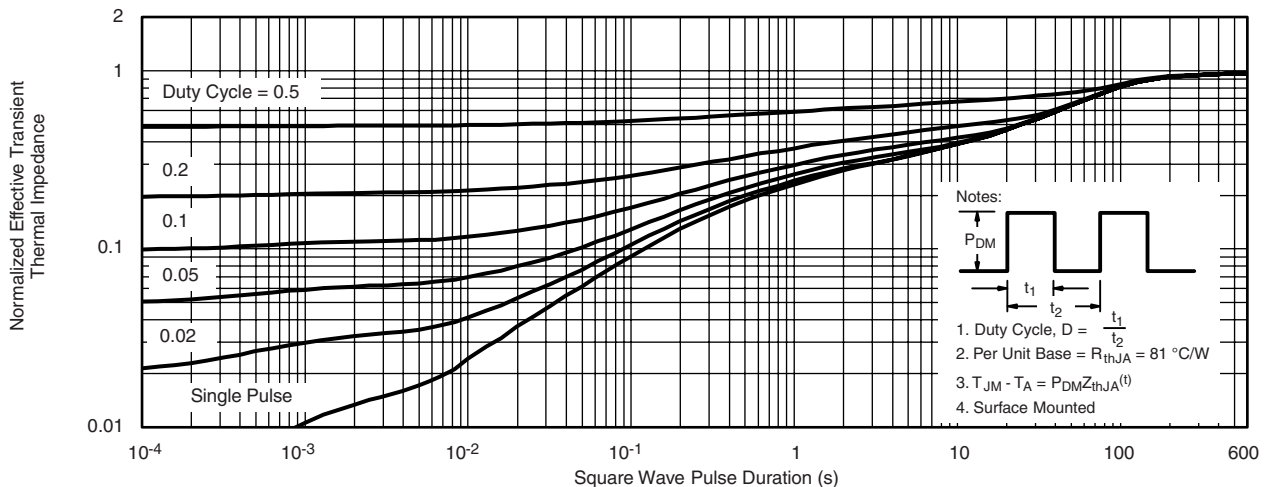
Single Pulse Power, Junction-to-Ambient



V_{DS} - Drain-to-Source Voltage (V)

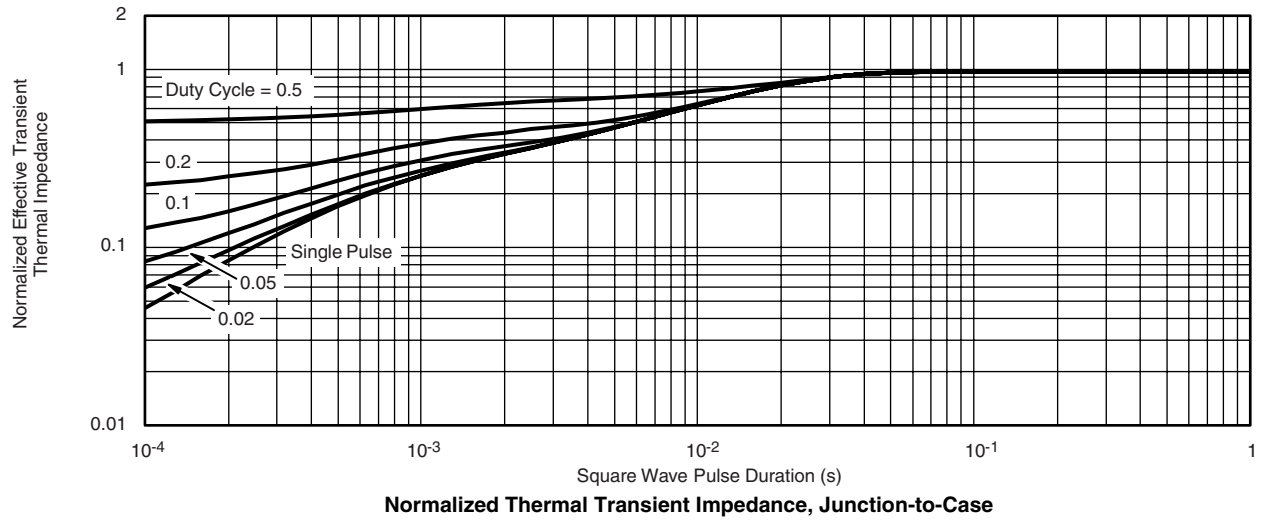
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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