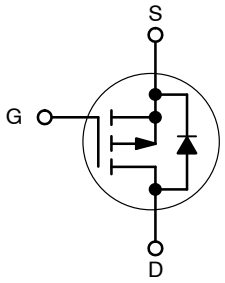
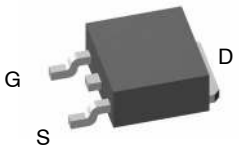
MOSFET – P-Channel, POWERTRENCH®

60 V

FDD5614P



P–Channel MOSFET



DPAK3 (TO–252 3 LD)
CASE 369AS

General Description

This 60 V P–Channel MOSFET uses **onsemi**'s high voltage POWERTRENCH process. It has been optimized for power management applications.

Features

- –15 A, –60 V
  - $R_{DS(ON)}$ = 100 mΩ at V_{GS} = –10 V
  - $R_{DS(ON)}$ = 130 mΩ at V_{GS} = –4.5 V
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- High Power and Current Handling Capability
- This is a Pb–Free Device

Applications

- DC/DC Converter
- Power Management
- Load Switch

MARKING DIAGRAM

FDD5614P = Specific Device Code
$Y = **onsemi** Logo
&Z = Assembly Plant Code
&3 = 3–Digit Date Code
&K = 2–Digits Lot Run Traceability Code

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain–Source Voltage	–60	V
V_{GSS}	Gate–Source Voltage	±20	V
I_D	Drain Current – Continuous (Note 3) – Pulsed (Note 1a)	–15 –45	A
P_D	Power Dissipation for Single Operation (Note 1) (Note 1a) (Note 1b)	 42 3.8 1.6	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
FDD5614P	TO–252–3 (Pb–Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	3.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	96	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

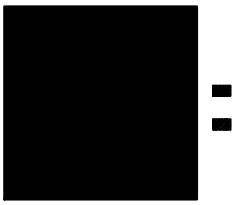
Symbol	Parameter	Condition	Min	Typ	Max	Unit
DRAIN−SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain−Source Avalanche Energy	V_{DD} = −30 V, I_D = −4.5 A	–	–	90	mJ
I_{AR}	Maximum Drain−Source Avalanche Current		–	–	−4.5	A
OFF CHARACTERISTICS						
B_{VDSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA	−60	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	–	−49	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −48 V, V_{GS} = 0 V	–	–	−1	μA
I_{GSSF}	Gate−Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate−Body Leakage, Reverse	V_{GS} = −20 V, V_{DS} = 0 V	–	–	−100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate to Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−1	−1.6	−3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	–	4	–	mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS}= −10 V, I_D = −4.5 A	–	76	100	mΩ
		V_{GS}= −4.5 V, I_D = −3.9 A	–	99	130	
		V_{GS}= −10 V, I_D = −4.5 A, T_J = 125°C	–	137	185	
$I_{D(on)}$	On−State Drain Current	V_{GS}= −10 V, V_{DS} = −5 V	−20	–	–	A
g_{FS}	Forward Transconductance	V_{DS} = −5 V, I_D = −3 A	–	8	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −30 V, V_{GS} = 0 V, f = 1 MHz	–	759	–	pF
C_{oss}	Output Capacitance		–	90	–	pF
C_{rss}	Reverse Transfer Capacitance		–	39	–	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −30 V, I_D = −1 A, V_{GS} = −10 V, R_{GEN} = 6 Ω	–	7	14	ns
t_r	Turn−On Rise Time		–	10	20	ns
$t_{d(off)}$	Turn−Off Delay Time		–	19	34	ns
t_f	Turn−Off Fall Time		–	12	22	ns
Q_g	Total Gate Charge	V_{DS} = −30 V, I_D = −4.5 A, V_{GS} = −10 V	–	15	24	nC
Q_{gs}	Gate−Source Charge		–	2.5	–	nC
Q_{gd}	Gate−Drain Charge		–	3.0	–	nC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
DRAIN−SOURCE AVELANCHE RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	−3.2	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = −3.2 A (Note 2)	–	−0.8	−1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA}$ = 40°C/W when mounted on a 1 in^2 pad of 2 oz copper.

b) $R_{\theta JA}$ = 96°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.
3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

   where P_D is maximum power dissipation at T_C = 25°C and $R_{DS(on)}$ is at $T_{J(max)}$ and V_{GS} = 10 V. Package current limitation is 21 A.

TYPICAL CHARACTERISTICS

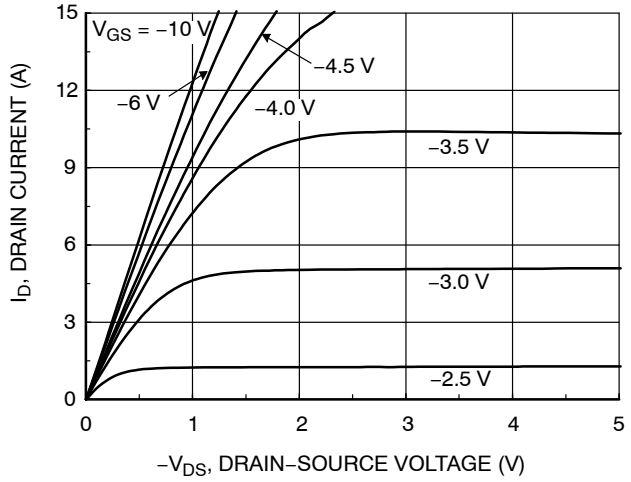


Figure 1. On−Region Characteristics

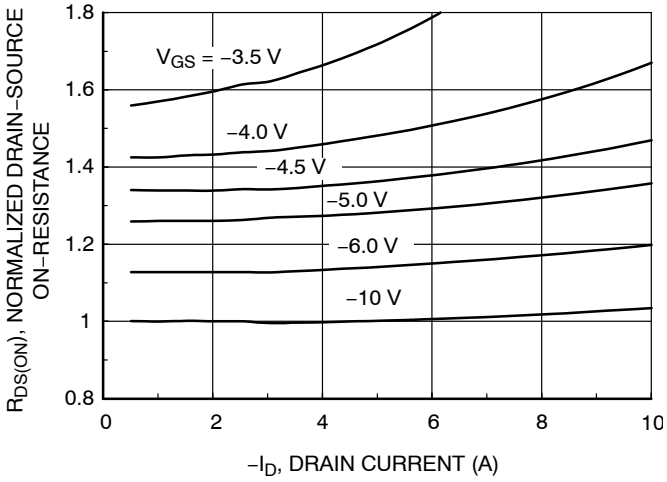


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

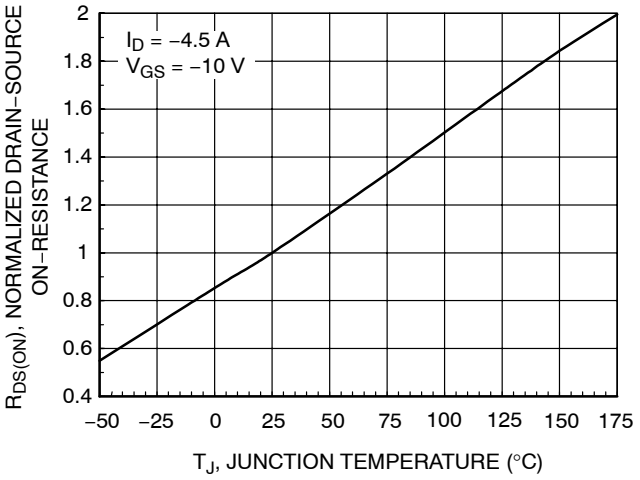


Figure 3. On−Resistance Variation with Temperature

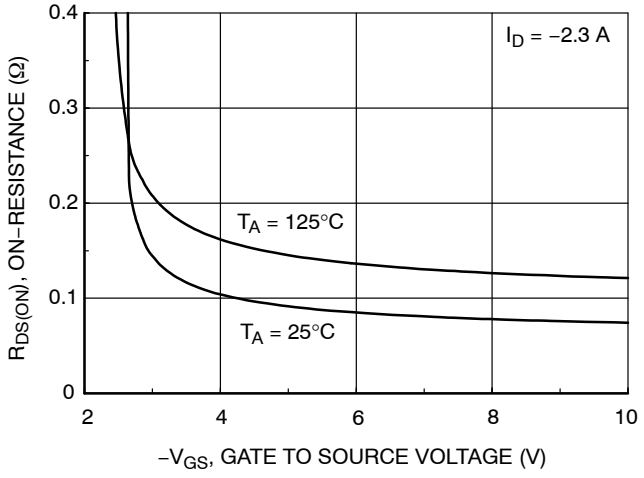


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

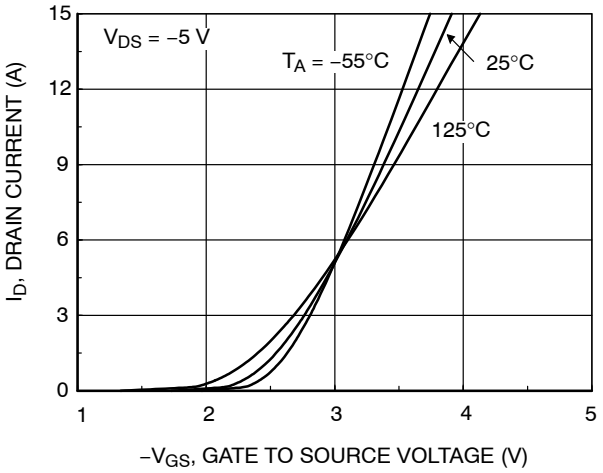


Figure 5. Transfer Characteristics

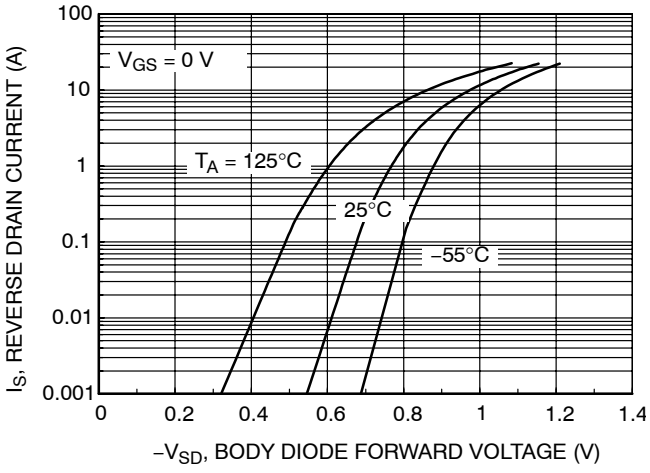


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

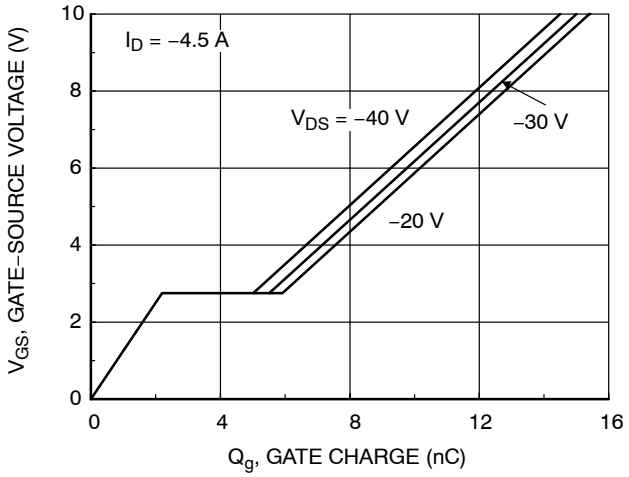


Figure 7. Gate Charge Characteristics

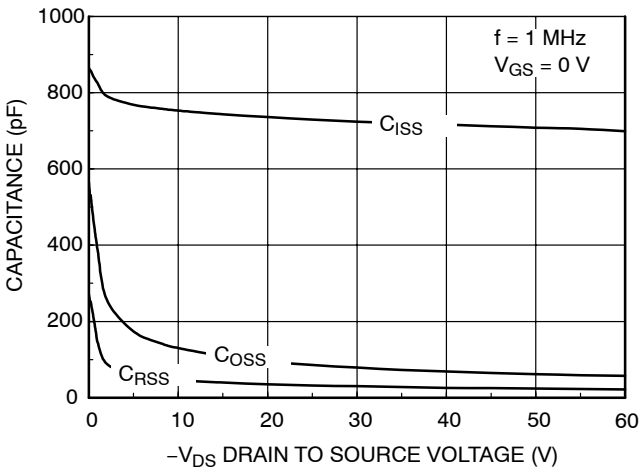


Figure 8. Capacitance Characteristics

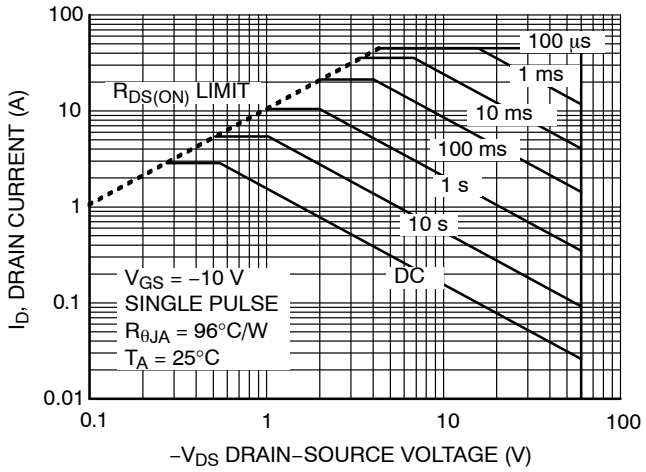


Figure 9. Maximum Safe Operating Area

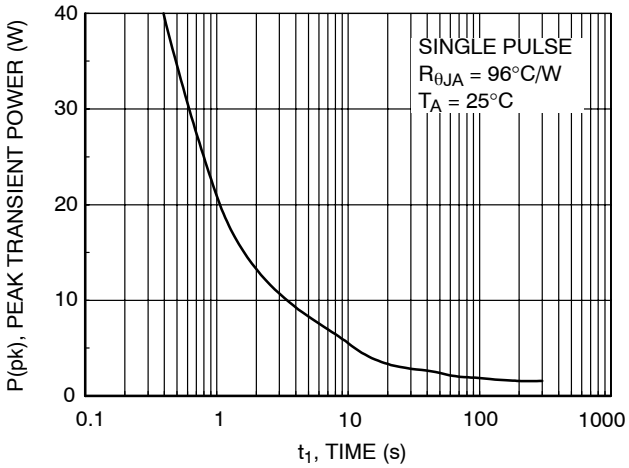
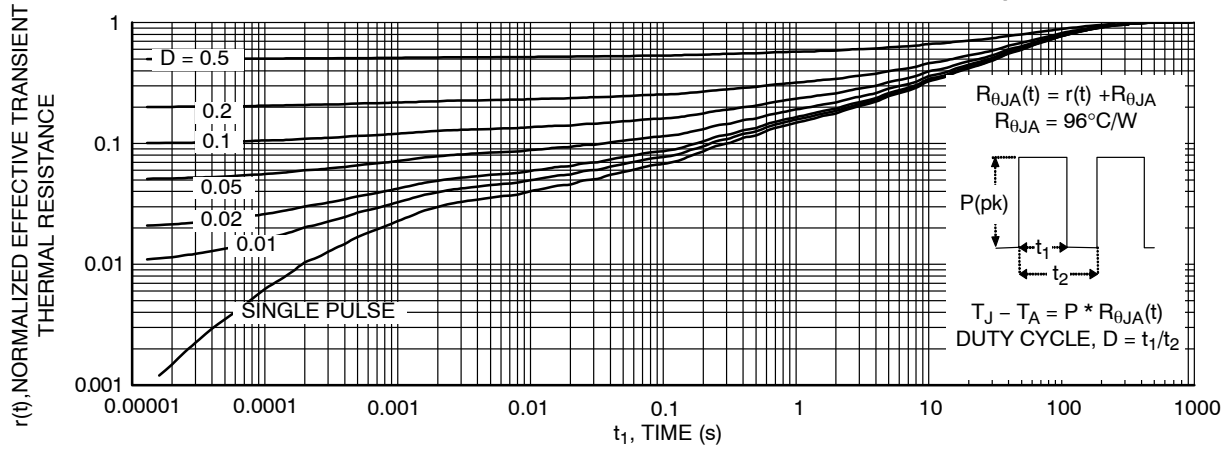


Figure 10. Single Pulse Maximum Power Dissipation



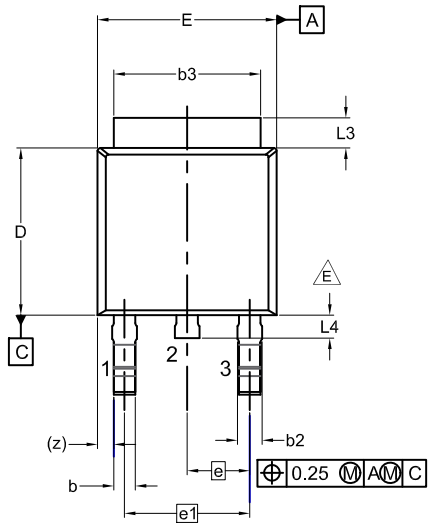
Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Figure 11. Transient Thermal Response Curve

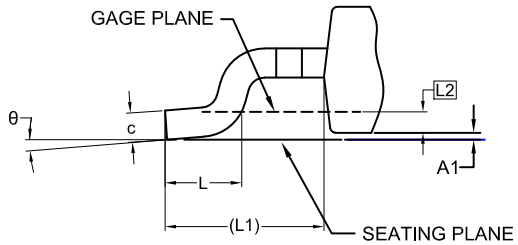
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

DPAK3 (TO−252 3 LD)
CASE 369AS
ISSUE A

DATE 28 SEP 2022



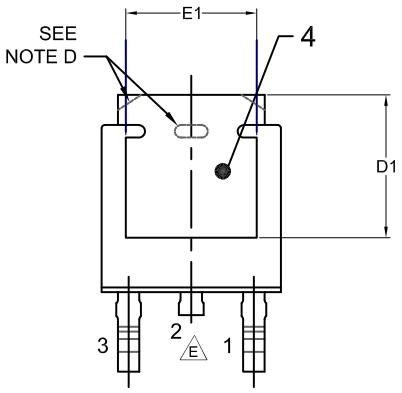
NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX.
F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



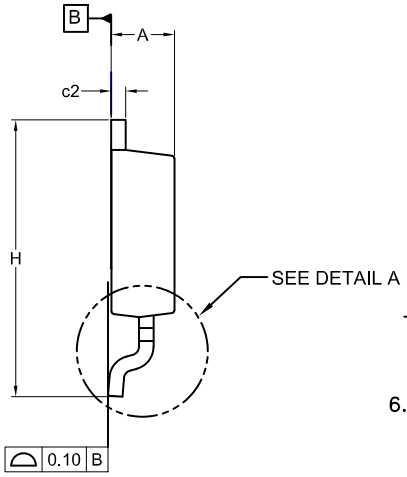
DETAIL A
(ROTATED -90°)
SCALE: 12X

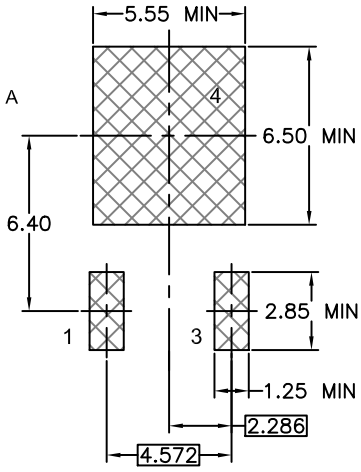
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	—	—
E	6.35	6.54	6.73
E1	4.32	—	—
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	—	—	1.02
θ	0°	---	10°

NON-DIODE PRODUCTS VERSION



NON-DIODE PRODUCTS VERSION





LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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