



EV1403-5000-A EVALUATION BOARD USER GUIDE



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Introduction

This user guide describes the evaluation board provided for the FS1403 μ POL™ product.

The board generates an output voltage (V_{OUT}) of 5V for loads of 0–3A from an input voltage (PV_{IN}) of 12V.

Specifications

- Input voltage (PV_{IN}) = +12V
- Output voltage (V_{OUT}) = +5V
- Output load (I_O) = 0–3A
- Switching frequency (F_{SW}) = 1.3MHz
- Output capacitance (C_O) = 2x22 μ F (MLCC)
- Input capacitance (C_{IN}) = 2x22 μ F (MLCC)
- Dimensions (width x length x thickness) = 63 x 84 x 1.5mm

Connections

Name	Identifier	Description
PV_{IN}	J1	Input voltage (+12V)
Gnd	J2	Ground for input voltage
V_{OUT}	J8	Output voltage (+5V)
Gnd	J7	Ground for output voltage
V_{CC}	TP2	Internal supply (V_{CC}) – output of an LDO regulator
Gnd	TP3	Ground for internal supply
En	TP11	Enable
PG	TP12	Power Good

The board is configured for a single input supply. An internal low drop-out regulator generates the internal supply (V_{CC}) from PV_{IN} . The Enable (En) input is connected to PV_{IN} through a resistor divider, so that no Enable signal is needed.

Operation

To use the evaluation board:

1. Connect a well-regulated +12V input supply to PV_{IN} (J1) and Gnd (J2).
2. Connect a load of 0–3A to V_{OUT} (J8) and Gnd (J7).

Description

The evaluation board consists of a 4-layer PCB made from FR4 glass-reinforced epoxy laminate material. All layers use 2oz copper (equating to a thickness of 0.0694mm). The major power components, including the FS1403, are mounted on the top side of the board.

Part reference	Quantity	Type	Description
FS1403 μ POL	1	–	Main IC
C9	1	2.2 μ F	0402, 10V, X7S
C10, C21	2	22 μ F	0805, 16V, X5R
C12	1	0.1 μ F	0402, 16V, X7R
C13	1	68 μ F	25V
C14, C15	2	22 μ F	0805, 6.3V, X5R
C26	1	1 μ F	0603, 25V, X5R
J1	1	Red	Banana connector
J2, J7	2	Black	Banana connector
J8	1	Green	Banana connector
J10, J11	2	–	3-pin header
R1	1	2.7 Ω	10%, 1/8W, 0805 case size
R3, R7	2	49.9k Ω	10%, 1/8W, 0805 case size
R4, R9, R11, R13, R17	5	0 Ω	0402 case size
R6	1	12.7k Ω	10%, 1/8W, 0805 case size
R18, R19	2	4.99k Ω	0402 case size
TP1-TP12, SW/NC15, VBUS, VEXTBUS, SCL, SDA	17	–	Test points

Figure 1 shows the layout of the board and Figure 2 shows a schematic of the electrical circuit.

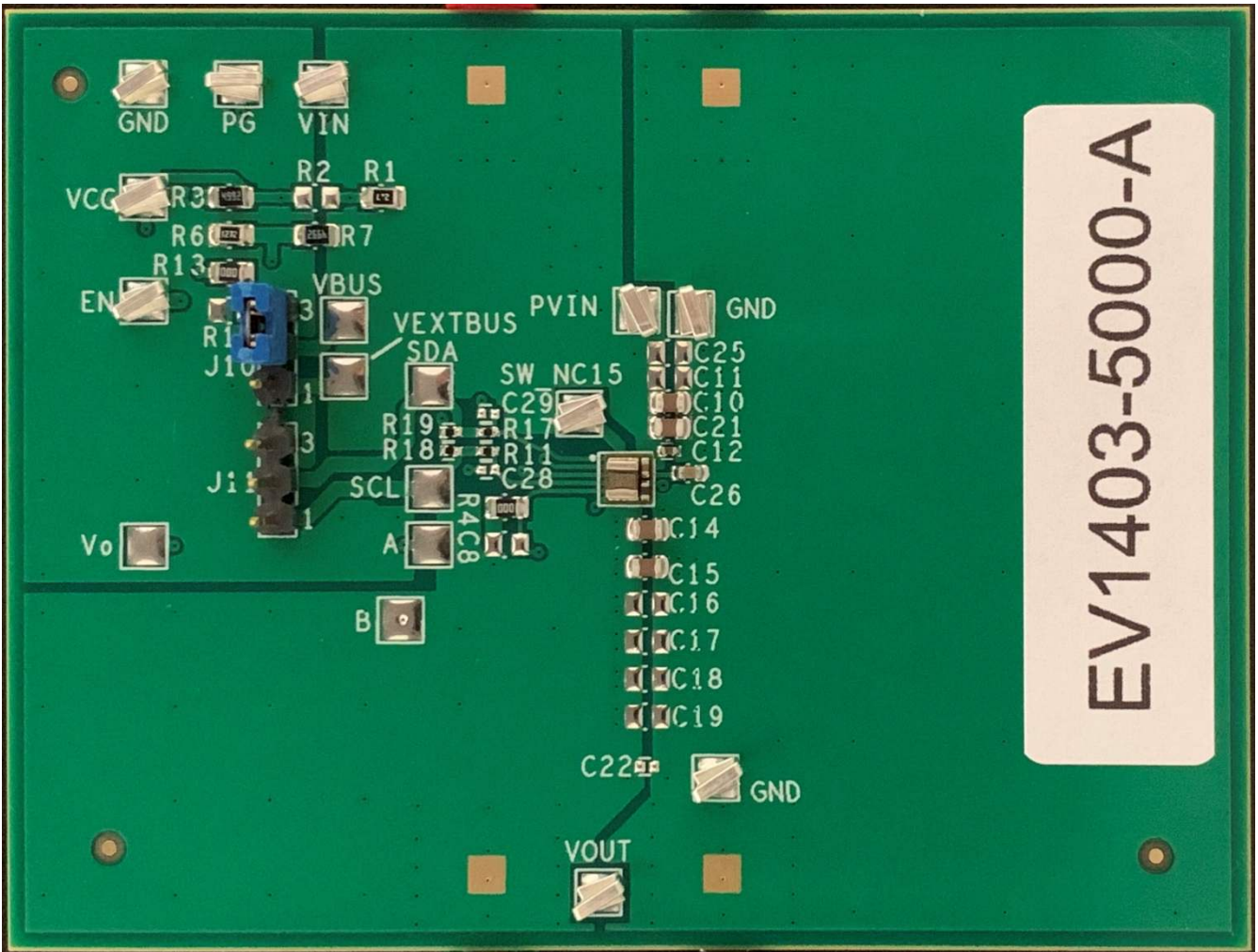


Figure 1 Board layout

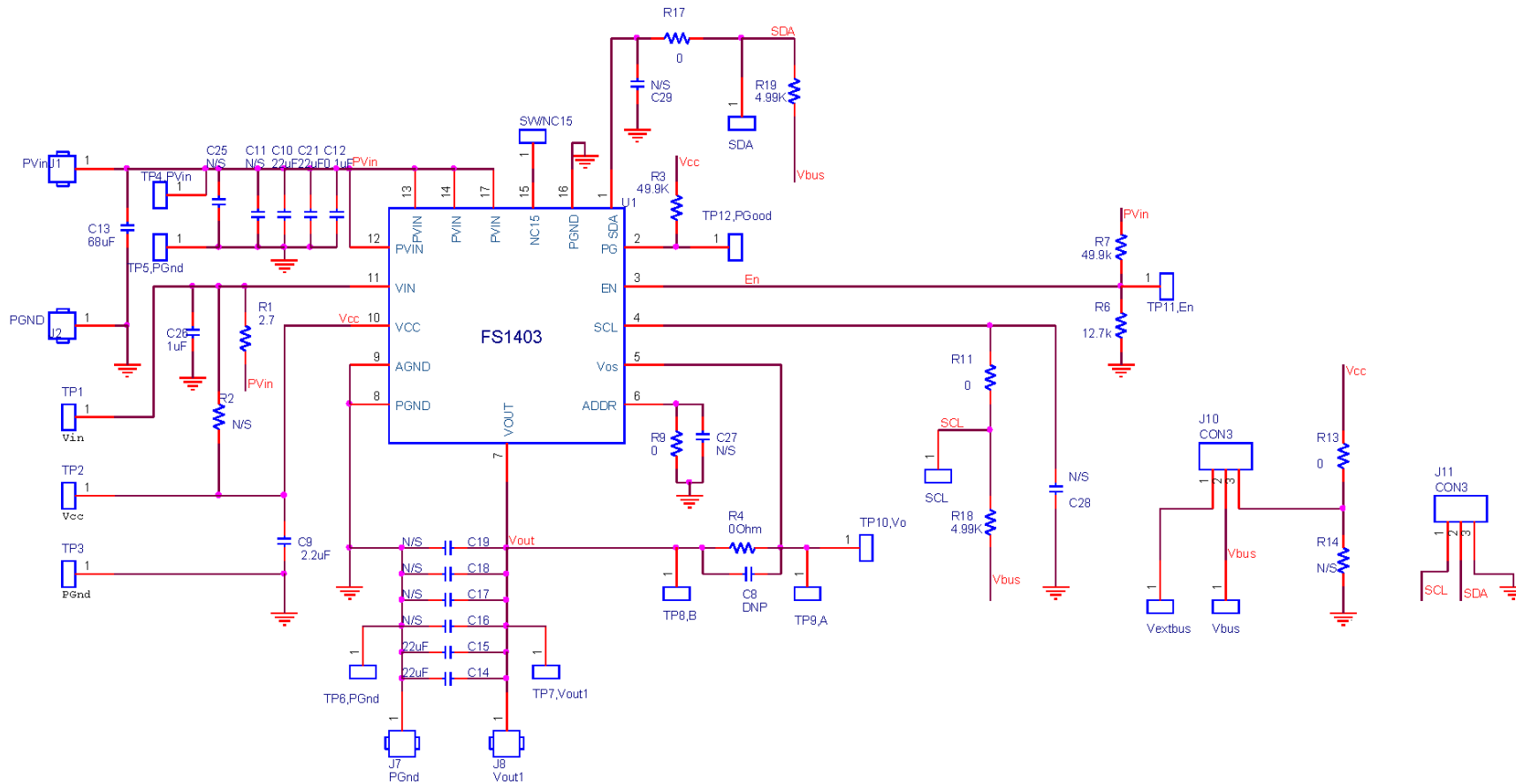


Figure 2 Schematic

Typical performance

Figure 3 to Figure 16 show typical operating waveforms for the evaluation board, while Figure 17 shows a thermal image of the board in operation. In all cases, the board is operating at room temperature with no airflow; PV_{IN} is 12V, V_{OUT} is 5V and I_O is 0–3A.

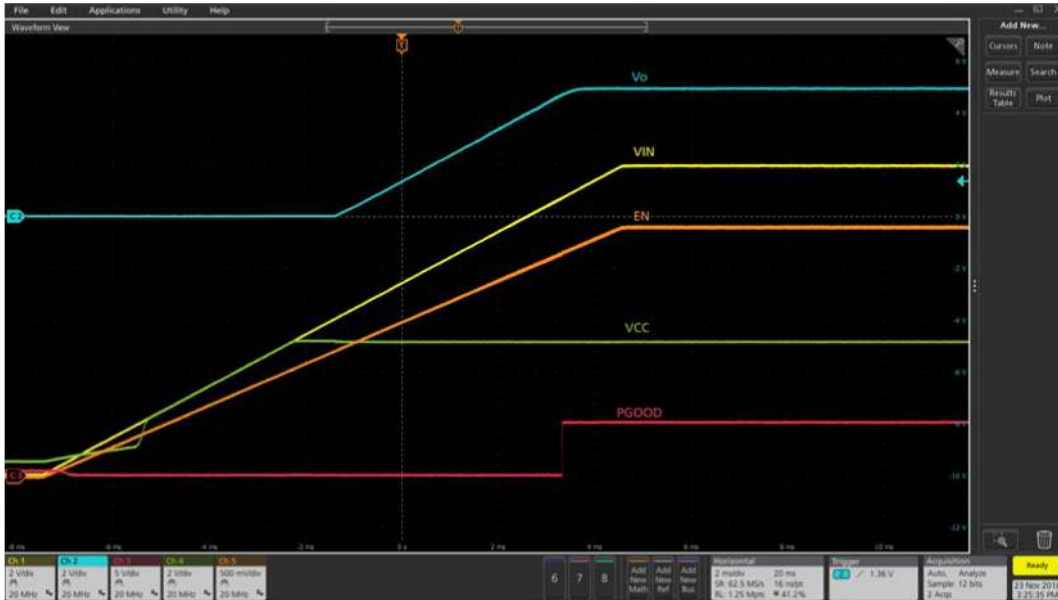


Figure 3 Startup with no load (Ch1: PV_{IN} , Ch2: V_{OUT} , Ch3: PG, Ch4: V_{CC} , Ch5: Enable)

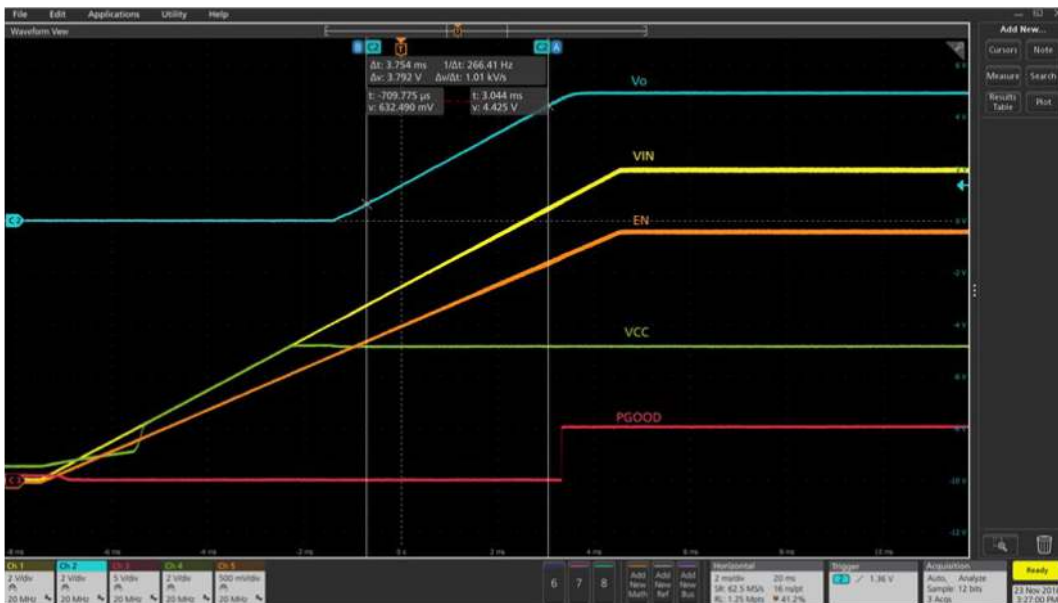


Figure 4 Startup with 3A load (Ch1: PV_{IN} , Ch2: V_{OUT} , Ch3: PG, Ch4: V_{CC} , Ch5: Enable)

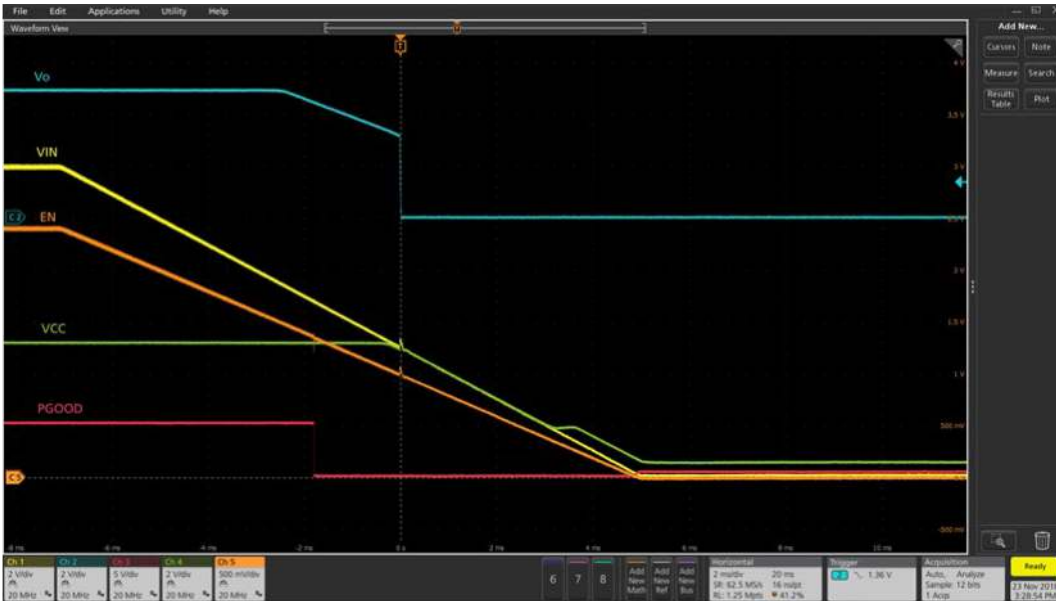


Figure 5 Shutdown with Enable de-assertion at 3A load (Ch1:PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch4:V_{CC}, Ch5: Enable)

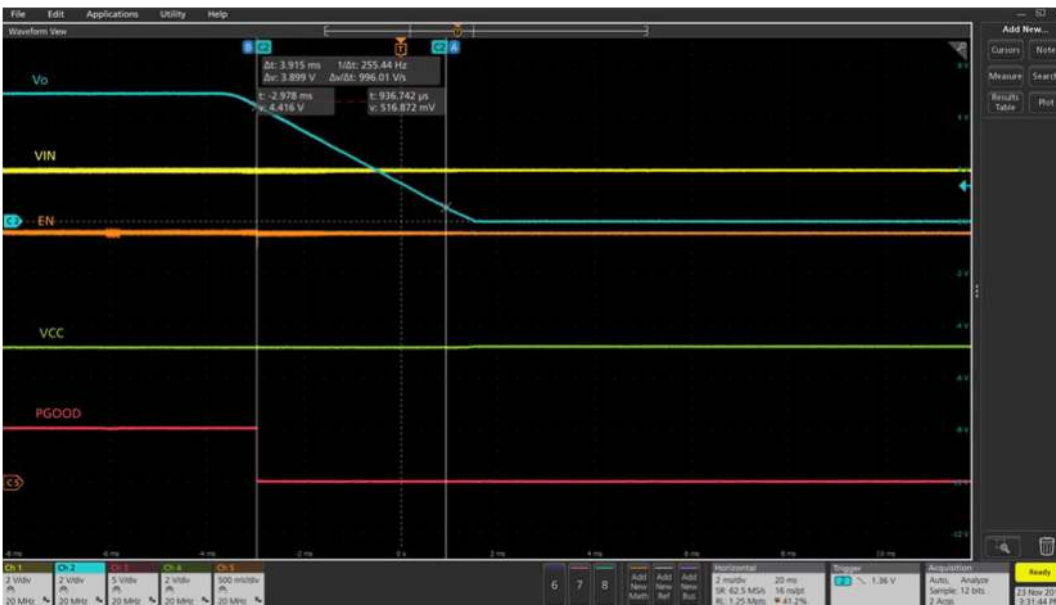


Figure 6 Soft turn off at 3A (Ch1:PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch4:V_{CC}, Ch5: Enable)

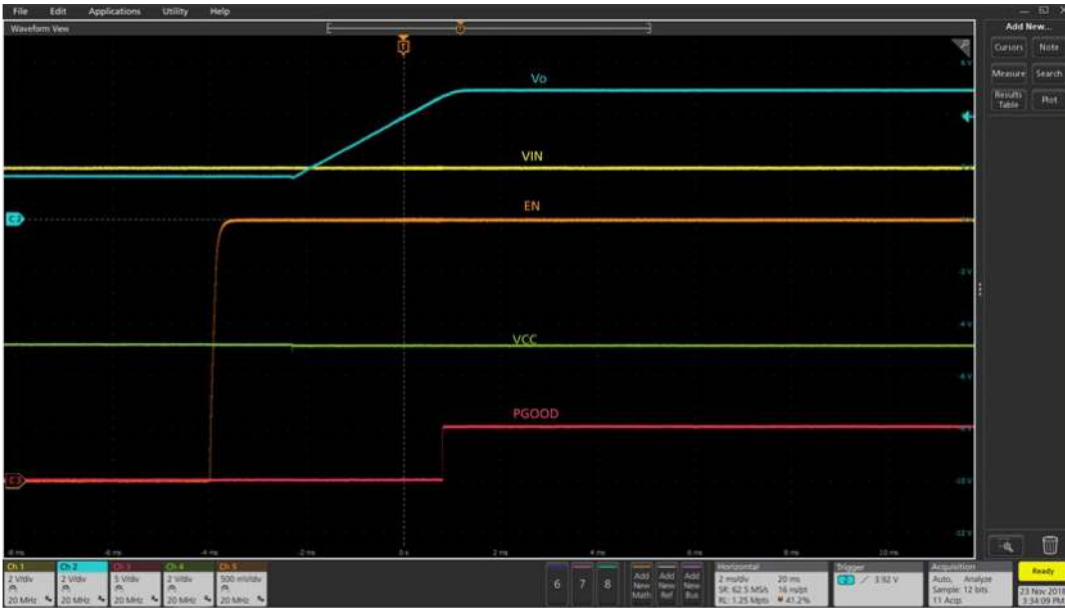


Figure 7 Startup into pre-bias
 (Ch1:PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch4:V_{CC}, Ch5: Enable)

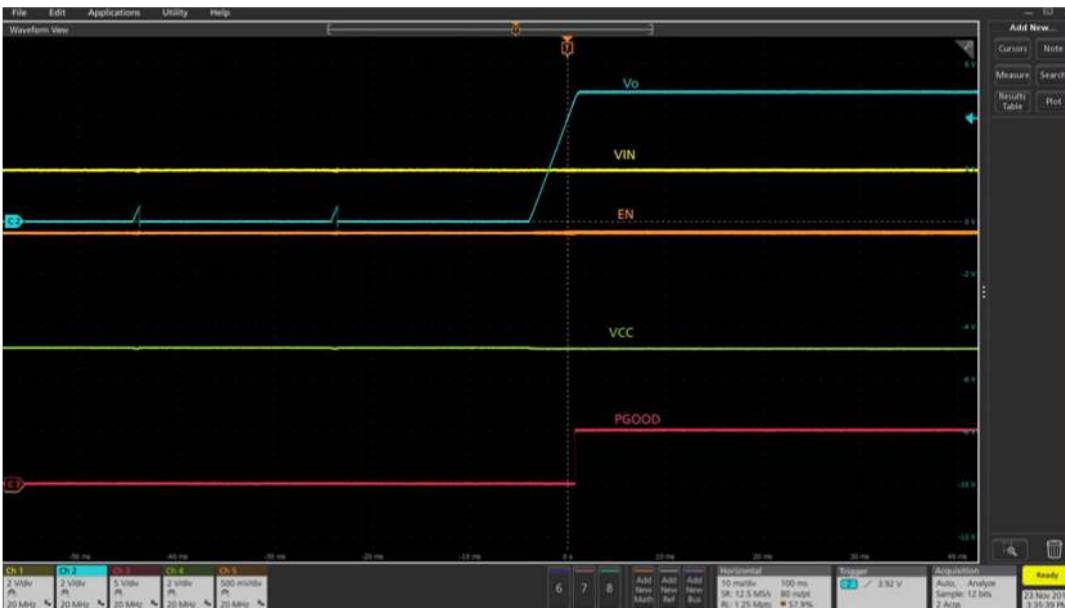


Figure 8 Over-current protection and auto-recover to 3A
 (Ch1:PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch4:V_{CC}, Ch5: Enable)

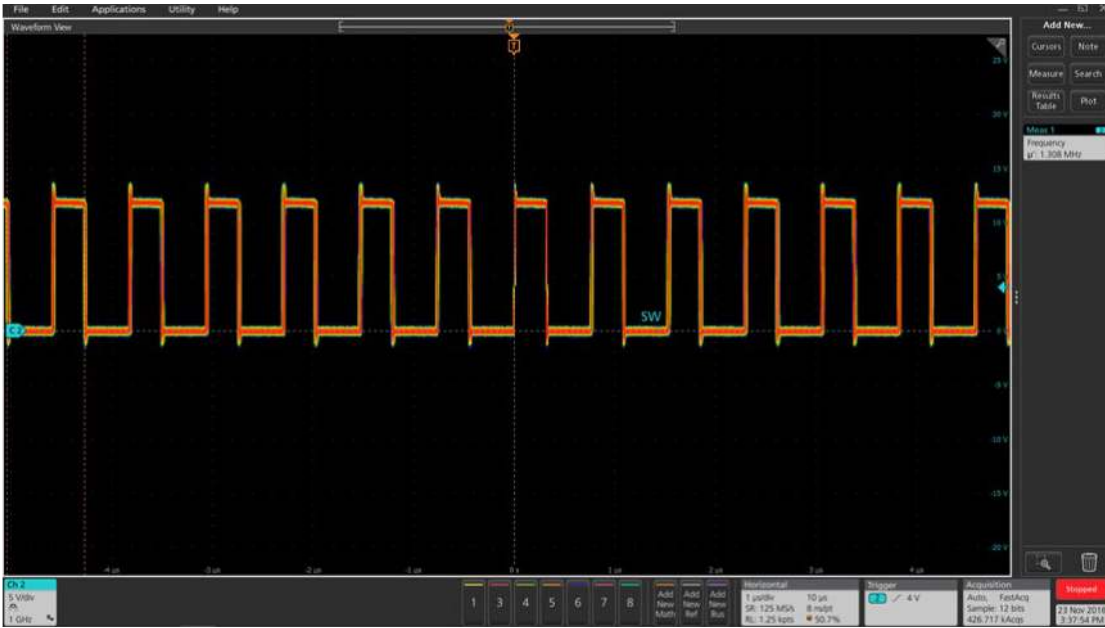


Figure 9 Sw at OA (Ch2: Sw)

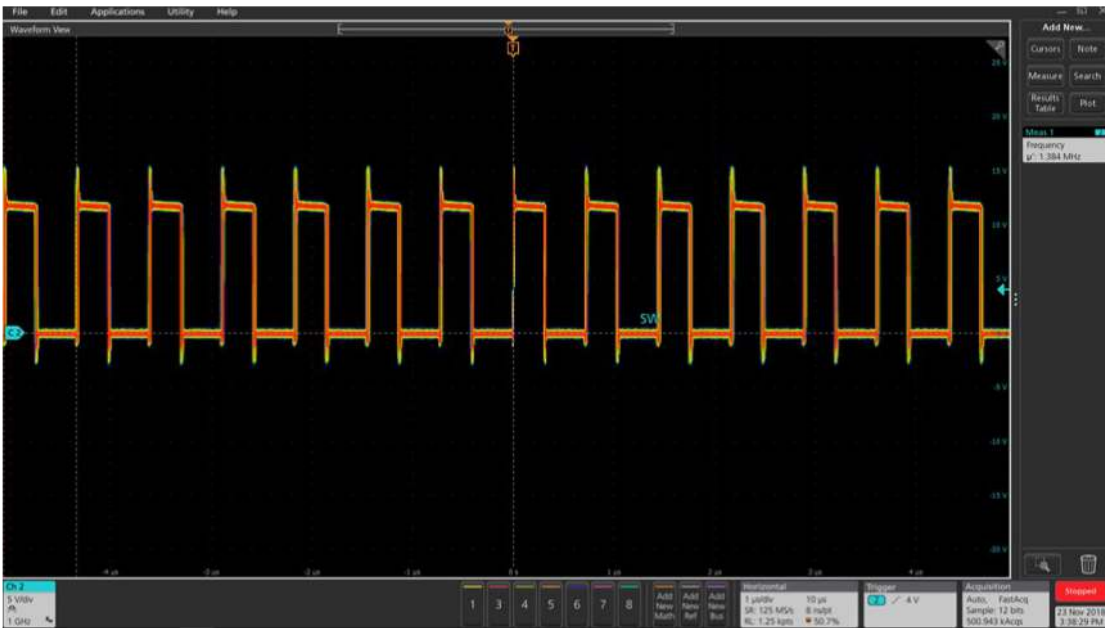


Figure 10 Sw at OA (Ch2: Sw)

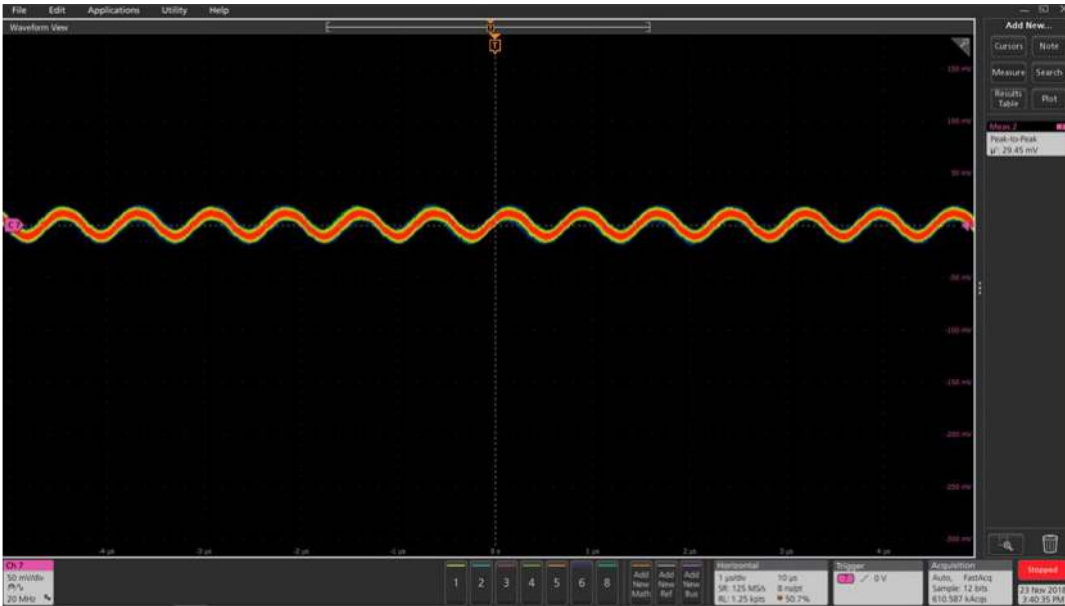


Figure 11 V_{OUT} ripple 30mV at 0A (Ch7:V_{OUT})

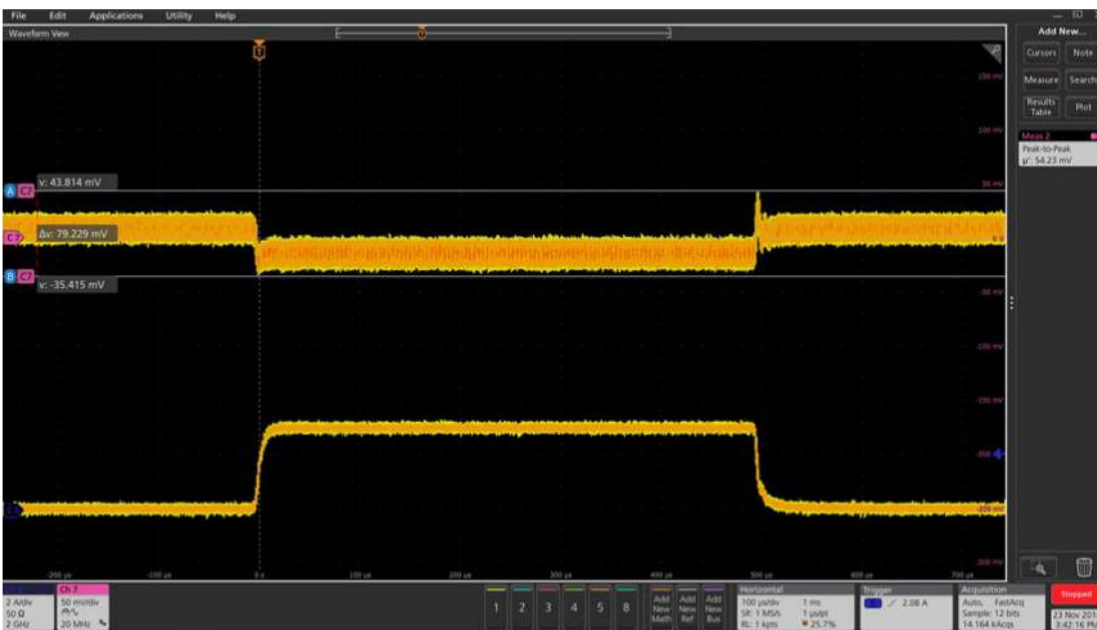


Figure 12 Transient response 0A to 3A (Ch6:I_O, Ch7: V_{OUT}), peak-peak deviation = 79mV

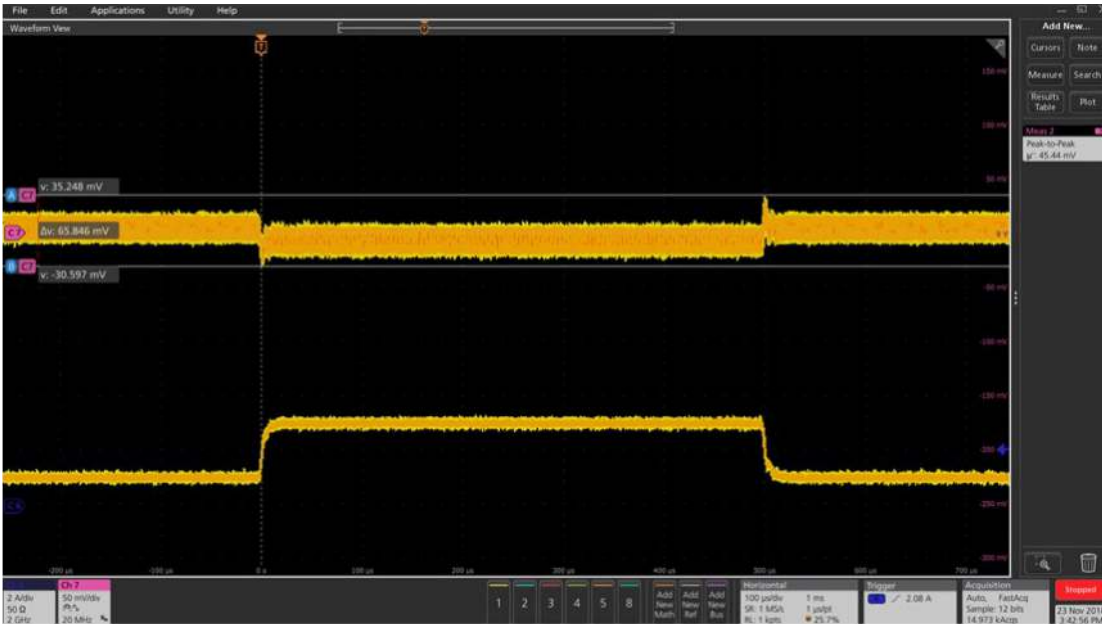


Figure 13 Transient response 1A to 3A (Ch6: I_o , Ch7: V_{out}), peak-peak deviation = 66mV

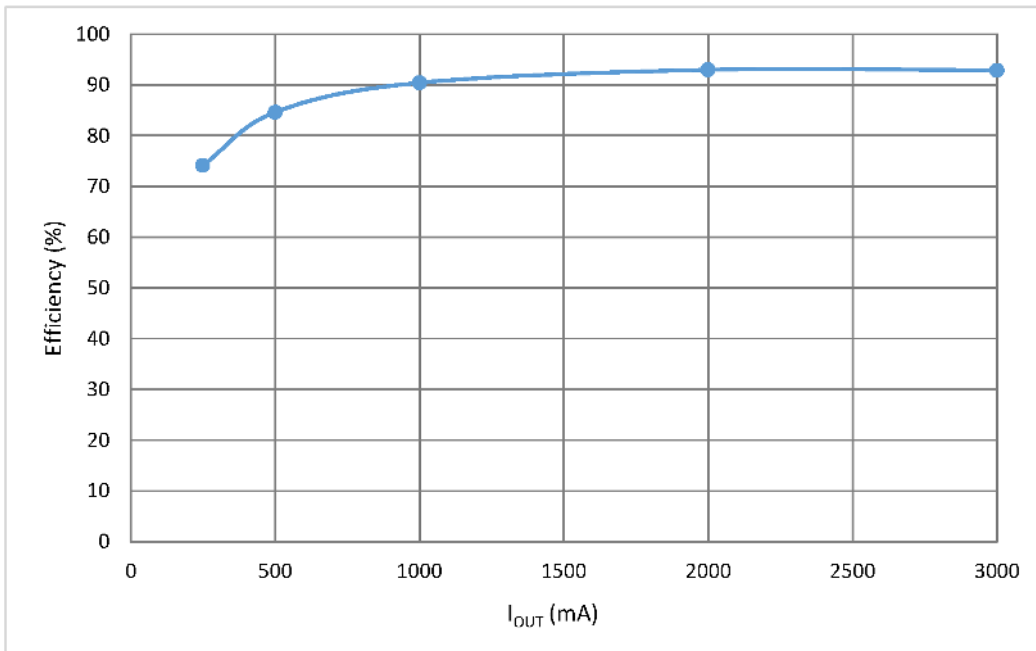


Figure 14 Efficiency

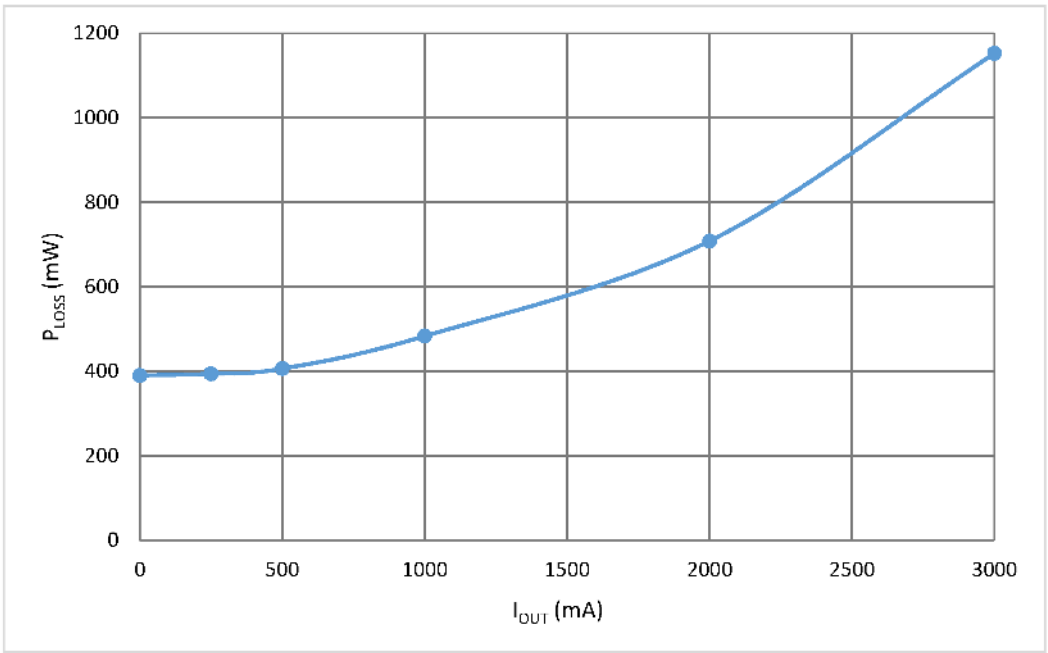


Figure 15 *Power loss*

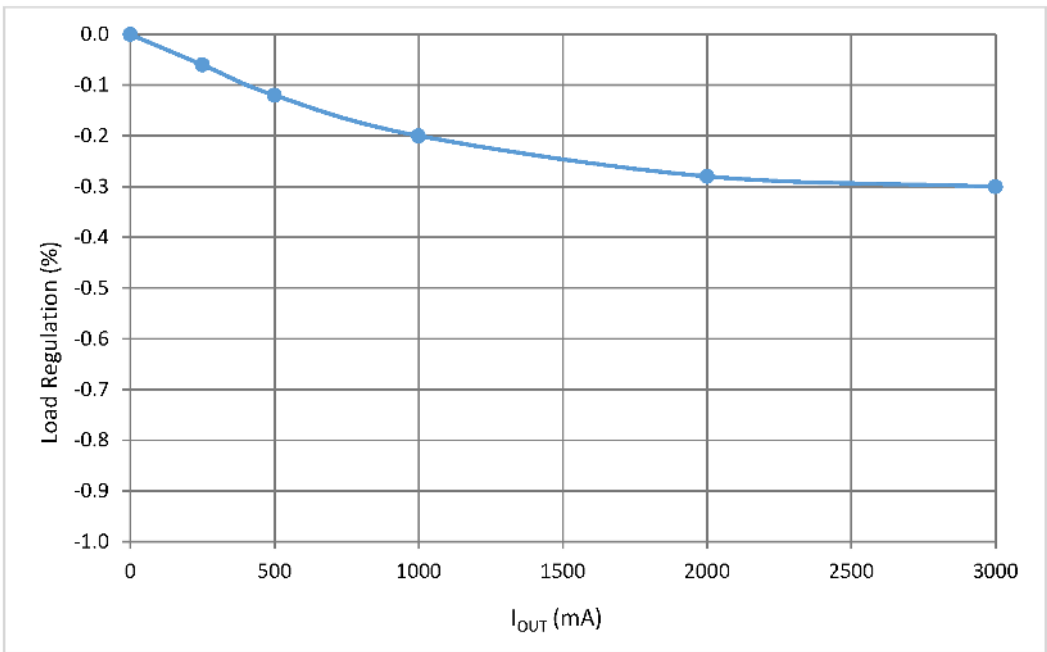


Figure 16 *Load regulation ($I_o = 0-3A$)*

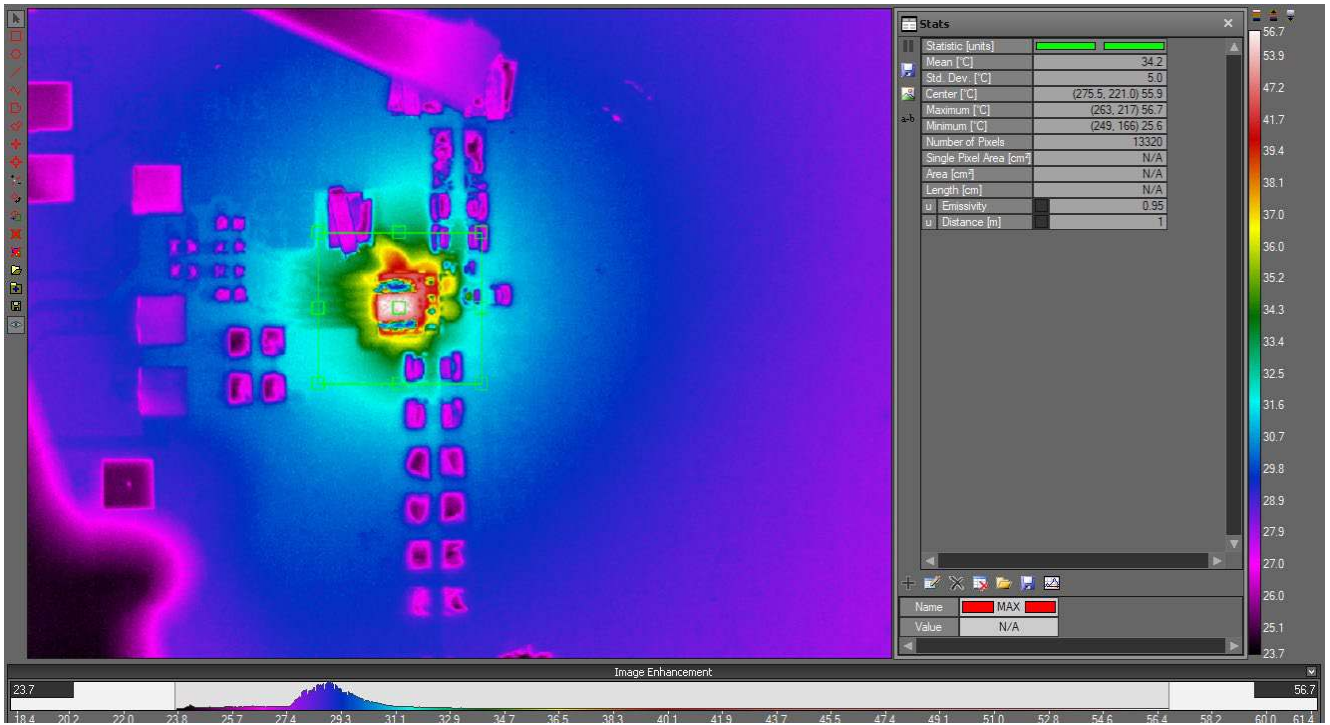


Figure 17 Thermal image – maximum temperature reached by FS1403 = 56.7°C

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6. Seabed equipment
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AU 3287379M 3287437AA 3290643AA 3291357AA

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