

SN54ALS174, SN54ALS175, SN54AS174, SN54AS175A SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SDAS207C – APRIL 1982 – REVISED OCTOBER 1995

- 'ALS174 and 'AS174 Contain Six Flip-Flops With Single-Rail Outputs
- 'ALS175, SN54AS175A, and SN74AS175B Contain Four Flip-Flops With Double-Rail Outputs
- Buffered Clock and Direct-Clear Inputs
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- Fully Buffered Outputs for Maximum Isolation From External Disturbances ('AS Only)
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

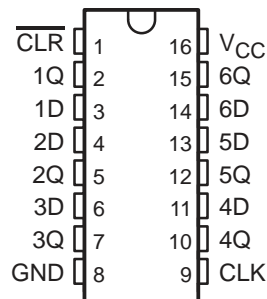
These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct-clear ($\overline{\text{CLR}}$) input, and the 'ALS175, SN54AS175A, and SN74AS175B feature complementary outputs from each flip-flop.

Information at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

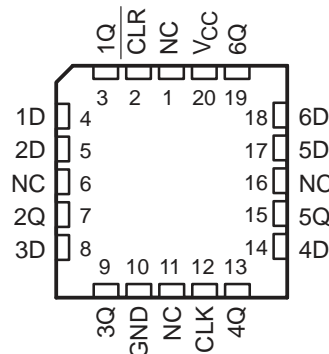
These circuits are fully compatible for use with most TTL circuits.

The SN54ALS174, SN54ALS175, SN54AS174, and SN54AS175A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS174, SN74ALS175, SN74AS174, and SN74AS175B are characterized for operation from 0°C to 70°C .

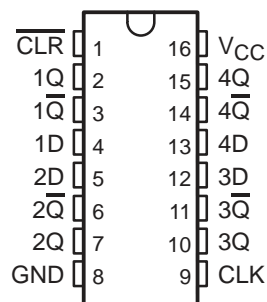
SN54ALS174, SN54AS174 . . . J PACKAGE
SN74ALS174, SN74AS174 . . . D OR N PACKAGE
(TOP VIEW)



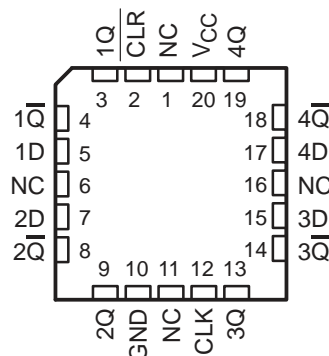
SN54ALS174, SN54AS174 . . . FK PACKAGE
(TOP VIEW)



SN54ALS175, SN54AS175A . . . J PACKAGE
SN74ALS175, SN74AS175B . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS175A, SN54AS175A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN54ALS174, SN54ALS175, SN54AS174, SN54AS175A SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

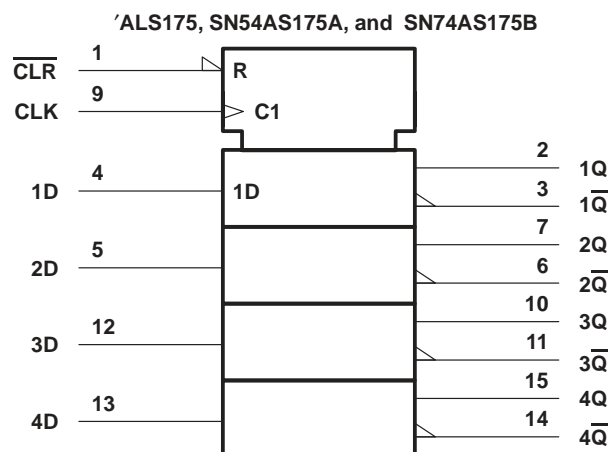
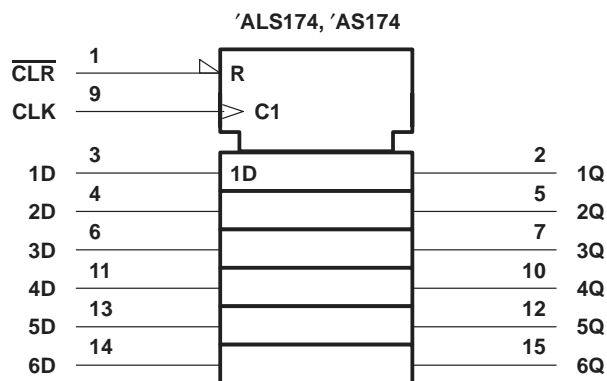
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FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS	
$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}^\dagger$
L	X	X	L	H
H	\uparrow	H	H	L
H	\uparrow	L	L	H
H	L	X	Q_0	$\overline{\text{Q}}_0$

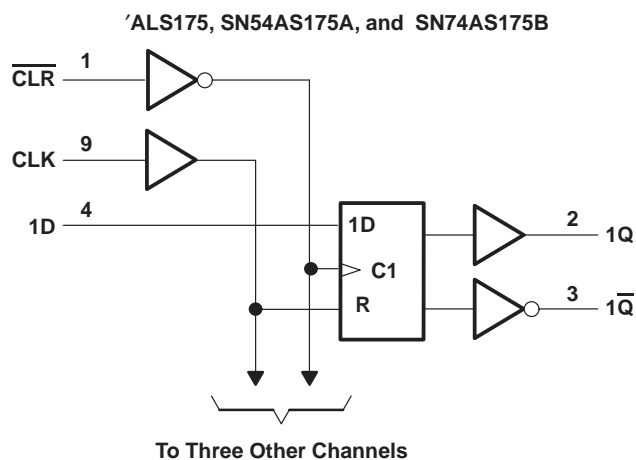
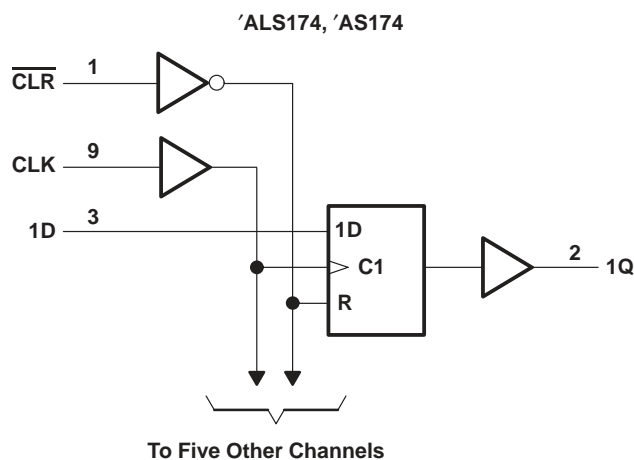
† 'ALS175, SN54AS175A, and SN74AS175B only

logic symbols ‡



‡ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

logic diagrams (positive logic)



Pin numbers shown are for the D, J, and N packages.

SN54ALS174, SN54ALS175, SN54AS174, SN54AS175A SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SDAS207C – APRIL 1982 – REVISED OCTOBER 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54ALS174, SN54ALS175	–55°C to 125°C
SN74ALS174, SN74ALS175	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
V_{IH}	High-level input voltage	2			2			V		
V_{IL}	Low-level input voltage			0.8			0.8	V		
I_{OH}	High-level output current			–0.4			–0.4	mA		
I_{OL}	Low-level output current			4			8	mA		
f_{clock}	Clock frequency	0		40	0		50	MHz		
t_w	Pulse duration	\overline{CLR} low			10			ns		
		CLK high		12.5	10					
		CLK low		12.5	10					
t_{su}	Setup time before CLK↑	Data		15	10			ns		
		\overline{CLR} inactive		8	6					
t_h	Hold time, data after CLK↑	0			0			ns		
T_A	Operating free-air temperature	–55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			–1.5			–1.5	V
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$		0.25	0.4	$I_{OL} = 4\text{ mA}$		V
		$I_{OL} = 8\text{ mA}$				$I_{OL} = 8\text{ mA}$		
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			20			20	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$	All others		–0.1		–0.1		mA
		CLK		–0.15				
$I_{O\text{§}}$	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	–20		–112	–30		–112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$, See Note 1	'ALS174		11	19	'ALS174		mA
		'ALS175		8	14	'ALS175		

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with D inputs and \overline{CLR} grounded, and CLK at 4.5 V.



**SN54ALS174, SN54ALS175, SN54AS174, SN54AS175A
SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR**

SDAS207C – APRIL 1982 – REVISED OCTOBER 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54ALS174 SN54ALS175		SN74ALS174 SN74ALS175		
			MIN	MAX	MIN	MAX	
f _{max}			40		50	MHz	
t _{PLH}	CLR	Any Q̄ ('ALS175) Any Q	3	20	5	18	ns
t _{PHL}			5	30	8	23	
t _{PLH}	CLK	Any Q (or Q, 'ALS175)	3	20	3	15	ns
t _{PHL}			5	24	5	17	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Operating free-air temperature range, T _A : SN54AS174, SN54AS175A	–55°C to 125°C
SN74AS174, SN74AS175B	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS174 SN54AS175A			SN74AS174 SN74AS175B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			–2			–2	mA
I _{OL}	Low-level output current			20			20	mA
f _{clock} *	Clock frequency	0		100	0		100	MHz
t _w *	Pulse duration	CLR low		5.5			5	ns
		CLK high		4			4	
		CLK low	'AS174		6			
t _{su} *	Setup time before CLK↑	Data	'AS174				4	ns
			SN54AS175A, SN74AS175B				3	
		CLR inactive						
t _h *	Hold time, data after CLK↑			1			1	ns
T _A	Operating free-air temperature	–55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



SN54ALS174, SN54ALS175, SN54AS174, SN54AS175A SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SDAS207C – APRIL 1982 – REVISED OCTOBER 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS174 SN54AS175A		SN74AS174 SN74AS175B		UNIT		
		MIN	TYP†	MAX	MIN		TYP†	MAX
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2		-1.2	V	
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -2\text{ mA}$	$V_{CC} - 2$		$V_{CC} - 2$			V	
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 20\text{ mA}$	0.35	0.5	0.35	0.5		V	
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$		0.1		0.1		mA	
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$		20		20		μA	
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$		-0.5		-0.5		mA	
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	-30	-112	-30	-112		mA	
I_{CC}	'AS174	$V_{CC} = 5.5\text{ V}$, See Note 2		30	45	30	45	mA
	SN54AS175A, SN74AS175B			22.5	34	22.5	34	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 2: I_{CC} is measured with D inputs, $\overline{\text{CLR}}$, and CLK grounded.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, $T_A = \text{MIN to MAX}\S$				UNIT
			SN54AS174		SN74AS174		
			MIN	MAX	MIN	MAX	
f_{max}^*			100		100		MHz
t_{PHL}	$\overline{\text{CLR}}$	Any Q	5	15	5	14	ns
t_{PLH}	CLK	Any Q	3.5	9.5	3.5	8	ns
t_{PHL}			4.5	11.5	4.5	10	

* On products compliant to MIL-STD-883, Class B, these parameters are based on characterization data but are not production tested.

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, $T_A = \text{MIN to MAX}\S$				UNIT
			SN54AS175A		SN74AS175B		
			MIN	MAX	MIN	MAX	
f_{max}^*			100		100		MHz
t_{PLH}	$\overline{\text{CLR}}$	Any Q or $\overline{\text{Q}}$	4	10	4	9	ns
t_{PHL}			4.5	15	4.5	13	
t_{PLH}	CLK	Any Q or $\overline{\text{Q}}$	4	8.5	3	7.5	ns
t_{PHL}			4	11	3	10	

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

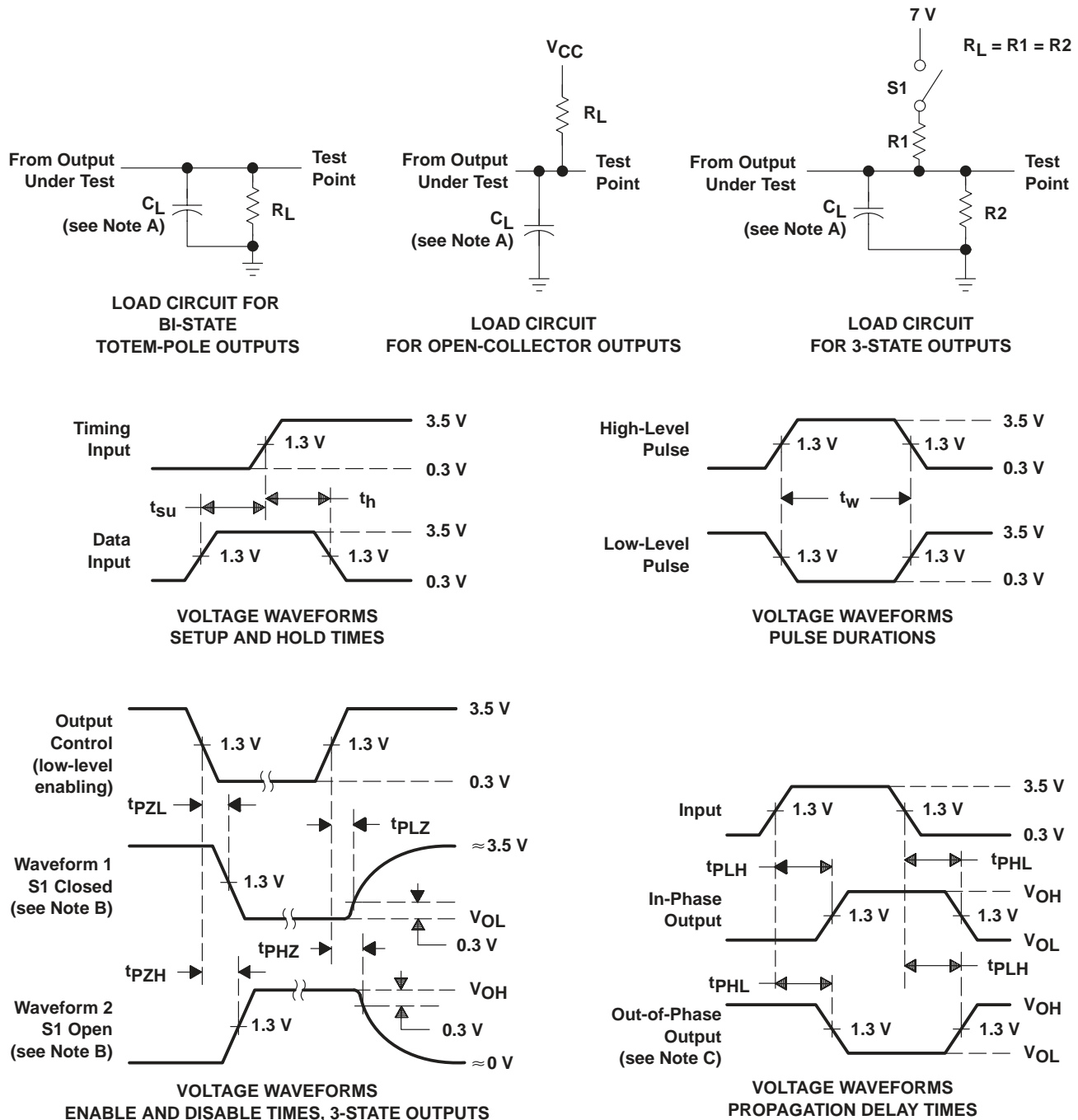
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



**SN54ALS174, SN54ALS175, SN54AS174, SN54AS175A
SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR**

SDAS207C – APRIL 1982 – REVISED OCTOBER 1995

**PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: PRR \leq 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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SN54AS175A, Quadruple D-type Flip-Flops With Clear

Device Status: Active

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Parameter Name	SN54AS175A
Voltage Nodes (V)	5

Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct-clear (CLR) input, and the 7ALS175, SN54AS175A, and SN74AS175B feature complementary outputs from each flip-flop.

Information at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

The SN54ALS174, SN54ALS175, SN54AS174, and SN54AS175A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS174, SN74ALS175, SN74AS174, and SN74AS175B are characterized for operation from 0°C to 70°C

Features

- 'ALS174 and 'AS174 Contain Six Flip-Flops With Single-Rail Outputs
- 'ALS175, SN54AS175A, and SN74AS175B Contain Four Flip-Flops With Double-Rail Outputs
- Buffered Clock and Direct-Clear Inputs
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- Fully Buffered Outputs for Maximum Isolation From External Disturbances ('AS Only)
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

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Datasheets

Full datasheet in Acrobat PDF: [sdas207c.pdf](#) (116 KB)

Full datasheet in Zipped PostScript: [sdas207c.psz](#) (114 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (°C)	Status	Price/unit USD (100-999)	Pack Qty	DSCC Number	Availability / Samples
5962-9553701Q2A	FK	20	-55 TO 125	ACTIVE	10.61	1		Check stock or order
5962-9553701QFA	W	16	-55 TO 125	ACTIVE	9.77	1		Check stock or order

SN54AS175AJ	<u>J</u>	16	-55 TO 125	ACTIVE	3.09	1		Check stock or order
SNJ54AS175AFK	<u>FK</u>	20	-55 TO 125	OBSOLETE				
SNJ54AS175AJ	<u>J</u>	16	-55 TO 125	ACTIVE	3.59	1	5962-9553701QEA	Check stock or order
SNJ54AS175AW	<u>W</u>	16	-55 TO 125	OBSOLETE				

Application Reports

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- [Advanced Schottky \(ALS and AS\) Logic Families \(SDAA010 - Updated: 08/01/1995\)](#)
- [Advanced Schottky Load Management \(SDYA016 - Updated: 02/01/1997\)](#)
- [Designing With Logic \(SDYA009C - Updated: 06/01/1997\)](#)
- [Input And Output Characteristics Of Digital Integrated Circuits \(SDYA010 - Updated: 10/01/1996\)](#)
- [Live Insertion \(SDYA012 - Updated: 10/01/1996\)](#)

Related Documents

- [Documentation Rules \(SAP\) And Ordering Information \(SZZU001B, 4 KB - Updated: 05/06/1999\)](#)
- [Logic Selection Guide Second Half 2000 \(SDYU001N, 5035 KB - Updated: 04/17/2000\)](#)
- [MicroStar Junior BGA Design Summary \(SCET004, 284 KB - Updated: 07/28/2000\)](#)
- [More Power In Less Space - Technical Article \(SCAU001A, 850 KB - Updated: 03/01/1996\)](#)

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