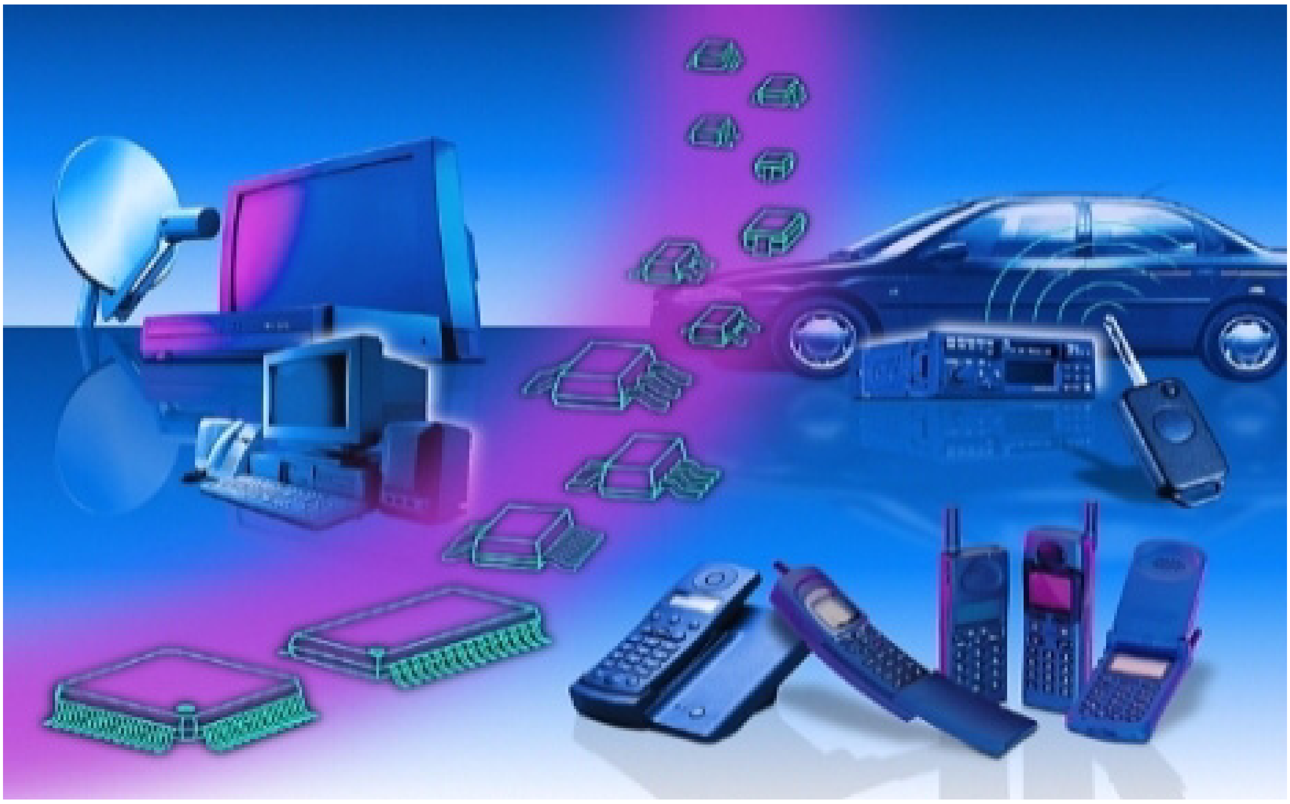

Wireless Components

ASK/FSK Transmitter 868/433 MHz

TDK 5100 Version 1.1

Specification May 2012

Preliminary **Revision History**		
Current Version: Version 1.1 as of 09.05.2012		
Previous Version: Version 1.0 as of 31.10.2002		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
Product Info	Product Info	Package Info corrected to PG-TSSOP-16 Ordering Code corrected to SP000014557

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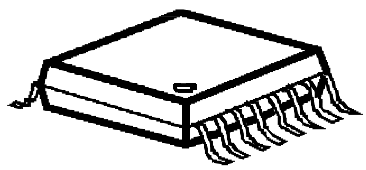
Product Info

General Description

The TDK 5100 is a single chip ASK/FSK transmitter for the frequency bands 433-435 and 868-870 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery life. Additionally features like a power down mode, a low power detect, a selectable crystal oscillator frequency and a divided clock output are implemented. The IC can be used for both ASK and FSK modulation.

Package



Features

- fully integrated frequency synthesizer
- VCO without external components
- ASK and FSK modulation
- switchable frequency range 433-435 MHz / 868-870 MHz
- high efficiency power amplifier (typically 5 dBm / 2 dBm)
- low supply current (typically 7mA)
- voltage supply range 2.1 - 4 V
- temperature range -40 ... +125°C
- power down mode
- low voltage sensor
- selectable crystal oscillator 6.78 MHz / 13.56 MHz
- programmable divided clock output for µC
- low external component count

Applications

- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

Ordering Information

Type	Ordering Code	Package
TDK 5100	SP000014557	PG-TSSOP-16
available on tape and reel		

1 Product Description

Contents of this Chapter

1.1 Overview

The TDK 5100 is a single chip ASK/FSK transmitter for the frequency bands 433-435 MHz and 868-870 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery life. Additional features like a power down mode, a low power detect, a selectable crystal oscillator frequency and a divided clock output are implemented. The IC can be used for both ASK and FSK modulation.

1.2 Applications

- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

1.3 Features

- fully integrated frequency synthesizer
- VCO without external components
- ASK and FSK modulation
- switchable frequency range 433-435 MHz / 868-870 MHz
- high efficiency power amplifier (typically 5 dBm / 2 dBm)
- low supply current (typically 7 mA)
- voltage supply range 2.1 - 4 V
- temperature range -40°C ... 125°C
- power down mode
- low voltage sensor
- selectable crystal oscillator 6.78 MHz / 13.56 MHz
- programmable divided clock output for µC
- low external component count

1.4 Package Outlines

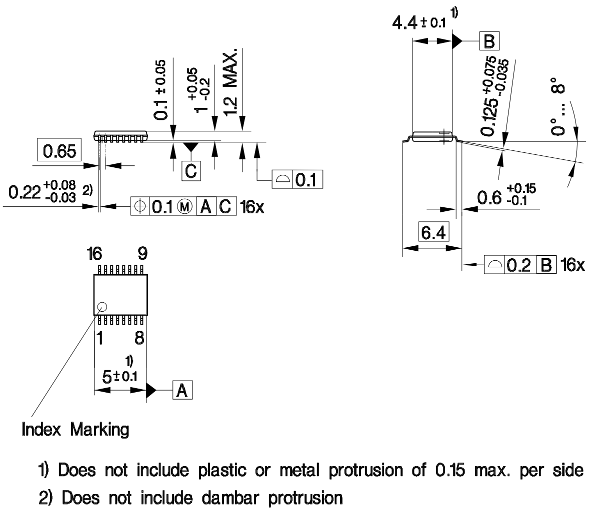
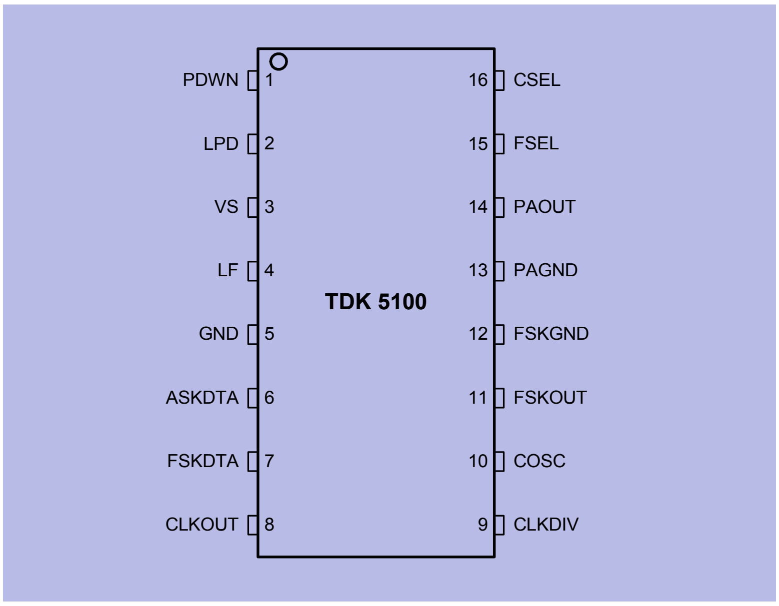


Figure 1-1 PG-TSSOP-16

2 Functional Description

Contents of this Chapter

2.1 Pin Configuration



Pin_config.wmf

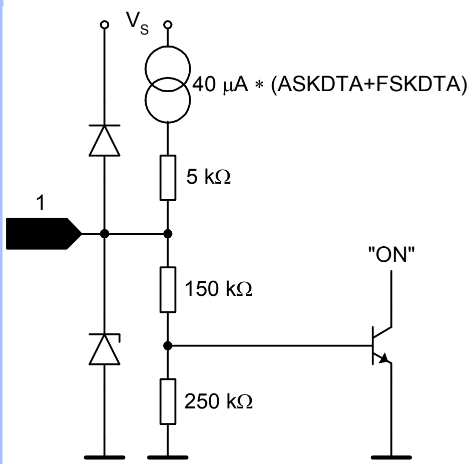
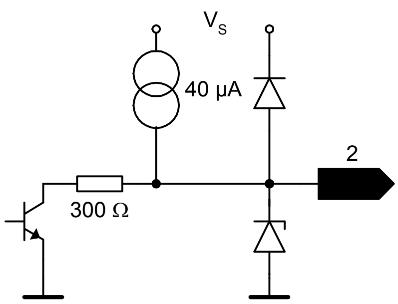
Figure 2-1 IC Pin Configuration

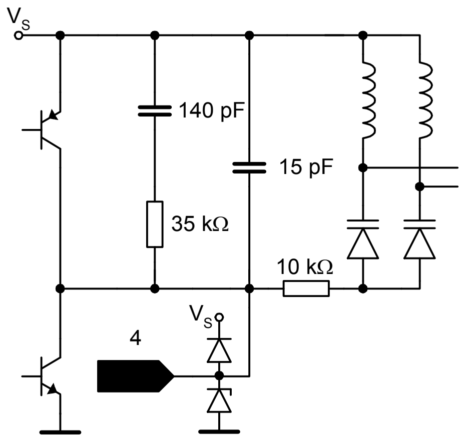
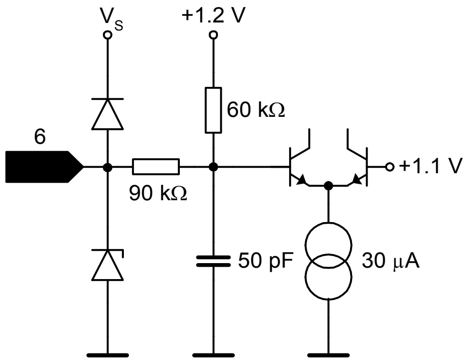
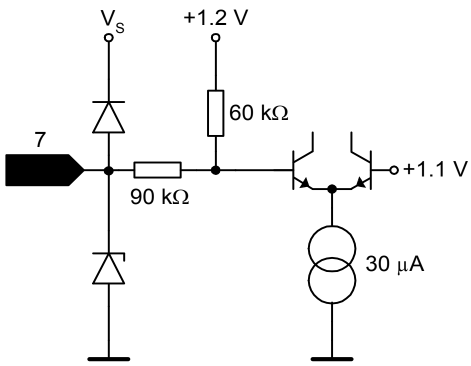
Table 2-1

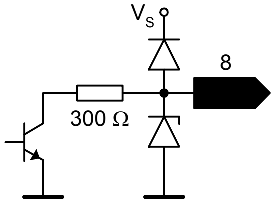
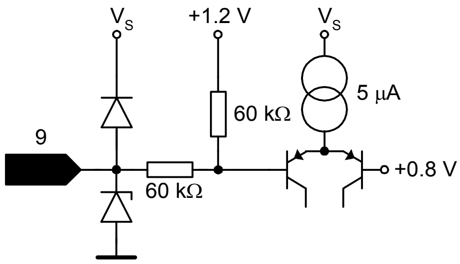
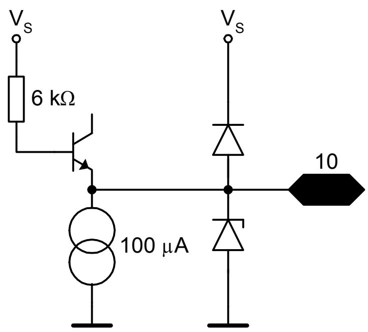
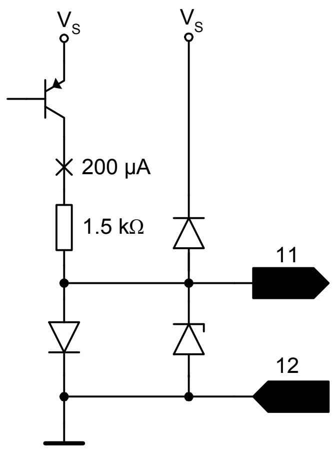
Pin No.	Symbol	Function
1	PDWN	Power Down Mode Control
2	LPD	Low Power Detect Output
3	VS	Voltage Supply
4	LF	Loop Filter
5	GND	Ground
6	ASKDTA	Amplitude Shift Keying Data Input
7	FSKDTA	Frequency Shift Keying Data Input
8	CLKOUT	Clock Driver Output
9	CLKDIV	Clock Divider Control (847.5 kHz or 3.34 MHz)
10	COSC	Crystal Oscillator Input
11	FSKOUT	Frequency Shift Keying Switch Output
12	FSKGND	Frequency Shift Keying Ground
13	PAGND	Power Amplifier Ground
14	PAOUT	Power Amplifier Output
15	FSEL	Frequency Range Selection (433 or 868 MHz)
16	CSEL	Crystal Frequency Selection (6.78 or 13.56 MHz)

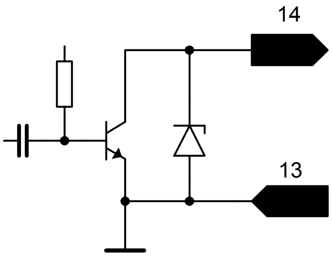
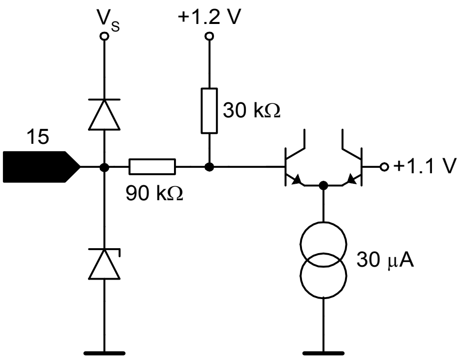
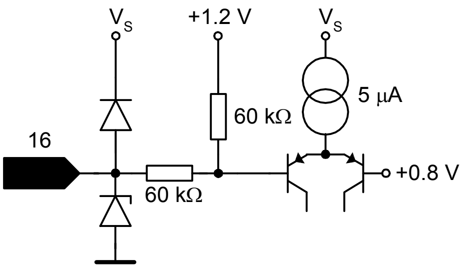
2.2 Pin Definitions and Functions

Table 2-2

Pin No.	Symbol	Interface Schematic*)	Function
1	PDWN		Disable pin for the complete transmitter circuit. A logic low (PDWN < 0.7 V) turns off all transmitter functions. A logic high (PDWN > 1.5 V) gives access to all transmitter functions. PDWN input will be pulled up by 40 µA internally by either setting FSKDTA or ASKDTA to a logic high-state.
2	LPD		This pin provides an output indicating the low-voltage state of the supply voltage VS. VS < 2.15 V will set LPD to the low-state. An internal pull-up current of 40 µA gives the output a high-state at supply voltages above 2.15 V.
3	VS		This pin is the positive supply of the transmitter electronics. An RF bypass capacitor should be connected directly to this pin and returned to GND (pin 5) as short as possible.

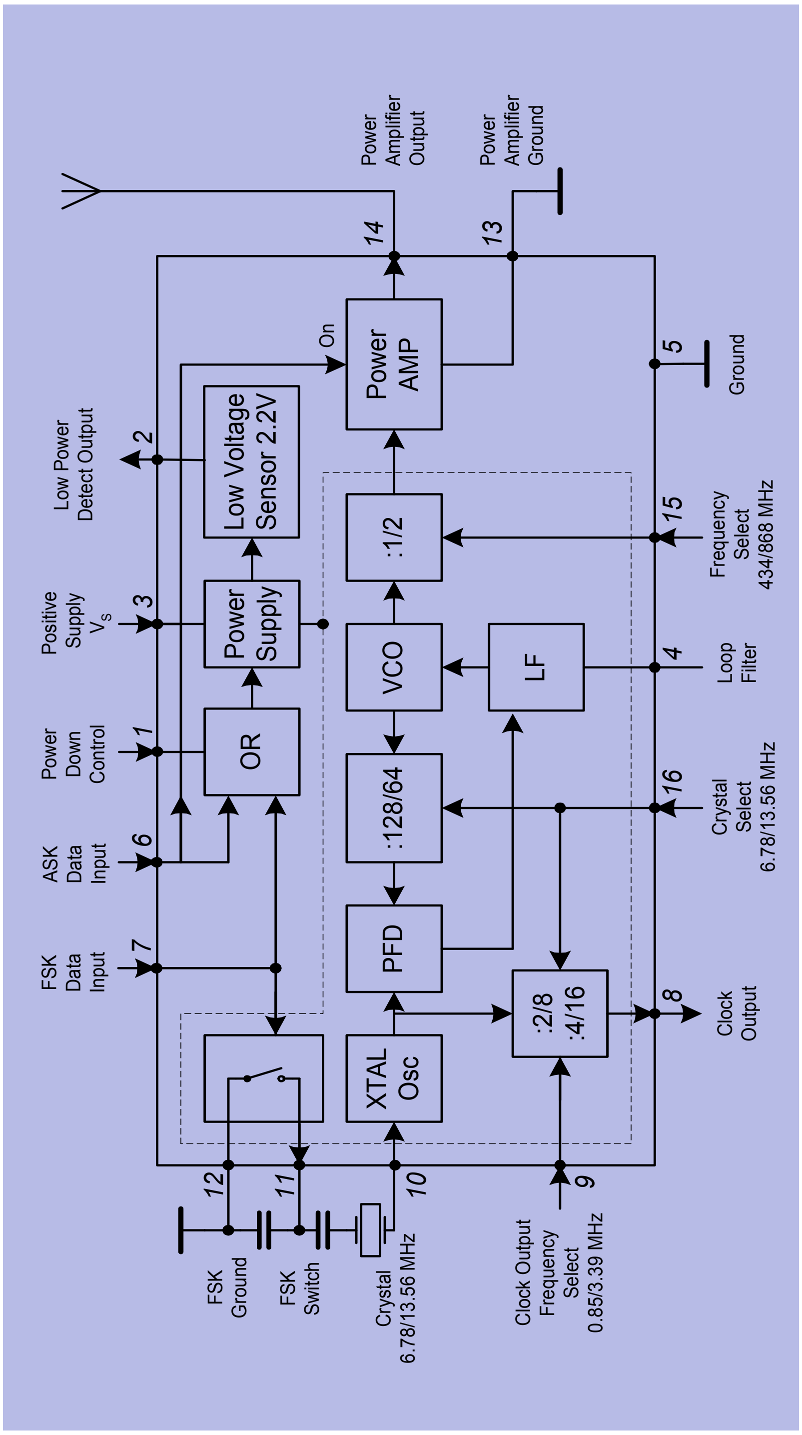
4	LF		Output of the charge pump and input of the VCO control voltage. The loop bandwidth of the PLL is 150 kHz when only the internal loop filter is used. The loop bandwidth may be reduced by applying an external RC network referencing to the positive supply VS (pin 3).
5	GND		General ground connection.
6	ASKDTA		Digital amplitude modulation can be imparted to the Power Amplifier through this pin. A logic high (ASKDTA > 1.5 V or open) enables the Power Amplifier. A logic low (ASKDTA < 0.5 V) disables the Power Amplifier.
7	FSKDTA		Digital frequency modulation can be imparted to the Xtal Oscillator by this pin. The VCO-frequency varies in accordance to the frequency of the reference oscillator. A logic high (FSKDTA > 1.5V or open) sets the FSK switch to a high impedance state. A logic low (FSKDTA < 0.5 V) closes the FSK switch from FSKOUT (pin 11) to FSKGND (pin 12). A capacitor can be switched to the reference crystal network this way. The Xtal Oscillator frequency will be shifted giving the designed FSK frequency deviation.

8	CLKOUT		Clock output to supply an external device. An external pull-up resistor has to be added in accordance to the driving requirements of the external device. A clock frequency of 3.39 MHz is selected by a logic low at CLKDIV input (pin9). A clock frequency of 847.5 kHz is selected by a logic high at CLKDIV input (pin9).
9	CLKDIV		This pin is used to select the desired clock division rate for the CLKOUT signal. A logic low (CLKDIV < 0.2 V) applied to this pin selects the 3.39 MHz output signal at CLKOUT (pin 8). A logic high (CLKDIV open) applied to this pin selects the 847.5 kHz output signal at CLKOUT (pin 8).
10	COSC		This pin is connected to the reference oscillator circuit. The reference oscillator is working as a negative impedance converter. It presents a negative resistance in series to an inductance at the COSC pin.
11	FSKOUT		This pin is connected to a switch to FSK-GND (pin 12). The switch is closed when the signal at FSKDTA (pin 7) is in a logic low state. The switch is open when the signal at FSKDTA (pin 7) is in a logic high state. FSKOUT can switch an additional capacitor to the reference crystal network to pull the crystal frequency by an amount resulting in the desired FSK frequency shift of the transmitter output frequency.
12	FSKGND		Ground connection for FSK modulation output FSKOUT.

13	PAGND		Ground connection of the power amplifier. The RF ground return path of the power amplifier output PAOUT (pin 14) has to be concentrated to this pin.
14	PAOUT		RF output pin of the transmitter. A DC path to the positive supply VS has to be supplied by the antenna matching network.
15	FSEL		This pin is used to select the desired transmitter frequency. A logic low (FSEL < 0.5 V) applied to this pin sets the transmitter to the 433 MHz frequency range. A logic high (FSEL open) applied to this pin sets the transmitter to the 868 MHz frequency range.
16	CSEL		This pin is used to select the desired reference frequency. A logic low (CSEL < 0.2 V) applied to this pin sets the internal frequency divider to accept a reference frequency of 6.78 MHz. A logic high (CSEL open) applied to this pin sets the internal frequency divider to accept a reference frequency of 13.56 MHz.

*) Indicated voltages and currents apply for PLL Enable Mode and Transmit Mode.
In Power Down Mode, the values are zero or high-ohmic.

2.3 Functional Block diagram



Block_diagram.wmf

Figure 2-2 Functional Block diagram

2.4 Functional Blocks

2.4.1 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a Voltage Controlled Oscillator (VCO), an asynchronous divider chain, a phase detector, a charge pump and a loop filter. It is fully implemented on chip. The tuning circuit of the VCO consisting of spiral inductors and varactor diodes is on chip, too. Therefore no additional external components are necessary. The nominal center frequency of the VCO is 869 MHz. The oscillator signal is fed both, to the synthesizer divider chain and to the power amplifier. The overall division ratio of the asynchronous divider chain is 128 in case of a 6.78 MHz crystal or 64 in case of a 13.56 MHz crystal and can be selected via CSEL (pin 16). The phase detector is a Type IV PD with charge pump. The passive loop filter is realized on chip.

2.4.2 Crystal Oscillator

The crystal oscillator operates either at 6.78 MHz or at 13.56 MHz.

The reference frequency can be chosen by the signal at CSEL (pin 16).

Table 2-3

CSEL (pin 16)	Crystal Frequency
Low*)	6.78 MHz
Open†)	13.56 MHz

*) Low: Voltage at pin < 0.2 V
†) Open: Pin open

For both quartz frequency options, 847.5 kHz or 3.39 MHz are available as output frequencies of the clock output CLKOUT (pin 8) to drive the clock input of a micro controller.

The frequency at CLKOUT (pin 8) is controlled by the signal at CLKDIV (pin 9)

Table 2-4

CLKDIV (pin 9)	CLKOUT Frequency
Low*)	3.39 MHz
Open†)	847.5 kHz

*) Low: Voltage at pin < 0.2 V
†) Open: Pin open

To achieve FSK transmission, the oscillator frequency can be detuned by a fixed amount by switching an external capacitor via FSKOUT (pin 11).

The condition of the switch is controlled by the signal at FSKDTA (pin 7).

Table 2-5

FSKDTA (pin7)	FSK Switch
Low*)	CLOSED
Open†), High‡)	OPEN

*) Low: Voltage at pin < 0.5 V
†) Open: Pin open
‡) High: Voltage at pin > 1.5 V

2.4.3 Power Amplifier

In case of operation in the 868-870 MHz band, the power amplifier is fed directly from the voltage controlled oscillator. In case of operation in the 433-435 MHz band, the VCO frequency is divided by 2. This is controlled by FSEL (pin 15) as described in the table below.

Table 2-6

FSEL (pin 15)	Radiated Frequency Band
Low*)	433 MHz
Open†)	868 MHz

*) Low: Voltage at pin < 0.5 V
†) Open: Pin open

The Power Amplifier can be switched on and off by the signal at ASKDTA (pin 6).

Table 2-7

ASKDTA (pin 6)	Power Amplifier
Low*)	OFF
Open†), High‡)	ON

*) Low: Voltage at pin < 0.5 V
†) Open: Pin open
‡) High: Voltage at pin > 1.5 V

The Power Amplifier has an Open Collector output at PAOUT (pin 14) and requires an external pull-up coil to provide bias. The coil is part of the tuning and matching LC circuitry to get best performance with the external loop antenna. To achieve the best power amplifier efficiency, the high frequency voltage swing at PAOUT (pin 14) should be twice the supply voltage.

The power amplifier has its own ground pin PAGND (pin 13) in order to reduce the amount of coupling to the other circuits.

2.4.4 Low Power Detect

The supply voltage is sensed by a low power detector. When the supply voltage drops below 2.15 V, the output LPD (pin 2) switches to the low-state. To minimize the external component count, an internal pull-up current of 40 µA gives the output a high-state at supply voltages above 2.15 V.

The output LPD (pin 2) can either be connected to ASKDTA (pin 6) to switch off the PA as soon as the supply voltage drops below 2.15 V or it can be used to inform a micro-controller to stop the transmission after the current data packet.

2.4.5 Power Modes

The IC provides three power modes, the POWER DOWN MODE, the PLL ENABLE MODE and the TRANSMIT MODE.

2.4.5.1 Power Down Mode

In the POWER DOWN MODE the complete chip is switched off.

The current consumption is typically 0.3 nA at 3 V 25°C.

This current doubles every 8°C. The values for higher temperatures are typically 14 nA at 85°C and typically 600 nA at 125°C.

2.4.5.2 PLL Enable Mode

In the PLL ENABLE MODE the PLL is switched on but the power amplifier is turned off to avoid undesired power radiation during the time the PLL needs to settle. The turn on time of the PLL is determined mainly by the turn on time of the crystal oscillator and is less than 1 msec when the specified crystal is used.

The current consumption is typically 3.5 mA.

2.4.5.3 Transmit Mode

In the TRANSMIT MODE the PLL is switched on and the power amplifier is turned on too.

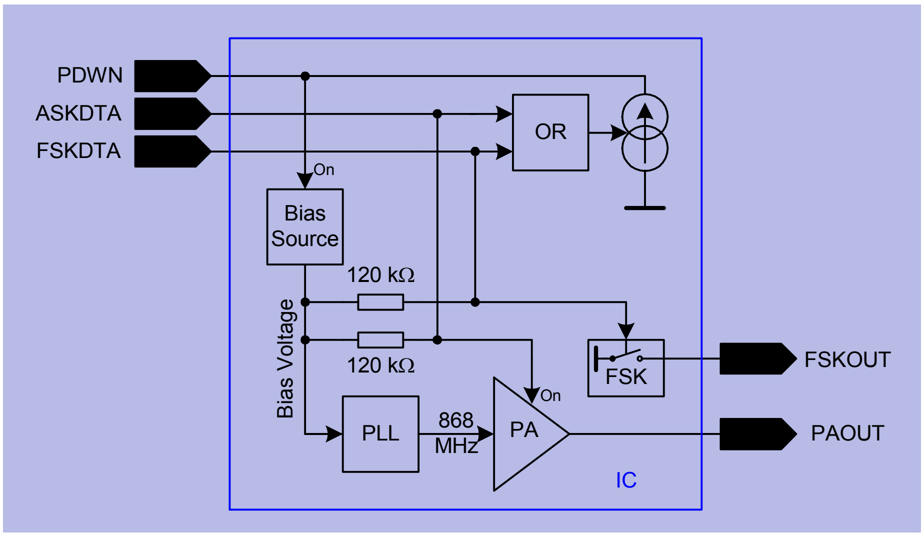
The current consumption of the IC is typically 7 mA when using a proper transforming network at PAOUT, see Figure 3-1.

2.4.5.4 Power mode control

The bias circuitry is powered up via a voltage V > 1.5 V at the pin PDWN (pin 1). When the bias circuitry is powered up, the pins ASKDTA and FSKDTA are pulled up internally.
Forcing the voltage at the pins low overrides the internally set state.

Alternatively, if the voltage at ASKDTA or FSKDTA is forced high externally, the PDWN pin is pulled up internally via a current source. In this case, it is not necessary to connect the PDWN pin, it is recommended to leave it open.

The principle schematic of the power mode control circuitry is shown in Figure 3-5.



Power_Mode.wmf

Figure 2-5 Power mode control circuitry

Table 3-8 provides a listing of how to get into the different power modes

Table 2-8

PDWN	FSKDTA	ASKDTA	MODE
Low*)	Low, Open	Low, Open	POWER DOWN
Open†)	Low	Low	
High‡)	Low, Open, High	Low	PLL ENABLE
Open	High	Low	
High	Low, Open, High	Open, High	TRANSMIT
Open	High	Open, High	
Open	Low, Open, High	High	

*) Low: Voltage at pin < 0.7 V (PDWN)
Voltage at pin < 0.5 V (FSKDTA, ASKDTA)
†) Open: Pin open
‡) High: Voltage at pin > 1.5 V

Other combinations of the control pins PDWN, FSKDTA and ASKDTA are not recommended.

2.4.6 Recommended timing diagrams for ASK- and FSK-Modulation

ASK Modulation using FSKDTA and ASKDTA, PDWN not connected

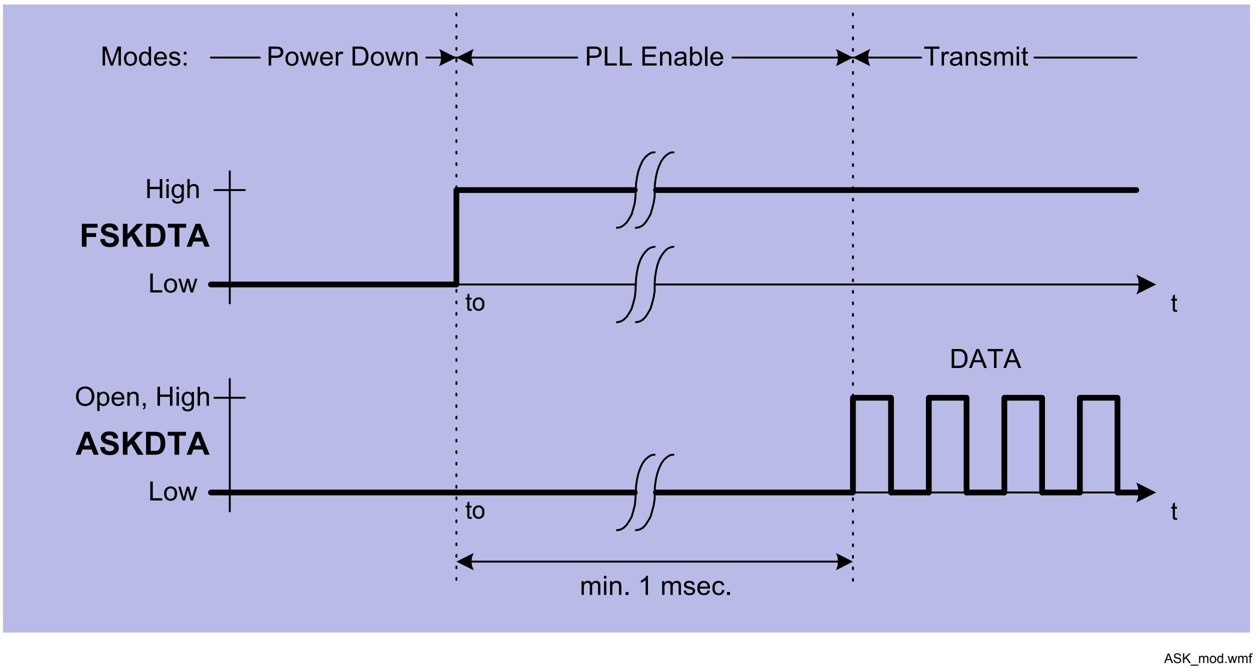


Figure 2-6 ASK Modulation

FSK Modulation using FSKDTA and ASKDTA, PDWN not connected

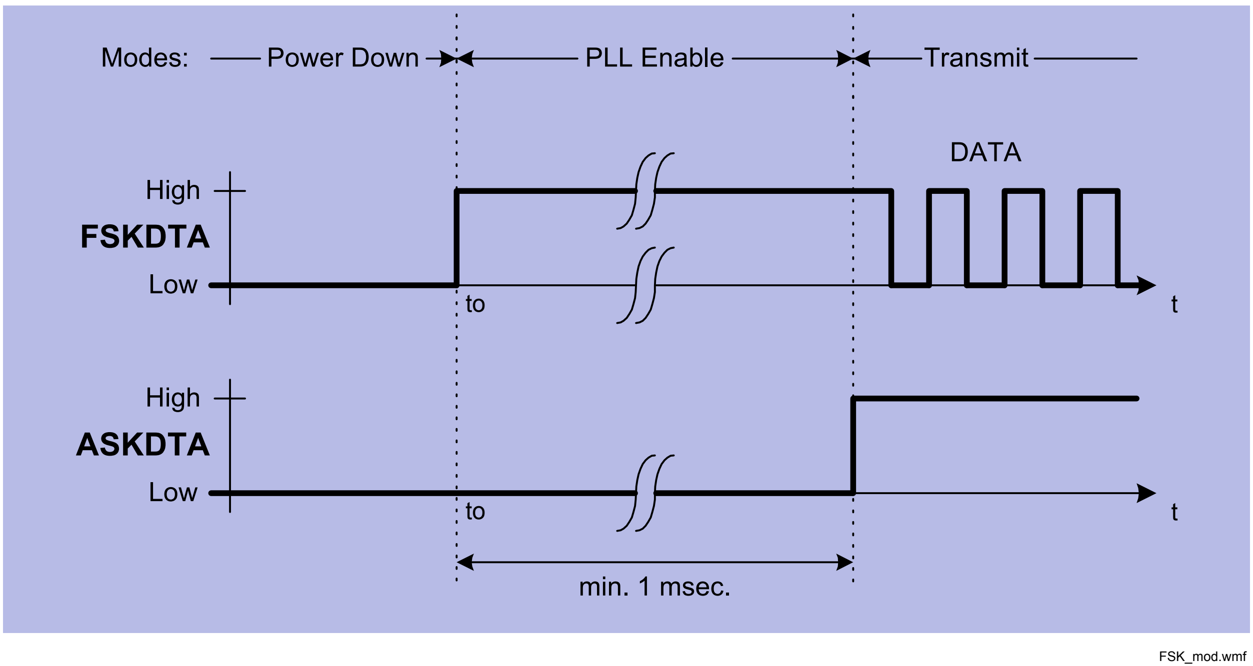


Figure 2-7 FSK Modulation

Alternative ASK Modulation, FSKDTA not connected.

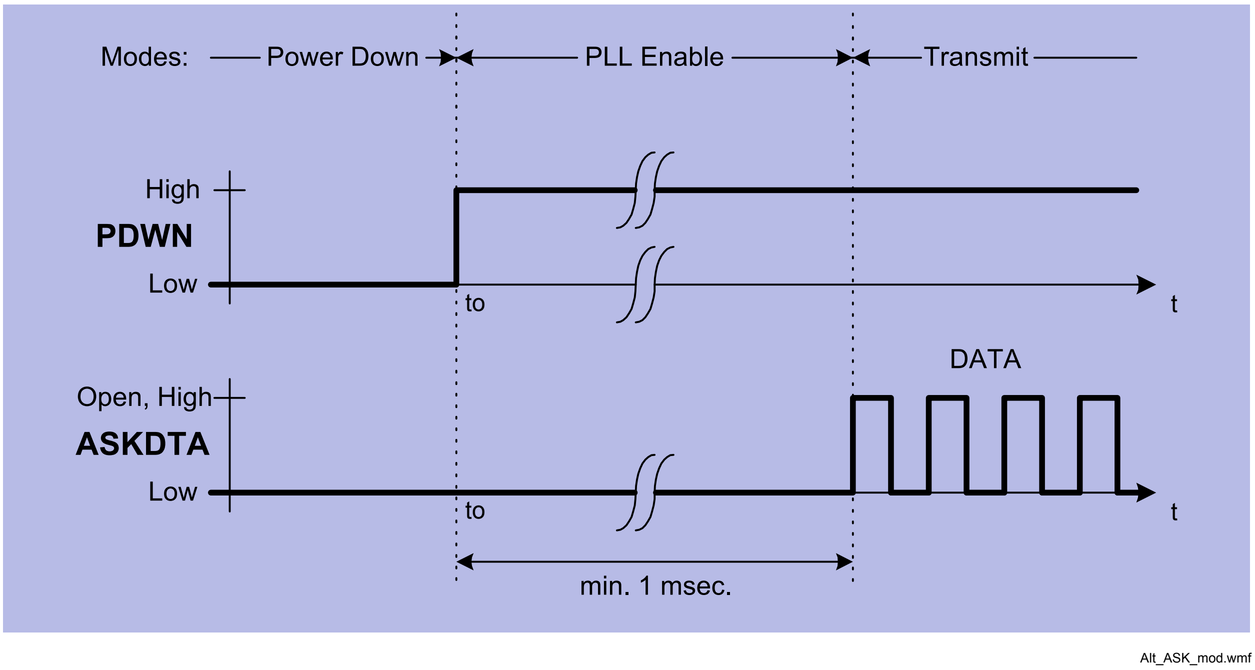


Figure 2-8 Alternative ASK Modulation

Alternative FSK Modulation

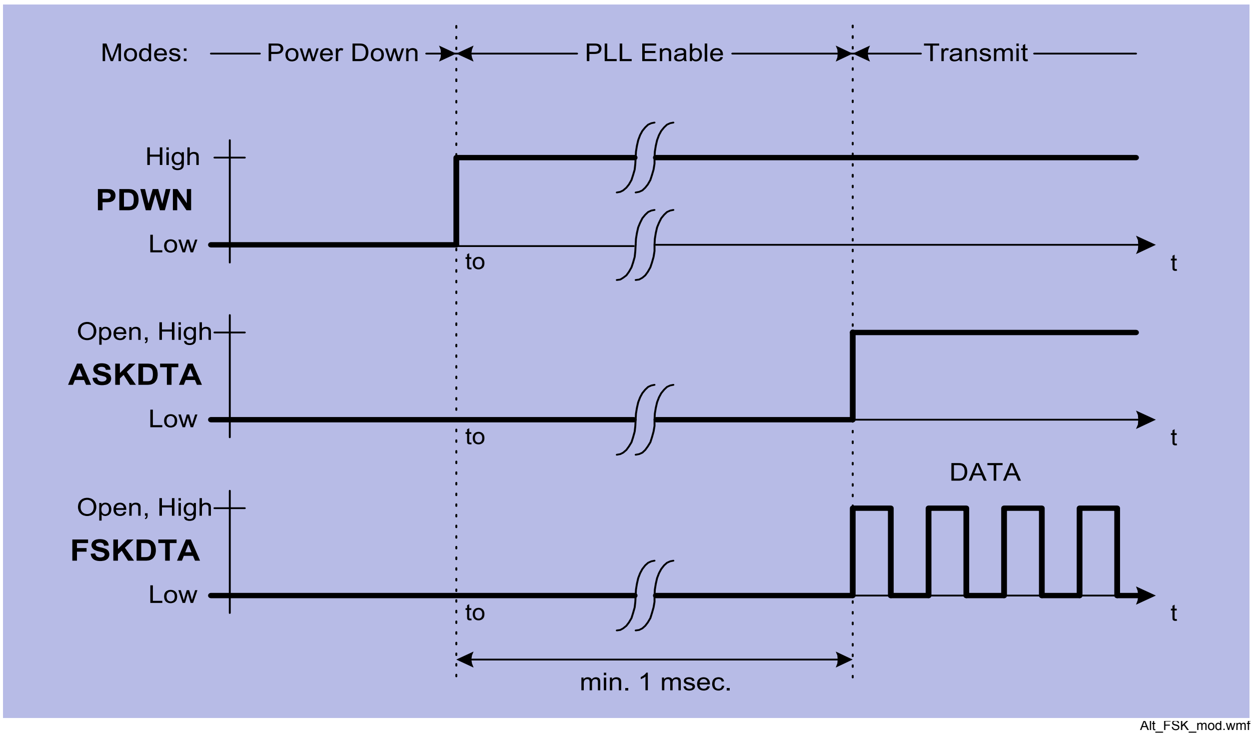
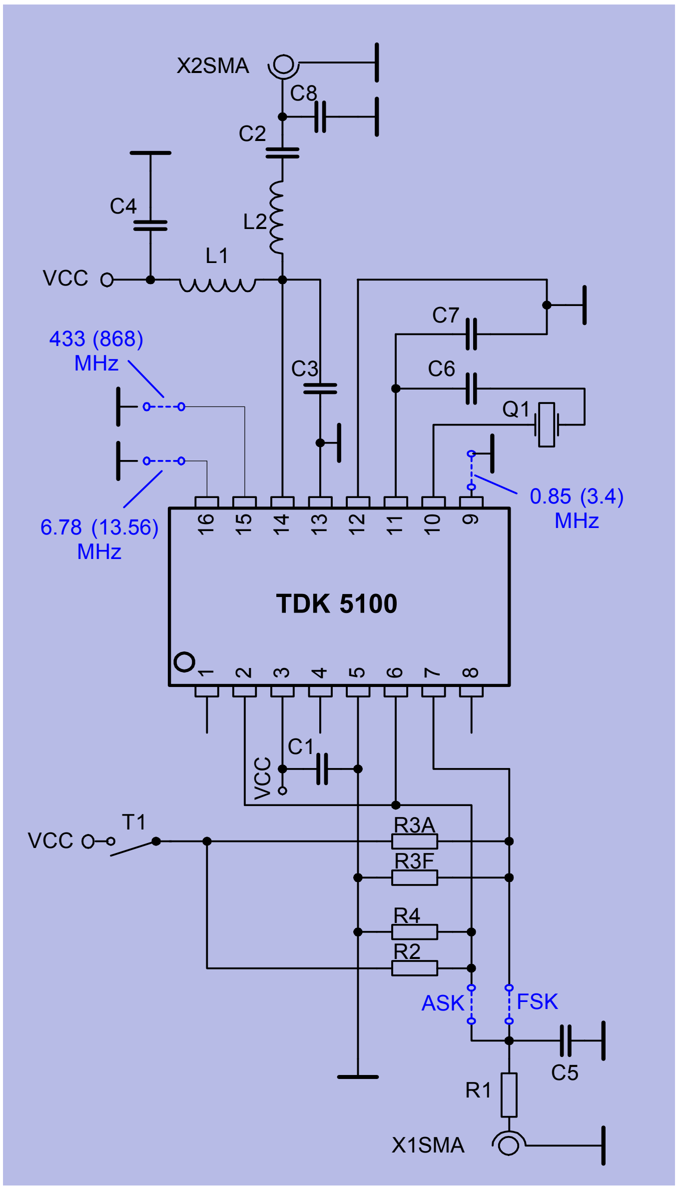


Figure 2-9 Alternative FSK Modulation

3 Applications

Contents of this Chapter

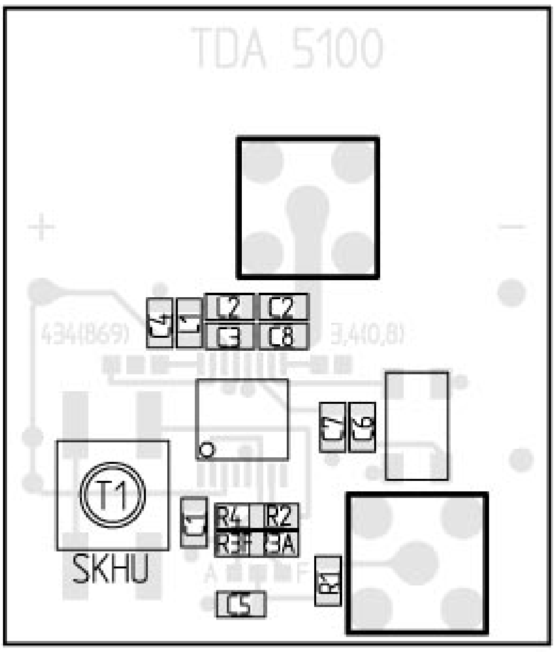
3.1 50 Ohm-Output Testboard Schematic



50ohm_test_v5.wmf

Figure 3-1 50 Ω - output testboard schematic

3.2 50 Ohm-Output Testboard Layout



Oben (3.00 09/14/99 tda5100_v5.tc)

Figure 3-2 Top Side of TDK 5100-Testboard with 50 Ω - Output

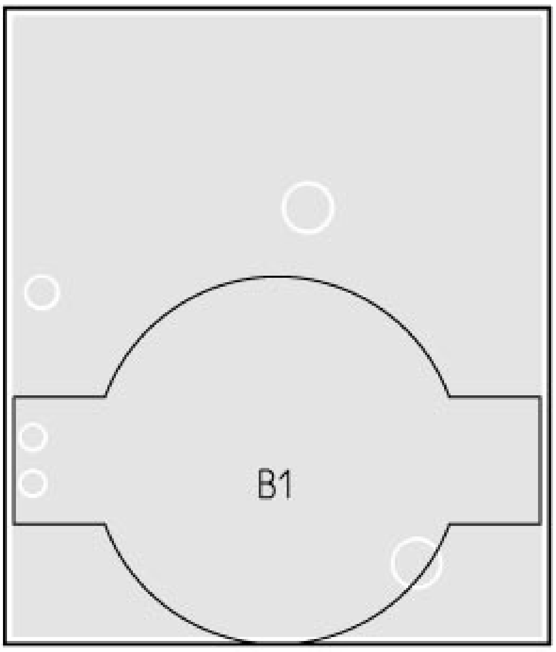


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Figure 3-3 Bottom Side of TDK 5100-Testboard with 50 Ω - Output

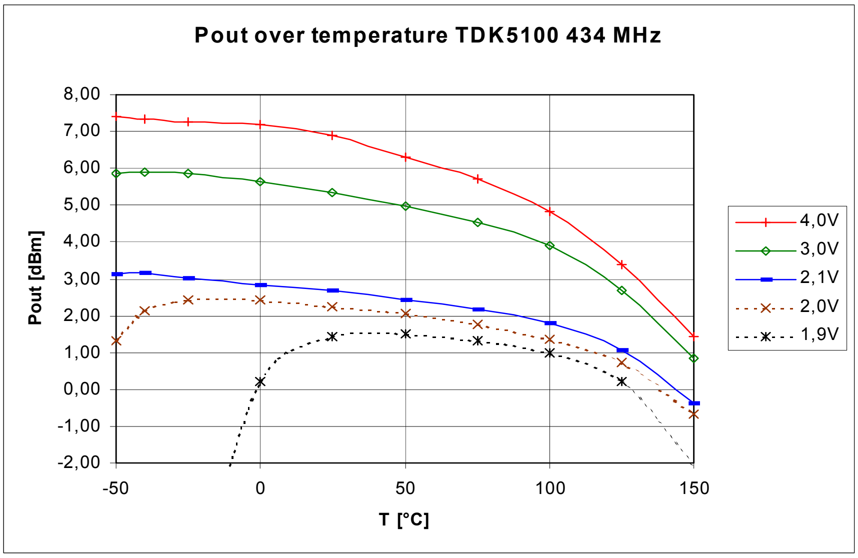
3.3 Bill of material (50 Ohm-Output Testboard)

Table 3-1 Bill of material

Part	Value	434 MHz	869 MHz	ASK	FSK	Specification
R1	4.7 kΩ					0805, ± 5%
R2					12 kΩ	0805, ± 5%
R3A				15 kΩ		0805, ± 5%
R3F					15 kΩ	0805, ± 5%
R4	open					0805, ± 5%
C1	47 nF					0805, X7R, ± 10%
C2		39 pF	47 pF			0805, COG, ± 5%
C3		3.9 pF	1.8 pF			0805, COG, ± 0.1 pF
C4		330 pF	100 pF			0805, COG, ± 5%
C5	1 nF					0805, X7R, ± 10%
C6	8.2 pF					0805, COG, ± 0.1 pF
C7				0Ω Jumper	434MHz: 22 pF 868MHz: 47pF	0805, COG, ± 5% 0805, 0Ω Jumper
C8		15 pF	8.2 pF			0805, COG, ± 5%
L1		100 nH	33 nH			TOKO LL2012-J
L2		39 nH	15 nH			39 nH: TOKO LL2012-J 15 nH: TOKO LL1608-J
Q1	13.56875 MHz, CL=20pF					Tokyo Denpa TSS-3B 13568.75 kHz Spec.No. 10-50205
IC1	TDK5100					
T1	Push-button					replaced by a short
X1	SMA-S					SMA standing
X2	SMA-S					SMA standing

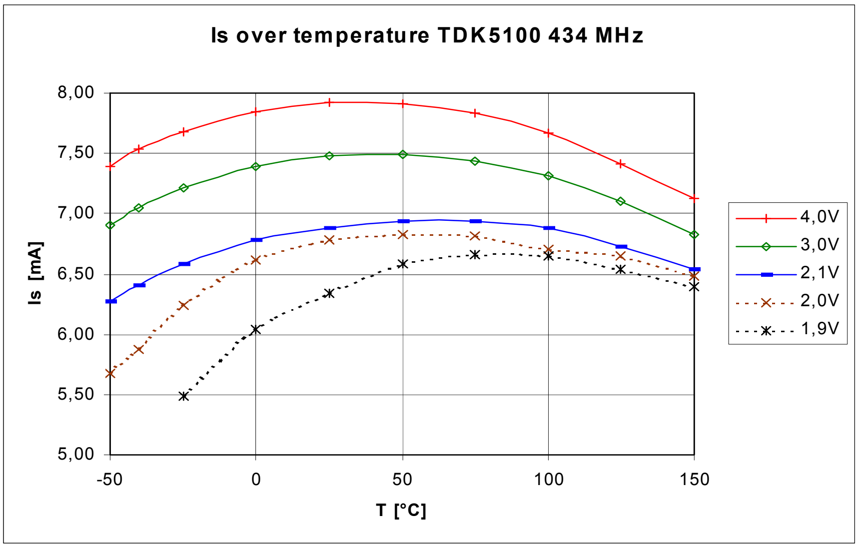
3.4 50 Ohm-Output Testboard: Measurement results

Note the specified operating range: 2.1 V to 4.0 V and -40°C to +125°C.



pout_over_temp_434.wmf

Figure 3-4 Output power over temperature of the 50 Ω - testboard with TDK 5100 at 434 MHz



Is_over_temp_434.wmf

Figure 3-5 Supply current over temperature of the 50 Ω - testboard with TDK 5100 at 434 MHz

Note the specified operating range: 2.1 V to 4.0 V and -40°C to +125°C.

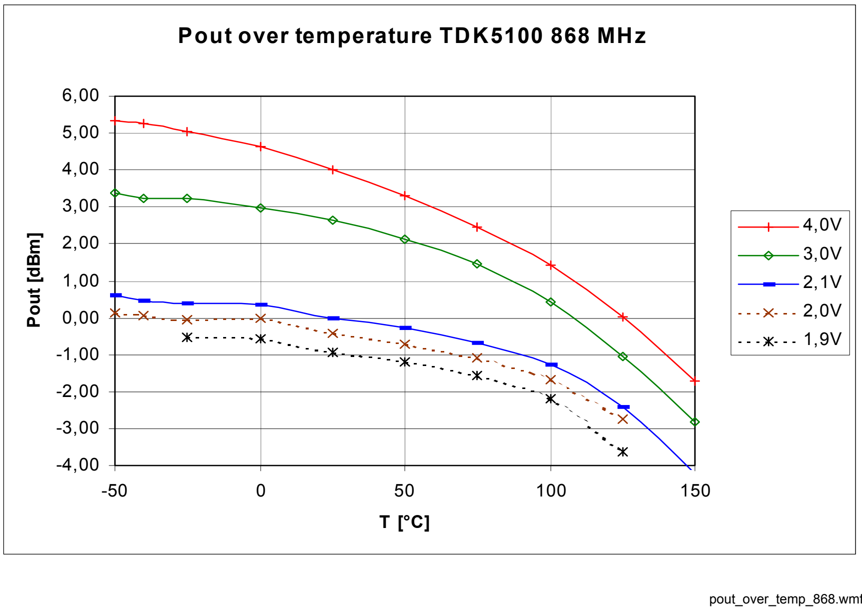


Figure 3-6 Output power over temperature of the 50 Ω - testboard with TDK 5100 at 868 MHz

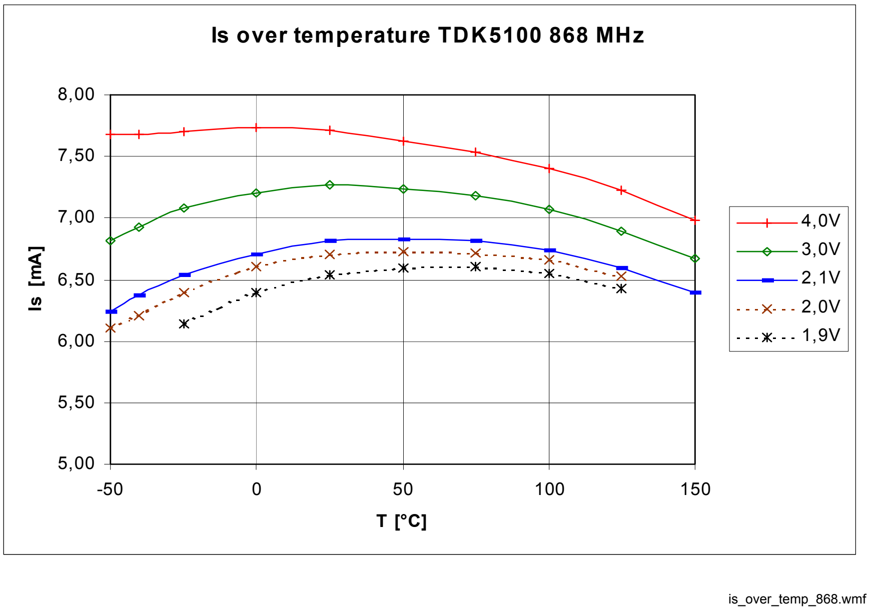
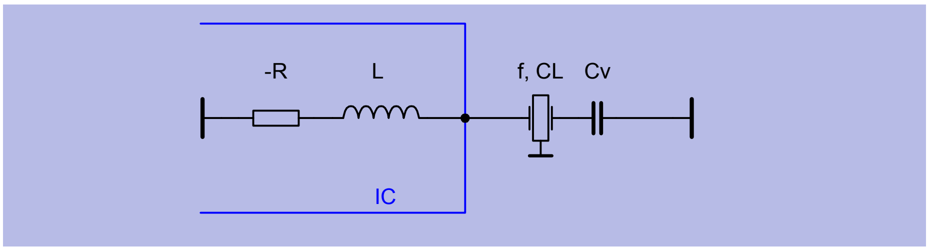


Figure 3-7 Supply current over temperature of the 50 Ω - testboard with TDK 5100 at 868 MHz

3.5 Application Hints on the Crystal Oscillator

1. Application Hints on the crystal oscillator

The crystal oscillator achieves a turn on time less than 1 msec when the specified crystal is used. To achieve this, a NIC oscillator type is implemented in the TDK 5100. The input impedance of this oscillator is a negative resistance in series to an inductance. Therefore the load capacitance of the crystal CL (specified by the crystal supplier) is transformed to the capacitance Cv.



$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 L}$$ Formula 1)

CL: crystal load capacitance for nominal frequency

ω: angular frequency

L: inductance of the crystal oscillator

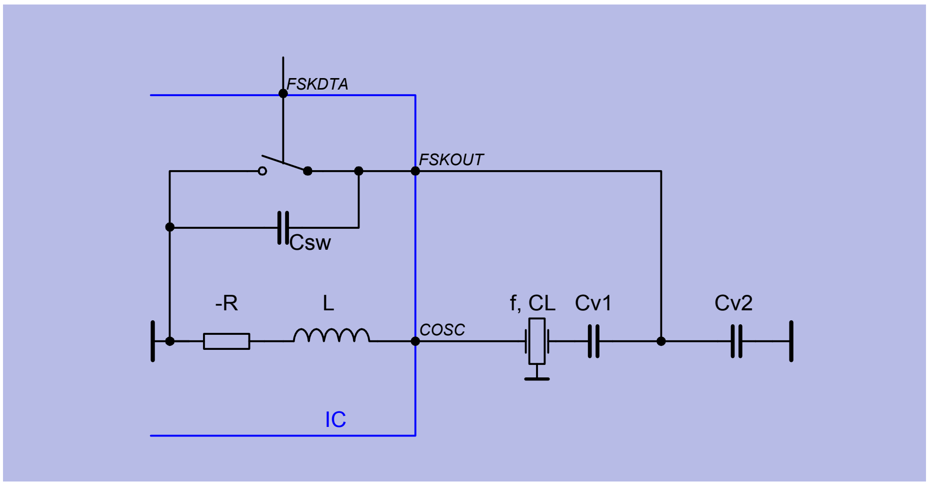
Example for the ASK-Mode:

Referring to the application circuit, in ASK-Mode the capacitance C7 is replaced by a short to ground. Assume a crystal frequency of 13.56 MHz and a crystal load capacitance of CL = 20 pF. The inductance L at 13.5 MHz is about 4.6 mH. Therefore C6 is calculated to 12 pF.

$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 L} = C6$$

Example for the FSK-Mode:

FSK modulation is achieved by switching the load capacitance of the crystal as shown below.



The frequency deviation of the crystal oscillator is multiplied with the divider factor N of the Phase Locked Loop to the output of the power amplifier. In case of small frequency deviations (up to +/- 1000 ppm), the two desired load capacitances can be calculated with the formula below.

$$CL\pm = \frac{CL \mp C0\frac{\Delta f}{N * f1}(1+\frac{2(C0+CL)}{C1})}{1 \pm \frac{\Delta f}{N * f1}(1+\frac{2(C0+CL)}{C1})}$$

C_L: crystal load capacitance for nominal frequency
C_0: shunt capacitance of the crystal
f: frequency
ω: $\omega = 2\pi f$: angular frequency
N: division ratio of the PLL
df: peak frequency deviation

Because of the inductive part of the TDK 5100, these values must be corrected by Formula 1). The value of Cv± can be calculated.

$$Cv\pm = \frac{1}{\frac{1}{CL\pm} + \omega^2 L}$$

If the FSK switch is closed, Cv_ is equal to Cv1 (C6 in the application diagram). If the FSK switch is open, Cv2 (C7 in the application diagram) can be calculated.

$$Cv2 = C7 = \frac{Csw * Cv1 - (Cv+) * (Cv1 + Csw)}{(Cv+) - Cv1}$$

Csw: parallel capacitance of the FSK switch (3 pF incl. layout parasitics)

Remark: These calculations are only approximations. The necessary values depend on the layout also and must be adapted for the specific application board.

3.6 Design Hints on the Clock Output (CLKOUT)

The CLKOUT pin is an open collector output. An external pull up resistor (RL) should be connected between this pin and the positive supply voltage. The value of RL is depending on the clock frequency and the load capacitance CLD (PCB board plus input capacitance of the microcontroller). RL can be calculated to:

$$RL = \frac{1}{fCLKOUT * 8 * CLD}$$

Table 3-2

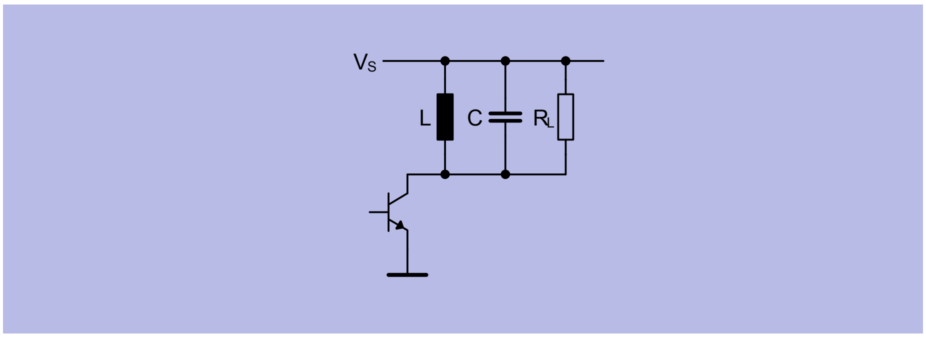
fCLKOUT= 847 kHz		fCLKOUT= 3.39 MHz	
CL[pF]	RL[kOhm]	CL[pF]	RL[kOhm]
5	27	5	6.8
10	12	10	3.3
20	6.8	20	1.8

Remark: To achieve a low current consumption and a low spurious radiation, the largest possible RL should be chosen.

Even harmonics of the signal at CLKOUT can interact with the crystal oscillator input COSC preventing the start-up of oscillation. Care must be taken in layout by sufficient separation of the signal lines to ensure sufficiently small coupling.

3.7 Application Hints on the Power-Amplifier

The power amplifier operates in a high efficient class C mode. This mode is characterized by a pulsed operation of the power amplifier transistor at a current flow angle of $\theta << \pi$. A frequency selective network at the amplifier output passes the fundamental frequency component of the pulse spectrum of the collector current to the load. The load and its resonance transformation to the collector of the power amplifier can be generalized by the equivalent circuit of Figure 3-8. The tank circuit L//C//RL in parallel to the output impedance of the transistor should be in resonance at the operating frequency of the transmitter.



Equivalent_power_wmf.

Figure 3-8 Equivalent power amplifier tank circuit

The optimum load at the collector of the power amplifier for “critical” operation under idealized conditions at resonance is:

$$R_{LC} = \frac{V_S^2}{2 * P_O}$$

The theoretical value of R_{LC} for an RF output power of P_o= 5 dBm (3.16 mW) is:

$$R_{LC} = \frac{3^2}{2 * 0.00316} = 1423\,\Omega$$

“Critical” operation is characterized by the RF peak voltage swing at the collector of the PA transistor to just reach the supply voltage V_S.
The high degree of efficiency under “critical” operating conditions can be explained by the low power losses at the transistor. During the conducting phase of the transistor, its collector voltage is very small. This way the power loss of the transistor, equal to $i_C * u_{CE}$, is minimized. This is particularly true for small current flow angles of $\theta << \pi$.
In practice the RF-saturation voltage of the PA transistor and other parasitics reduce the “critical” R_{LC}.

The output power P_o is reduced by operating in an "overcritical" mode characterised by $R_L > R_{LC}$.
The power efficiency (and the bandwidth) increase when operating at a slightly higher R_L, as shown in Figure 3-9.
The collector efficiency E is defined as

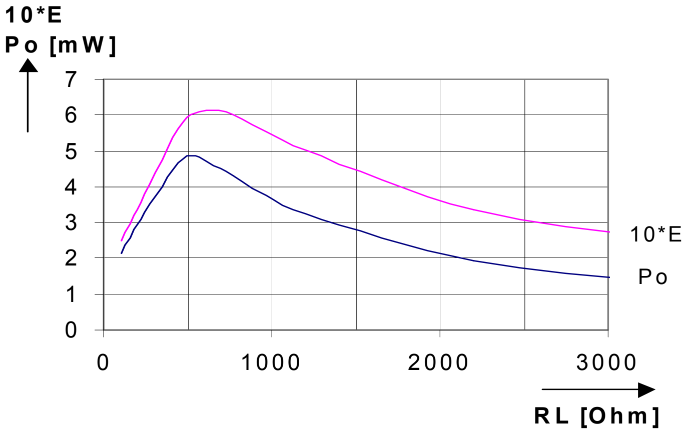
$$E = \frac{P_O}{V_S I_C}$$

The diagram of Figure 3-9 was measured directly at the PA-output at V_S = 3 V. Losses in the matching circuitry decrease the output power by about 1.5 dB. As can be seen from the diagram, 700 Ω is the optimum impedance for operation at 3 V. For an approximation of R_{OPT} and P_{OUT} at other supply voltages those two formulas can be used:

$$R_{OPT} \sim V_S$$

and

$$P_{OUT} \sim R_{OPT}$$



Power_output.wmf

Figure 3-9 Output power P_o (mW) and collector efficiency E vs. load resistor R_L.

The DC collector current I_c of the power amplifier and the RF output power P_o vary with the load resistor R_L. This is typical for overcritical operation of class C amplifiers. The collector current will show a characteristic dip at the resonance frequency for this type of "overcritical" operation. The depth of this dip will increase with higher values of R_L.

As Figure 3-10 shows, detuning beyond the bandwidth of the matching circuit results in an increase of the collector current of the power amplifier and in some loss of output power. This diagram shows the data for the circuit of the test board at the frequency of 434 MHz. The behaviour at 868 MHz is similar. The effective load resistance of this circuit is R_L = 700 Ω, which is the optimum impedance for operation at 3 V. This will lead to a dip of the collector current of approx. 40%.

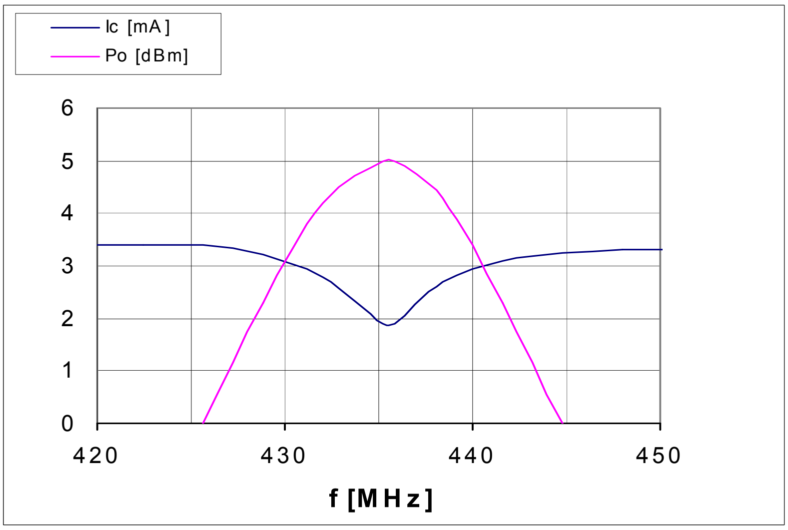
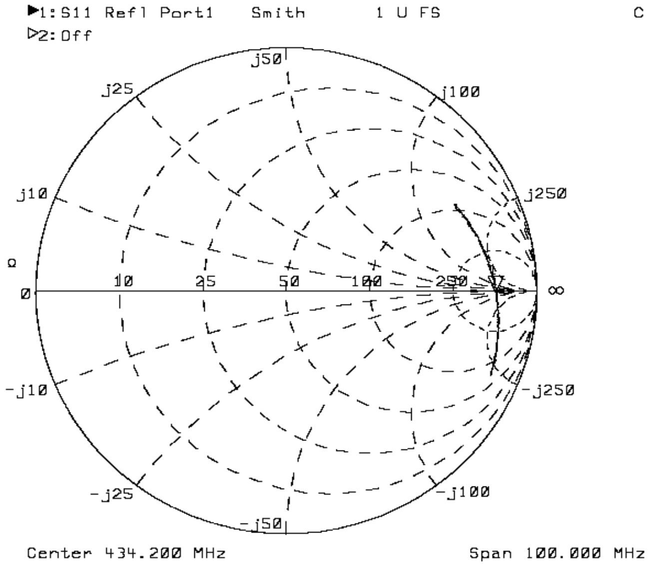


Figure 3-10 Output power and collector current vs. frequency

C3, L2-C2 and C8 are the main matching components which are used to transform the 50 Ω load at the SMA-RF-connector to a higher impedance at the PA-output (700 Ω @ 3 V). L1 can be used for some finetuning of the resonant frequency but should not become too small in order to keep its losses low.

The transformed impedance of 700+j0 Ω at the PA-output-pin can be verified with a network analyzer using the following measurement procedure:

1. Calibrate your network analyzer.
2. Connect some short, low-loss 50 Ω cable to your network analyzer with an open end on one side. Semirigid cable works best.
3. Use the „Port Extension“ feature of your network analyzer to shift the reference plane of your network analyzer to the open end of the cable.
4. Connect the center-conductor of the cable to the solder pad of the pin „PA“ of the IC. The outer conductor has to be grounded. Very short connections have to be used. Do not remove the IC or any part of the matching-components!
5. Screw a 50 Ω dummy-load on the RF-I/O-SMA-connector
6. Be sure that your network analyzer is AC-coupled and turn on the power supply of the IC. The TDK5100 must not be in Transmit-Mode.
7. Measure the S-parameter S11



LoadImpedance50ohmBoard.wmf

Figure 3-11 S-parameters of the load at the PA-output

Above you can see the measurement of the evalboard with a span of 100 MHz. The evalboard has been optimized for 3 V. The load is about 700+j0 Ω at the transmit frequency.

A tuning-free realization requires a careful design of the components within the matching network. A simple linear CAE-tool will help to see the influence of tolerances of matching components.

Suppression of spurious harmonics may require some additional filtering within the antenna matching circuit. The total spectrum of a typical 50 Ω - Output testboard can be summarized as:

Table 3-3

Frequency	Output Power 434 MHz Testboard	Output Power 868 MHz Testboard
Fundamental	+5 dBm	+2 dBm
Fund - 13.56 MHz	-81 dBc	-78 dBc
Fund + 13.56 MHz	-88 dBc	-75 dBc
2^{nd} harmonic	-40 dBc	-43 dBc
3^{rd} harmonic	-52 dBc	-52 dBc

4 Reference

Contents of this Chapter

4.1 Absolute Maximum Ratings

The AC / DC characteristic limits are not guaranteed. The maximum ratings must not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.

Table 4-1

Parameter	Symbol	Limit Values		Unit	Remarks
		Min	Max		
Junction Temperature	T_J	-40	+150	°C	
Storage Temperature	T_s	-40	+125	°C	
Thermal Resistance	R_{thJA}		230	K/W	
Supply voltage	V_S	-0.3	+4.0	V	
Voltage at any pin excluding pin 14	V_{pins}	-0.3	V_S + 0.3	V	
Voltage at pin 14	V_{pin14}	-0.3	2 * V_S	V	No ESD-Diode to V_S
Current into pin 11	I_{pin11}	-10	10	mA	
ESD integrity, all pins	V_{ESD}	-1	+1	kV	JEDEC Standard JESD22-A114-C
ESD integrity, all pins excluding pin 14	V_{ESD}	-2	+2	kV	JEDEC Standard JESD22-A114-C

Ambient Temperature under bias: T_A = -40°C to +125°C

Note: All voltages referred to ground (pins) unless stated otherwise.

Pins 5, 12 and 13 are grounded.

4.2 Operating Range

Within the operational range the IC operates as described in the circuit description.

Table 4-2

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min	Max		
Supply voltage	V_S	2.1	4.0	V	
Ambient temperature	T_A	-40	125	°C	

4.3 AC/DC Characteristics

4.3.1 AC/DC Characteristics at 3V, 25°C

Table 4-3 Supply Voltage V_S = 3 V, Ambient temperature T_{amb} = 25°C

Parameter	Symbol	Limit Values Min	Limit Values Typ	Limit Values Max	Unit	Test Conditions
Current consumption						
Power Down mode	$I_{S\ PDWN}$		0.3	100	nA	V (Pins 1, 6 and 7) < 0.2 V
PLL Enable mode	$I_{S\ PLL\_EN}$		3.5	4.2	mA	
Transmit mode 434 MHz	$I_{S\ TRANSM}$		7	8.8	mA	Load tank see Figure 4-1 and 4-2
Transmit mode 868 MHz	$I_{S\ TRANSM}$		7	9	mA	Load tank see Figure 4-1 and 4-2
Power Down Mode Control (Pin 1)						
Power Down mode	V_{PDWN}	0		0.7	V	V_{ASKDTA} < 0.2 V V_{FSKDTA} < 0.2 V
PLL Enable mode	V_{PDWN}	1.5		V_S	V	V_{ASKDTA} < 0.5 V
Transmit mode	V_{PDWN}	1.5		V_S	V	V_{ASKDTA} > 1.5 V
Input bias current PDWN	I_{PDWN}			30	µA	$V_{PDWN} = V_S$
Low Power Detect Output (Pin 2)						
Internal pull up current	I_{LPD1}	30			µA	V_S = 2.3 V ... V_S
Input current low voltage	I_{LPD2}	1			mA	V_S = 1.9 V ... 2.1 V
Loop Filter (Pin 4)						
VCO tuning voltage	V_{LF}	V_S - 1.5		V_S - 0.7	V	f_{VCO} = 867.84 MHz
Output frequency range 868 MHz-band	$f_{OUT,\ 868}$	854	869	884	MHz	$V_{FSEL} = V_S$ $f_{OUT} = f_{VCO}$
Output frequency range 433 MHz-band	$f_{OUT,\ 433}$	427	434.5	442	MHz	V_{FSEL} = 0 V $f_{OUT} = f_{VCO} / 2$
ASK Modulation Data Input (Pin 6)						
ASK Transmit disabled	V_{ASKDTA}	0		0.5	V	
ASK Transmit enabled	V_{ASKDTA}	1.5		V_S	V	
Input bias current ASKDTA	I_{ASKDTA}			30	µA	$V_{ASKDTA} = V_S$
Input bias current ASKDTA	I_{ASKDTA}	-20			µA	V_{ASKDTA} = 0 V
ASK data rate	f_{ASKDTA}			20	kHz	

Table 4-3 Supply Voltage V_S = 3 V, Ambient temperature T_{amb} = 25°C						
Parameter	**Symbol**	**Limit Values**			**Unit**	**Test Conditions**
		Min	**Typ**	**Max**		
FSK Modulation Data Input (Pin 7)						
FSK Switch on	V_{FSKDTA}	0		0.5	V	
FSK Switch off	V_{FSKDTA}	1.5		V_S	V	
Input bias current FSKDTA	I_{FSKDTA}			30	µA	$V_{FSKDTA} = V_S$
Input bias current FSKDTA	I_{FSKDTA}	-20			µA	V_{FSKDTA} = 0 V
FSK data rate	f_{FSKDTA}			20	kHz	
Clock Driver Output (Pin 8)						
Output current (High)	I_{CLKOUT}			5	µA	$V_{CLKOUT} = V_S$
Saturation Voltage (Low)[*)]	V_{SATL}			0.56	V	I_{CLKOUT} = 1 mA
Clock Divider Control (Pin 9)						
Setting Clock Driver output frequency f_{CLKOUT}=3.39 MHz	V_{CLKDIV}	0		0.2	V	
Setting Clock Driver output frequency f_{CLKOUT}=847.5kHz	V_{CLKDIV}				V	pin open
Input bias current CLKDIV	I_{CLKDIV}			30	µA	$V_{CLKDIV} = V_S$
Input bias current CLKDIV	I_{CLKDIV}	-20			µA	V_{CLKDIV} = 0 V
Crystal Oscillator Input (Pin 10)						
Load capacitance	$C_{COSCmax}$			5	pF	
Serial Resistance of the crystal				100	Ω	f = 6.78 MHz
Input inductance of the COSC pin		3.25	4.25	5.25	µH	f = 6.78 MHz
Serial Resistance of the crystal				100	Ω	f = 13.56 MHz
Input inductance of the COSC pin		3.6	4.6	5.6	µH	f = 13.56 MHz
FSK Switch Output (Pin 11)						
On resistance	R_{FSKOUT}			250	Ω	V_{FSKDTA} = 0 V
On capacitance	C_{FSKOUT}			6	pF	V_{FSKDTA} = 0 V
Off resistance	R_{FSKOUT}	10			kΩ	$V_{FSKDTA} = V_S$
Off capacitance	C_{FSKOUT}			1.5	pF	$V_{FSKDTA} = V_S$

Table 4-3 Supply Voltage V_S = 3 V, Ambient temperature T_{amb} = 25°C						
Parameter	**Symbol**	**Limit Values**			**Unit**	**Test Conditions**
		Min	**Typ**	**Max**		
Power Amplifier Output (Pin 14)						
Output Power†) transformed to 50 Ohm	P_{OUT433}	4	5	6	dBm	f_{OUT} = 433 MHz V_{FSEL} = 0 V
	P_{OUT868}	0	2	4	dBm	f_{OUT} = 868 MHz V_{FSEL} = V_S
Frequency Range Selection (Pin 15)						
Transmit frequency 433 MHz	V_{FSEL}	0		0.5	V	
Transmit frequency 868 MHz	V_{FSEL}				V	pin open
Input bias current FSEL	I_{FSEL}			30	µA	V_{FSEL} = V_S
Input bias current FSEL	I_{FSEL}	-20			µA	V_{FSEL} = 0 V
Crystal Frequency Selection (Pin 16)						
Crystal frequency 6.78 MHz	V_{CSEL}	0		0.2	V	
Crystal frequency 13.56 MHz	V_{CSEL}				V	pin open
Input bias current CSEL	I_{CSEL}			50	µA	V_{CSEL} = V_S
Input bias current CSEL	I_{CSEL}	-25			µA	V_{CSEL} = 0 V

*) Derating linearly to a saturation voltage of max. 140 mV at I_{CLKOUT} = 0 mA

†) Power amplifier in overcritical C-operation
Matching circuitry as used in the 50 Ohm-Output Testboard at the specified frequency.
Tolerances of the passive elements not taken into account.

4.3.2 AC/DC Characteristics at 2.1 V ... 4.0 V, -40°C ... +125°C

Table 4-4 Supply Voltage V_S = 2.1 V ... 4.0 V, Ambient temperature T_{amb} = -40°C ... +125°C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
Current consumption						
Power Down mode	$I_{S\ PDWN}$			4	mA	V (Pins 1, 6 and 7) < 0.2 V
PLL Enable mode	$I_{S\ PLL\_EN}$		3.5	4.6	mA	
Transmit mode	$I_{S\ TRANSM}$		7	9.5	mA	Load tank see Figure 4-1 and 4-2
Power Down Mode Control (Pin 1)						
Power Down mode	V_{PDWN}	0		0.5	V	V_{ASKDTA} < 0.2 V V_{FSKDTA} < 0.2 V
PLL Enable mode	V_{PDWN}	1.5		V_S	V	V_{ASKDTA} < 0.5 V
Transmit mode	V_{PDWN}	1.5		V_S	V	V_{ASKDTA} > 1.5 V
Input bias current PDWN	I_{PDWN}			38	µA	$V_{PDWN} = V_S$
Low Power Detect Output (Pin 2)						
Internal pull up current	I_{LPD1}	30			µA	V_S = 2.3 V ... V_S
Input current low voltage	I_{LPD2}	0.5			mA	V_S = 1.9 V ... 2.1 V
Loop Filter (Pin 4)						
VCO tuning voltage	V_{LF}	V_S - 1.8		V_S - 0.5	V	f_{VCO} = 867.84 MHz
Output frequency range *) 868 MHz-band	$f_{OUT,\ 868}$	864	869	874	MHz	$V_{FSEL} = V_S$ $f_{OUT} = f_{VCO}$
Output frequency range 433 MHz-band	$f_{OUT,\ 433}$	432	434.5	437	MHz	V_{FSEL} = 0 V $f_{OUT} = f_{VCO} / 2$
ASK Modulation Data Input (Pin 6)						
ASK Transmit disabled	V_{ASKDTA}	0		0.5	V	
ASK Transmit enabled	V_{ASKDTA}	1.5		V_S	V	
Input bias current ASKDTA	I_{ASKDTA}			33	µA	$V_{ASKDTA} = V_S$
Input bias current ASKDTA	I_{ASKDTA}	-20			µA	V_{ASKDTA} = 0 V
ASK data rate	f_{ASKDTA}			20	kHz	

Table 4-4 Supply Voltage V_S = 2.1 V ... 4.0 V, Ambient temperature T_{amb} = -40°C ... +125°C						
Parameter	**Symbol**	**Limit Values**			**Unit**	**Test Conditions**
		Min	**Typ**	**Max**		
FSK Modulation Data Input (Pin 7)						
FSK Switch on	V_{FSKDTA}	0		0.5	V	
FSK Switch off	V_{FSKDTA}	1.5		V_S	V	
Input bias current FSKDTA	I_{FSKDTA}			35	µA	$V_{FSKDTA} = V_S$
Input bias current FSKDTA	I_{FSKDTA}	-20			µA	V_{FSKDTA} = 0 V
FSK data rate	f_{FSKDTA}			20	kHz	
Clock Driver Output (Pin 8)						
Output current (High)	I_{CLKOUT}			5	µA	$V_{CLKOUT} = V_S$
Saturation Voltage (Low)†)	V_{SATL}			0.5	V	I_{CLKOUT} = 0.6 mA
Clock Divider Control (Pin 9)						
Setting Clock Driver output frequency f_{CLKOUT}=3.39 MHz	V_{CLKDIV}	0		0.2	V	
Setting Clock Driver output frequency f_{CLKOUT}=847.5kHz	V_{CLKDIV}				V	pin open
Input bias current CLKDIV	I_{CLKDIV}			30	µA	$V_{CLKDIV} = V_S$
Input bias current CLKDIV	I_{CLKDIV}	-20			µA	V_{CLKDIV} = 0 V
Crystal Oscillator Input (Pin 10)						
Load capacitance	$C_{COSCmax}$			5	pF	
Serial Resistance of the crystal				100	Ω	f = 6.78 MHz
Input inductance of the COSC pin		2.9	4.25	6	µH	f = 6.78 MHz
Serial Resistance of the crystal				100	Ω	f = 13.56 MHz
Input inductance of the COSC pin		3.2	4.6	6.3	µH	f = 13.56 MHz
FSK Switch Output (Pin 11)						
On resistance	R_{FSKOUT}			280	Ω	V_{FSKDTA} = 0 V
On capacitance	C_{FSKOUT}			6	pF	V_{FSKDTA} = 0 V
Off resistance	R_{FSKOUT}	10			kΩ	$V_{FSKDTA} = V_S$
Off capacitance	C_{FSKOUT}			1.5	pF	$V_{FSKDTA} = V_S$

Table 4-4 Supply Voltage V_S = 2.1 V ... 4.0 V, Ambient temperature T_{amb} = -40°C ... +125°C						
Parameter	**Symbol**	**Limit Values**			**Unit**	**Test Conditions**
		Min	**Typ**	**Max**		
Power Amplifier Output (Pin 14)						
Output Power ‡) at 434 MHz transformed to 50 Ohm.	$P_{OUT, 434}$	-0.5	2.4		dBm	V_S = 2.1 V
	$P_{OUT, 434}$	0.5	5	7	dBm	V_S = 3.0 V
V_{FSEL} = 0 V	$P_{OUT, 434}$	1.5	6.6		dBm	V_S = 4.0 V
Output Power **) at 868 MHz transformed to 50 Ohm.	$P_{OUT, 868}$	-4	0		dBm	V_S = 2.1 V
	$P_{OUT, 868}$	-3.6	2	5	dBm	V_S = 3.0 V
V_{FSEL} = V_S	$P_{OUT, 868}$	-3	3.2		dBm	V_S = 4.0 V
Frequency Range Selection (Pin 15)						
Transmit frequency 434 MHz	V_{FSEL}	0		0.5	V	
Transmit frequency 868 MHz	V_{FSEL}				V	pin open
Input bias current FSEL	I_{FSEL}			35	µA	V_{FSEL} = V_S
Input bias current FSEL	I_{FSEL}	-20			µA	V_{FSEL} = 0 V
Crystal Frequency Selection (Pin 16)						
Crystal frequency 6.78 MHz	V_{CSEL}	0		0.2	V	
Crystal frequency 13.56 MHz	V_{CSEL}				V	pin open
Input bias current CSEL	I_{CSEL}			55	µA	V_{CSEL} = V_S
Input bias current CSEL	I_{CSEL}	-25			µA	V_{CSEL} = 0 V

*) The output-frequency range can be increased by limiting the temperature and supply voltage range.
Minimum f_{VCO} - 1 MHz => Minimum T_{amb} + 5°C
Maximum f_{VCO} + 1 MHz => Maximum T_{amb} - 5°C
Maximum f_{VCO} + 1 MHz => Minimum V_S + 25 mV, max. + 40 MHz.

†) Derating linearly to a saturation voltage of max. 140 mV at I_{CLKOUT} = 0 mA

‡) Matching circuitry as used in the 50 Ohm-Output Testboard for 434 MHz operation.
Tolerances of the passive elements not taken into account.
Range @ 2.1 V, +25°C: 2.4 dBm +/- 0.7 dBm
Typ. temperature dependency at 2.1 V: +0.4 dBm@-40°C and -1.4 dBm@+125°C, reference +25°C
Range @ 3.0 V, +25°C: 5.0 dBm +/- 1.0 dBm
Typ. temperature dependency at 3.0 V: +0.5 dBm@-40°C and -1.9 dBm@+125°C, reference +25°C
Range @ 4.0 V, +25°C: 6.6 dBm +/- 2.0 dBm
Typ. temperature dependency at 4.0 V: +0.6 dBm@-40°C and -3.1 dBm@+125°C, reference +25°C

**) Matching circuitry as used in the 50 Ohm-Output Testboard for 868 MHz operation.
Tolerances of the passive elements not taken into account.
Range @ 2.1 V, +25°C: 0.0 dBm +/- 1.0 dBm
Typ. temperature dependency at 2.1 V: +0.6 dBm@-40°C and -2.5 dBm@+125°C, reference +25°C
Range @ 3.0 V, +25°C: 2.0 dBm +/- 2.0 dBm
Typ. temperature dependency at 3.0 V: +0.9 dBm@-40°C and -3.6 dBm@+125°C, reference +25°C
Range @ 4.0 V, +25°C: 3.2 dBm +/- 2.7 dBm
Typ. temperature dependency at 4.0 V: +1.3 dBm@-40°C and -4.0 dBm@+125°C, reference +25°C

A smaller load impedance reduces the supply-voltage dependency.
A higher load impedance reduces the temperature dependency.