Lattice Sentry Demo Board for MachXO3D

User Guide

FPGA-UG-02097-1.1

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
BMC	Baseboard Management Controller
CPLD	Complex Programmable Logic Device
CS	Chip Selected
DC	Direct Current
DIP	Dual Inline Package
EEPROM	Electrically Erasable Programmable Read Only Memory
ESD	Electro-Static Discharge
ESPI	Enhanced Serial Peripheral Interface
FPGA	Field Programmable Gate Array
FTDI	Future Technology Devices International Ltd.
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
LDO	Low Dropout Regulator
LED	Light Emitting Diode
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
MSPI	Master Serial Peripheral Interface Mode
OLED	Organic Light Emitting Diode
OOB	Out of Band
PC	Personal Computer
PCB	Printed Circuit Board
PCH	Platform Controller Hub
PFR	Platform Firmware Resiliency
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RTC	Real Time Clock
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

1. Introduction

The purpose of this document is to introduce the hardware resources and basic functions enabling for the Lattice Platform Firmware Resiliency (PFR) demo board.

1.1. Overview

Lattice Sentry Demo Board for MachXO3D is a single-board, system-level demo environment for the Lattice PFR system security solution. The demo board includes three main devices:

- MachXO3D LCMXO3D-9400HC-6BG484C
  This device is a next generation CPLD with enhanced secure control applications including hardware root-of-trust and dual boot capabilities. For a complete description of the MachXO3D device, refer to MachXO3D Device Family Data Sheet (FPGA-DS-02026).
- ECP5 LFE5U-85F-8BG381C
  This device is part of the ECP5 family of FPGA devices that are optimized to deliver high performance through advanced in-device architecture and the use of 40 nm technology, making the devices suitable for high-volume, high-speed, affordable applications. For a complete description of the ECP5 device, refer to ECP5 and ECP-5G Family Data Sheet (FPGA-DS-02012). On this demo board, there are two ECP5 devices:
  - ECP5 (BMC) simulates the BMC behavior
  - ECP5 (PCH) simulates the PCH behavior

Lattice Sentry Demo Board for MachXO3D demonstrates the Lattice PFR system security capability on a hardware platform that can be controlled through a dedicated user interface on a PC workstation. MachXO3D device authenticates the boot code of ECP5 (BMC) and ECP5 (PCH). MachXO3D device detects and blocks illegal flash operations, and can recover damaged boot images automatically. Before the system booting up and throughout the system operation, these functions secure the system at hardware level. For more details on Lattice Sentry Demo Board for MachXO3D demonstration, refer to MachXO3D Root of Trust PFR Demo User Guide (FPGA-UG-02099).

This user guide includes functional descriptions of the various hardware modules of Lattice Sentry Demo Board for MachXO3D. This document also provides descriptions of the on-board connectors, status LEDs, switches, push buttons, and JTAG function enablement.

Figure 1.1 shows the top view of Lattice Sentry Demo Board for MachXO3D. Figure 1.2 shows the bottom view of Lattice Sentry Demo Board for MachXO3D.

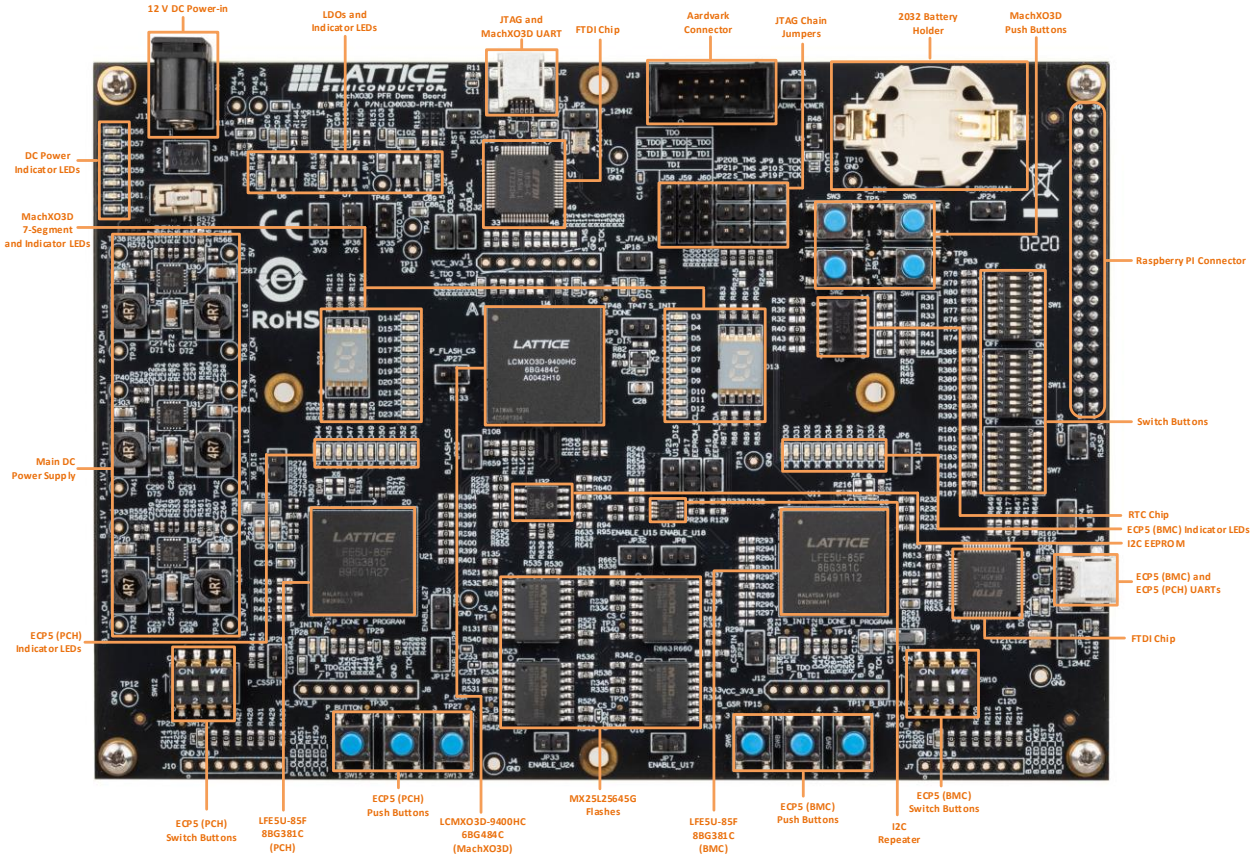


Figure 1.1. Lattice Sentry Demo Board for MachXO3D, Top View

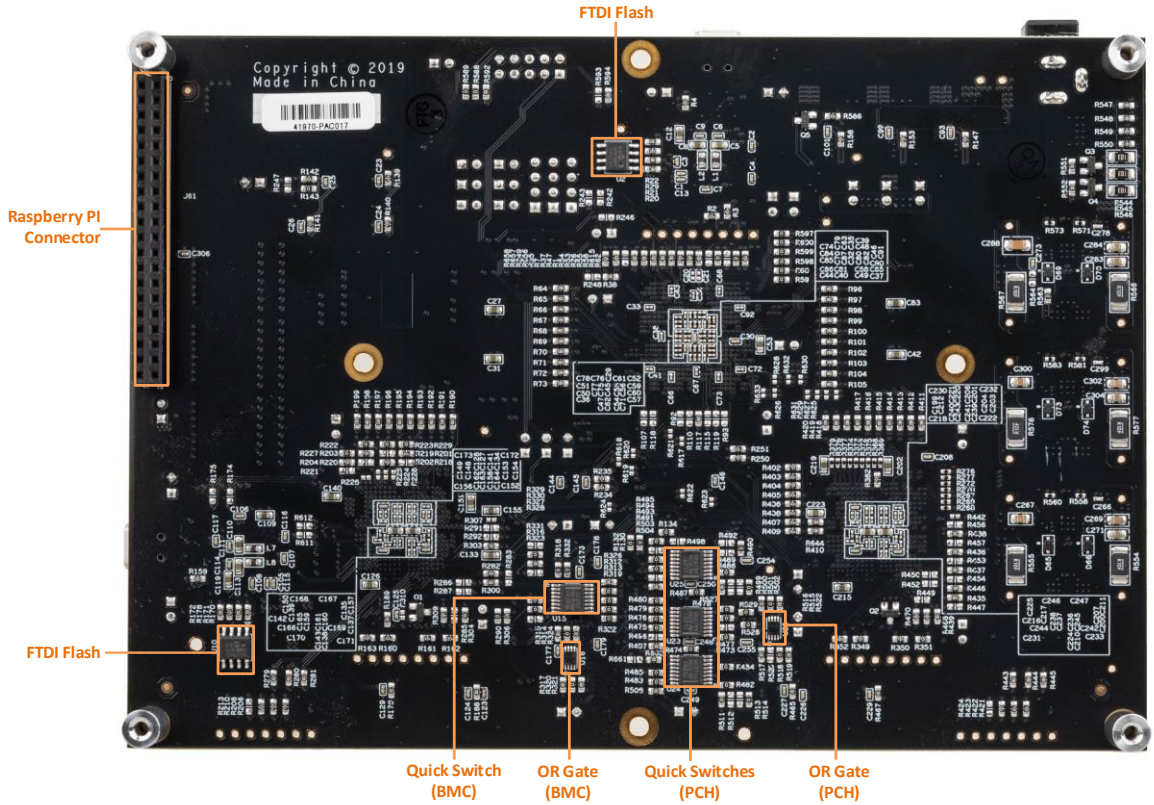


Figure 1.2. Lattice Sentry Demo Board for MachXO3D, Bottom View

2. Features

The key features of the Lattice Sentry Demo Board for MachXO3D are:

- Lattice security solution PFR demo support
- PFR system-level behavior validation
- USB connection for device programming
- Two per ECP5 device on-board configuration 256 M SPI/QSPI flash devices
- Flexible expansion Raspberry PI header
- LEDs, switches, push buttons for various purposes
- Lattice Diamond® programming support

Caution:

- The Lattice Sentry Demo Board for MachXO3D contains ESD-sensitive components. ESD safe practices should be followed while handling and using the demo board.
- To prevent power surge impact on USB port, remove the USB cable before you plug in or remove the 12 V DC power cable.

Note: This document describes the production Lattice Sentry Demo Board for MachXO3D. Early prototypes include some minor silkscreen differences. These have no impact on the board schematic or demonstration function. The production board includes the following updates to the top layer silkscreen:

- Added a direction silkscreen marker to the power components U6, U7, and U8.
- Corrected the LED direction markers on MachXO3D, ECP5 (BMC), and ECP5 (PCH) indicator LEDs and some power-up indicator LEDs.

3. Applying Power

The Lattice Sentry Demo Board for MachXO3D comes ready to power up. This board can power up using a 12 V DC power source input. The power supply can be connected with the right-angle DC power input jack J11, which is fused with a surface mounted fuse F1, as shown in Figure 3.1 and Table 3.1.

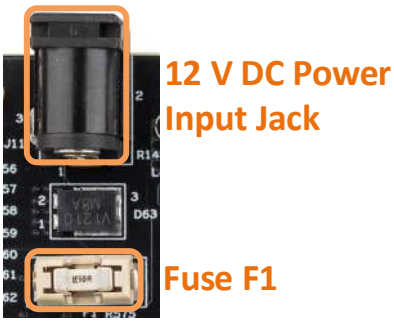


Figure 3.1. 12 V DC Power Supply

Table 3.1. Board Power Supply

Part Designator	Description
J11	12 V DC Input Supply Jack
F1	12 V DC Input Supply Fuse

The Lattice Sentry Demo Board for MachXO3D contains three logic devices. It works within appropriate power supply conditions. Using an incorrect power supply may cause permanent device and board damage. The recommended operating conditions can be found in MachXO3D Device Family Data Sheet (FPGA-DS-02026) and ECP5 and ECP-5G Family Data Sheet (FPGA-DS-02012). The 10 A fuse prevents the crashed current from flowing into the internal circuits and cause serious damage.

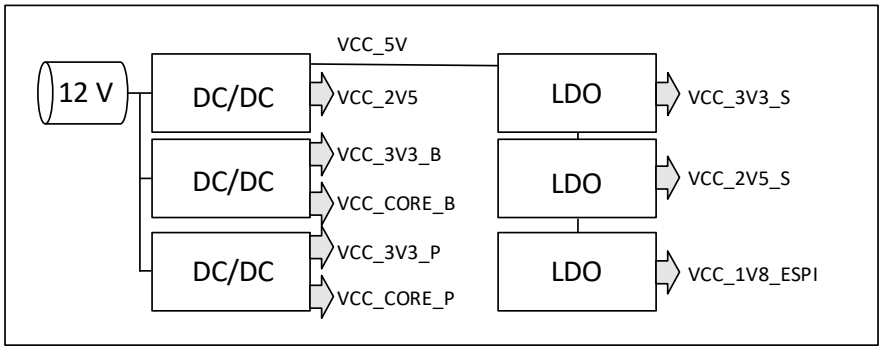


Figure 3.2. Power Tree

The Lattice Sentry Demo Board for MachXO3D provides status LEDs to provide a visual indication of power status (Table 3.2).

Table 3.2. Status LED Definitions

LED Designator	Color	Description
D1	Green	J2 USB header plug in
D25	Green	VCCIO_VAR 3V3 power on
D26	Green	VCCIO_VAR 2V5 power on
D27	Green	VCCIO_VAR 1V8 power on
D28	Green	J6 USB header plug in
D56	Green	ECP5 (BMC) 3V3 power on
D57	Green	ECP5 (PCH) 3V3 power on
D58	Green	5V power on
D59	Green	2V5 power on
D60	Green	12 V power on
D61	Green	ECP5 (BMC) 1V1 power on
D62	Green	ECP5 (PCH) 1V1 power on

The Lattice Sentry Demo Board for MachXO3D features three LDO devices for one variable VCCIO_VAR power level among partial FPGA/CPLD GPIO banks. The jumpers JP34, JP35, and JP36 can set VCCIO_VAR power level. Set the input pin type according to VCCIO_VAR power level. Closed JP34 is the default setting.

- Closed JP34 sets VCCIO_VAR power level to 3V3 power level.
- Closed JP35 sets VCCIO_VAR power level to 1V8 power level.
- Closed JP36 sets VCCIO_VAR power level to 2V5 power level.

Note: Only one of three jumpers, JP34, JP35, or JP36, can be set.

4. Programming FPGA/CPLD Configuration

The Lattice Sentry Demo Board for MachXO3D has a built-in download controller for programming the MachXO3D, ECP5 (BMC), and ECP5 (PCH) device. The built-in module consists of a Mini-USB connector and FTDI device. This module can translate USB format data into JTAG type stream and allows you to configure the FPGA directly through a USB cable. To use the built-in download controller, connect a standard Mini-B USB to a USB-A cable from J2 to your PC (with Diamond programming software installed). The USB hub on the PC detects the addition of the USB function, making the built-in controller available for use with the Diamond programming software.

4.1. Setting Configuration Mode

The MachXO3D, ECP5 (BMC), and ECP5 (PCH) devices support a variety of configuration modes, including 1149.1 JTAG and Master SPI. For detailed information, refer to the MachXO3D Programming and Configuration Usage Guide (FPGA-TN-02069) and ECP5 and ECP5-5G sysCONFIG Usage Guide (FPGA-TN-02039). The Lattice Sentry Demo Board for MachXO3D has a default configuration to scan all three devices on the board. The default jumper setting of JTAG chain is shown in Figure 4.1. The Lattice Sentry Demo Board for MachXO3D supports various JTAG chain options. The jumper settings are provided in Figure 4.2.

Figure 4.1. Default JTAG Chain Jumper Setting

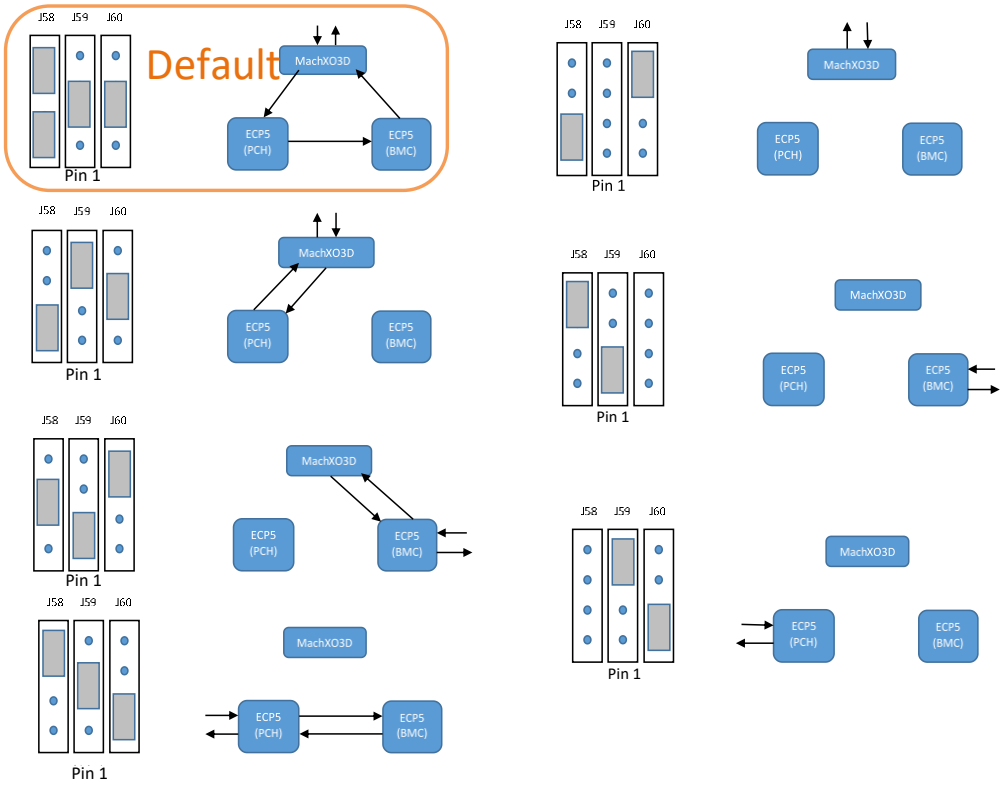


Figure 4.2. JTAG Chain Setting Diagram

The ECP5 (BMC)/ECP5 (PCH) configuration mode can be selected using the CFG Setting DIP Switches SW10/SW12, as shown in Figure 4.3 and Table 4.1. Master SPI should be selected to work with the PFR demonstration.

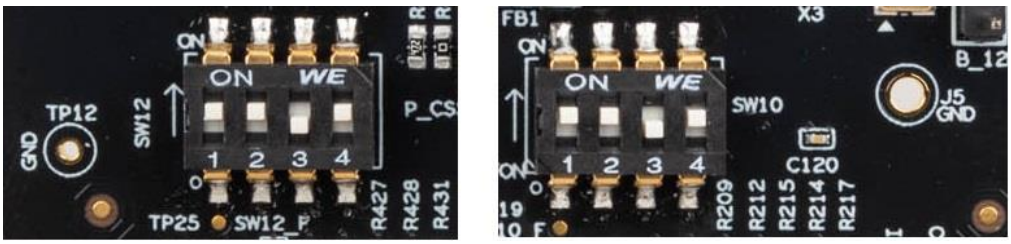


Figure 4.3. SW10 and SW12 Configuration

Table 4.1. CFG[2:0] Selection[1]

Configuration Mode	CFG[2:0]	SW10/SW12[4]	SW10/SW12[3]	SW10/SW12[2]
1149.1 JTAG only	000	Up	Up	Up
Slave SPI	001	Up	Up	Down
Master SPI[2]	010	Up	Down	Up
SCM (Slave_Serial)	101	Down	Up	Down
SCM (Slave_Parallel)	111	Down	Down	Down

Notes:

1. SW10/SW12[1] are floating pins on the current PCB version. They do not affect how the system works.
2. Master SPI Configuration Mode is in use on the current Lattice Sentry Demo Board for MachXO3D.

4.2. Programming LEDs and Buttons

The Lattice Sentry Demo Board for MachXO3D can control three main device programming processes and indicate the programming status through LEDs. Resources are shown in Figure 4.4 and Table 4.2.

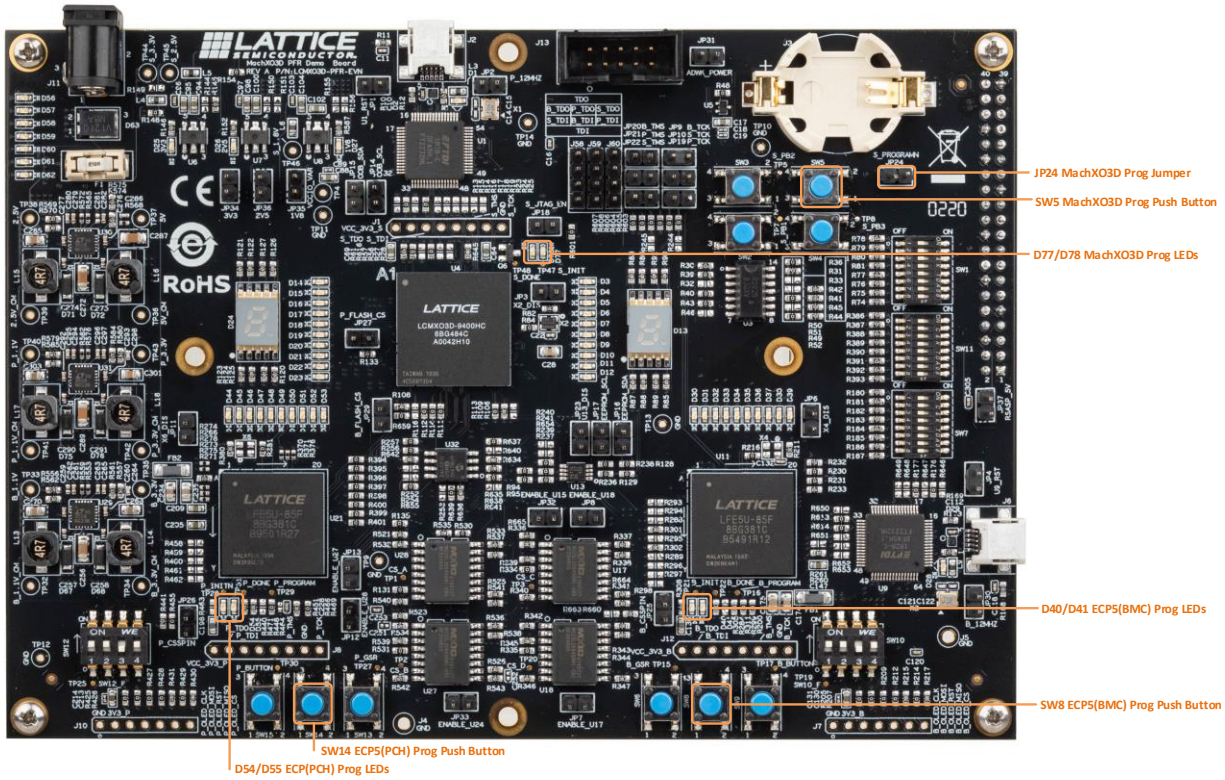


Figure 4.4. Programming Status LEDs and Push Buttons

Note: For the MachXO3D device, make sure you have updated the Feature Row register to enable LED indicator functions. For more details, refer to Step 2 of the MachXO3D Programming Modes section.

Table 4.2. Programming Status LED Definitions

LED Designator	Color	Description
D77	Green	Indicates that MachXO3D programming is aborted or reinitialized, driving the INITN output low.
D78	Green	Indicates that the MachXO3D successful completion of configuration by releasing the open collector DONE output pin.
D40	Green	Indicates that the ECP5 (BMC) programming is aborted or reinitialized, driving the INITN output low.
D41	Green	Indicates the ECP5 (BMC) successful completion of configuration by releasing the open collector DONE output pin.
D54	Green	Indicates that ECP5 (PCH) programming is aborted or reinitialized, driving the INITN output low.
D55	Green	Indicates the ECP5 (PCH) successful completion of configuration by releasing the open collector DONE output pin.

4.3. Programming Flash Memory

In the Lattice Sentry Demo Board for MachXO3D, the MachXO3D device programs its internal flash memory and the two ECP5 devices program their four external SPI flash. Of the four SPI flash devices, U17 and U18 belong to the ECP5 (BMC) device, and U27 and U28 belong to the ECP5 (PCH) device. Before starting to program external SPI flash, configure the jumpers as indicated in Table 4.3 and Figure 4.5.

Table 4.3. Jumper Description

Jumper Designator	Description
JP32	Asserts/de-asserts the enable logic on quick switches U15. Close the jumper cap drives a logic level *0* to the enable device. When programming the ECP5 (BMC) flashes, JP32 must be closed.
JP33	Asserts/de-asserts the enable logic on quick switches U24. Close the jumper cap drives a logic level *0* to the enable device. When programming the ECP5 (PCH) flashes, JP33 must be closed.
JP7	Asserts/de-asserts the CS logic on external SPI flash U17. Close the jumper cap drives a logic level *0* to the selected device. When programming flash U17, JP7 must be closed.
JP8	Asserts/de-asserts the CS logic on external SPI flash U18. Close the jumper cap drives a logic level *0* to the selected device. When programming flash U18, JP8 must be closed. JP7 and JP8 are alternative.
JP12	Asserts/de-asserts the CS logic on external SPI flash U28. Close the jumper cap drives a logic level *0* to the device selection device. When programming flash U28, JP12 must be closed.
JP13	Asserts/de-asserts the CS logic on external SPI flash U27. Close the jumper cap drives a logic level *0* to the selected device. When programming flash U27, JP8 must be closed. JP12 and JP13 are alternative.

Note: When running the demonstration program, the JP7, JP8, JP12, JP13, JP32, JP33 jumpers are not installed.

Table 4.4. Programming Jumper Selection

Target Flash Programming	JP7	JP8	JP12	JP13	JP32	JP33
U17	Closed	—	—	—	Closed	—
U18	—	Closed	—	—	Closed	—
U27	—	—	—	Closed	—	Closed
U28	—	—	Closed	—	—	Closed
PFR Demo	—	—	—	—	—	—

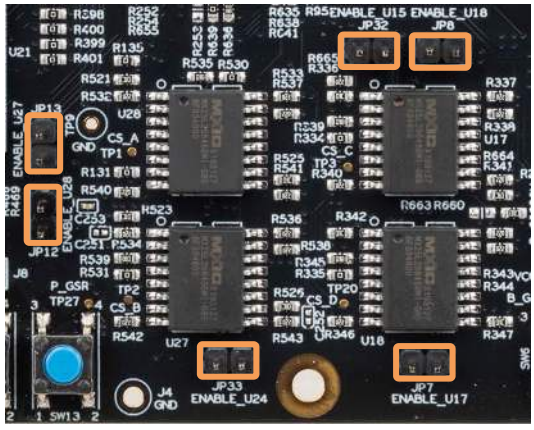


Figure 4.5. Flash Programming Jumpers

Four SPI (16-pin SO16W, 256M) flash memory devices, U17, U18, U27, and U28 are on-board for non-volatile configuration memory storage. The Macronix MX25L25645GMI device is populated on current PCB version. When programming external flash, the Lattice Diamond Programmer locates and indicates the device in the Device Properties dialog box. The SPI flash memory device can be configured through the USB cable. The Master SPI configuration mode enables the three main devices to be programmed at power-up or assertion of PROGRAMN by the bitstream stored in the internal and external memories.

4.3.1. Building the JTAG Chain

To build the JTAG chain:

1. Open the Diamond Programmer.
2. Connect connector J2 of the Lattice Sentry Demo Board for MachXO3D to your PC using the USB cable.
3. Click the **Detect Cable** button to scan the cable (Figure 4.6). The **Programmer: Multiple Cables Detected** dialog box pops up.
4. In the **Programmer: Multiple Cables Detected** dialog box, select **FTUSB-0 (Dual RS232-HS A Location 0000)**. Click **OK**.
5. After scanning the cable, click the  button to scan the JTAG chain. The three main devices are located as shown in Figure 4.6.

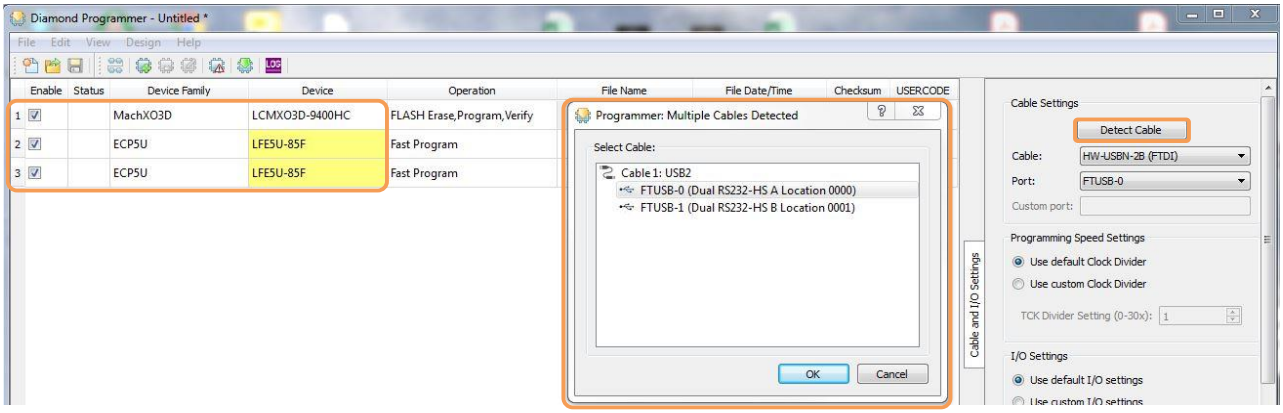


Figure 4.6. Diamond Programmer JTAG Chain

6. Click on the desired device, such as LFE5U-85F, from the **Device** column (Figure 4.7) to program.

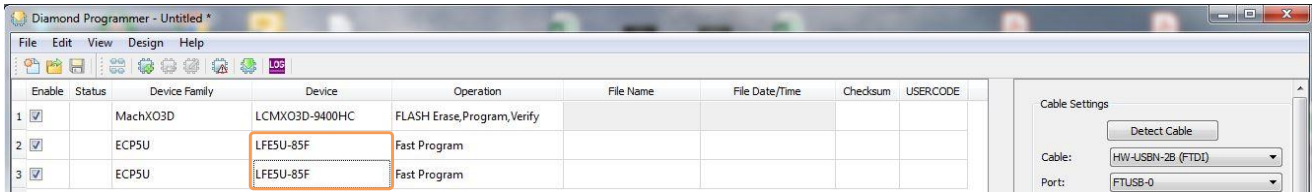


Figure 4.7. Device Selection

4.3.2. Programming the Internal Flash or External Flash in One-time Mode

To program the internal flash or external flash using one-time mode.

1. Double click **Operation**. The **Device Properties** dialog box opens.
2. Select the **Access mode**.
3. Click the button to program the bitstream to target device consecutively.

   You can program the bitstream stored in FPGA/CPLD RAM. The bitstream can Fast Program the FPGA/CPLD to validate. SPI Flash Background Programming mode programs the bitstream to external SPI flash. The FPGA/CPLD can upload bitstream automatically from external SPI flash.

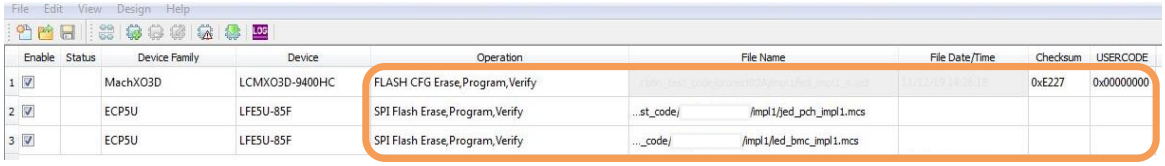


Figure 4.8. One-time Access Mode Operation

Note: In the PFR demonstration, the ECP5 devices need to be configured before programming the MachXO3D device. If not, the ECP5 device may fail to configure. The MachXO3D PFR function has impact on the configuration process.

4.3.3. Programming the Internal Flash or External Flash in Bypass Mode.

To program the internal flash or external flash using bypass mode:

1. Double click **Operation**. The **Device Properties** dialog box opens.
2. Select the **Access mode**.
3. Set **Operation** as **Bypass** mode.
4. Click the button to program the bitstream to target devices selectively.

   Note: The Bypass device is not programmed.

Figure 4.9. Bypass Access Mode Operation

4.3.4. MachXO3D Programming Modes

The MachXO3D device has three programming modes for the Lattice Sentry Demo Board for MachXO3D.

To use the MachXO3D programming modes:

1. Double click **Operation**. The **Device Properties** dialog box opens.
2. Under **Operation**, select:
   - **FLASH CFG, Erase, Program, Verify** – bitstream is uploaded to internal flash, and MachXO3D device is booted automatically when powered up.
   - **FLASH UFM, Erase, Program, Verify** – for PFR demo setting, UFM space needs to be programmed.
   - **Feature Row, Erase, Program, Verify** – updating the Feature Row registers to set the basic boot features for the MachXO3D device.

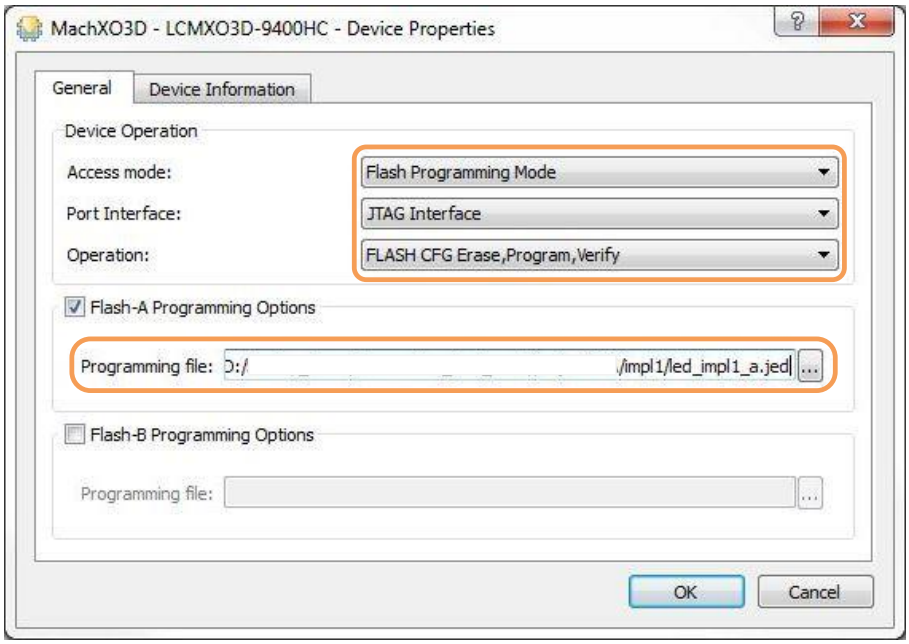


Figure 4.10. Flash CFG Mode Operation

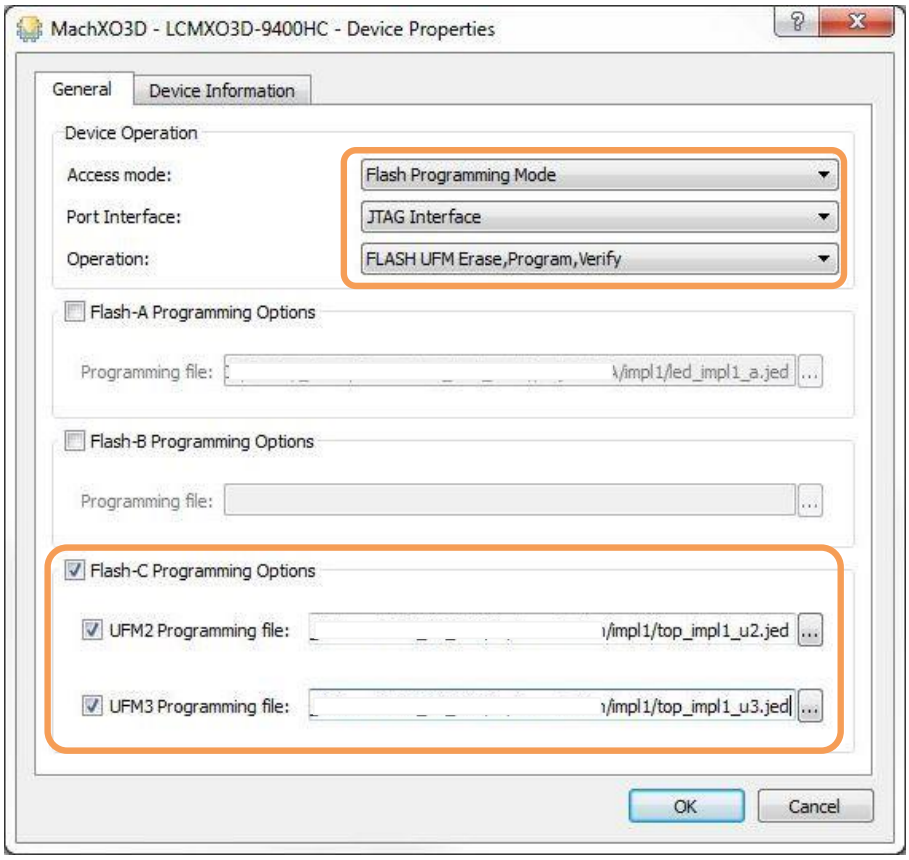


Figure 4.11. Flash UFM Mode Operation

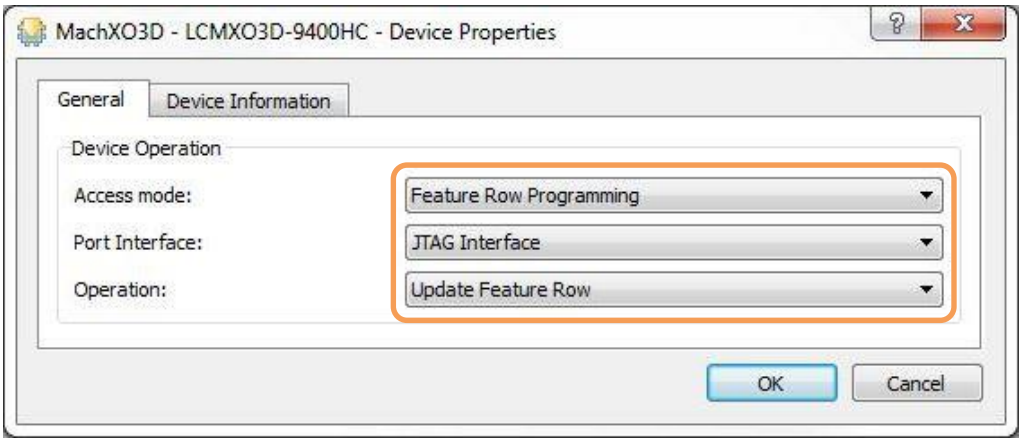


Figure 4.12. Feature Row Mode Operation

3. Update the two register values indicated in Figure 4.13 to enable the LED indicator function for MachXO3D device.

Figure 4.13. Feature Row Update

Note: Confirm that the PROGRAM Persistence Disable register is *0*. If not the JTAG chain configuration is affected.

ECP5 cannot program its external flash while running. If the bitstream booted from external SPI flash is running with ECP5 internal RAM, the external SPI flash may not be programmed. The current bitstream blocks the program interface. You need to erase the current bitstream or to enable Master SPI Port configuration to reopen this program interface. It is recommended executing the **Erase Only** command in **Operation** before programming external SPI flash.

Two options are available:

- Erase ECP5 RAM operation when programming external flash every time, as shown in Figure 4.14.
- Enable the MASTER_SPI_PORT configuration (Figure 4.15) in Lattice Diamond Software kit.

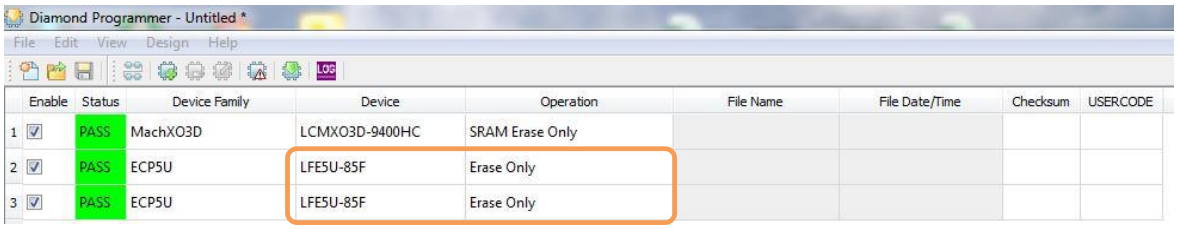


Figure 4.14. Erase RAM Operation

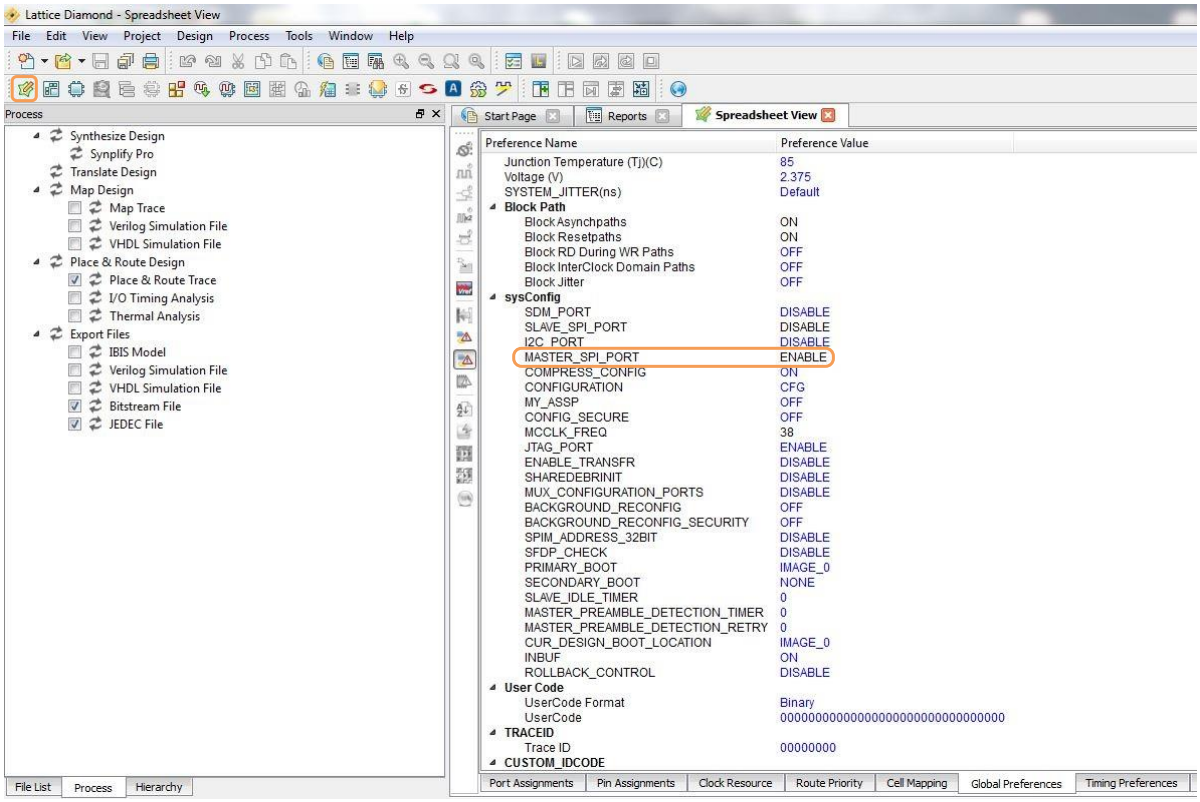


Figure 4.15. Enable Master SPI Port

4.3.5. ECP5 Programming Mode

The ECP5 device has two programming modes (Figure 4.16 and Figure 4.17) for the Lattice Sentry Demo Board for MachXO3D.

- Internal RAM Mode – bitstream is uploaded to internal RAM, and the ECP5 device is booted automatically; when the ECP5 device is powered up again, the bitstream becomes invalid.
- External SPI Flash Mode – bitstream is uploaded to external SPI flash, and the ECP5 device is rebooted automatically.

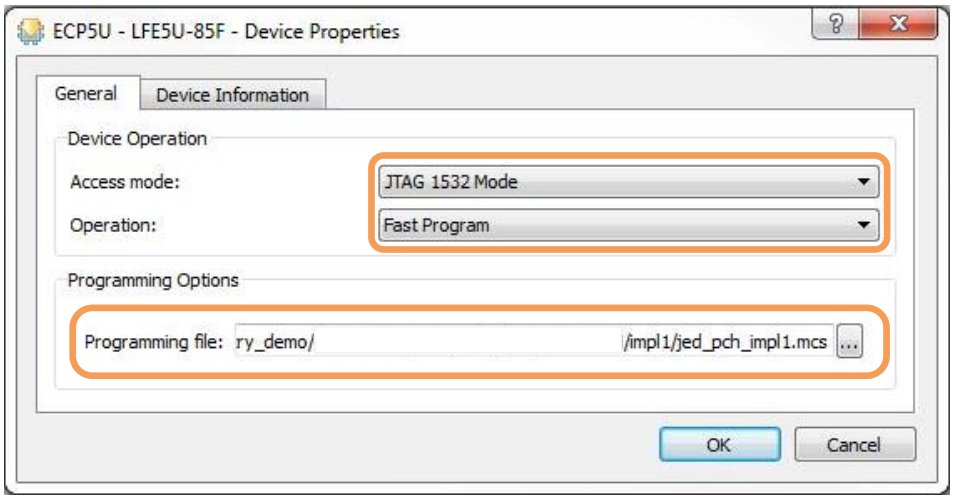


Figure 4.16. Internal RAM Mode Operation

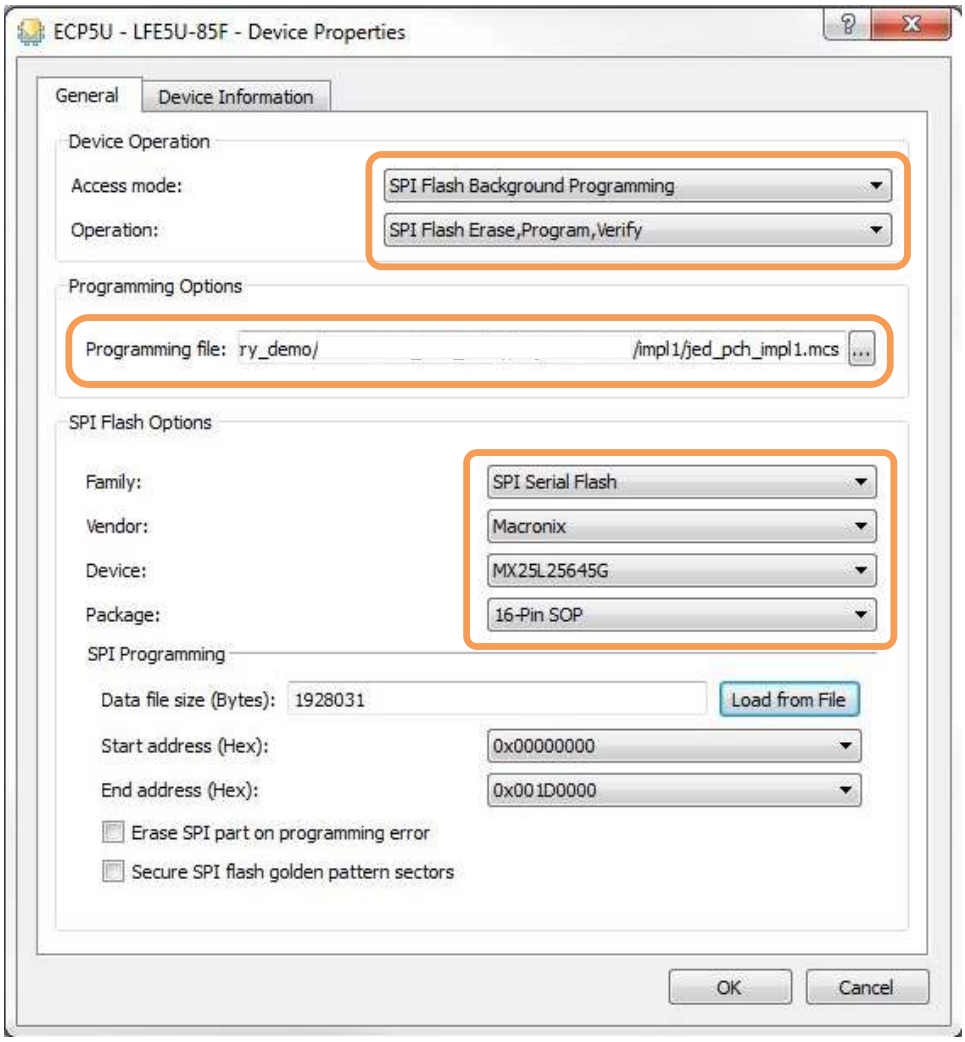


Figure 4.17. External SPI Flash Mode Operation

To select external SPI Flash mode (Figure 4.17):

1. From the **Device Properties** dialog box, set the **Access mode** to **SPI Flash Background Programming** and **Operation** to **SPI Flash Erase, Program, Verify**.
2. Under the **SPI Flash Options**, select the following options as shown in Figure 4.17:

   Family – **SPI Serial Flash**

   Vendor – **Macronix**

   Device – **MX25L25645G**

   Package – **16-Pin SOP**
3. Set the programming file path. Click **OK** and go back to the main configuration window.
4. To execute program operation, click the **Program** button in the **Toolbar**. Note that the **SPI Flash Background Programming** operation is only possible when either the ECP5 device is erased or the active design has the MASTER_SPI_PORT mode enabled. For more details, see ECP5 and ECP5-5G sysCONFIG Usage Guide (FPGA-TN-02039). The operation status information is displayed in the **Output** pane (Figure 4.18).

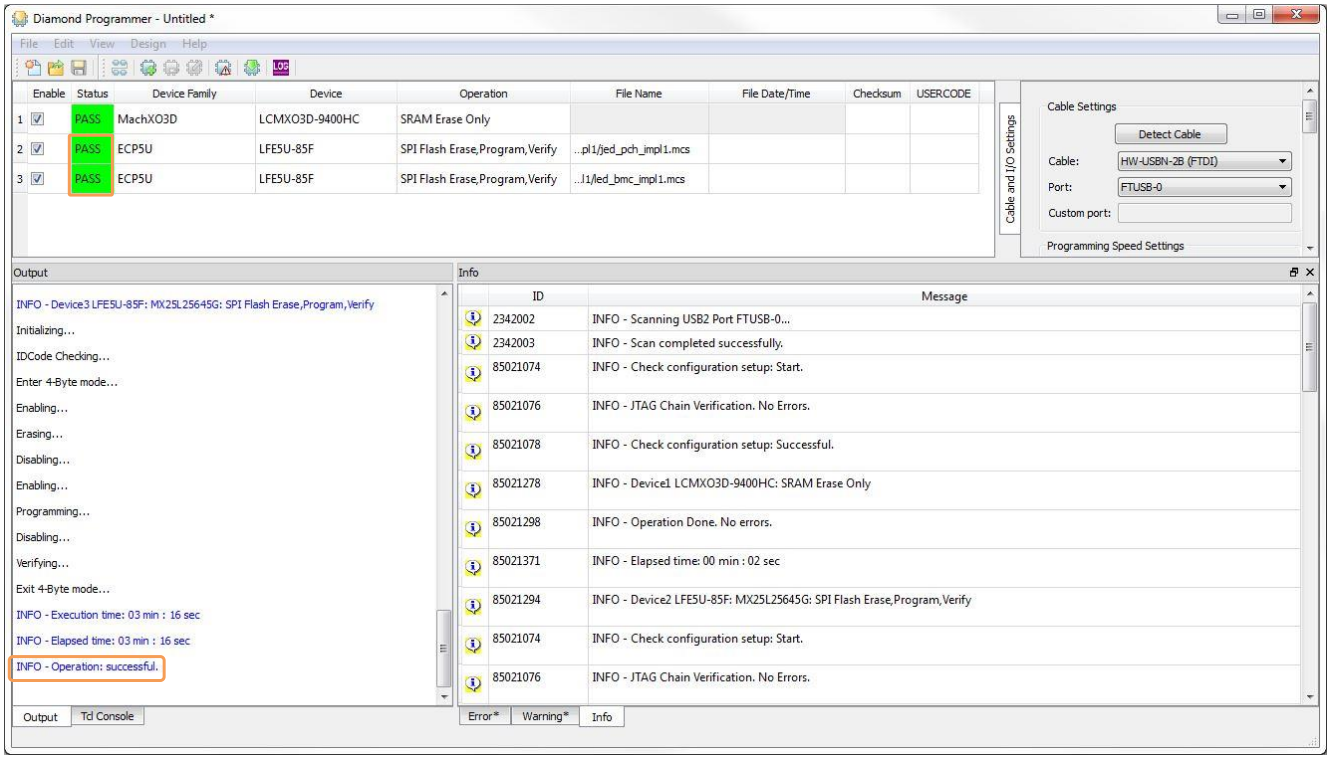


Figure 4.18. Main Configuration Status Output Pane

5. FPGA/CPLD Resources

The Lattice Sentry Demo Board for MachXO3D supports various development resources including 40 LEDs, 20 of which belong to MachXO3D device, 10 belong to ECP5 (BMC) device, and 10 belong to ECP5 (PCH) device. There are two 7-Segment LEDs, which belong to MachXO3D device. There is a switch for each of the MachXO3D, ECP5 (BMC), and ECP5 (PCH) devices. There are four push buttons located near the MachXO3D device, three located near the ECP5 (BMC) device, and three located near the ECP5 (PCH) device. Among MachXO3D, ECP5 (BMC), and ECP5 (PCH) devices, there are some reserved GPIO connections. You can utilize these resources through the FPGA/CPLD logic coding.

5.1. General Purpose 40 LEDs

The 40 LEDs provided on the Lattice Sentry Demo Board for MachXO3D are connected to general purpose I/O. These green LEDs provide visual status indication for user designs. The LEDs are illuminated when the FPGA/CPLD output is driven LOW. Figure 5.1 and Table 5.1 show the MachXO3D LEDs and associated pins name. Figure 5.2 and Table 5.2 show the ECP5 (BMC) LEDs and associated pins name. Figure 5.3 and Table 5.3 shows the ECP5 (PCH) LEDs and associated pins name. These pins are within an I/O bank connected to 3.3 V and you should program these pins to be LVCMOS33 type output in the design.

Figure 5.1. 20 Green LEDs for MachXO3D Device

Table 5.1. MachXO3D LED Definitions

LED Designator	MachXO3D U4 Pin Number	Signal Name
D3	R18	S_LED_0
D4	R17	S_LED_1
D5	R16	S_LED_2
D6	T20	S_LED_3
D7	T19	S_LED_4
D8	T18	S_LED_5
D9	T17	S_LED_6
D10	U20	S_LED_7
D11	Y22	S_LED_8
D12	W21	S_LED_9
D14	V6	S_LED_10
D15	U6	S_LED_11
D16	Y4	S_LED_12
D17	W5	S_LED_13
D18	U7	S_LED_14
D19	T8	S_LED_15
D20	Y5	S_LED_16
D21	Y6	S_LED_17

LED Designator	MachXO3D U4 Pin Number	Signal Name
D22	W6	S_LED_18
D23	V7	S_LED_19

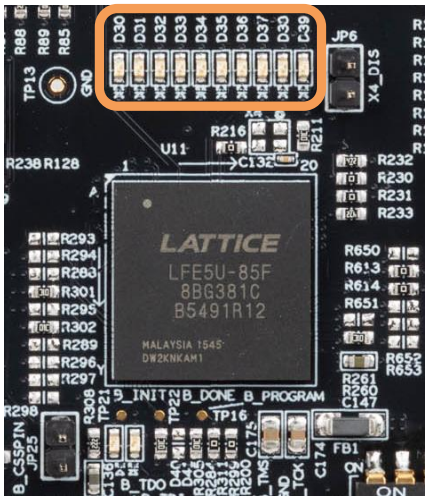


Figure 5.2. 10 Green LEDs for ECP5 (BMC) Device

Table 5.2. ECP5 (BMC) LED Definitions

LED Designator	ECP5 (BMC) U11 Pin Number	Signal Name
D30	E8	B_LED_1
D31	D8	B_LED_2
D32	D9	B_LED_3
D33	E9	B_LED_4
D34	D10	B_LED_5
D35	E10	B_LED_6
D36	E6	B_LED_7
D37	D6	B_LED_8
D38	E7	B_LED_9
D39	D7	B_LED_10

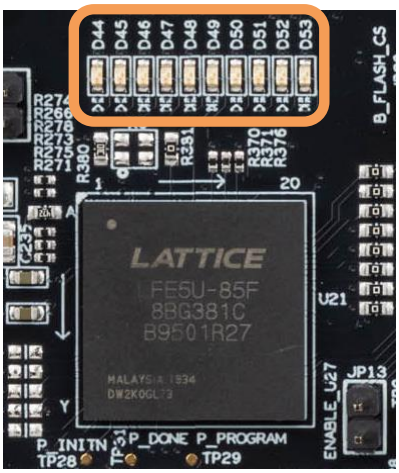


Figure 5.3. 10 Green LEDs for ECP5 (PCH) Device

Table 5.3. ECP5 (PCH) LED Definitions

LED Designator	ECP5 (PCH) U21 Pin Number	Signal Name
D44	C6	P_LED_1
D45	C7	P_LED_2
D46	E8	P_LED_3
D47	D8	P_LED_4
D48	C8	P_LED_5
D49	C11	P_LED_6
D50	E6	P_LED_7
D51	D6	P_LED_8
D52	E7	P_LED_9
D53	D7	P_LED_10

5.2. 7-Segment LEDs

Two 7-Segment LEDs provided on Lattice Sentry Demo Board for MachXO3D are connected to MachXO3D general purpose I/O. These blue LEDs provide visual status indication for user design. The LEDs are illuminated when the FPGA/CPLD output is driven *LOW*. Figure 5.4 and Table 5.4 show the MachXO3D 7-Segment LEDs and associated pins name. These pins are within an I/O bank connected to 3.3 V and you should program these pins to be LVCMOS33 type output in the design.

Figure 5.4. Two 7-Segment LEDs for MachXO3D Device

Table 5.4. MachXO3D 7-Segment LED Definitions

LED Designator	MachXO3D U4 Pin Number	Signal Name
D13.5	J17	S_SEG_DP_P
D13.10	J18	S_SEG_G_P
D13.9	J19	S_SEG_F_P
D13.1	J21	S_SEG_E_P
D13.2	J22	S_SEG_D_P
D13.4	J20	S_SEG_C_P
D13.6	K20	S_SEG_B_P
D13.7	K19	S_SEG_A_P
D24.5	R6	S_SEG_DP_B
D24.10	U5	S_SEG_G_B
D24.9	R7	S_SEG_F_B
D24.1	T3	S_SEG_E_B
D24.2	T5	S_SEG_D_B
D24.4	T6	S_SEG_C_B
D24.6	T4	S_SEG_B_B
D24.7	W4	S_SEG_A_B

5.3. General Purpose DIP Switches

General purpose FPGA/CPLD pins are available for user applications. FPGA/CPLD pins are connected to DIP switches, SW1, SW11, and SW7. SW1 belongs to MachXO3D device, SW7 belongs to ECP5 (BMC) device, SW11 belongs to ECP5 (PCH) device. Switch position OFF is indicated with *1* logic input. The switches are connected to logic level *0* input when moved to the ON position. You must program inputs to be the LVCMOS33 type in the design. Figure 5.5 and Table 5.5, Table 5.6, Table 5.7show the switches and associated FPGA/CPLD pins.

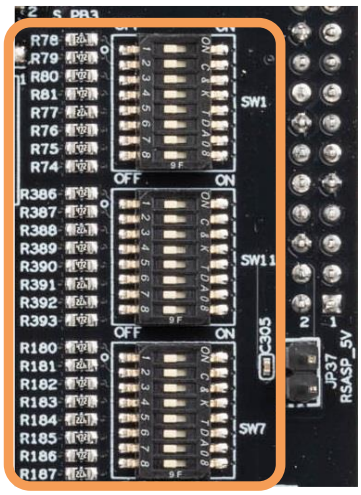


Figure 5.5. Switches

Table 5.5. MachXO3D Pins to DIP Switch Position

SW1 DIP Switch Position	MachXO3D U4 Pin Number	Signal Name
1	P17	S_DIP_SW1
2	P16	S_DIP_SW2
3	U22	S_DIP_SW3
4	U21	S_DIP_SW4
5	V22	S_DIP_SW5
6	W22	S_DIP_SW6
7	R20	S_DIP_SW7
8	R19	S_DIP_SW8

Table 5.6. ECP5 (BMC) Pins to DIP Switch Position

SW7 DIP Switch Position	ECP5 (BMC) U11 Pin Number	Signal Name
1	L4	B_DIP_SW1
2	L5	B_DIP_SW2
3	M5	B_DIP_SW3
4	M4	B_DIP_SW4
5	N5	B_DIP_SW5
6	N3	B_DIP_SW6
7	M3	B_DIP_SW7
8	L3	B_DIP_SW8

Table 5.7. ECP5 (PCH) Pins to DIP Switch Position

SW11 DIP Switch Position	ECP5 (PCH) U21 Pin Number	Signal Name
1	C18	P_DIP_SW1
2	D17	P_DIP_SW2
3	E16	P_DIP_SW3
4	F16	P_DIP_SW4
5	D18	P_DIP_SW5
6	E17	P_DIP_SW6
7	E18	P_DIP_SW7
8	F18	P_DIP_SW8

5.4. General Purpose Clock Sources

There are three clock sources, one for each device (Table 5.8).

Table 5.8. FPGA/CPLD Clock Source

Clock Source	Clock Frequency (MHz)	MachXO3D U4 Pin Number	ECP5 (BMC) U11 Pin Number	ECP5 (PCH) U21 Pin Number	Comment
X1	12	—	—	H2	Closing JP2 to enable clock input.
X2	25	M22	—	—	Closing JP3, or output *0* to pin M20 of the U4 device to disable clock output.
X3	12	—	A10	—	Closing JP30 to enable clock input.

5.5. Push Buttons

The Lattice Sentry Demo Board for MachXO3D supports 10 push buttons (Figure 5.6) for general or dedicated purpose FPGA/CPLD pins. SW2, SW3, SW4, and SW5 (Table 5.9) belong to the MachXO3D device, SW6, SW8, and SW9 (Table 5.10) belong to the ECP5 (BMC) device, and SW13, SW14, SW15 (Table 5.11) belong to the ECP5 (PCH) device. When a push button is pressed, the logic *0* is sent to FPGA/CPLD. You must program inputs to be the LVCMOS33 type in the design for SW5, SW6, SW8, SW9, SW13, SW14, and SW15. But for SW2, SW3, and SW4 push buttons, the pull-up power is VCCIO_VAR, which is a variable power supply.

Note: If VCCIO_VAR power level is floated, the SW2, SW3, and SW4 push buttons are not pull-up power to output. This affects the system function.

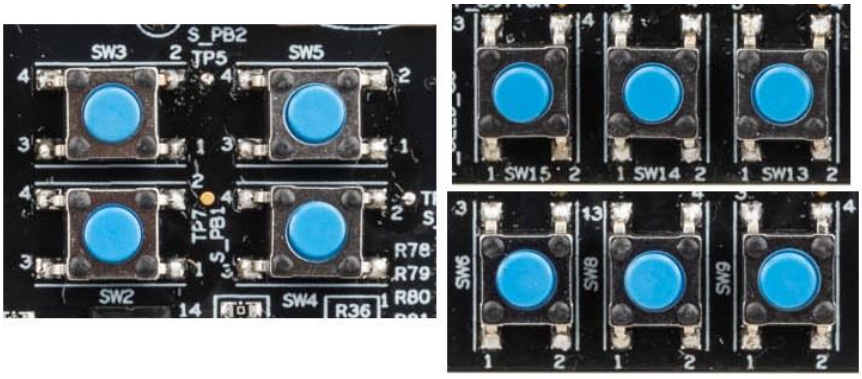


Figure 5.6. Push Buttons

Table 5.9. Push Buttons to MachXO3D Pins Position

Push Button Designator	MachXO3D U4 Pin Number	Signal Name
SW2	D3	S_PB1
SW3	D4	S_PB2
SW4	F6	S_PB3
SW5	E15	S_PROGRAMN

Table 5.10. Push Buttons to ECP5 (BMC) Pins Position

Push Button Designator	ECP5 (BMC) U11 Pin Number	Signal Name
SW6	G2	B_GSRN
SW8	W3	B_PROGRAMN
SW9	P4	B_BUTTON

Table 5.11. Push Buttons to ECP5 (PCH) Pins Position

Push Button Designator	ECP5 (PCH) U21 Pin Number	Signal Name
SW13	G2	P_GSRN
SW14	W3	P_PROGRAMN
SW15	J4	P_BUTTON

5.6. MachXO3D Connections for SPI/QSPI Monitor

The Lattice Sentry Demo Board for MachXO3D provides two SPI/QSPI monitor paths. MachXO3D can detect and block illegal data transaction by these paths. The signal definitions of the MachXO3D device are provided in Table 5.12 and Table 5.13.

Table 5.12. MachXO3D and ECP5 (BMC) SPI/QSPI Monitor Interface Definitions

MachXO3D U4 Pin Number	Signal Name	Signal Comment
Y18	S_QSBMC_EN	Quick switch enable signal
AB16	S_B_QSPI_CS_MNT	GPIO QSPI CS signal
T9 (Reserved)	S_MCLK	Flash clock signal
AA3 (Reserved)	S_CSSPIN	Flash CS signal
AA21 (Reserved)	S_SISPI	Flash data0 signal
U9 (Reserved)	S_SPISO	Flash data1 signal
AA10	S_FLASH_CLK_MNT	GPIO SPI clock signal
AB10	S_FLASH_CS_MNT	GPIO SPI CS signal
AA18	S_FLASH_DQ0_MNT	GPIO SPI data0 signal
AB9	S_FLASH_DQ1_MNT	GPIO SPI data1 signal
Y11	S_FLASH_DQ2	Flash data2 signal
Y12	S_FLASH_DQ3	Flash data3 signal
AB14	S_FLASHC_RSTN	Flash C reset signal
AA14	S_FLASHD_RSTN	Flash D reset signal
A2	S_OR_DISC	Flash C selection signal
B1	S_OR_DISD	Flash D selection signal
AB20	S_B_MSPI_CS_MNT	MSPI CS signal
AA20	S_B_SPI_CS_MNT	GPIO SPI CS signal

Table 5.13. MachXO3D and ECP5 (PCH) SPI/QSPI Monitor Interface Definitions

MachXO3D U4 Pin Number	Signal Name	Signal Comment
AA6	S_QSPCH00_EN	Quick switch enable signal
AB6	S_QSPCH01_EN	Quick switch enable signal
AA7	S_QSPCH10_EN	Quick switch enable signal
W2	P_FLASH_CLK_MNT	Flash clock signal
R2	P_FLASH_CS_MNT	Flash CS signal
R3	QSPCH_QSPI_IO0_MNT	Flash data0 signal
W1	QSPCH_QSPI_IO1_MNT	Flash data1 signal
U3	QSPCH_QSPI_IO2_MNT	Flash data2 signal
T1	QSPCH_QSPI_IO3_MNT	Flash data3 signal
AB19	S_OR_DISA	Flash A selection signal
AA19	S_OR_DISB	Flash B selection signal
AB15	S_FLASHA_RSTN	Flash A reset signal
AA15	S_FLASHB_RSTN	Flash B reset signal
AB7	S_QSPCH00_QSPI_CS_MNT	Quick switch CS signal
AB2	S_P_QSPI_CS_MNT	GPIO QSPI CS signal

5.7. ECP5 (BMC) SPI/QSPI and Control Interface

ECP5 (BMC) device has three SPI/QSPI data paths to access to external flash. The signal definitions of the ECP5 (BMC) device are provided in Table 5.14.

Table 5.14. ECP5 (BMC) SPI/QSPI and Control Interface Definitions

ECP5 (BMC) U11 Pin Number	Signal Name	Signal Comment
U3	B_MCLK	MSPI clock signal
R2	B_CSSPIN	MSPI CS signal
W2	B_DQ0_MOSI	MSPI data0 signal
V2	B_DQ1_MISO	MSPI data1 signal
A6	B_QSBMC_SPI_CLK	GPIO SPI clock signal
B8	B_QSBMC_SPI_CS	GPIO SPI CS signal
B9	B_QSBMC_SPI_IO0	GPIO SPI data0 signal
B6	B_QSBMC_SPI_IO1	GPIO SPI data1 signal
P19	B_QSBMC_SEL	Quick switch selection signal
L19	B_QSPCH00_QSPI_CLK	QSPI clock signal
L20	B_QSPCH00_QSPI_CS	QSPI CS signal
M20	B_QSPCH00_QSPI_IO0	QSPI data0 signal
L18	B_QSPCH00_QSPI_IO1	QSPI data1 signal
M19	B_QSPCH00_QSPI_IO2	QSPI data2 signal
N18	B_QSPCH00_QSPI_IO3	QSPI data3 signal
P19	B_QSBMC_SEL	Quick switch selection signal

5.8. ECP5 (PCH) SPI/QSPI and Control Interface

ECP5 (PCH) device has two SPI/QSPI data paths to access to external flash. The signal definitions of the ECP5 (PCH) device are provided in Table 5.15.

Table 5.15. ECP5 (CPH) SPI/QSPI and Control Interface Definitions

ECP5 (PCH) U21 Pin Number	Signal Name	Signal Comment
U3	P_MCLK	MSPI clock signal
R2	P_CSSPIN	MSPI CS signal
W2	P_DQ0_MOSI	MSPI data0 signal
V2	P_DQ1_MISO	MSPI data1 signal
B8	P_QSPCH00_QSPI_CLK	QSPI clock signal
A7	P_QSPCH00_QSPI_CS	QSPI CS signal
B9	P_QSPCH00_QSPI_IO0	QSPI data0 signal
A8	P_QSPCH00_QSPI_IO1	QSPI data1 signal
A9	P_QSPCH00_QSPI_IO2	QSPI data2 signal
B10	P_QSPCH00_QSPI_IO3	QSPI data3 signal
B11	P_QSPCH1_SEL	Quick switch selection signal

5.9. Reset Signals

The Lattice Sentry Demo Board for MachXO3D has three reset signals among the three main chips. The signal definitions of reset signals are provided in Table 5.16.

Table 5.16. Reset Signals Definitions

MachXO3D U4 Pin Number	ECP5 (BMC) U11 Pin Number	ECP5 (PCH) U21 Pin Number	Signal Name
C14	M17	—	B_S_RESETN
—	K4	K20	B_P_RESETN
N1	—	J18	S_PCH_RESETN

5.10. OOB Interface

The Lattice Sentry Demo Board for MachXO3D has one OOB data path between the MachXO3D and ECP5 (BMC) devices, and the data can be encrypted transmitted. The signal definitions of OOB path are provided in Table 5.17.

Table 5.17. OOB Interface Definitions

MachXO3D U4 Pin Number	ECP5 (BMC) U11 Pin Number	Signal Name
A3	P20	BMC_S_SDA-6_OOB
B2	R20	BMC_S_SCL-6_OOB
B3	T19	BMC_S_INT_OOB
A4	R18	BMC_S_PWM_OOB
A17	L16	B_S_OUT_BAND0
B18	J19	B_S_OUT_BAND1
D17	C13	B_S_OUT_BAND2
A18	J20	B_S_OUT_BAND3
B19	D16	B_S_OUT_BAND4

5.11. I²C Interface

The Lattice Sentry Demo Board for MachXO3D has multiple I²C paths on this demo board. They can implement many types of I²C functions. The signal definitions of I²C paths are provided in Table 5.18, Table 5.19, Table 5.20, Table 5.21, and Table 5.22.

Table 5.18. I²C between MachXO3D and ECP5 (PCH) Signal Definitions

MachXO3D U4 Pin Number	ECP5 (PCH) U21 Pin Number	Signal Name	Comment
K2	D20	S_PCH_SDA-1	ECP5 (PCH) to MachXO3D I²C SDA signal
K1	E19	S_PCH_SCL-1	ECP5 (PCH) to MachXO3D I²C SCL signal
AB13	F20	S_PCH_SDA-2	ECP5 (PCH) to MachXO3D I²C SDA signal
AA13	G20	S_PCH_SCL-2	ECP5 (PCH) to MachXO3D I²C SCL signal
AA11	G19	S_PCH_SDA-3	ECP5 (PCH) to MachXO3D I²C SDA signal
AB11	H20	S_PCH_SCL-3	ECP5 (PCH) to MachXO3D I²C SCL signal
V1	E20	S_PCH_SDA-4	ECP5 (PCH) to MachXO3D I²C SDA signal
U2	F19	S_PCH_SCL-4	ECP5 (PCH) to MachXO3D I²C SCL signal
AA22	C20	S_BMC_SDA-0	MachXO3D to ECP5 (PCH) I²C SDA signal
Y21	D19	S_BMC_SCL-0	MachXO3D to ECP5 (PCH) I²C SCL signal

Table 5.19. Interconnections among MachXO3D, ECP5 (BMC), and Repeater Signal Definitions

MachXO3D U4 Pin Number	ECP5 (BMC) U11 Pin Number	Repeater U13 Pin Number	Signal Name	Comment
AB17	U18	6	B_RP_SDA-5	ECP5 (BMC)/MachXO3D to repeater I²C SDA signal
AA17	U17	7	B_RP_SCL-5	ECP5 (BMC)/MachXO3D to repeater I²C SCL signal
A12	T20	—	BMC_S_SDA-7_PRG	ECP5 (BMC) to MachXO3D program I²C SDA signal
B12	U20	—	BMC_S_SCL-7_PRG	ECP5 (BMC) to MachXO3D program I²C SCL signal
Y10	—	5	S_RP_EN	MachXO3D to repeater chip enable signal
U1	A16	—	S_B_I3C_U1*	ECP5 (BMC) to MachXO3D I²C signal
Y1	A15	—	S_B_I3C_Y1*	ECP5 (BMC) to MachXO3D I²C signal
T2	A17	—	S_B_I3C_T2*	ECP5 (BMC) to MachXO3D I²C signal
AA1	A12	—	S_B_I3C_AA1*	ECP5 (BMC) to MachXO3D I²C signal

***Note**: These signals can be used for I3C, too.

Table 5.20. Interconnections among MachXO3D, ECP5 (BMC), ECP5 (PCH), and EEPROM Signal Definitions

MachXO3D U4 Pin Number	ECP5 (BMC) U11 Pin Number	ECP5 (PCH) U21 Pin Number	EEPROM U32 Pin Number	Signal Name	Comment
Y2	—	T20	5	P_EEPROM_SDA-5	ECP5 (PCH)/MachXO3D to EEPROM I²C SDA signal
W3	—	U20	6	P_EEPROM_SCL-5	ECP5 (PCH)/MachXO3D to EEPROM I²C SCL signal
W10	—	—	7	S_EEPROM_WP	MachXO3D to EEPROM write protect signal
—	U16	—	1	B_EEPROM_ADR_A0	ECP5 (BMC) to EEPROM address bit 0
—	T18	—	2	B_EEPROM_ADR_A1	ECP5 (BMC) to EEPROM address bit 1
—	P18	—	3	B_EEPROM_ADR_A2	ECP5 (BMC) to EEPROM address bit 2

Table 5.21. Interconnections between MachXO3D and RTC Signal Definitions

MachXO3D U4 Pin Number	RTC U3 Pin Number	Signal Name	Comment
C19	13	S_RTC_SDA	MachXO3D to RTC I^2C SDA signal
C20	2	S_RTC_SCL	MachXO3D to RTC I^2C SCL signal
B10	3	S_RTC_S_32KCLKOUT	RTC 32.768 kHz clock output signal
B11	7	S_RTC_CLKOUT_CTL	RTC 32.768 kHz clock output control signal
B21	10	RTC_S_INTA	RTC interrupt output signal
A20	12	RTC_S_INTB	RTC interrupt output signal

Table 5.22. I^2C between MachXO3D and FTDI Device Signal Definitions

MachXO3D U4 Pin Number	FTDI U1 Pin Number	Signal Name	Comment
B12	38	S_FTDI_SCL_PRG*	MachXO3D to FTDI device I^2C SDA signal
A12	39,40	S_FTDI_SDA_PRG*	MachXO3D to FTDI device I^2C SCL signal

***Note**: These signals are not connected.

5.12. ESPI Interface

The Lattice Sentry Demo Board for MachXO3D has two ESPI paths on this demo board. They can implement ESPI data transition functions. The signal definitions of ESPI paths describe as Table 5.23 and Table 5.24.

Table 5.23. ESPI between ECP (BMC) and ECP (PCH) Definitions

ECP5 (BMC) U11 Pin Number	ECP5 (PCH) U21 Pin Number	Signal Name	Comment
F2	C1	B_P_ESPI_CLK	ECP5 (BMC) to ECP5 (PCH) ESPI clock signal
H3	B1	B_P_ESPI_CS	ECP5 (BMC) to ECP5 (PCH) ESPI CS signal
G3	D2	B_P_ESPI_ALERT	ECP5 (BMC) to ECP5 (PCH) ESPI alert signal
H5	C2	B_P_ESPI_DATA0	ECP5 (BMC) to ECP5 (PCH) ESPI data0signal
G5	E1	B_P_ESPI_DATA1	ECP5 (BMC) to ECP5 (PCH) ESPI data1 signal
H4	B2	B_P_ESPI_DATA2	ECP5 (BMC) to ECP5 (PCH) ESPI data2 signal
E1	D1	B_P_ESPI_DATA3	ECP5 (BMC) to ECP5 (PCH) ESPI data3 signal
D2	G5	B_P_ESPI_DATA4	ECP5 (BMC) to ECP5 (PCH) ESPI data4 signal
D1	F2	B_P_ESPI_DATA5	ECP5 (BMC) to ECP5 (PCH) ESPI data5 signal
C1	H5	B_P_ESPI_DATA6	ECP5 (BMC) to ECP5 (PCH) ESPI data6 signal
C2	G3	B_P_ESPI_DATA7	ECP5 (BMC) to ECP5 (PCH) ESPI data7 signal
B2	H3	B_P_ESPI_DATA8	ECP5 (BMC) to ECP5 (PCH) ESPI data8 signal
B1	H4	B_P_ESPI_DATA9	ECP5 (BMC) to ECP5 (PCH) ESPI data9 signal

Table 5.24. ESPI between MachXO3D and ECP (PCH) Definitions

MachXO3D U4 Pin Number	ECP5 (PCH) U21 Pin Number	Signal Name	Comment
H4	D12	S_P_ESPI_CLK	MachXO3D to ECP5 (PCH) ESPI clock signal
G2	C12	S_P_ESPI_CS	MachXO3D to ECP5 (PCH) ESPI CS signal
J7	E14	S_P_ESPI_ALERT	MachXO3D to ECP5 (PCH) ESPI alert signal
J6	D14	S_P_ESPI_DATA0	MachXO3D to ECP5 (PCH) ESPI data0signal
J5	C14	S_P_ESPI_DATA1	MachXO3D to ECP5 (PCH) ESPI data1 signal
J2	A14	S_P_ESPI_DATA2	MachXO3D to ECP5 (PCH) ESPI data2 signal
H3	E13	S_P_ESPI_DATA3	MachXO3D to ECP5 (PCH) ESPI data3 signal
J3	D13	S_P_ESPI_DATA4	MachXO3D to ECP5 (PCH) ESPI data4 signal
H1	C13	S_P_ESPI_DATA5	MachXO3D to ECP5 (PCH) ESPI data5 signal
H2	B13	S_P_ESPI_DATA6	MachXO3D to ECP5 (PCH) ESPI data6 signal
G1	A13	S_P_ESPI_DATA7	MachXO3D to ECP5 (PCH) ESPI data7 signal
J4	A12	S_P_ESPI_DATA8	MachXO3D to ECP5 (PCH) ESPI data8 signal
H5	E12	S_P_ESPI_DATA9	MachXO3D to ECP5 (PCH) ESPI data9 signal

5.13. UART Interface

The Lattice Sentry Demo Board for MachXO3D has three UART interfaces. Connect the PC that is installed with serial terminal software to connector J2 with a USB cable. The MachXO3D device can communicate PC through UART interface. Connect PC and connector J6 with a USB cable in the same way. The ECP5 (BMC) and the ECP5 (PCH) devices can input order and output information with UART interface. The signal definitions are described in Table 5.25, Table 5.26, and Table 5.27.

Table 5.25. MachXO3D UART Definitions

MachXO3D U4 Pin Number	FTDI U1 Pin Number	Signal Name
A13	38	S_UART_TXD
B13	39	S_UART_RXD

Table 5.26. ECP5 (BMC) UART Definitions

ECP5 (BMC) U11 Pin Number	FTDI U9 Pin Number	Signal Name
P2	16	B_UART_TXD
P3	17	B_UART_RXD

Table 5.27. ECP5 (PCH) UART Definitions

ECP5 (PCH) U21 Pin Number	FTDI U9 Pin Number	Signal Name
P1	38	P_UART_TXD
P2	39	P_UART_RXD

5.14. Expansion Signals

There are four expansion connectors on the Lattice Sentry Demo Board for MachXO3D. The connector J61 is the Raspberry PI connector. It is installed on the bottom side of the board. The connectors J7 and J10 are OLED connectors. The connector J13 is Aardvark connector. The expansion signals of the four connectors, J61, J7, J10, and J13, are LVCMOS33 power level. You can use these expansion signals for your own purpose. The signal definitions are described in Table 5.28, Table 5.29, Table 5.30, and Table 5.31.

Table 5.28. Raspberry PI Connector Signal Definitions

MachXO3D U4 Pin Number	Raspberry PI Connector J61 Pin Number	Signal Name
C21	33	S_RASP_IO02
C22	32	S_RASP_IO03
F17	7	S_RASP_IO04
F22	23	S_RASP_IO05
G22	21	S_RASP_IO06
H19	15	S_RASP_IO07
H20	16	S_RASP_IO08
E21	27	S_RASP_IO09
E22	26	S_RASP_IO10
E19	29	S_RASP_IO11
K22	13	S_RASP_IO12
F18	37	S_RASP_IO13
G20	24	S_RASP_IO14
G19	12	S_RASP_IO15
L21	10	S_RASP_IO16
G16	40	S_RASP_IO17
G18	5	S_RASP_IO18
F19	36	S_RASP_IO19
L22	11	S_RASP_IO20
M17	3	S_RASP_IO21
D20	31	S_RASP_IO22
H22	18	S_RASP_IO23
H21	19	S_RASP_IO24
G17	38	S_RASP_IO25
G21	22	S_RASP_IO26
D19	35	S_RASP_IO27
H18	8	S_RASP_ID_SC
E20	28	S_RASP_ID_SD

Table 5.29. OLED Signal between ECP5 (BMC) and Connector Definitions

ECP5 (BMC) U11 Pin Number	OLED Connector J7 Pin Number	Signal Name
F1	4	B_OLED_MOSI
H2	7	B_OLED_CS
G1	3	B_OLED_CLK
J4	6	B_OLED_MISO
J5	5	B_OLED_RST

Table 5.30. OLED Signal between ECP5 (PCH) and Connector Definitions

ECP5 (PCH) U21 Pin Number	OLED Connector J10 Pin Number	Signal Name
T19	4	P_OLED_MOSI
R18	7	P_OLED_CS
U19	3	P_OLED_CLK
T18	6	P_OLED_MISO
U18	5	P_OLED_RST

Table 5.31. Aardvark Connector Signal Definitions

MachXO3D U4 Pin Number	Aardvark Connector J13 Pin Number	Signal Name
B2	1	BMC_S_SCL-6
A3	3	BMC_S_SDA-6
C9	5	AWK_S_SO
D9	7	AWK_S_MCLK
A9	8	AWK_S_SI
B9	9	AWK_S_CS

5.15. Reserved Interconnections

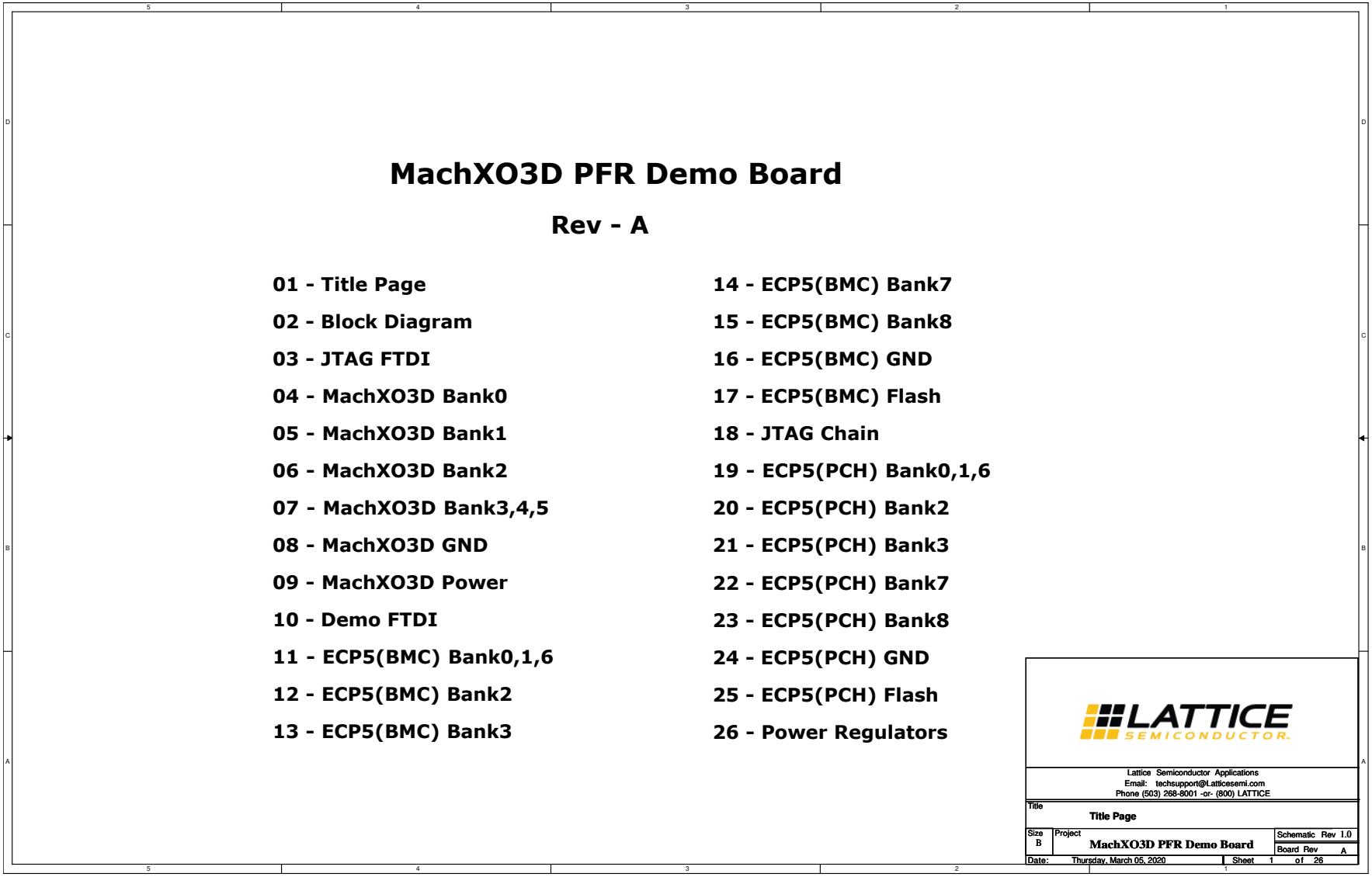
The Lattice Sentry Demo Board for MachXO3D reserved many signals. These signals have same key words RSV in the net name. The reserved signal is either differential line or single line. If differential lines are needed, the terminal 100 Ω resistor must be installed. You can use these signal lines for your purpose.

Many signal lines are not directly connected to each other. There is a 0 Ω jumper resistor in the middle of the signal lines. This 0 Ω jumper resistor is not installed on the Lattice Sentry Demo Board for MachXO3D. You can use these signal lines for your purpose after installing the 0 Ω jumper resistor.

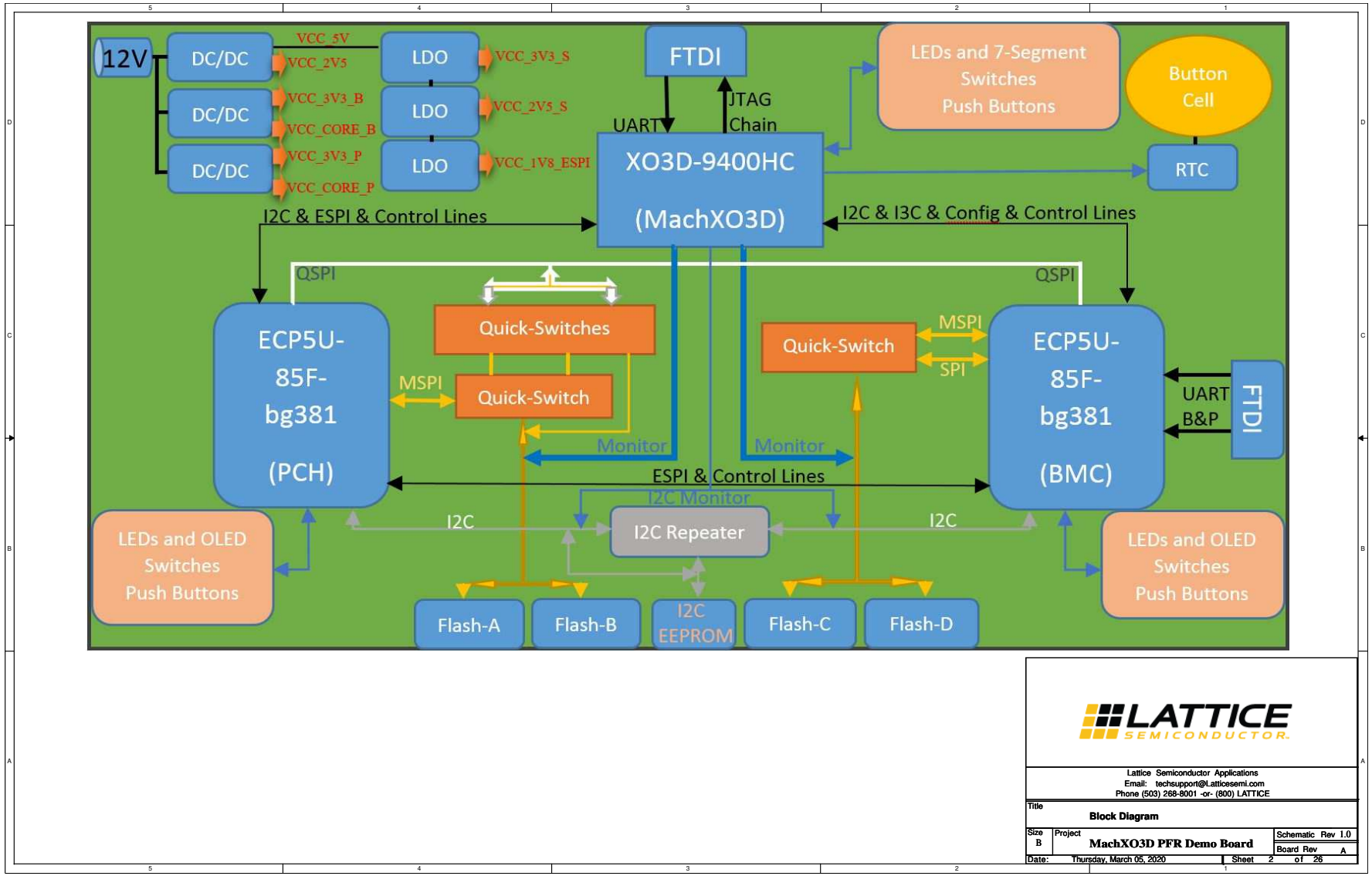
Reserved interconnections increase the flexibility of the design to meet unpredictable requirement. For detailed information of the design, refer to Appendix A. Schematics of Lattice Sentry Demo Board for MachXO3D.

Appendix A. Schematics of Lattice Sentry Demo Board for MachXO3D

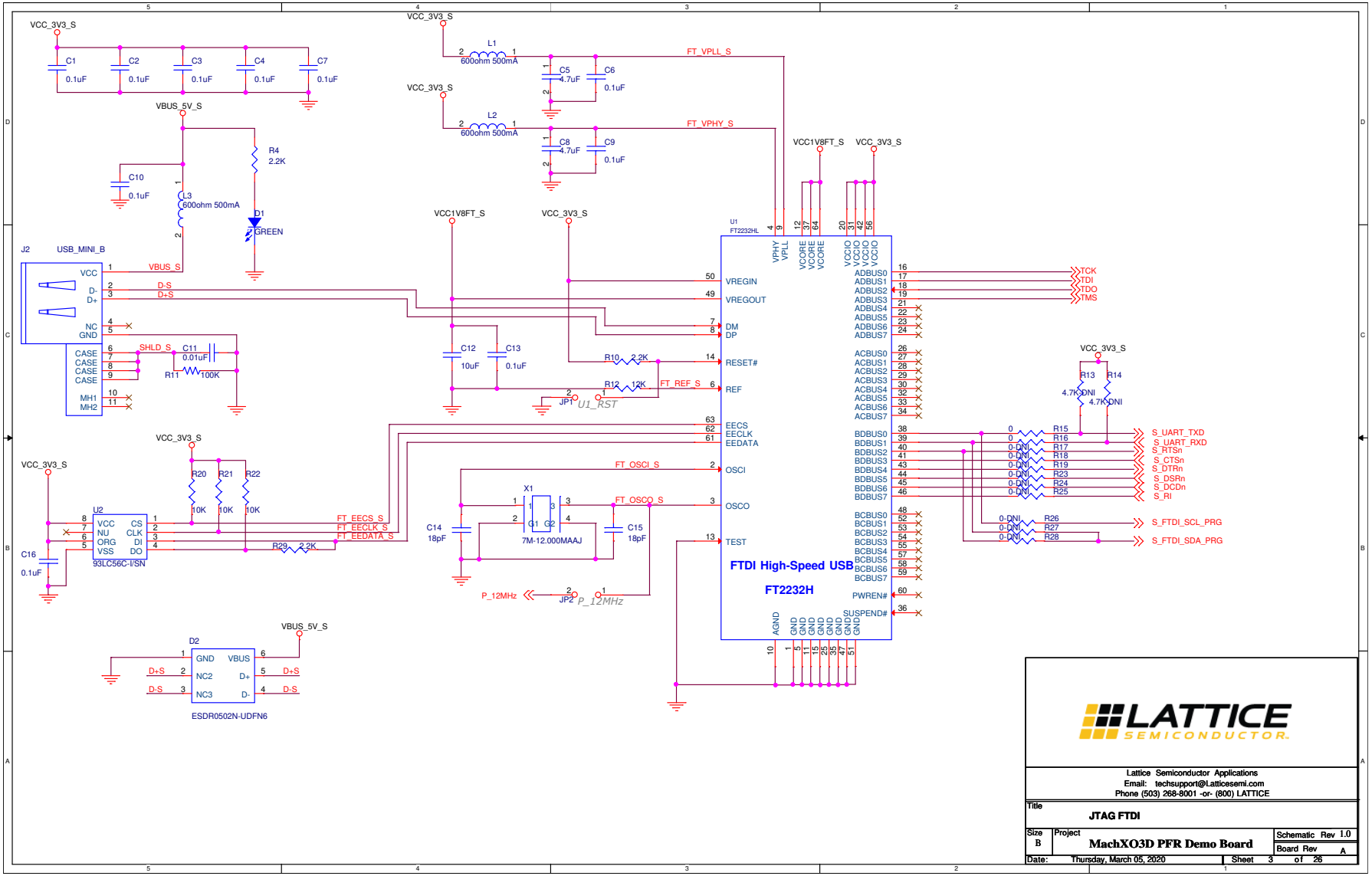
01 – Title Page



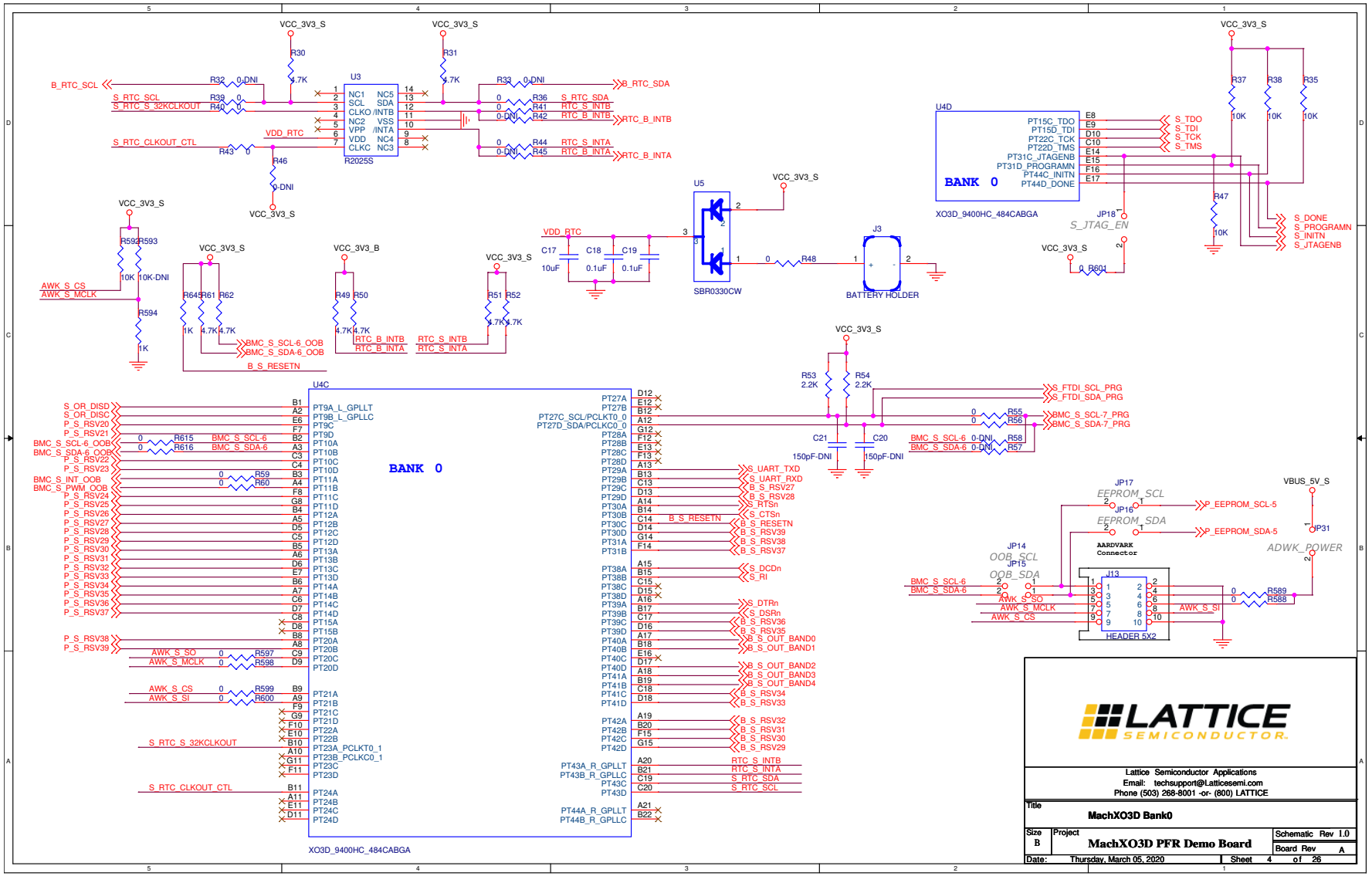
02 – Block Diagram



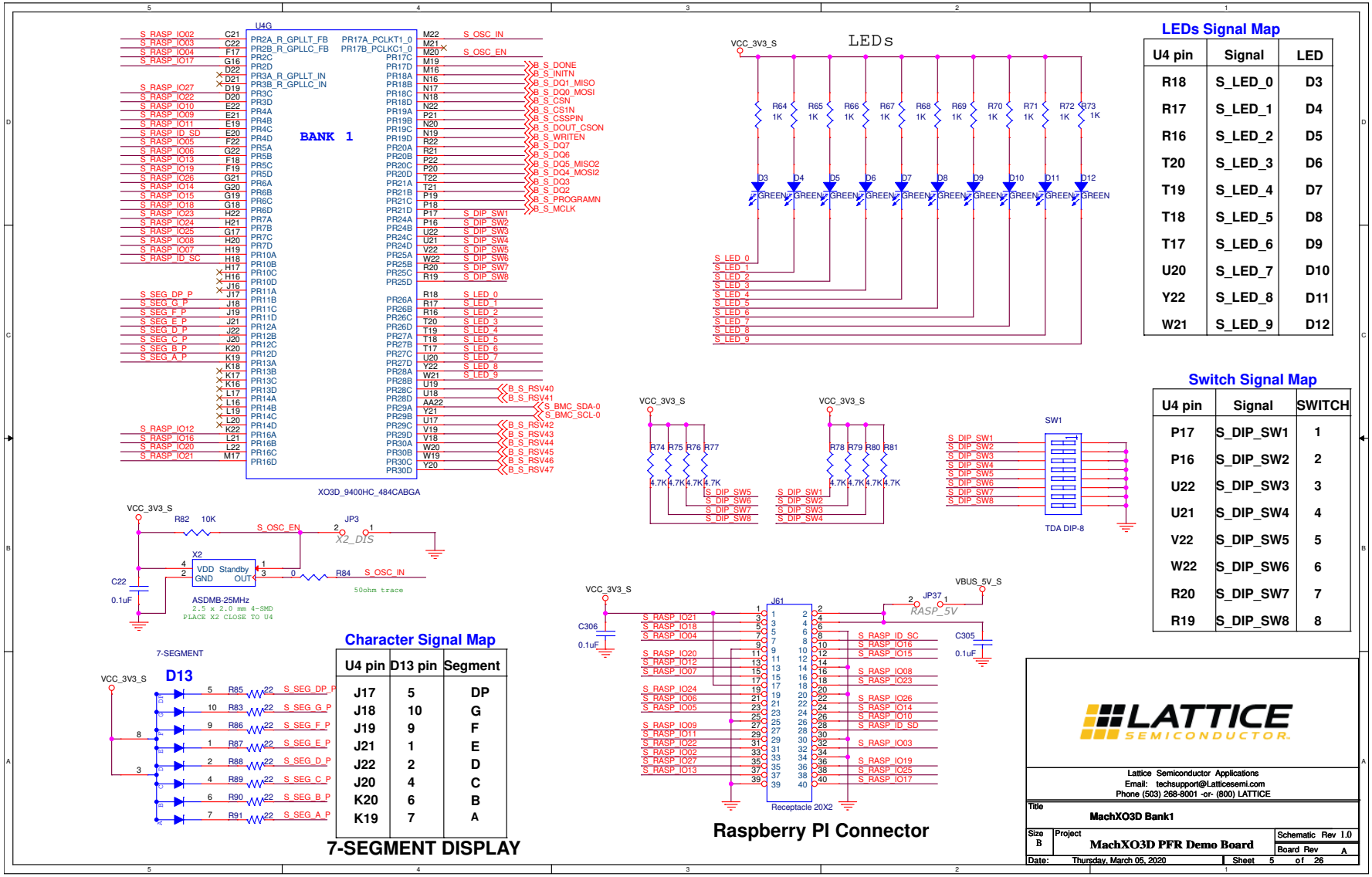
03 – JTAG FTDI



04 – MachXO3D Bank0



05 – MachXO3D Bank1



LEDs Signal Map

U4 pin	Signal	LED
R18	S_LED_0	D3
R17	S_LED_1	D4
R16	S_LED_2	D5
T20	S_LED_3	D6
T19	S_LED_4	D7
T18	S_LED_5	D8
T17	S_LED_6	D9
U20	S_LED_7	D10
Y22	S_LED_8	D11
W21	S_LED_9	D12

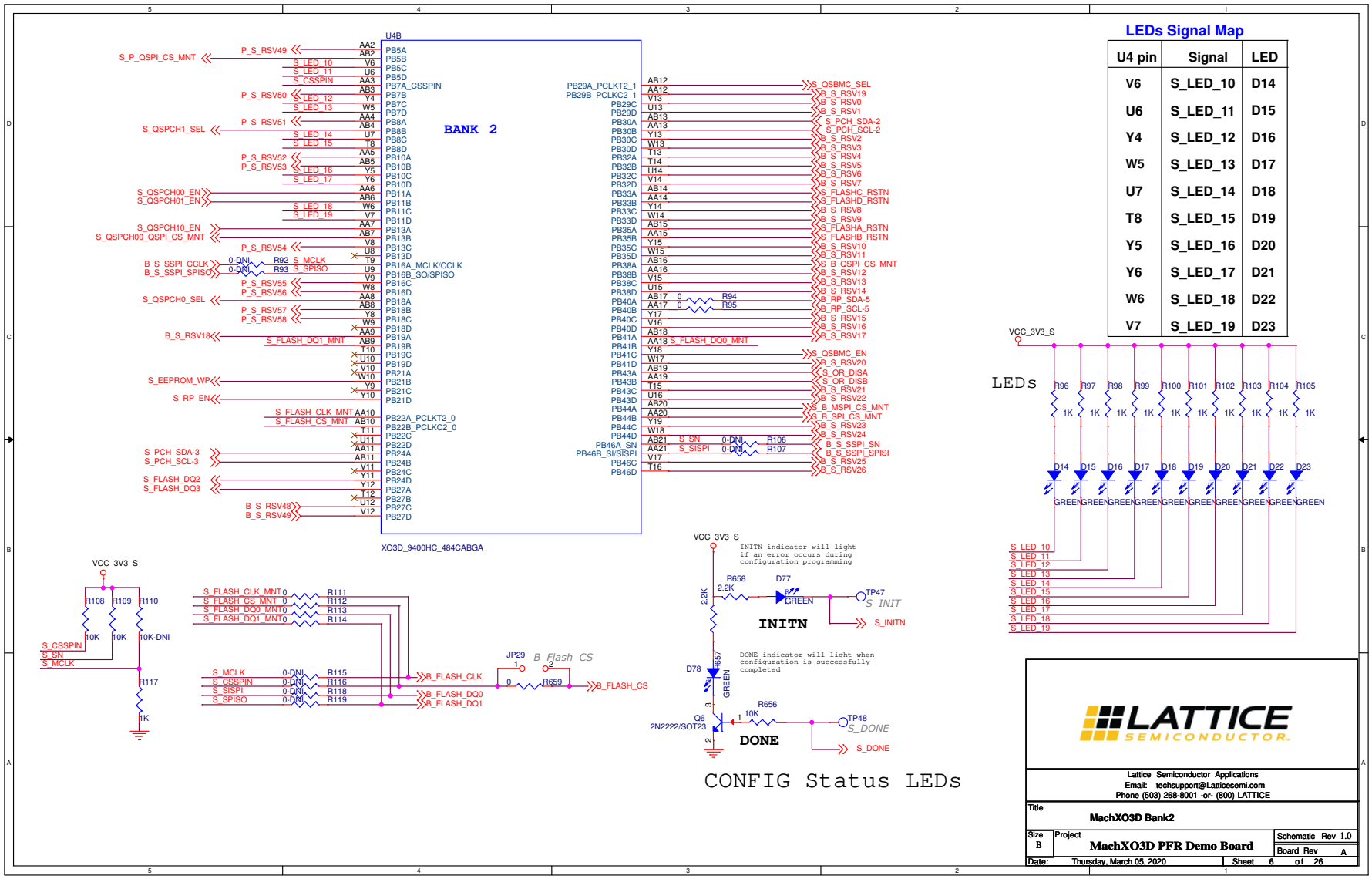
Switch Signal Map

U4 pin	Signal	SWITCH
P17	S_DIP_SW1	1
P16	S_DIP_SW2	2
U22	S_DIP_SW3	3
U21	S_DIP_SW4	4
V22	S_DIP_SW5	5
W22	S_DIP_SW6	6
R20	S_DIP_SW7	7
R19	S_DIP_SW8	8

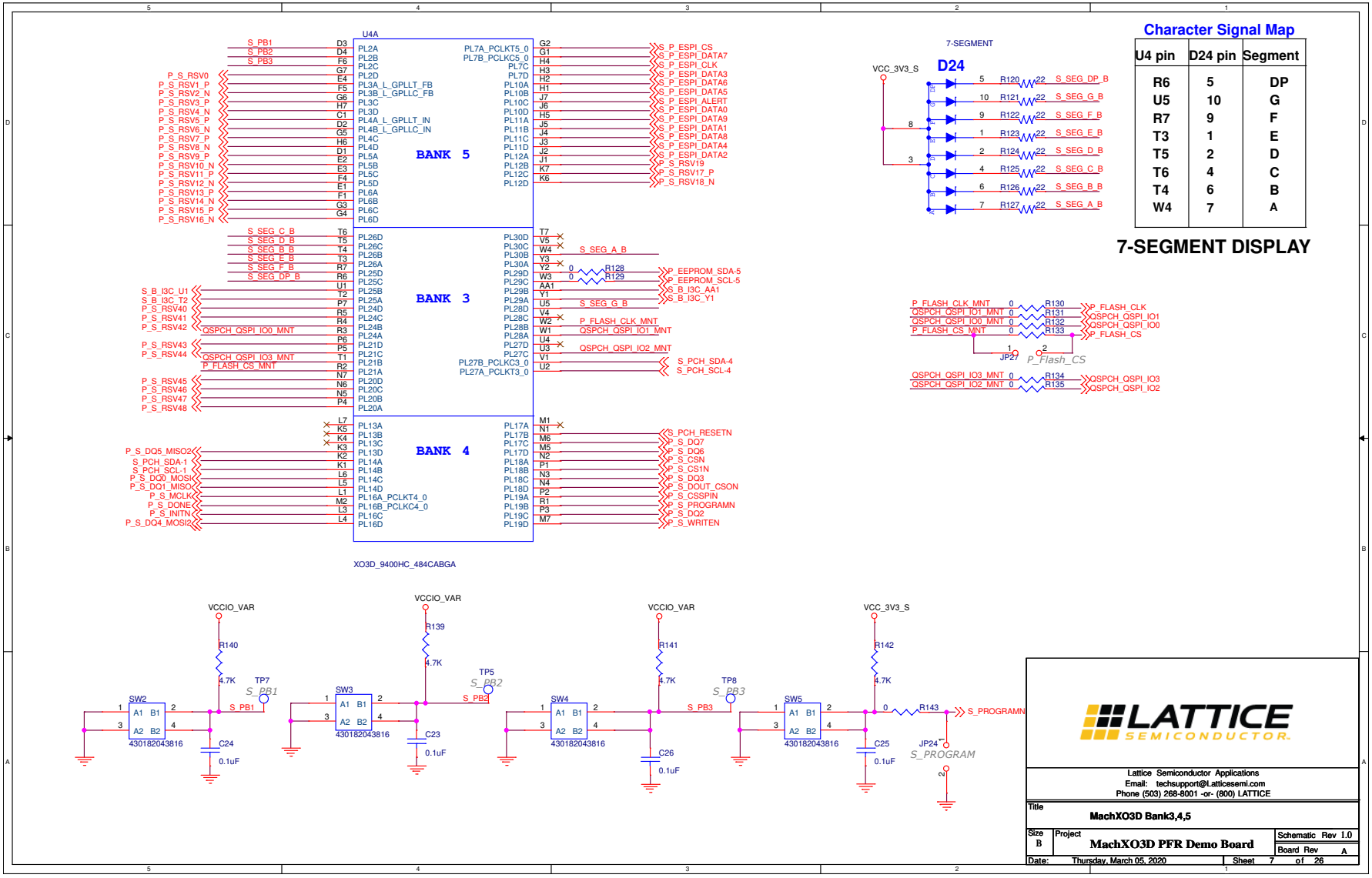
Character Signal Map

U4 pin	D13 pin	Segment
J17	5	DP
J18	10	G
J19	9	F
J21	1	E
J22	2	D
J20	4	C
K20	6	B
K19	7	A

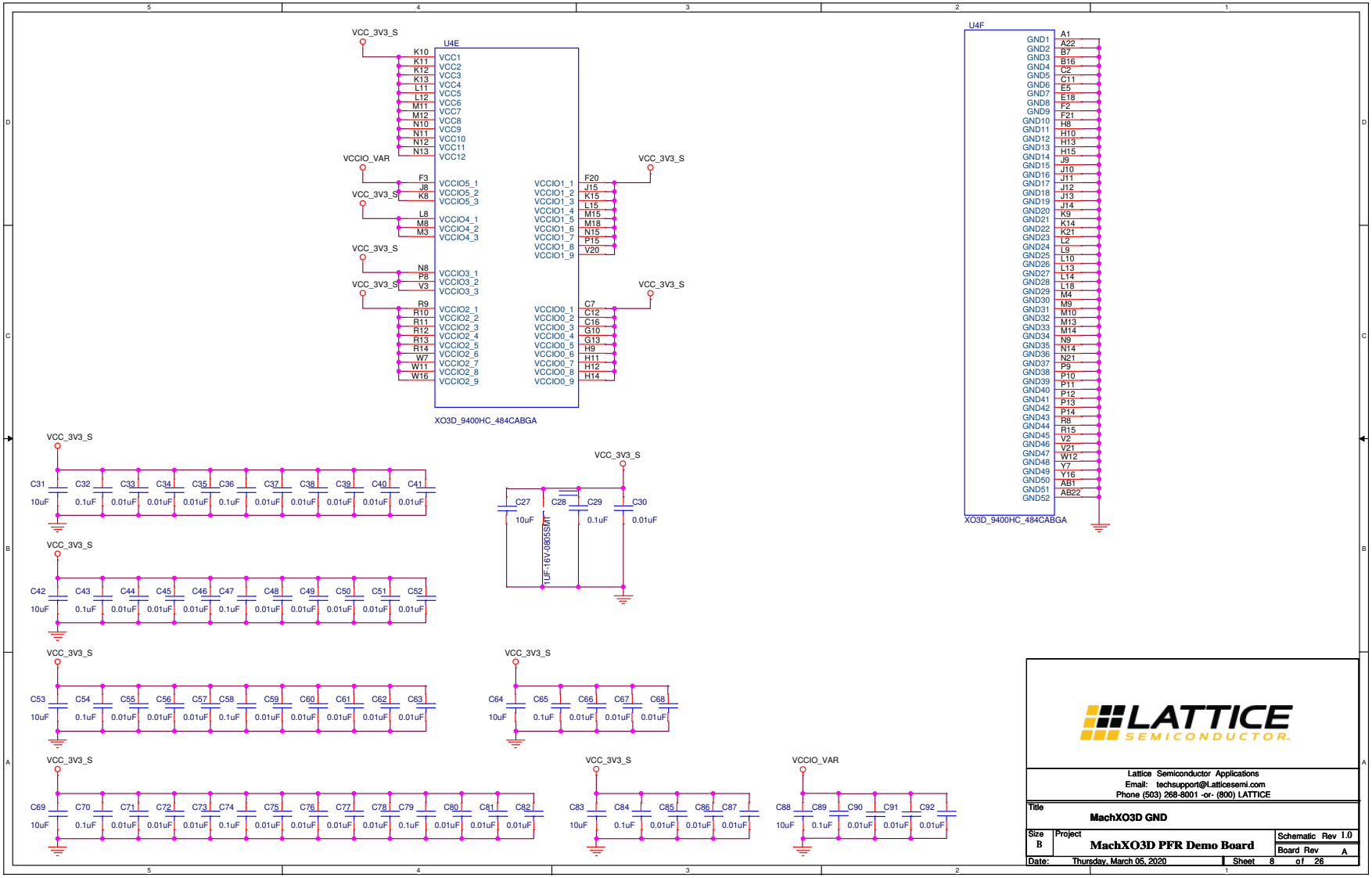
06 – MachXO3D Bank2



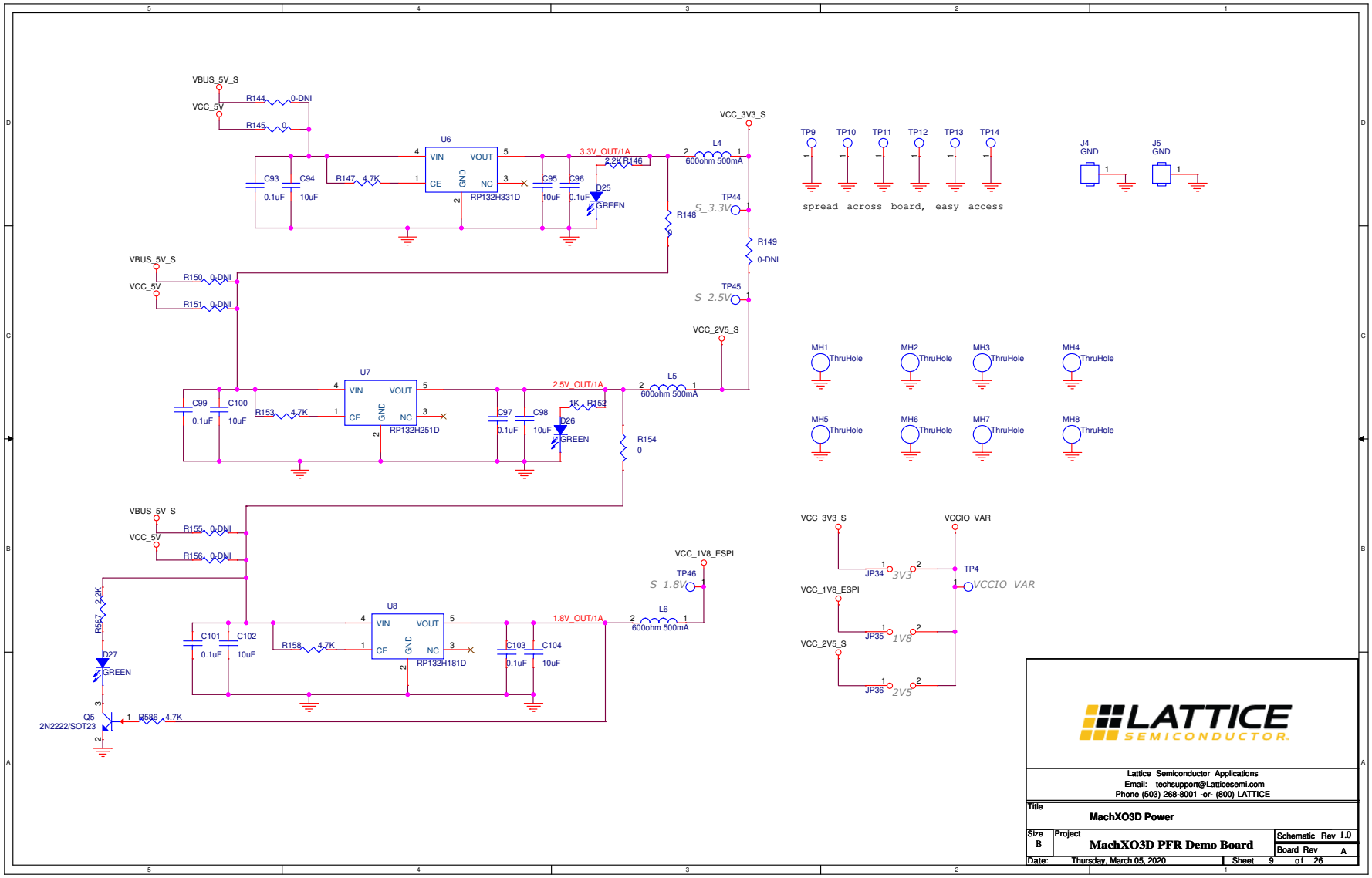
07 – MachXO3D Bank3,4,5



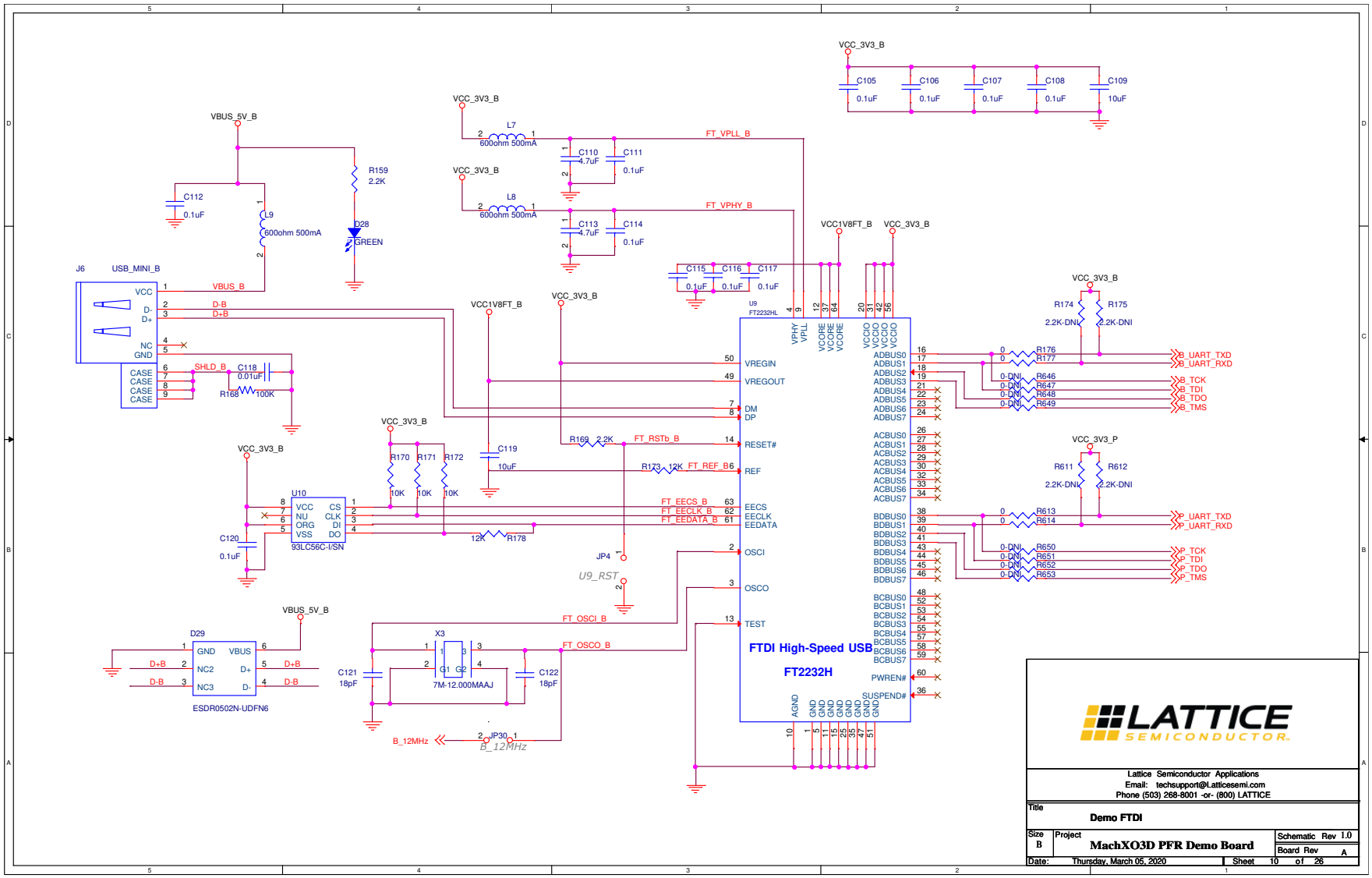
08 – MachXO3D GND



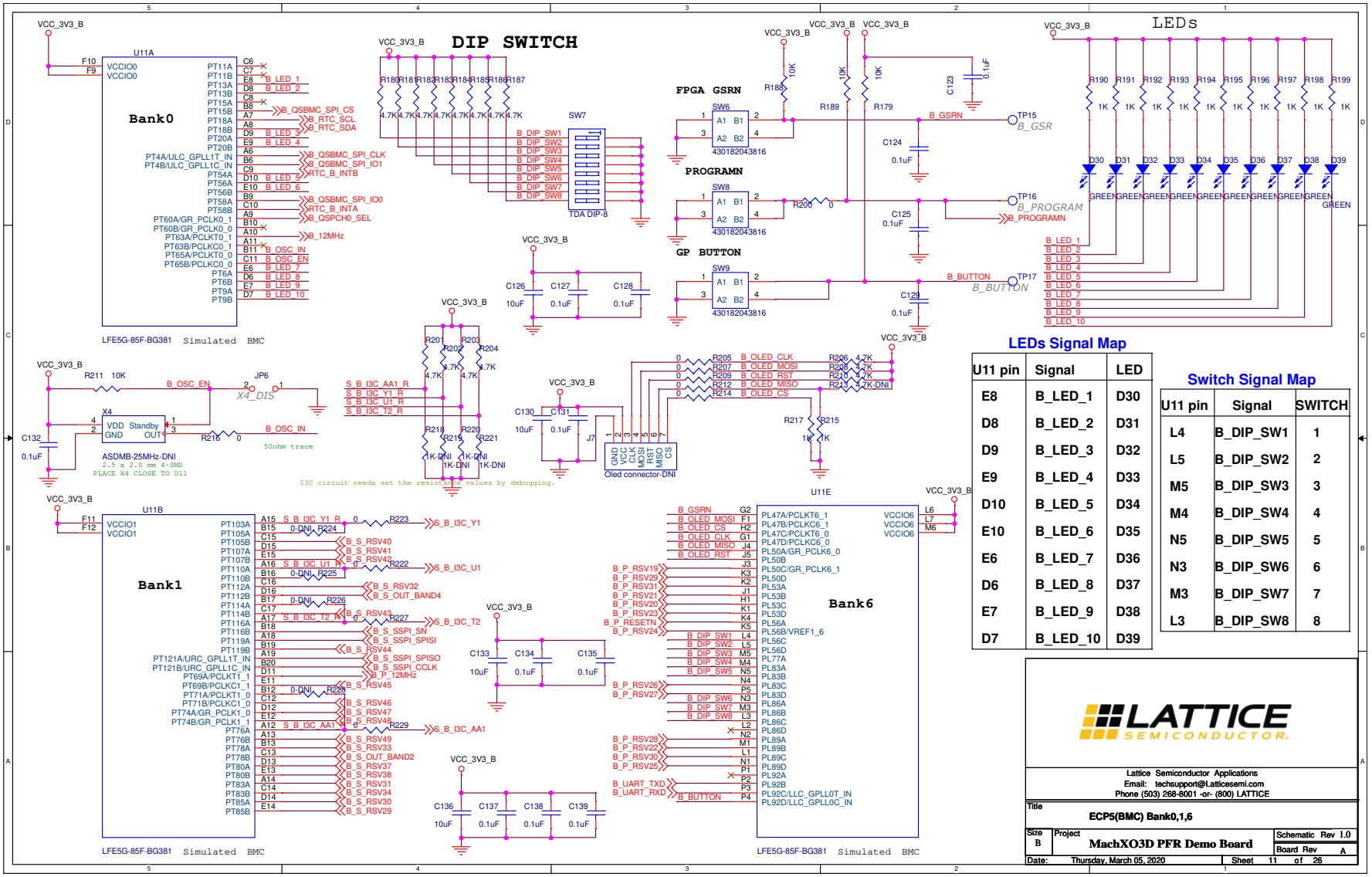
09 – MachXO3D Power



10 – Demo FTDI



11 – ECP5(BMC) Bank0,1,6



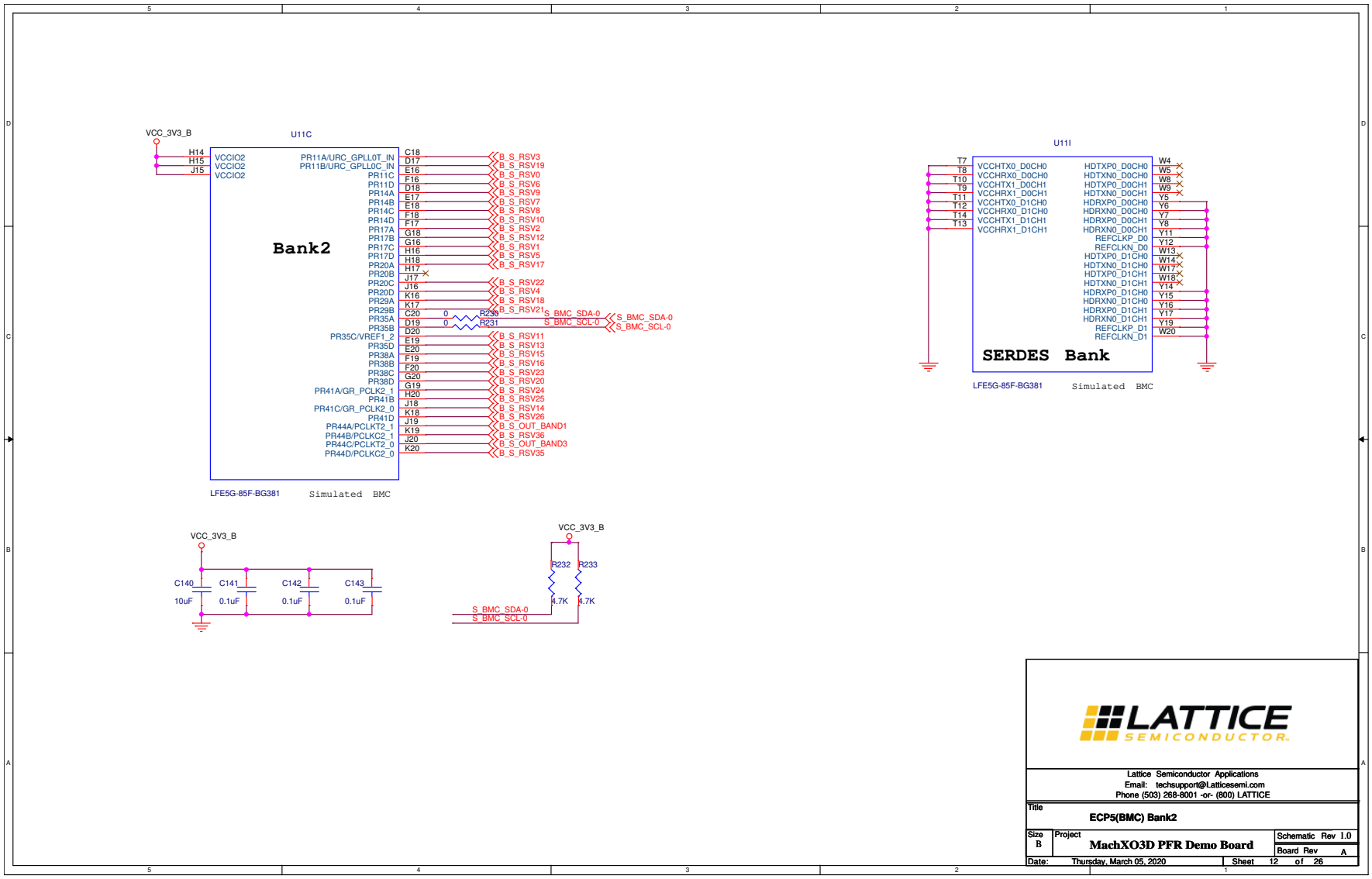
LEDs Signal Map

U11 pin	Signal	LED
E8	B_LED_1	D30
D8	B_LED_2	D31
D9	B_LED_3	D32
E9	B_LED_4	D33
M5	B_DIP_SW3	3
D10	B_LED_5	D34
M4	B_DIP_SW4	4
E10	B_LED_6	D35
N5	B_DIP_SW5	5
E6	B_LED_7	D36
N3	B_DIP_SW6	6
D6	B_LED_8	D37
M3	B_DIP_SW7	7
E7	B_LED_9	D38
L3	B_DIP_SW8	8
D7	B_LED_10	D39

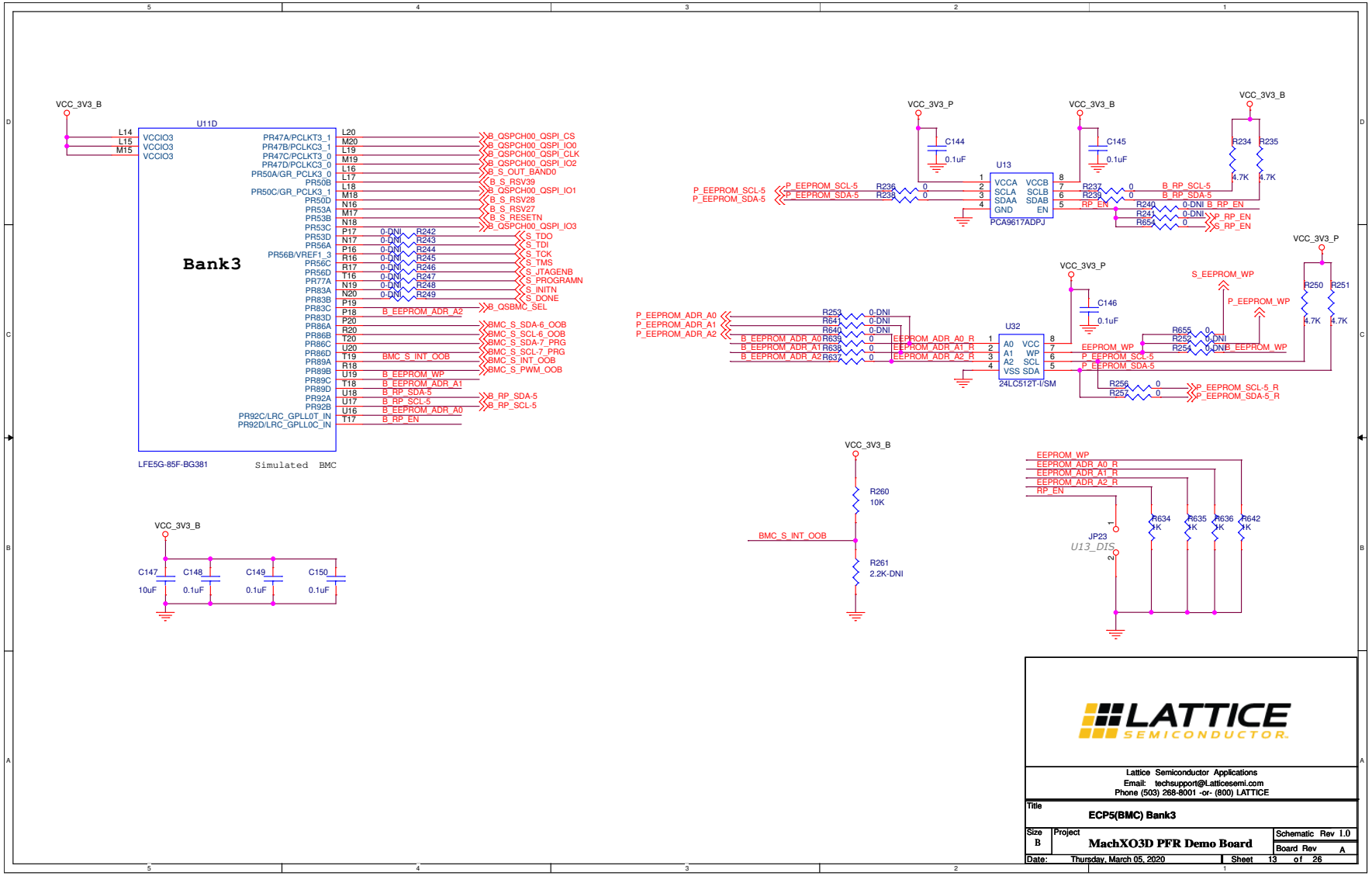
Switch Signal Map

U11 pin	Signal	SWITCH
L4	B_DIP_SW1	1
L5	B_DIP_SW2	2
M5	B_DIP_SW3	3
M4	B_DIP_SW4	4
N5	B_DIP_SW5	5
N3	B_DIP_SW6	6
M3	B_DIP_SW7	7
L3	B_DIP_SW8	8

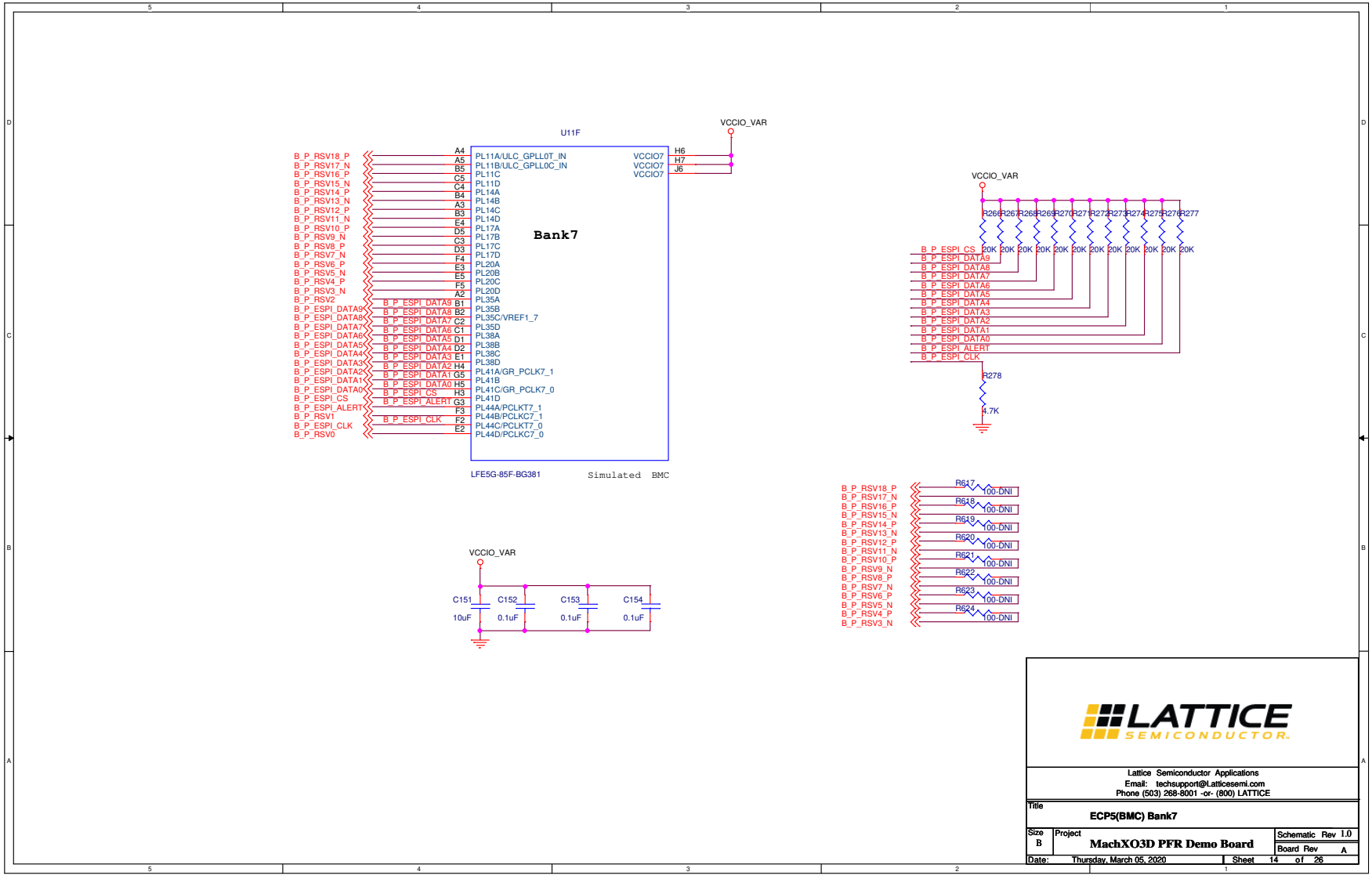
12 – ECP5(BMC) Bank2



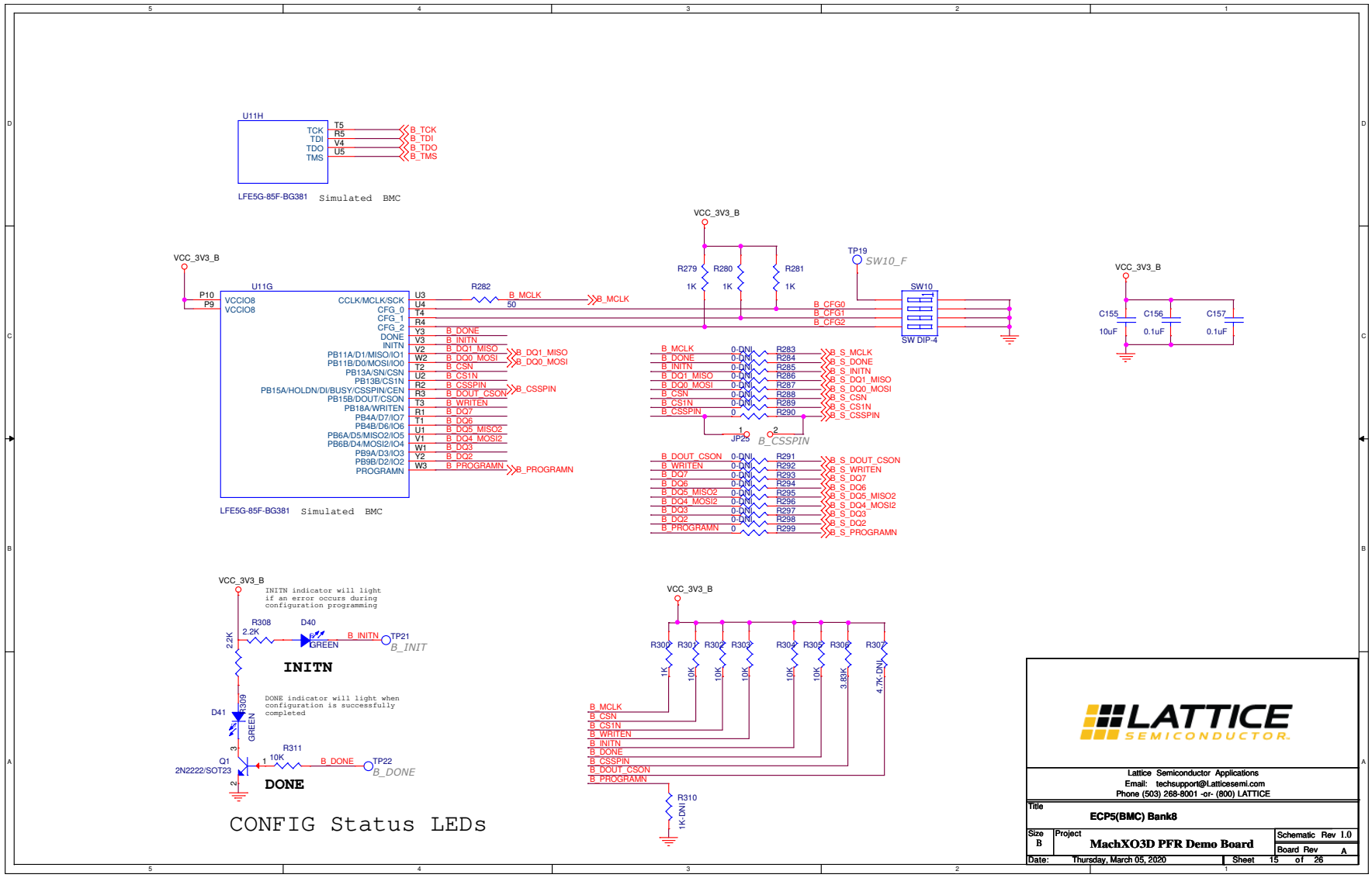
13 – ECP5(BMC) Bank3



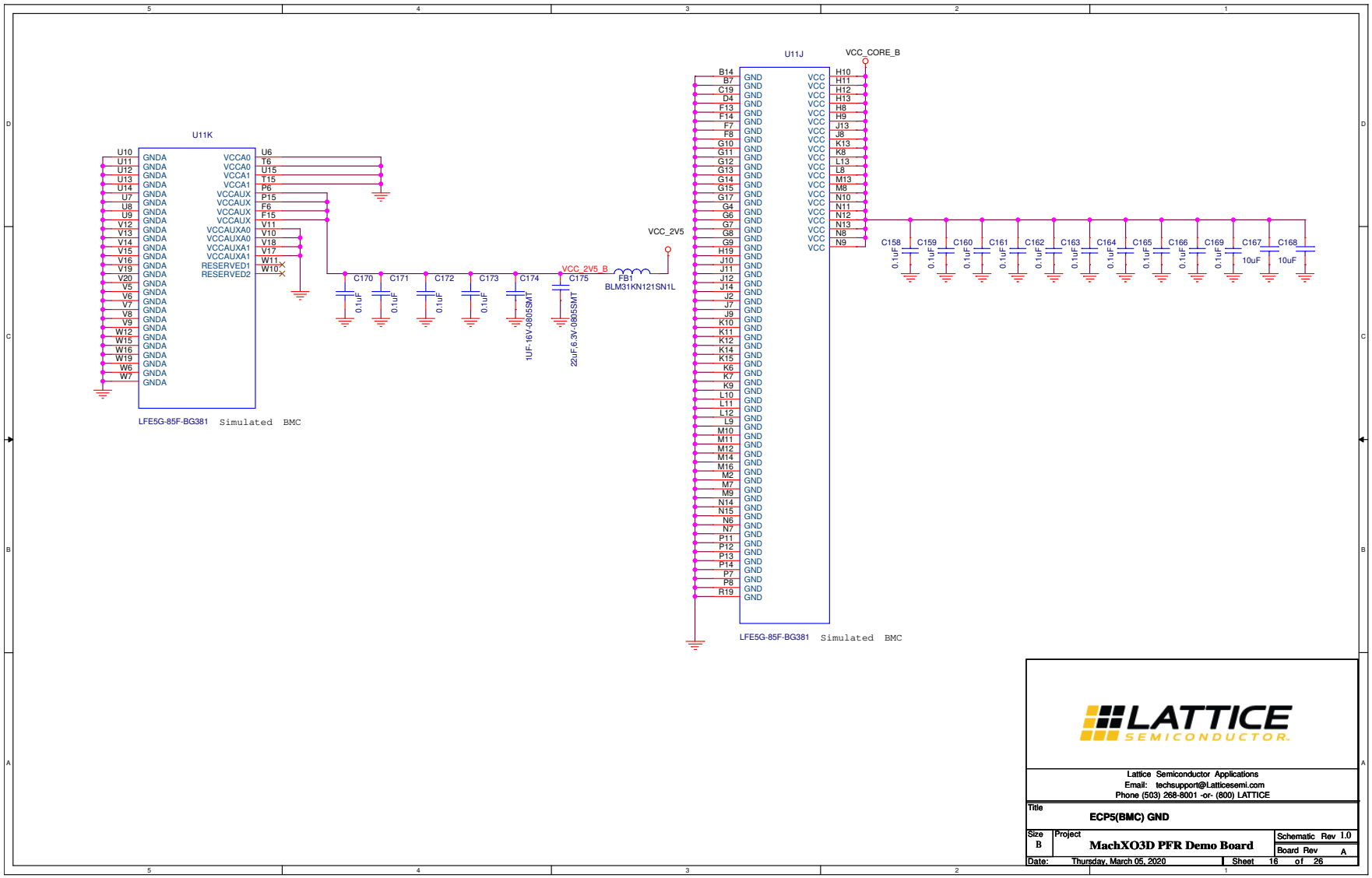
14 – ECP5(BMC) Bank7



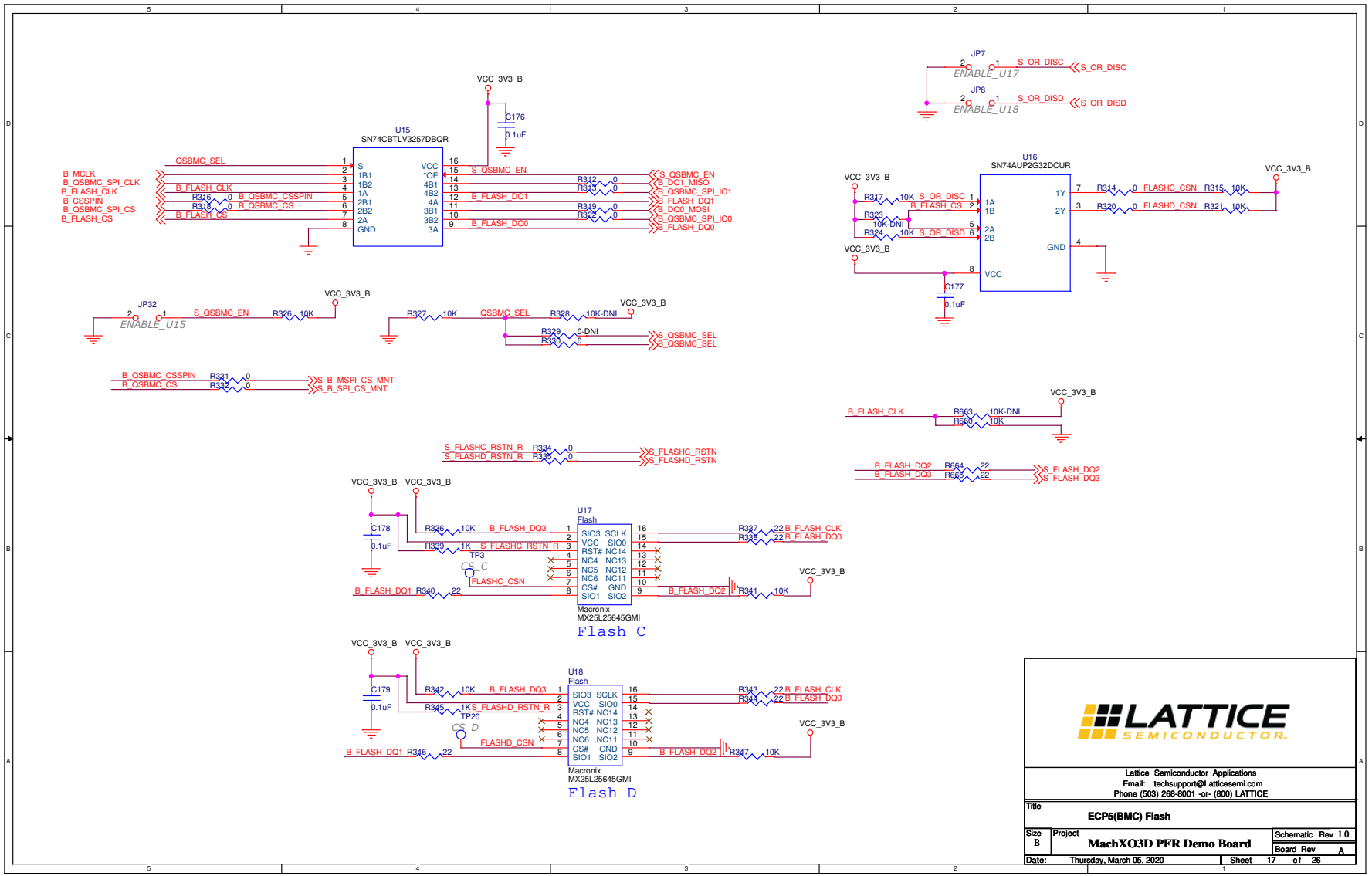
15 – ECP5(BMC) Bank3



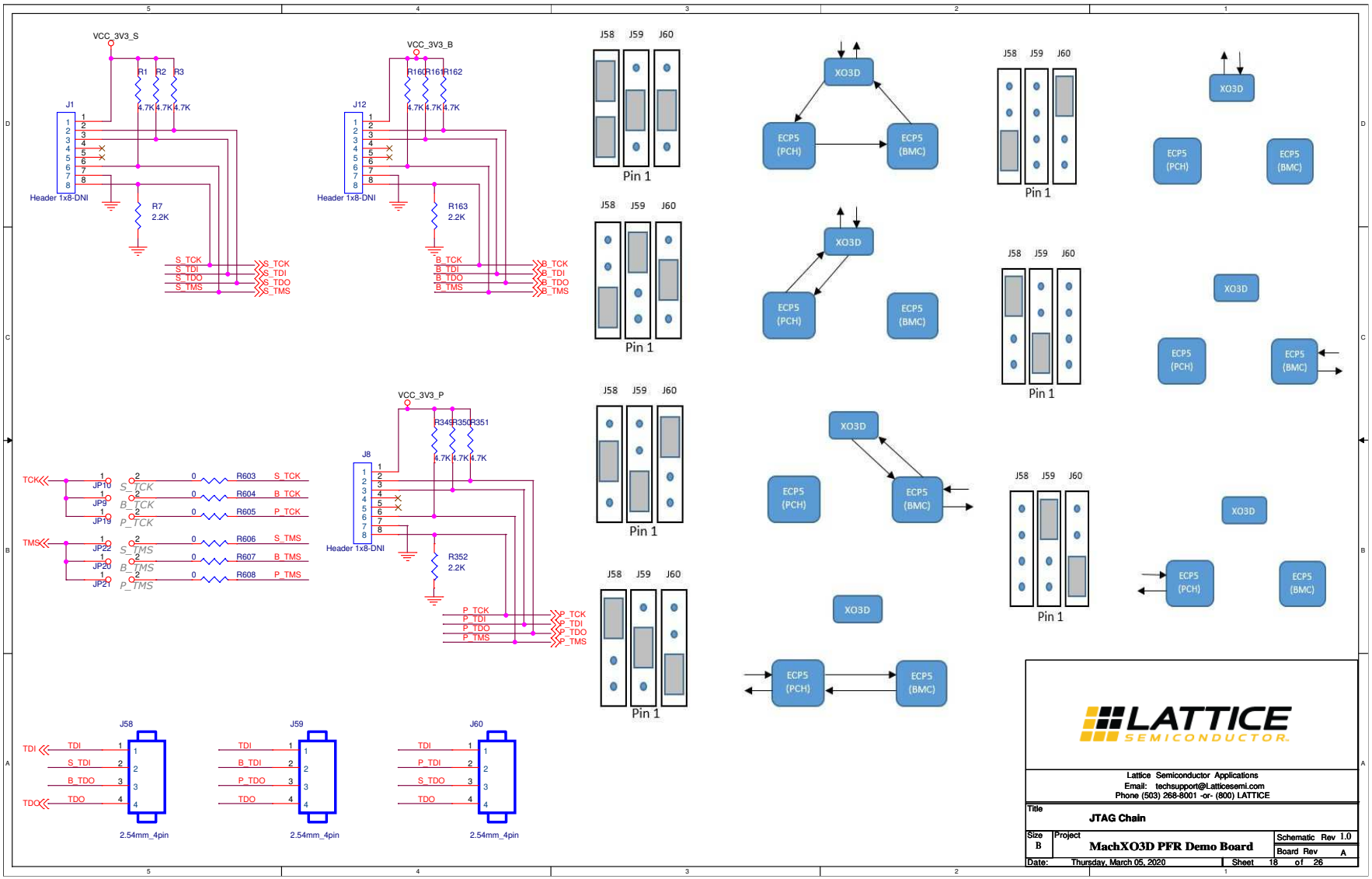
16 – ECP5(BMC) GND



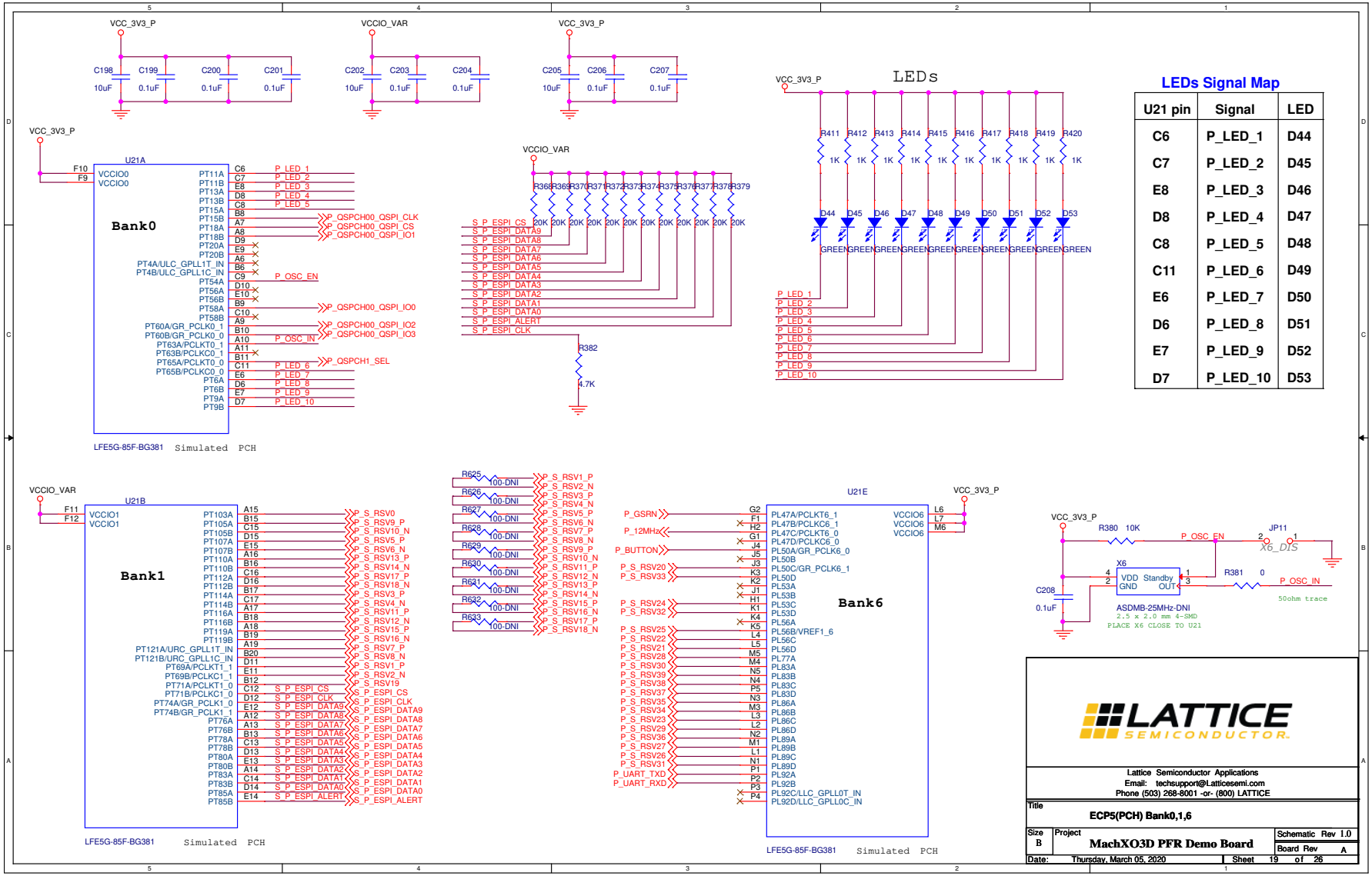
17 – ECP5(BMC) Flash



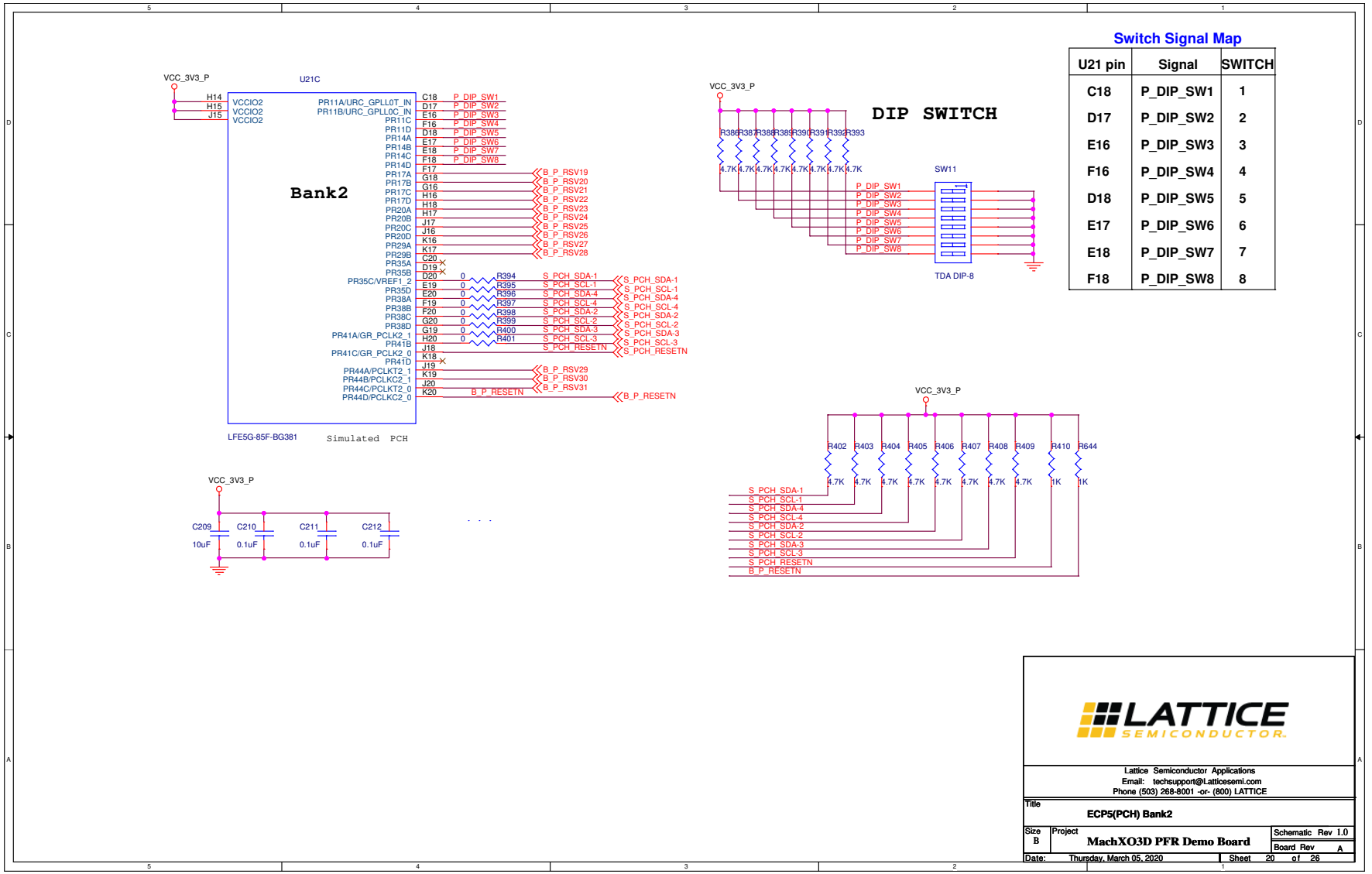
18 – JTAG Chain



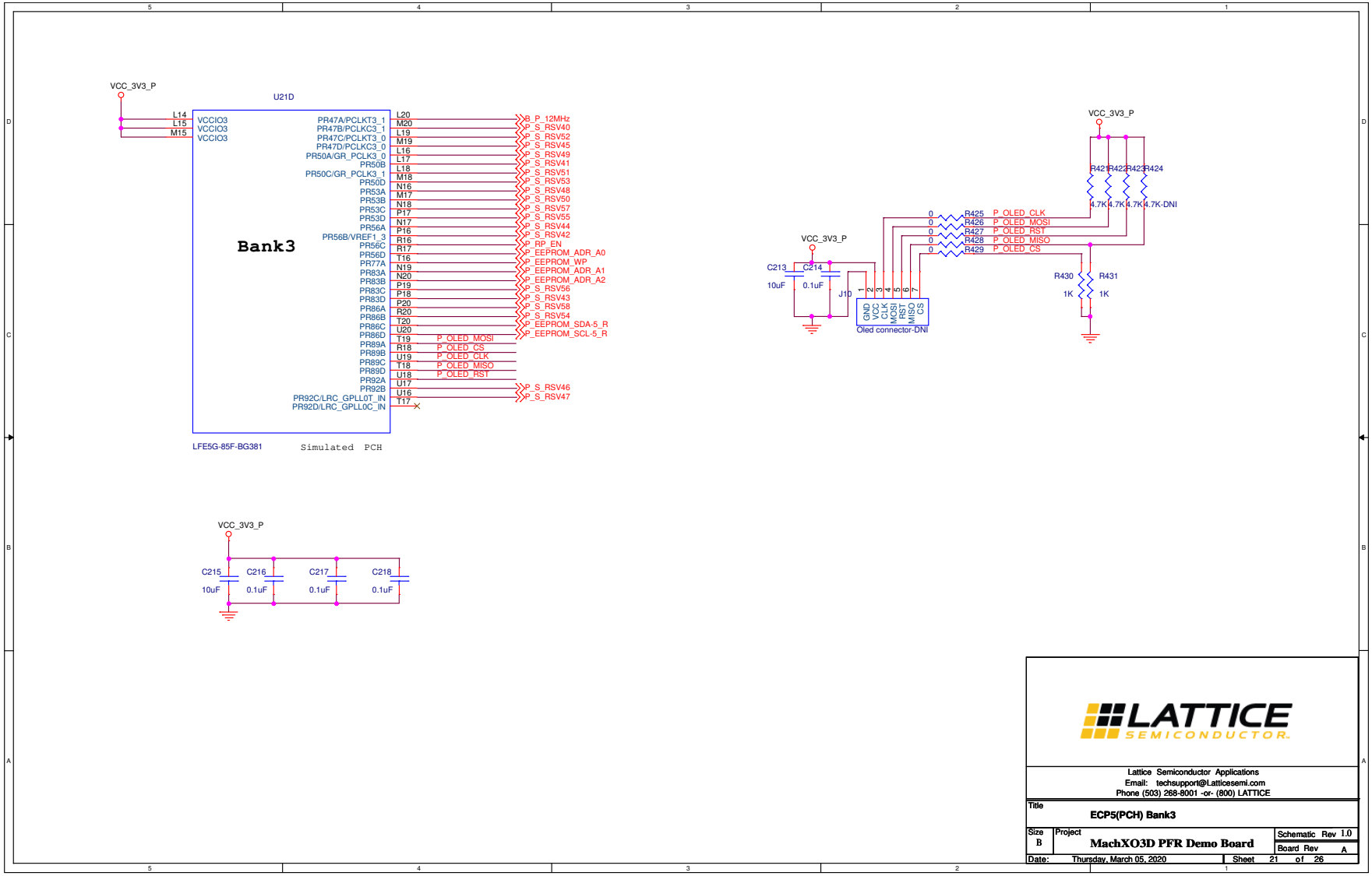
19 – ECP5 (PCH) Bank0,1,6



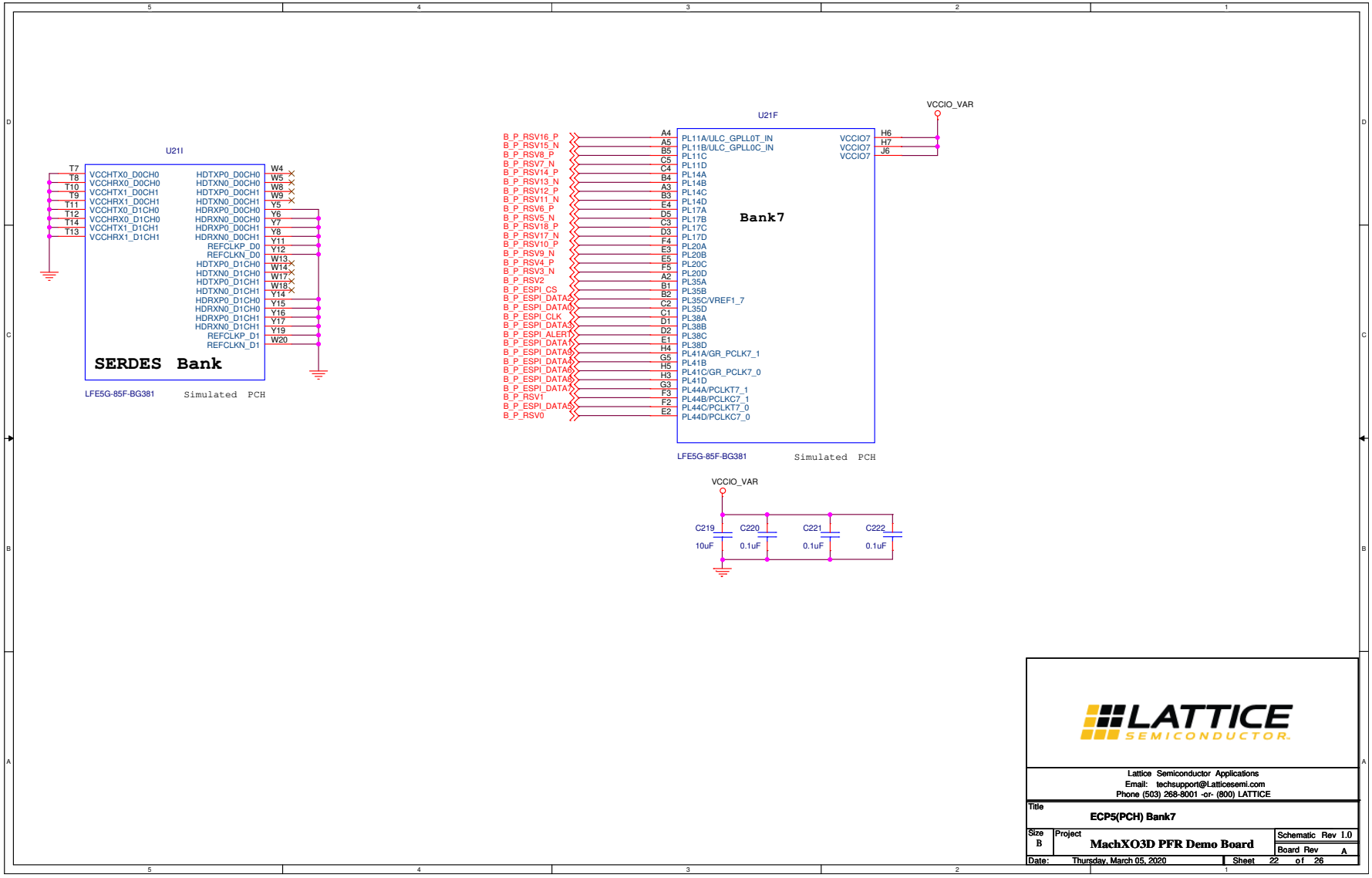
20 – ECP5 (PCH) Bank2



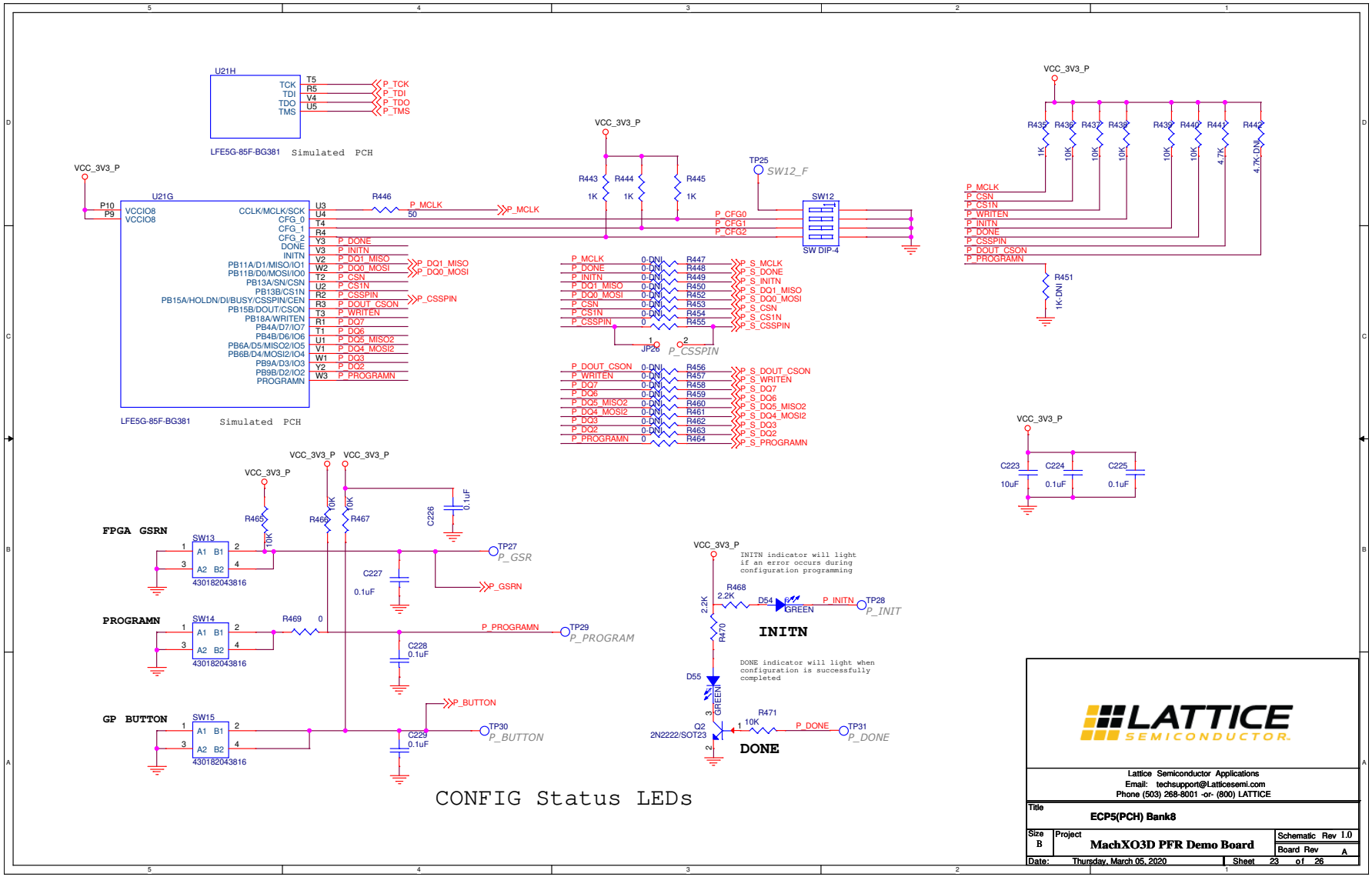
21 – ECP5 (PCH) Bank3



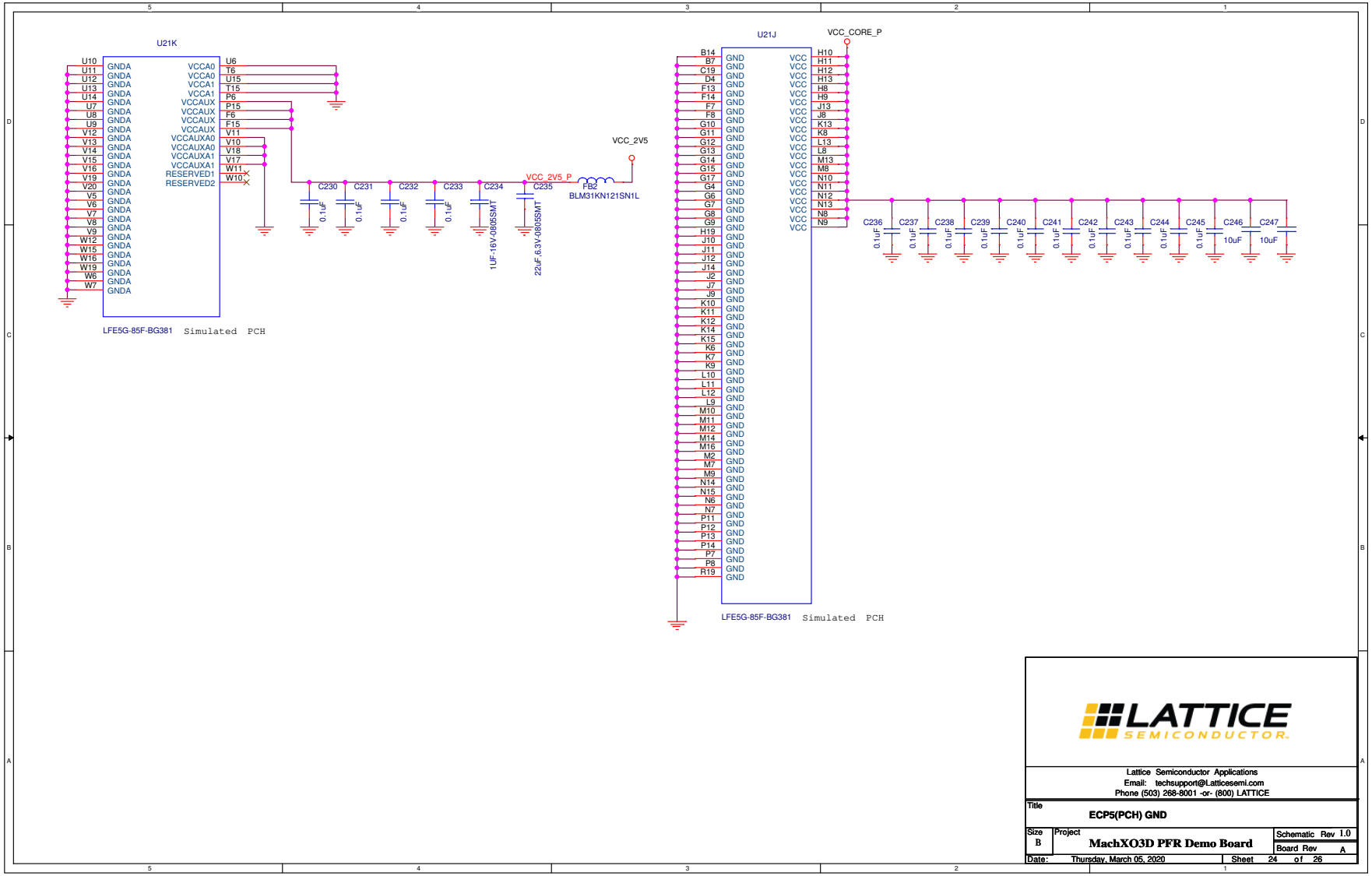
22 – ECP5 (PCH) Bank7



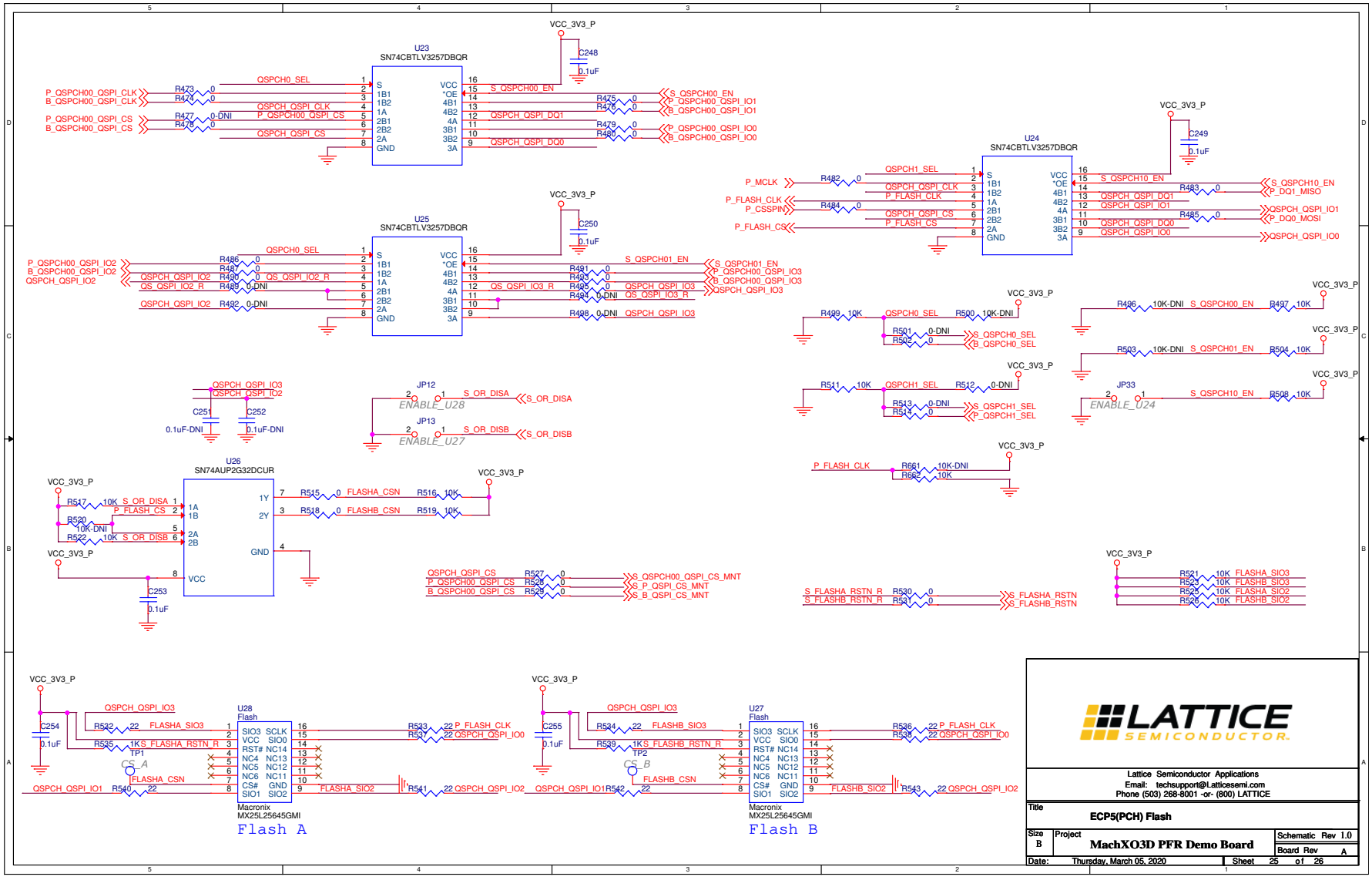
23 – ECP5 (PCH) Bank8



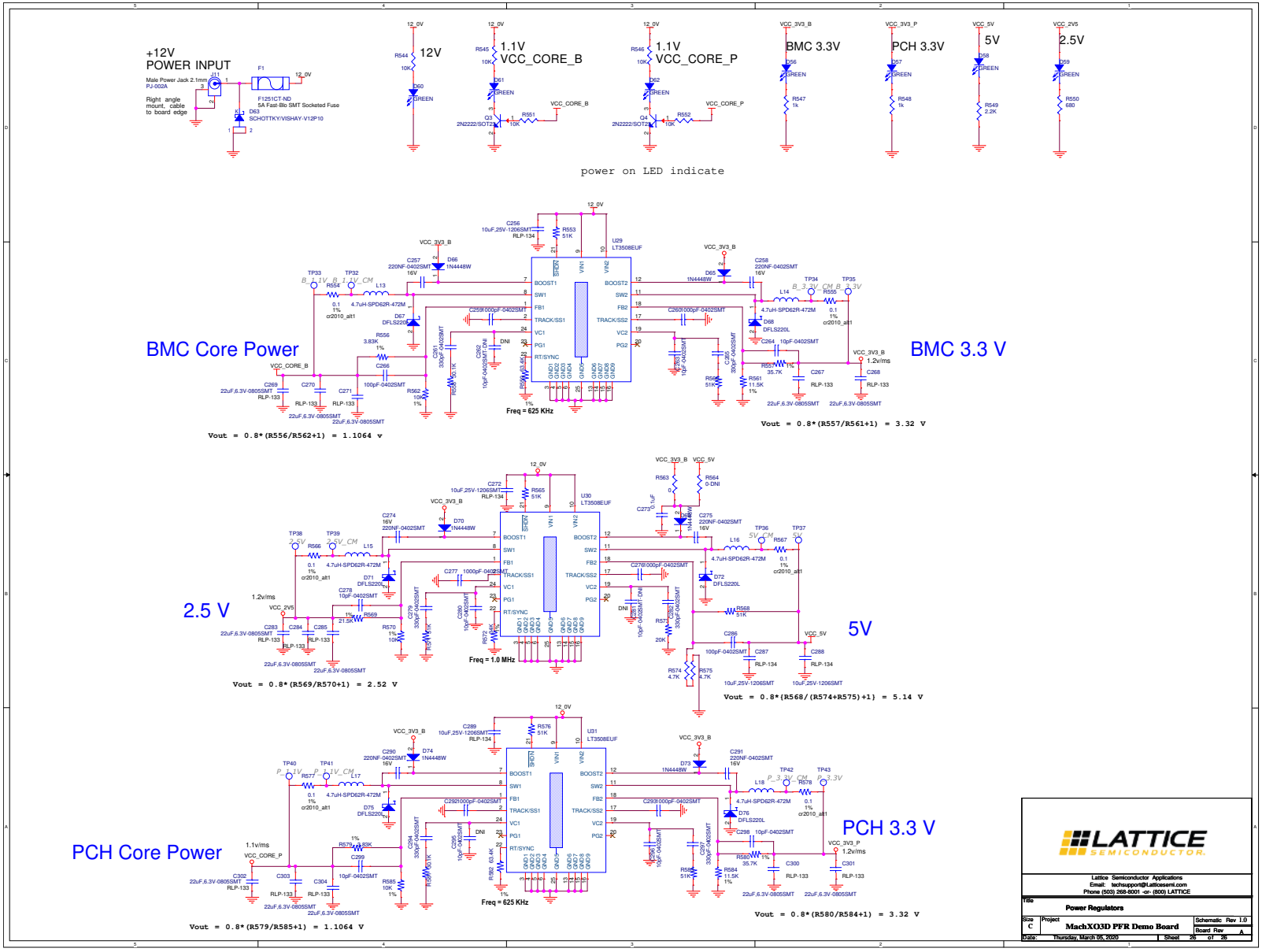
24 – ECP5 (PCH) GND



25 – ECP5 (PCH) Flash



26 – Power Regulators



Appendix B. Bill of Materials

Item	Qty	Reference	Part	PCB Footprint	Comment	Part Number	Manufacturer	Description
1	65	C1,C2,C3,C4,C6,C7,C9,C10,C13, C16,C22,C23,C24,C25,C26,C29, C93,C96,C97,C99,C101,C103, C105,C106,C107,C108,C111, C112,C114,C115,C116,C117, C120,C123,C124,C125,C129, C132,C144,C145,C146,C170, C171,C173,C176,C177,C178, C179,C208,C226,C227,C228, C229,C230,C231,C233,C248, C249,C250,C253,C254,C255, C273,C305,C306	0.1 µF	C0402	—	CL05B104KA5NNNC	Samsung	CAP CER 0.1 µF 25V 10% X7R 0402
2	4	C5,C8,C110,C113	4.7 µF	C0603	—	CL10A475KA8NQNC	Samsung	CAP CER 4.7 µF 6.3V 10% X5R 0603
3	3	C11,C30,C118	0.01 µF	C0402	—	CL05B103KA5NNNC	Samsung	CAP CER 10000PF 16V 5% X7R 0402
4	38	C12,C17,C27,C31,C42,C53,C64, C69,C83,C88,C94,C95,C98,C100, C102,C104,C109,C119,C126, C130,C133,C136,C140,C147, C151,C155,C167,C168,C198, C202,C205,C209,C213,C215, C219,C223,C246,C247	10 µF	C0603	—	LMK107BJ106MALTD	Taiyo Yuden	CAP CER 10 µF 10V X5R 20% 0603
5	4	C14,C15,C121,C122	18 pF	C0402	—	CL05C180JA5NNNC	Samsung	CAP CER 18PF 25V 10% NP0 0402
6	74	C18,C19,C32,C36,C43,C47,C54, C58,C65,C70,C74,C79,C84,C89, C127,C128,C131,C134,C135, C137,C138,C139,C141,C142, C143,C148,C149,C150,C152, C153,C154,C156,C157,C158, C159,C160,C161,C162,C163, C164,C165,C166,C169,C172, C199,C200,C201,C203,C204, C206,C207,C210,C211,C212, C214,C216,C217,C218,C220, C221,C222,C224,C225,C232, C236,C237,C238,C239,C240, C241,C242,C243,C244,C245	0.1 µF	C0201	—	C0603X5R1C104K030BC	TDK	CAP CER 0.1 µF 16V 10% X5R 0201
7	2	C20,C21	150 pF	C0402	DNI	—	—	CAP CER 150PF 16V 5% X7R 0402
8	3	C28,C174,C234	1 µF	RLP-133	—	CL21B105KOFNNNG	Samsung	CAP CER 1 µF 16V X7R 0805
9	43	C33,C34,C35,C37,C38,C39,C40, C41,C44,C45,C46,C48,C49,C50, C51,C52,C55,C56,C57,C59,C60, C61,C62,C63,C66,C67,C68,C71, C72,C73,C75,C76,C77,C78,C80, C81,C82,C85,C86,C87,C90,C91, C92	0.01 µF	C0201	—	CL03A103KA3NNNC	Samsung	CAP CER 10000PF 16V 10% X7R 0201
10	15	C175,C235,C267,C268,C269, C270,C271,C283,C284,C285, C300,C301,C302,C303,C304	22 µF	RLP-133	—	CL21A226MQQNNNE	Samsung	CAP CER 22 µF 6.3V X5R 0805

Item	Qty	Reference	Part	PCB Footprint	Comment	Part Number	Manufacturer	Description
11	2	C251,C252	0.1 µF	C0402	DNI	—	—	CAP CER 0.1 µF 25V 10% X7R 0402
12	5	C256,C272,C287,C288,C289	10 µF	RLP-134	—	TMK316 B7106KL -TD	Taiyo Yuden	CAP CER 10 µF 25V X7R 1206
13	6	C257,C258,C274,C275,C290, C291	220 nF	RLP-130-A	—	CL05A22 4KO5NN NC	Samsung	CAP CER 0.22 µF 16V X5R 0402
14	6	C259,C260,C276,C277,C292, C293	1000 pF	RLP-130-A	—	CL05B10 2KB5NF NC	Samsung	CAP CER 1000PF 50V X7R 0402
15	6	C261,C265,C279,C282,C294, C297	330 pF	RLP-130-A	—	CL05B33 1KB5NN NC	Samsung	CAP CER 330PF 50V X7R 0402
16	2	C262,C281	10 pf	RLP-130-A	DNI	—	—	—
17	8	C263,C264,C278,C280,C295, C296,C298,C299	10 pF	RLP-130-A	—	CL05C10 0CB5NN NC	Samsung	CAP CER 10PF 50V C0G/NP0 0402
18	2	C266,C286	100 pF	RLP-130-A	—	CL05C10 1JB51PN C	Samsung	CAP CER 100PF 50V C0G/NP0 0402
19	58	D1,D3,D4,D5,D6,D7,D8,D9,D10, D11,D12,D14,D15,D16,D17,D18, D19,D20,D21,D22,D23,D25,D26, D27,D28,D30,D31,D32,D33,D34, D35,D36,D37,D38,D39,D40,D41, D44,D45,D46,D47,D48,D49,D50, D51,D52,D53,D54,D55,D56,D57, D58,D59,D60,D61,D62,D77,D78	GREEN	APT1608	—	APT1608 SGC	Kingbright	LED GREEN CLEAR 0603 SMD
20	2	D2,D29	ESDR0502N	UDFN6_0 40	—	ESDR050 2NMUTB G	ON semi	TVS DIODE 5.5VWM 6UDFN
21	2	D13,D24	7-SEGMENT	LED10-057-394-XZFBBA05A	—	XZFBBA0 5A	SunLED	DISPLAY LED 0.2" BLUE CA SMD
22	1	D63	SCHOTTKY/VISHAY-V12P10	V12P10	—	V12P10-M3/86A	Vishay	DIODE SCHOTTKY 100V 12A TO277A
23	6	D65,D66,D69,D70,D73,D74	1N4448W	1N4448W	—	1N4448 WS	On Semi	DIODE GEN PURP 75V 150MA SOD323F
24	6	D67,D68,D71,D72,D75,D76	DFLS220L	DFLS220L	—	DFLS220 L-7	Diodes Incorporated	DIODE SCHOTTKY 20V 2A POWERDI123
25	2	FB1,FB2	BLM31KN121S N1L	BLM41P	—	BLM41P G600SN 1L	Murata	FERRITE BEAD 60 OHM 1806 1LN
26	1	F1	F1251CT-ND	154010	—	0154010 .DR	Littelfuse	FUSE BRD MNT 10A 125VAC/VDC SMD

Item	Qty	Reference	Part	PCB Footprint	Comment	Part Number	Manufacturer	Description
27	35	JP1,JP2,JP3,JP4,JP6,JP7,JP8,JP9, JP10,JP11,JP12,JP13,JP14,JP15, JP16,JP17,JP18,JP19,JP20,JP21, JP22,JP23,JP24,JP25,JP26,JP27, JP29,JP30,JP31,JP32,JP33,JP34, JP35,JP36,JP37	JUMPER	Header_1 x2	—	Regular 100Mil Header	—	—
28	3	J1,J8,J12	Header 1x8	hdr_amp_ 87220_8_ 1x8_100	DNI	—	—	—
29	2	J2,J6	USB_MINI_B	usb2-0-rec-240-0001-9	—	UX60-MB-5ST	Hirose	CONN RECEPT MINI USB2.0 5POS
30	1	J3	BATTERY HOLDER	CR2032	—	BU2032SM-FH-GTR	MPD	CR2032 BATTERY HOLDER SURFACE MOUNT
31	2	J4,J5	GND	TUR_TH	GND Through hole	—	—	—
32	2	J7,J10	OLED connector	2P54X7	DNI	—	—	—
33	1	J11	PJ-002A	pj_002a_3 p	—	PJ-002A	CUI Inc.	CONN PWR JACK 2X5.5MM SOLDER
34	1	J13	HEADER 5X2	HDR254-2X5_SHR OUDED	—	30310-6002HB	3M	CONN HEADER 10POS DL STR GOLD
35	3	J58,J59,J60	2.54mm_4pin	HDR100-4X1	—	Regular 100Mil Header	—	—
36	1	J61	Receptacle 20X2	HDR254-2X20_soc ket	—	PPTC202 LFBN-RC	Sullins	CONN HEADER FEM 40POS .1" DL TIN
37	9	L1,L2,L3,L4,L5,L6,L7,L8,L9	600ohm 500mA	fb0603	—	BLM18A G601SN 1D	Murata	FERRITE CHIP 600 OHM 500MA 0603
38	6	L13,L14,L15,L16,L17,L18	4.7µH-SPD62R-472M	SPD62R	—	SPD62R-472M	API Delevan Inc.	FIXED IND 4.7 µH 2A 150 MOHM SMD
39	8	MH1,MH2,MH3,MH4,MH5,MH6 ,MH7,MH8	Through Hole	MTG125	—	—	—	—
40	6	Q1,Q2,Q3,Q4,Q5,Q6	2N2222/SOT23	MMBT222 2ALT-1		MMBT2 222ALT1 G	ON Semiconductor	TRANS NPN 40V 0.6A SOT23
41	78	R1,R2,R3,R30,R31,R49,R50,R51, R52,R61,R62,R74,R75,R76,R77, R78,R79,R80,R81,R139,R140, R141,R142,R147,R153,R158, R160,R161,R162,R180,R181, R182,R183,R184,R185,R186, R187,R201,R202,R203,R204, R206,R208,R210,R232,R233, R234,R235,R250,R251,R278, R349,R350,R351,R382,R386, R387,R388,R389,R390,R391, R392,R393,R402,R403,R404,	4.7K	RLP-101	—	RC0603FR-074K7L	Yageo	RES SMD 4.7K OHM 1/10W 1% 0603

Item	Qty	Reference	Part	PCB Footprint	Comment	Part Number	Manufacturer	Description
		R405,R406,R407,R408,R409, R421,R422,R423,R441,R574, R575,R586						
42	19	R4,R7,R10,R29,R53,R54,R146, R159,R163,R169,R308,R309, R352,R468,R470,R549,R587, R657,R658	2.2K	RLP-101	—	RC0603FR-072K2L	Yageo	RES SMD 2.2K OHM 1% 1/10W 0603
43	2	R11,R168	100K	RLP-101	—	RC0603FR-07100KL	Yageo	RES SMD 100K OHM 1% 1/10W 0603
44	3	R12,R173,R178	12K	RLP-101	—	RC0603FR-0712KL	Yageo	RES SMD 12K OHM 1/10W 1% 0603
45	4	R13,R14,R213,R424	4.7K	RLP-101	DNI	—	—	RES SMD 4.7K OHM 1/10W 1% 0603
46	135	R15,R16,R36,R39,R40,R41,R43, R44,R48,R55,R56,R59,R60,R84, R94,R95,R111,R112,R113,R114, R128,R129,R130,R131,R132, R133,R134,R135,R143,R145, R148,R154,R176,R177,R200, R205,R207,R209,R212,R214, R216,R222,R223,R227,R229, R230,R231,R236,R237,R238, R239,R256,R257,R290,R299, R312,R313,R314,R316,R318, R319,R320,R322,R330,R331, R332,R334,R335,R381,R394, R395,R396,R397,R398,R399, R400,R401,R425,R426,R427, R428,R429,R455,R464,R469, R473,R474,R475,R476,R478, R479,R480,R482,R483,R484, R485,R486,R487,R490,R491, R493,R495,R502,R514,R515, R518,R527,R528,R529,R530, R531,R563,R588,R589,R597, R598,R599,R600,R601,R603, R604,R605,R606,R607,R608, R613,R614,R615,R616,R637, R638,R639,R654,R655,R659	0	RLP-101	—	RC0603FR-070RL	Yageo	RES SMD 0 OHM JUMPER 1/10W 0603
47	96	R17,R18,R19,R23,R24,R25,R26, R27,R28,R32,R33,R42,R45,R46, R57,R58,R92,R93,R106,R107, R115,R116,R118,R119,R144, R149,R150,R151,R155,R156, R240,R241,R242,R243,R244, R245,R246,R247,R248,R249, R252,R253,R254,R283,R284, R285,R286,R287,R288,R289, R291,R292,R293,R294,R295, R296,R297,R298,R329,R447, R448,R449,R450,R452,R453, R454,R456,R457,R458,R459,	0	RLP-101	DNI	—	—	RES SMD 0 OHM JUMPER 1/10W 0603

Item	Qty	Reference	Part	PCB Footprint	Comment	Part Number	Manufacturer	Description
		R460,R461,R462,R463,R477, R489,R492,R494,R496,R498, R500,R501,R503,R512,R513, R564,R640,R641,R646,R647, R648,R649,R650,R651,R652, R653						
48	66	R20,R21,R22,R35,R37,R38,R47, R82,R108,R109,R170,R171, R172,R179,R188,R189,R211, R260,R301,R302,R303,R304, R305,R311,R315,R317,R321, R324,R326,R327,R336,R341, R342,R347,R380,R436,R437, R438,R439,R440,R465,R466, R467,R471,R497,R499,R504, R508,R511,R516,R517,R519, R521,R522,R523,R525,R526, R551,R552,R562,R570,R585, R592,R656,R660,R662	10K	RLP-101	—	RC0603FR-0710KL	Yageo	RES SMD 10K OHM 1% 1/10W 0603
49	68	R64,R65,R66,R67,R68,R69,R70, R71,R72,R73,R96,R97,R98,R99, R100,R101,R102,R103,R104, R105,R117,R152,R190,R191, R192,R193,R194,R195,R196, R197,R198,R199,R215,R217, R279,R280,R281,R300,R339, R345,R410,R411,R412,R413, R414,R415,R416,R417,R418, R419,R420,R430,R431,R435, R443,R444,R445,R535,R539, R547,R548,R594,R634,R635, R636,R642,R644,R645	1K	RLP-101	—	RC0603FR-071KL	Yageo	RES SMD 1K OHM 1/10W 1% 0603
50	34	R83,R85,R86,R87,R88,R89,R90, R91,R120,R121,R122,R123, R124,R125,R126,R127,R337, R338,R340,R343,R344,R346, R532,R533,R534,R536,R537, R538,R540,R541,R542,R543, R664,R665	22	RLP-101	—	RC0603FR-0722RL	Yageo	RES SMD 22 OHM 1% 1/10W 0603
51	7	R110,R323,R328,R520,R593, R661,R663	10K	RLP-101	DNI	—	—	RES SMD 10K OHM 1% 1/10W 0603
52	5	R174,R175,R261,R611,R612	2.2K	RLP-101	DNI	—	—	RES SMD 2.2K OHM 1% 1/10W 0603
53	4	R218,R219,R220,R221	1K	RLP-101	DNI	—	—	RES SMD 1K OHM 1% 1/10W 0603
54	4	R224,R225,R226,R228	0	RLP-100	DNI	—	—	RES SMD 0 OHM 1% 1/16W 0402
55	25	R266,R267,R268,R269,R270, R271,R272,R273,R274,R275, R276,R277,R368,R369,R370, R371,R372,R373,R374,R375, R376,R377,R378,R379,R573	20K	RLP-100	—	ERJ-2RKF2002X	Panasonic	RES SMD 20K OHM 1% 1/16W 0402
56	2	R282,R446	50	RLP-101	—	RC0603FR-0749R9L	Yageo	RES SMD 49.9 OHM 1% 1/10W 0603
57	3	R544,R545,R546	10K	RLP-103	—	RC1206J	Yageo	RES SMD

Item	Qty	Reference	Part	PCB Footprint	Comment	Part Number	Manufacturer	Description
						R-0710KL		10K OHM 5% 1/4W 1206
58	1	R550	680	RLP-101	—	ERJ-3EKF6800V	Panasonic	RES SMD 680 OHM 1% 1/10W 0603
59	7	R553,R560,R565,R568,R571, R576,R583	51K	RLP-100	—	RC0402FR-0751KL	Yageo	RES SMD 51K OHM 1% 1/16W 0402
60	6	R554,R555,R566,R567,R577, R578	0.1	cr2010_alt1	—	WSL2010R1000FEA	Vishay Dale	RES 0.1 OHM 1% 1/2W 2010
61	3	R306,R556,R579	3.83K	RLP-101	—	ERJ-3EKF3831V	Panasonic	RES SMD 3.83K OHM 1/10W 1% 0603
62	2	R307,R442	4.7K	RLP-100	DNI	—	—	RES SMD 4.7K OHM 1% 1/16W 0402
63	2	R310,R451	1K	RLP-100	DNI	—	—	RES SMD 1K OHM 1% 1/16W 0402
64	2	R557,R580	35.7K	RLP-101	—	RC0603FR-0735K7L	Yageo	RES SMD 35.7K OHM 1% 1/10W 0603
65	2	R558,R581	30.1K	RLP-100	—	ERJ-2RKF3012X	Panasonic	RES SMD 30.1K OHM 1% 1/16W 0402
66	2	R559,R582	63.4K	RLP-100	—	ERJ-2RKF6342X	Panasonic	RES SMD 63.4K OHM 1% 1/10W 0402
67	2	R561,R584	11.5K	RLP-101	—	RC0603FR-0711K5L	Yageo	RES SMD 11.5K OHM 1% 1/10W 0603
68	1	R569	21.5K	RLP-101	—	RC0603FR-0721K5L	Yageo	RES SMD 21.5K OHM 1% 1/10W 0603
69	1	R572	34K	RLP-100	—	RC0402FR-0734KL	Yageo	RES SMD 34K OHM 1% 1/16W 0402
70	17	R617,R618,R619,R620,R621, R622,R623,R624,R625,R626, R627,R628,R629,R630,R631, R632,R633	100	RLP-100	DNI	—	—	RES SMD 100 OHM 1% 1/16W 0402
71	3	SW1,SW7,SW11	TDA DIP-8	TDA08H0SB1	—	TDA08H0SB1	C&K Components	SWITCH SLIDE DIP SPST 25MA 24V
72	10	SW2,SW3,SW4,SW5,SW6,SW8, SW9,SW13,SW14,SW15	430182043816	430182043816	—	PTS645SM43SMTR92 LFS	C&K Components	SWITCH TACTILE SPST-NO 0.05A 12V
73	2	SW10,SW12	SW DIP-4	41812127 0804	—	4181212 70804	Wurth	SWITCH SLIDE DIP SPST 25MA 24V

Item	Qty	Reference	Part	PCB Footprint	Comment	Part Number	Manufacturer	Description
74	21	TP1,TP2,TP3,TP5,TP7,TP8,TP15, TP16,TP17,TP19,TP20,TP21, TP22,TP25,TP27,TP28,TP29, TP30,TP31,TP47,TP48	TestPoint_SMT	TPC32	Test Point	—	—	—
75	22	TP4,TP9,TP10,TP11,TP12,TP13, TP14,TP32,TP33,TP34,TP35, TP36,TP37,TP38,TP39,TP40, TP41,TP42,TP43,TP44,TP45, TP46	TestPoint_Hole	TP	Test Point	—	—	—
76	2	U1,U9	FT2232HL	tqfp64_0p5_12p2x12p2_h1p6	—	FT2232HL-REEL	FTDI	IC USB HS DUAL UART/FIFO 64-LQFP
77	2	U2,U10	93LC56C-I/SN	so8_50_244	—	93LC56C-I/SN	Microchip Technology	IC EEPROM 2KBIT 3MHZ 8SOIC
78	1	U3	R2025S	SOP14	—	R2025S-E2-FE	RICOH	IC High precision I2C-Bus Real-Time Clock Module SOP14
79	1	U4	XO3D_9400HC_484CABGA	BGA484-080	—	LCMXO3D-9400HC-*BG484*	Lattice	XO3D-HC9400 CPLD device
80	1	U5	SBR0330CW	SOT323	—	SBR0330CW-7	Diodes Incorporated	0.3A SBR SUPER BARRIER RECTIFIER
81	1	U6	RP132H331D	SOT89-5	—	RP132H331D-T1-FE	RICOH	IC 1A LDO Regulator 3.3V OUTPUT SOT-89-5
82	1	U7	RP132H251D	SOT89-5	—	RP132H251D-T1-FE	RICOH	IC 1A LDO Regulator 2.5V OUTPUT SOT-89-5
83	1	U8	RP132H181D	SOT89-5	—	RP132H181D-T1-FE	RICOH	IC 1A LDO Regulator 1.8V OUTPUT SOT-89-5
84	2	U11,U21	LFE5G-85F-BG381	LFE5G-85F-BG381	—	LFE5U-85F-8BG381C	Lattice	83.6K LUTS, 205 I/O, 1.1V, -8 SPE
85	1	U13	PCA9617ADPJ	TSSOP8	—	PCA9617ADPJ	NXP	IC I2C-bus repeater 2 channel Level translating
86	4	U15,U23,U24,U25	Multiplexer	SSOP16-25-150	—	SN74CBTLV3257DBQR	TI	IC LV DUAL FET MUX/DEMUX 16SSOP
87	2	U16,U26	OR-Gate	VSSOP_8	—	SN74AUP2G32DCUR	TI	IC GATE OR 2CH 2-INP US8

Item	Qty	Reference	Part	PCB Footprint	Comment	Part Number	Manufacturer	Description
88	4	U17,U18,U27,U28	Flash	16_pin_300milsoic	—	MX25L25645GMI-08G	Macronix	IC FLASH 256MBIT 104MHZ 16SOP
89	3	U29,U30,U31	LT3508EUF	LT3508EUF	—	LT3508EUF#PBF	Linear Technology/Analog Devices	IC REG BUCK ADJ 1.4A DL 24QFN
90	1	U32	24LC512T-I/SM	SOIJ	—	24LC512T-I/SM	Microchip	IC I2C Serial EEPROM 512 Kbit SOIJ Package
91	2	X1,X3	7M-12.000MAAJ	xtal_4p_7m	—	7M-12.000MAAJ-T	TXC	CRYSTAL 12MHZ 18PF SMD
92	1	X2	ASDMB-25MHz	x4-2520	—	ASDMB-25.000MHZ-XY-T	Abracon LLC	OSC MEMS 27.000MHZ CMOS SMD 10ppm
93	2	X4,X6	ASDMB-25MHz	x4-2520	DNI	ASDMB-25.000MHZ-XY-T	Abracon LLC	OSC MEMS 27.000MHZ CMOS SMD 10ppm
94	1	MachXO3D PFR Demo Board PCB	–	–	–	305-PD-20-0070	Pactron	–

References

- MachXO3D Device Family Data Sheet (FPGA-DS-02026)
- ECP5 and ECP-5G Family Data Sheet (FPGA-DS-02012)
- MachXO3D Programming and Configuration Usage Guide (FPGA-TN-02069)
- ECP5 and ECP5-5G sysCONFIG Usage Guide (FPGA-TN-02039)
- MachXO3D Root of Trust Platform Firmware Resiliency Demonstration Design User Guide (FPGA-UG-02099)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.1, August 2020

Section	Change Summary
All	Changed the document title to Lattice Sentry Demo Board for MachXO3D User Guide.

Revision 1.0, March 2020

Section	Change Summary
All	Initial release.

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