DAC-08 SERIES

8-Bit High-Speed Multiplying D/A Converter

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 70 ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 20-to-1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All DAC-08 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range. Device performance is essentially unchanged over the ±4.5 V to ±18 V power supply range, with 37 mW power consumption attainable at ±5.0 V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military aerospace applications.

Features

- Fast Settling Output Current − 70 ns
- Full-Scale Current Prematched to ±1.0 LSB
- Direct Interface to TTL, CMOS, ECL, HTL, PMOS
- Relative Accuracy to 0.1% Maximum Overtemperature Range
- High Output Compliance −10 V to +18 V
- True and Complemented Outputs
- Wide Range Multiplying Capability
- Low FS Current Drift − ±10ppm/°C
- Wide Power Supply Range − ±4.5 V to ±18 V
- Low Power Consumption − 37 mW at ±5.0 V
- Pb−Free Packages are Available*

Applications

- 8-Bit, 1.0 µs A-to-D Converters
- Servo-Motor and Pen Drivers
- Waveform Generators
- Audio Encoders and Attenuators
- Analog Meter Drivers
- Programmable Power Supplies
- CRT Display Drivers
- High-Speed Modems
- Other Applications where Low Cost, High Speed and Complete Input/Output Versatility are Required
- Programmable Gain and Attenuation
- Analog-Digital Multiplication

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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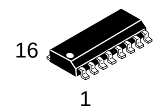
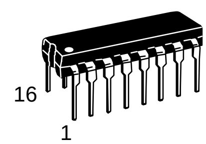


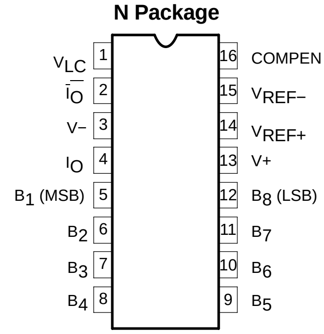
SOIC−16
D SUFFIX
CASE 751B



PDIP−16
N SUFFIX
CASE 648

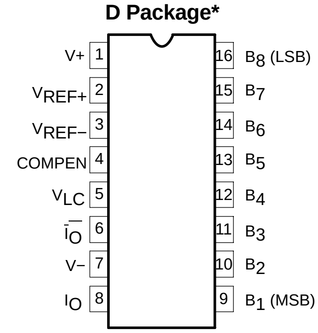
PIN CONNECTIONS

N Package



(Top View)

D Package*



(Top View)

*SO and non−standard pinouts.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 13 of this data sheet.

Publication Order Number:
DAC−08/D

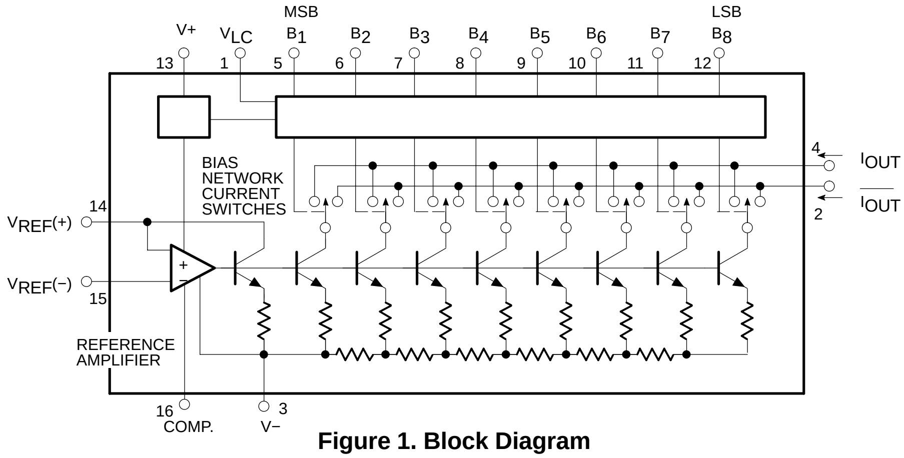


Figure 1. Block Diagram

PIN FUNCTION DESCRIPTION

Pin # N Package / D Package	Symbol	Description
1/5	V_{LC}	Logic Control Voltage
2/6	$\overline{I_O}$	Inverted Output Current
3/7	V−	Negative Power Supply
4/8	I_O	Non−Inverted Output Current
5/9	B_1	Output 1, Most Significant Bit (MSB)
6/10	B_2	Output 2
7/11	B_3	Output 3
8/12	B_4	Output 4
9/13	B_5	Output 5
10/14	B_6	Output 6
11/15	B_7	Output 7
12/16	B_8	Output 8, Least Significant Bit (LSB)
13/1	V+	Positive Power Supply
14/2	V_{REF+}	Positive Reference Voltage
15/3	V_{REF-}	Negative Reference Voltage
16/4	COMPEN	Compensator Capacitor Pin

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V+ to V−	36	V
Digital Input Voltage	V_5−V_{12}	V− to V− plus 36 V	−
Logic Threshold Control	V_{LC}	V− to V+	−
Applied Output Voltage	V_0	V− to +18	V
Reference Current	I_{14}	5.0	mA
Reference Amplifier Inputs	V_{14}, V_{15}	V_{EE} to V_{CC}	−
Maximum Power Dissipation T_{amb} = 25°C (Still-Air) (Note 1) N Package D Package	P_D	 1450 1090	mW
Thermal Resistance, Junction−to−Ambient N Package D Package	$R_{\theta JA}$	 75 105	°C/W
Lead Soldering Temperature (10 sec max)	T_{SOLD}	230	°C
Operating Temperature Range	T_{amb}	0 to +70	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Derate above 25°C, at the following rates: N package at 13.3 mW/°C
D package at 9.5 mW/°C.

DC ELECTRICAL CHARACTERISTICS Pin 3 must be at least 3.0 V more negative than the potential to which R_{15} is returned. V_{CC} = ±15 V , I_{REF} = 2.0 mA. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$ unless otherwise noted. T_{amb} = 0°C to 70°C.

Characteristic	Symbol	Test Conditions	DAC−08C			DAC−08E			Unit
			Min	Typ	Max	Min	Typ	Max	
Resolution	−	−	8.0	8.0	8.0	8.0	8.0	8.0	Bits
Monotonicity			8.0	8.0	8.0	8.0	8.0	8.0	
Relative Accuracy	−	Overtemperature Range	−	−	±0.39	−	−	±0.19	%FS
Differential Non-Linearity			−	−	±0.78	−	−	±0.39	
Full-Scale Tempco	TCI_{FS}	−	−	±10	−	−	±10	−	ppm/°C
Output Voltage Compliance	V_{OC}	Full-Scale Current Change < 1/2LSB	−10	−	+18	−10	−	+18	V
Full-Scale Current	I_{FS4}	V_{REF} = 10.000 V; R_{14}, R_{15} = 5.000 kΩ	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full-Scale Symmetry	I_{FSS}	I_{FS4}-I_{FS2}	−	±2.0	±16	−	±1.0	±8.0	μA
Zero-Scale Current	I_{ZS}	−	−	0.2	4.0	−	0.2	2.0	μA
Full-Scale Output Current Range	I_{FSR}	R_{14}, R_{15} = 5.000 kΩ							
		V_{REF} = +15 V, V− = −10 V	2.1	−	−	2.1	−	−	mA
		V_{REF} = +25 V, V− = −12 V	4.2	−	−	4.2	−	−	mA
Logic Input Levels		V_{LC} = 0 V							V
Low	V_{IL}		−	−	0.8	−	−	0.8	
High	V_{IH}		2.0	−	−	2.0	−	−	
Logic Input Current		V_{LC} = 0 V							μA
Low	I_{IL}	V_{IN} = −10 V to +0.8 V	−	−2.0	−10	−	−2.0	−10	
High	I_{IH}	V_{IN} = 2.0 V to 18 V	−	0.002	10	−	0.002	10	
Logic Input Swing	V_{IS}	V− = −15 V	−10	−	+18	−10	−	+18	V
Logic Threshold Range	V_{THR}	V_S = ±15 V	−10	−	+13.5	−10	−	+13.5	V
Reference Bias Current	I_{15}	−	−	−1.0	−3.0	−	−1.0	−3.0	μA
Reference Input Slew Rate	dI/dt	−	4.0	8.0	−	4.0	8.0	−	mA/μs
Power Supply Sensitivity		I_{REF} = 1.0 mA							
Positive	$PSSI_{FS+}$	V+ = 4.5 to 5.5 V, V− = −15 V; V+ = 13.5 to 16.5 V, V− = −15 V	−	0.0003	0.01	−	0.0003	0.01	%FS/%VS
Negative	$PSSI_{FS-}$	V− = −4.5 to −5.5 V, V+ = +15 V; V− = −13.5 to −16.5 V, V+ = +15 V	−	0.002	0.01	−	0.002	0.01	%FS/%VS
Power Supply Current									mA
Positive	I+	V_S = ±5.0 V, I_{REF} = 1.0 mA	−	3.1	3.8	−	3.1	3.8	
Negative	I−		−	−4.3	−5.8	−	−4.3	−5.8	
Positive	I+	V_S = +5.0 V, −15 V, I_{REF} = 2.0 mA	−	3.1	3.8	−	3.1	3.8	
Negative	I−		−	−7.1	−7.8	−	−7.1	−7.8	
Positive	I+	V_S = ±15 V, I_{REF} = 2.0 mA	−	3.2	3.8	−	3.2	3.8	
Negative	I−		−	−7.2	−7.8	−	−7.2	−7.8	
Power Dissipation	P_D	±5.0 V, I_{REF} = 1.0 mA	−	37	48	−	37	48	mW
		+5.0 V, −15 V, I_{REF} = 2.0 mA	−	122	136	−	122	136	
		±15 V, I_{REF} = 2.0 mA	−	156	174	−	156	174	

DC ELECTRICAL CHARACTERISTICS (continued) Pin 3 must be at least 3.0 V more negative than the potential to which R_{15} is returned. V_{CC} = +15 V , I_{REF} = 2.0 mA. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$ unless otherwise noted. T_{amb} = 0°C to 70°C.

Characteristic	Symbol	Test Conditions	DAC−08H Min	DAC−08H Typ	DAC−08H Max	Unit
Resolution Monotonicity	−	−	8.0 8.0	8.0 8.0	8.0 8.0	Bits
Relative Accuracy Differential Non-Linearity	−	Overtemperature Range	− −	− −	±0.1 ±0.19	%FS %FS
Full-Scale Tempco	TCI_{FS}	−	−	±10	±50	ppm/°C
Output Voltage Compliance	V_{OC}	Full-Scale Current Change 1/2LSB	−10	−	+18	V
Full-Scale Current	I_{FS4}	V_{REF} = 10.000 V, R_{14}, R_{15} = 5.000 kΩ	1.984	1.992	2.000	mA
Full-Scale Symmetry	I_{FSS}	$I_{FS4}−I_{FS2}$	−	±1.0	±4.0	μA
Zero-Scale Current	I_{ZS}	−	−	0.2	1.0	μA
Full-Scale Output Current Range	I_{FSR}	R_{14}, R_{15} = 5.000 kΩ V_{REF} = +15 V, V− = −10 V V_{REF} = +25 V, V−=−12 V	 2.1 4.2	 − −	 − −	 mA mA
Logic Input Levels Low High	 V_{IL} V_{IH}	V_{LC} = 0 V	 − 2.0	 − −	 0.8 −	V
Logic Input Current Low High	 I_{IL} I_{IH}	V_{LC} = 0 V V_{IN} = −10 V to +0.8 V V_{IN} = 2.0 V to 18 V	 − −	 −2.0 0.002	 −10 10	μA
Logic Input Swing	V_{IS}	V− = −15 V	−10	−	+18	V
Logic Threshold Range	V_{THR}	V_S = ±15 V	−10	−	+13.5	V
Reference Bias Current	I_{15}	−	−	−1.0	−3.0	μA
Reference Input Slew Rate	dI/dt	−	4.0	8.0	−	mA/μs
Power Supply Sensitivity Positive Negative	 $PSSI_{FS+}$ $PSSI_{FS−}$	I_{REF} = 1.0 mA V+ = 4.5 to 5.5 V, V− = −15 V; V+ = 13.5 to 16.5 V, V− = −15 V V− = −4.5 to −5.5 V, V+ = +15 V; V− = −13.5 to −16.5 V, V+ = +15 V	 − −	 0.0003 0.002	 0.01 0.01	 %FS/%VS %FS/%VS
Power Supply Current Positive Negative	 I+ I−	V_S = ±5.0 V, I_{REF} = 1.0 mA	 − −	 3.1 −4.3	 3.8 −5.8	mA
Positive Negative	I+ I−	V_S = +5.0 V, −15 V, I_{REF} = 2.0 mA	− −	3.1 −7.1	3.8 −7.8	
Positive Negative	I+ I−	V_S = ±15 V, I_{REF} = 2.0 mA	− −	3.2 −7.2	3.8 −7.8	
Power Dissipation	P_D	±5.0 V, I_{REF} = 1.0 mA +5.0 V, −15 V, I_{REF} = 2.0 mA ±15 V, I_{REF} = 2.0 mA	− − −	37 122 156	48 136 174	mW

AC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	DAC−08C			DAC−08E			DAC−08H			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Settling Time	t_S	To ±1/2LSB, All Bits Switched On or Off, T_{amb} = 25°C	−	70	135	−	70	135	−	70	135	ns
Propagation Delay Low-to-High High-to-Low	 t_{PLH} t_{PHL}	T_{amb} = 25°C, Each Bit All Bits Switched	−	35	60	−	35	60	−	35	60	ns

TEST CIRCUITS

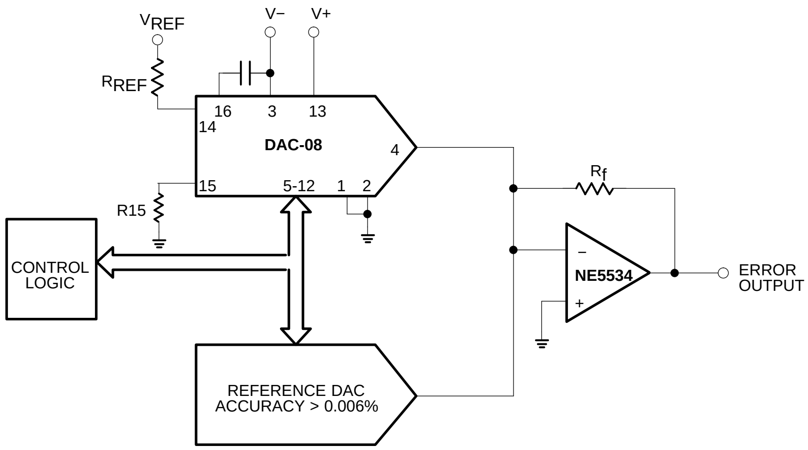


Figure 2. Relative Accuracy Test Circuit

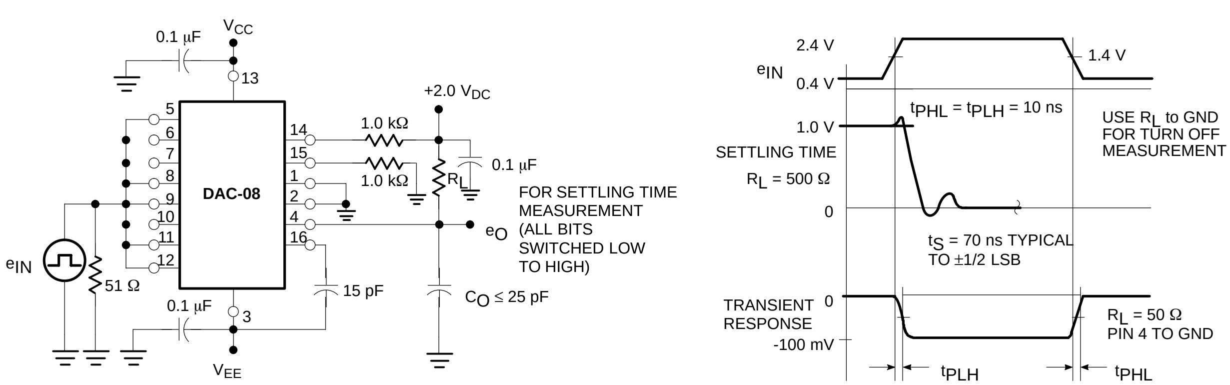


Figure 3. Transient Response and Settling Time

TEST CIRCUITS

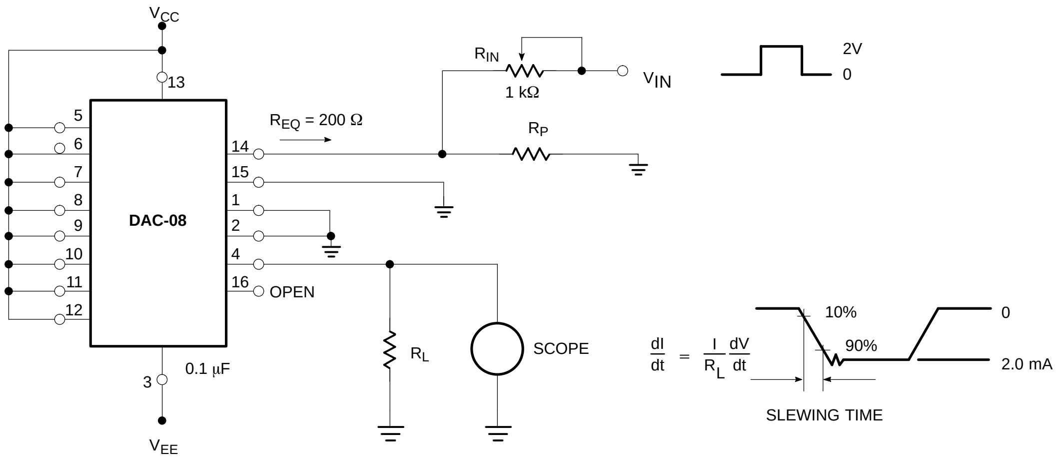
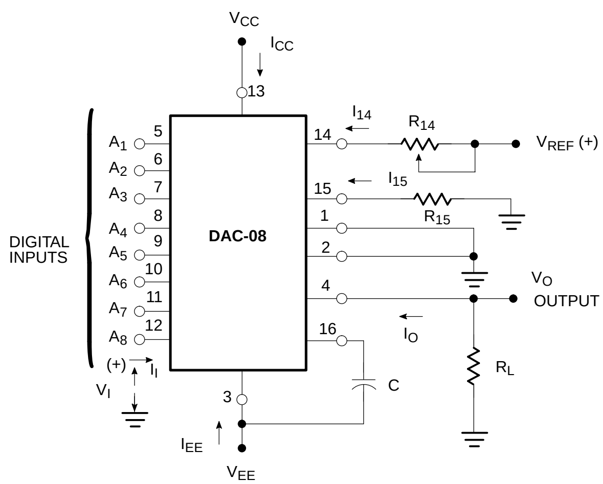


Figure 4. Reference Current Slew Rate Measurement



NOTES:
(See text for values of C.)
Typical values of $R_{14} = R_{15} = 1\ k\Omega$
$V_{REF} = +2.0\ V$
$C = 15\ pF$
V_I and I_I apply to inputs A_1 through A_8
The resistor tied to Pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left|\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256}\right|$$

where $K \approx \frac{V_{REF}}{R_{14}}$

and A_N = ‘1’ if A_N is at High Level
A_N = ‘0’ if A_N is at Low Level

Figure 5. Notation Definitions

TYPICAL PERFORMANCE CHARACTERISTICS

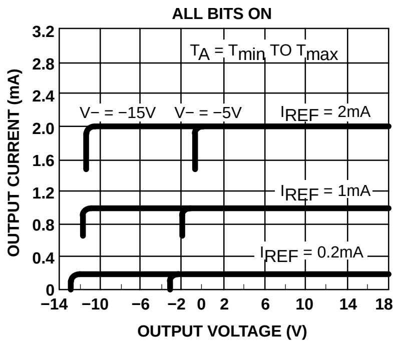


Figure 6. Output Current vs. Output Voltage (Output Voltage Compliance)

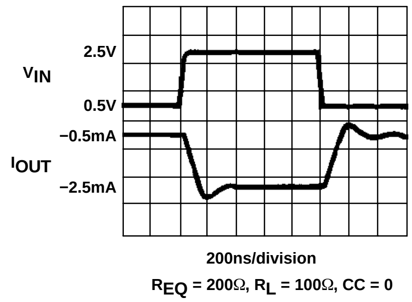


Figure 7. Fast Pulsed Reference Operation

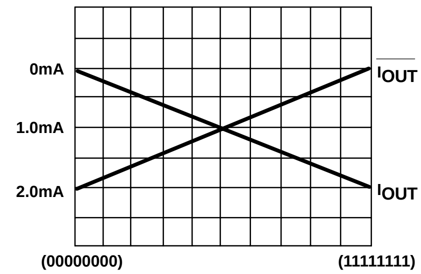


Figure 8. True and Complementary Output Operation

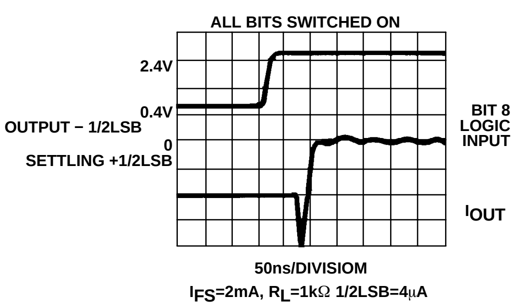


Figure 9. Full−Scale Settling Time

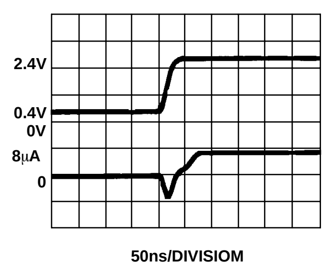


Figure 10. LSB Switching

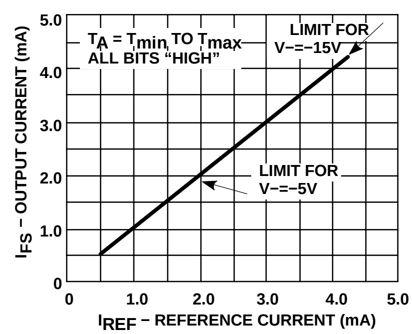


Figure 11. Full−Scale Current vs. Reference Current

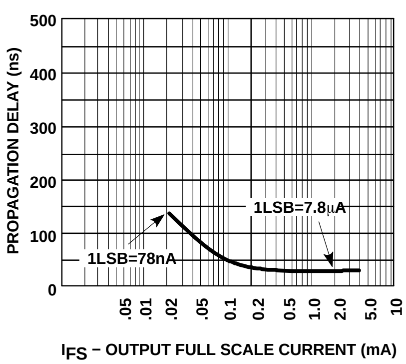


Figure 12. LSB Propagation Delay vs. IFS

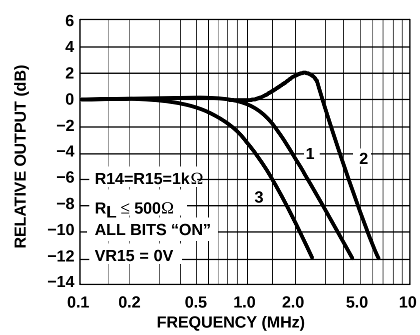


Figure 13. Reference Input Frequency Response

NOTES:

Curve 1: CC = 15pF, V_{IN} = 2.0V_{P-P} centered at +1.0V
Curve 1: CC = 15pF, V_{IN} = 5m0V_{P-P} centered at +200mV
Curve 1: CC = 15pF, V_{IN} = 100m0V_{P-P} centered at 0V and applied through 50Ω connected to Pin 14. +2.0V applied to R_{14}.

TYPICAL PERFORMANCE CHARACTERISTICS

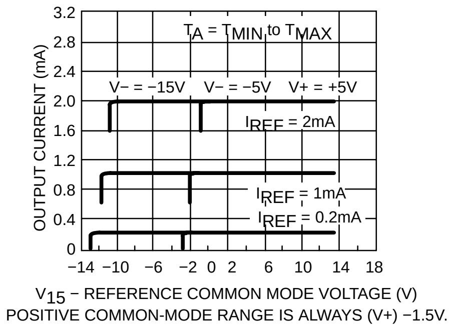


Figure 14. Reference AMP Common−Mode Range All Bits On

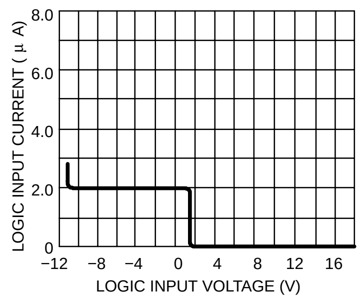


Figure 15. Logic Input Current vs. Input Voltage

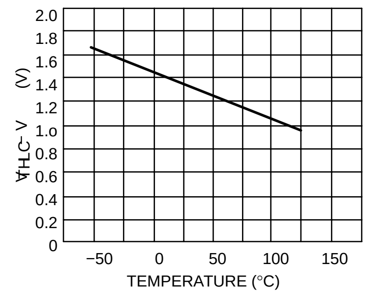


Figure 16. V_{TH}−V_{LC} vs. Temperature

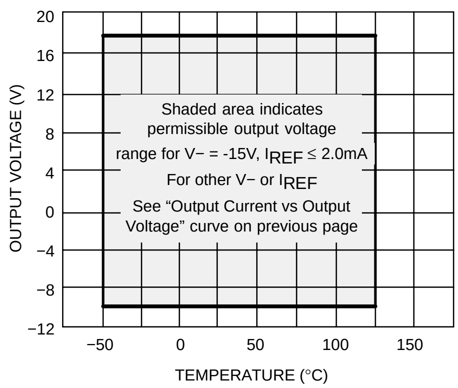


Figure 17. Output Voltage Compliance vs. Temperature

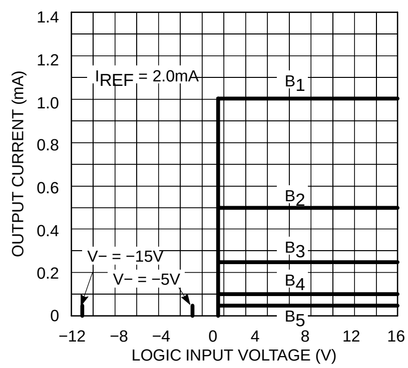


Figure 18. Bit Transfer Characteristics

NOTES:

B_1 through B_8 have identical transfer characteristics. Bits are fully switched, with less than 1/2LSB error, at less than ±100mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2.0V over the operating temperature range (V_{LC} = 0.0V).

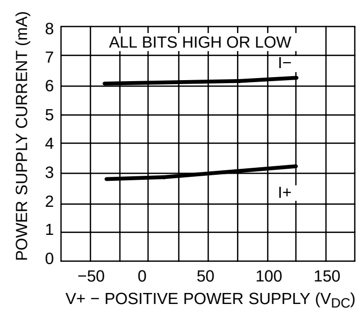


Figure 19. Power Supply Current vs. V+

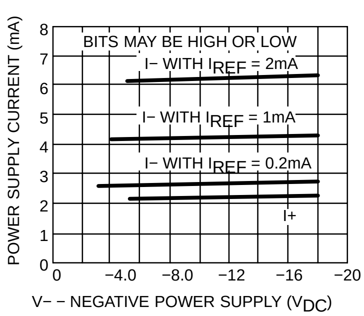


Figure 20. Power Supply Current vs. V−

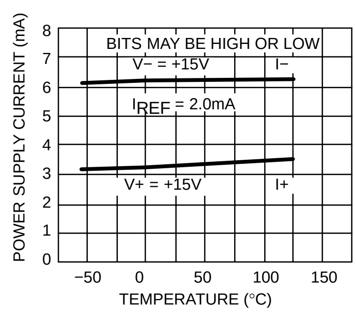


Figure 21. Power Supply Current vs. Temperature

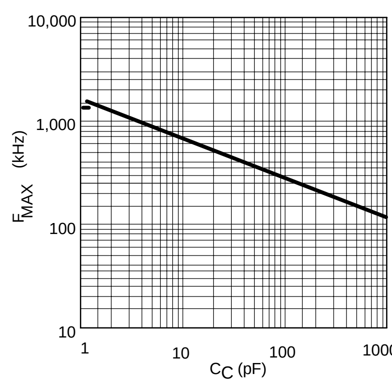


Figure 22. Maximum Reference Input Frequency vs. Compensation Capacitor Value

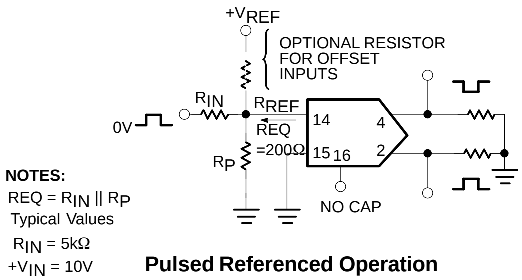


Figure 23. Typical Application

FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier input current must always flow into Pin 14 regardless of the setup method or reference supply voltage polarity.

Connections for a positive reference voltage are shown in Figure 2. The reference voltage source supplies the full reference current. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. R_{15} may be eliminated with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased as R_{14} value is increased. This is in order to maintain proper phase margin. For R_{14} values of 1.0, 2.5, and 5.0 kΩ, minimum capacitor values are 15, 37, and 75 pF, respectively. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection. (Fluctuations in the negative supply have more effect on accuracy than do any changes in the positive supply.)

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3.0 V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at Pin 15.

When using a DC reference voltage, capacitive bypass to ground is recommended. The 5.0 V logic supply is not recommended as a reference voltage, but if a well regulated 5.0 V supply which drives logic is to be used as the reference, R_{14} should be formed of two series resistors with the junction of the two resistors bypassed with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods applies and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage at Pin 4 must always be at least 4.5 V more positive than the voltage of the negative supply (Pin 3) when the reference current is 2.0 mA or less, and at least 8.0 V more positive than the negative supply when the reference current is between 2.0 mA and 4.0 mA. This is necessary to avoid saturation of the output transistors, which would cause serious accuracy degradation.

Output Current Range

Any time the full-scale current exceeds 2.0 mA, the negative supply must be at least 8.0 V more negative than the output voltage. This is due to the increased internal voltage drops between the negative supply and the outputs with higher reference currents.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy, full-scale accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current after zero-scale current has been nulled out. The relative accuracy of the DAC-08 series is essentially constant over the operating temperature range due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC-08 series has a very low full-scale current drift over the operating temperature range.

The DAC-08 series is guaranteed accurate to within ± LSB at +25°C at a full-scale output current of 1.992 mA. The relative accuracy test circuit is shown in Figure 2. The 12-bit converter is calibrated to a full-scale output current of 1.99219 mA, then the DAC-08 full-scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on the oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total of ± part in 65,536, or ± 0.00076%, which is much more accurate than the ± 0.19% specification of the DAC-08 series.

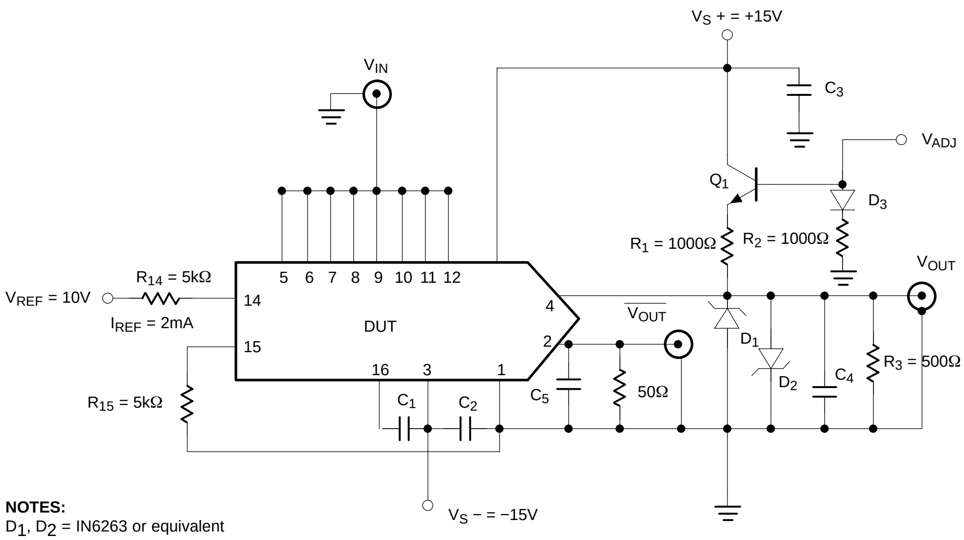
Monotonicity

A monotonic converter is one which always provides analog output greater than or equal to the preceding value for a corresponding increment in the digital input code. The DAC-08 series is monotonic for all values of reference current above 0.5 mA. The recommended range for operation is a DC reference current between 0.5 mA and 4.0 mA.

Settling Time

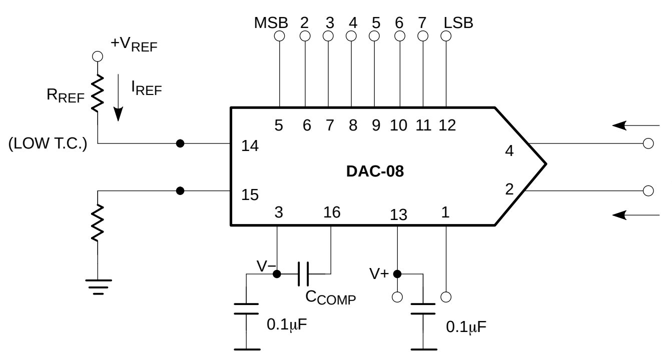
The worst-case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all input bits. This time is typically 70 ns for settling to within LSB for 8-bit accuracy. This time applies when $R_L < 500\ \Omega$ and $C_O < 25$ pF. The slowest single switch is the least significant bit, which typically turns on and settles in 65 ns. In applications where the DAC functions in a positive-going ramp mode, the worst-case condition does not occur and settling times less than 70 ns may be realized.

Extra care must be taken in board layout since this usually is the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, minimum scope lead length, and avoidance of ground loops are all mandatory.



NOTES:
D_1, D_2 = IN6263 or equivalent
D_3 = IN914 or equivalent
C_1 = 0.01μF
C_2, C_3 = 0.1μF
Q_1 = 2N3904
C_4, C_5 = 15pF and includes all probe and fixturing capacitance.

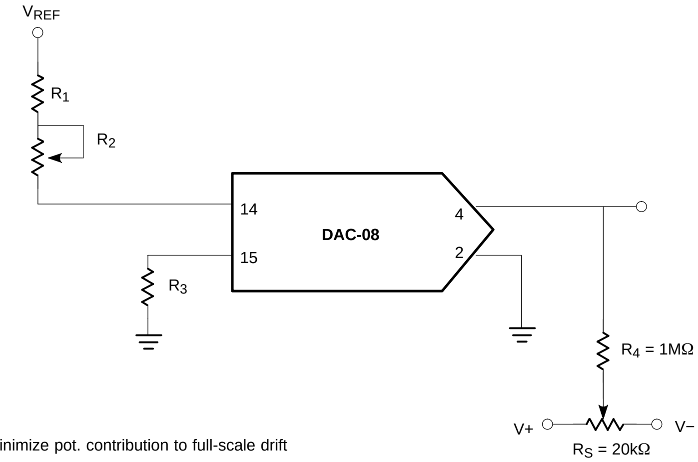
Figure 24. Settling Time and Propagation Delay



NOTES:

$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}\ ;\ I_O + \overline{I_O} = I_{FS} \text{ for all logic states}$$

Figure 25. Basic DAC−08 Configuration



NOTES:
R_1 = low T.C.
$R_3 = R_1 + R_2$
$R_2 \approx 0.1\ R_1$ to minimize pot. contribution to full-scale drift

Figure 26. Recommended Full−Scale and Zero−Scale Adjust

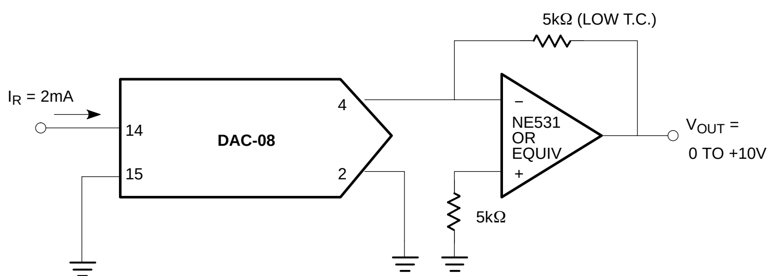
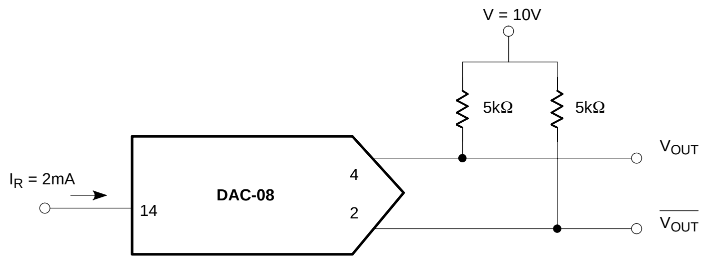
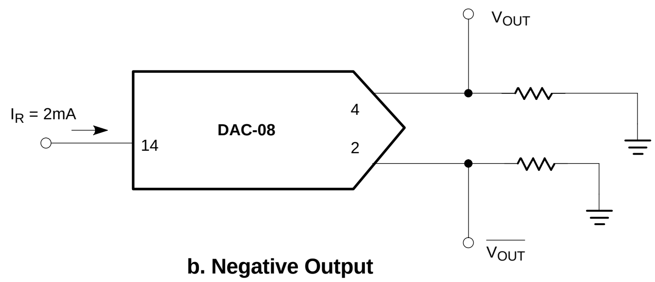


Figure 27. Unipolar Voltage Output for Low Impedance Output

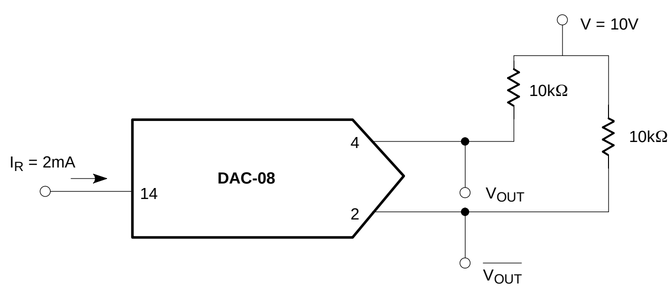


a. Positive Output



b. Negative Output

Figure 28. Unipolar Voltage Output for High Impedance Output



	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	V_{OUT}	$\overline{V_{OUT}}$
Positive full-scale	1	1	1	1	1	1	1	1	−9.920V	+10.000
Positive FS − 1LSB	1	1	1	1	1	1	1	0	−9.840V	+9.920
+ Zero-scale + 1LSB	1	0	0	0	0	0	0	1	−0.080V	+0.160
Zero-scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero-scale − 1LSB	0	1	1	1	1	1	1	1	0.080	0.000
Negative full scale − 1LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Negative full scale	0	0	0	0	0	0	0	0	+10.000	−9.920

Figure 29. Basic Bipolar Output Operation (Offset Binary)

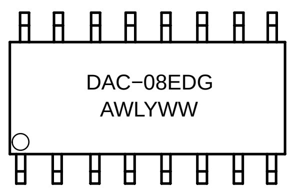
ORDERING INFORMATION

Device	Description	Temperature Range	Shipping†
DAC−08ED	16−Pin Plastic Small Outline Package	0 to +70°C	48 Units/Rail
DAC−08EDG	16−Pin Plastic Small Outline Package (Pb−Free)	0 to +70°C	48 Units/Rail
DAC−08EDR2	16−Pin Plastic Small Outline Package	0 to +70°C	2500 Tape & Reel
DAC−08EDR2G	16−Pin Plastic Small Outline Package (Pb−Free)	0 to +70°C	2500 Tape & Reel
DAC−08CN	16−Pin Plastic Dual In−Line Package	0 to +70°C	25 Units/Rail
DAC−08CNG	16−Pin Plastic Dual In−Line Package (Pb−Free)	0 to +70°C	25 Units/Rail
DAC−08EN	16−Pin Plastic Dual In−Line Package	0 to +70°C	25 Units/Rail
DAC−08ENG	16−Pin Plastic Dual In−Line Package (Pb−Free)	0 to +70°C	25 Units/Rail
DAC−08HN	16−Pin Plastic Dual In−Line Package	0 to +70°C	25 Units/Rail

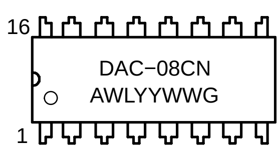
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

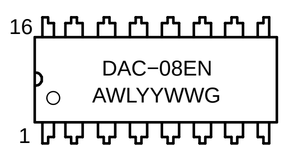
MARKING DIAGRAMS

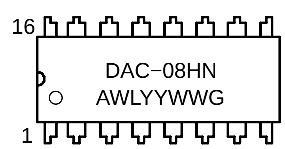
SOIC−16
D SUFFIX
CASE 751B



PDIP−16
N SUFFIX
CASE 648



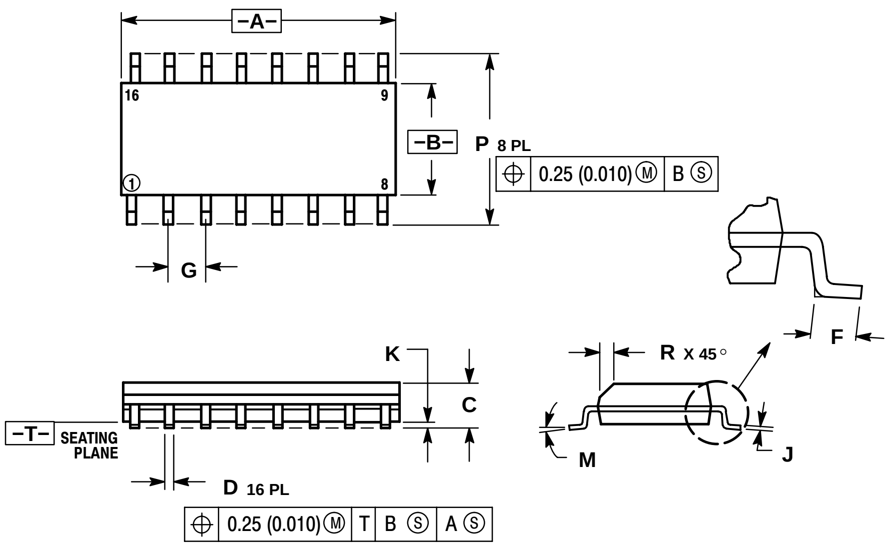




A = Assembly Location
WL = Wafer Lot
YY, Y = Year
WW = Work Week
G = Pb−Free Package

PACKAGE DIMENSIONS

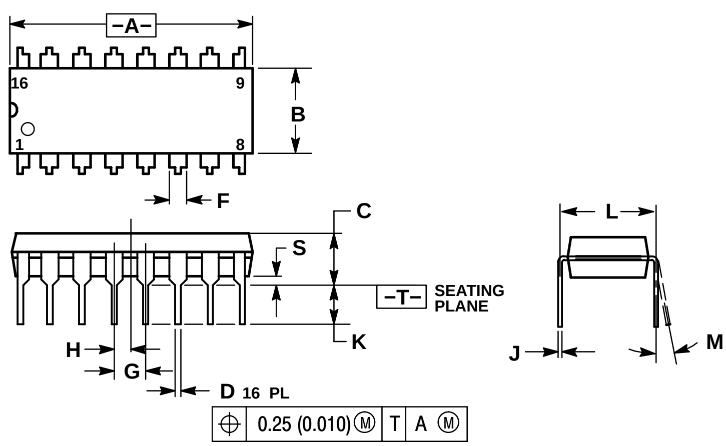
SOIC−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PDIP−16
N SUFFIX
CASE 648−08
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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