

# NTR3A085PZ

## MOSFET – Power, Single P-Channel, SOT-23 -20 V, -2.7 A

### Features

- Leading -20 V Trench for Low  $R_{DS(on)}$
- -1.8 V Rated for Low Voltage Gate Drive
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Power Load Switch

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	-20	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 8$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	-2.5	A
		$T_A = 85^\circ\text{C}$	-1.8	
	$t \leq 10\text{ s}$	$T_A = 25^\circ\text{C}$	-2.7	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	0.72	W
		$t \leq 10\text{ s}$	0.81	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	-1.9	A
		$T_A = 85^\circ\text{C}$	-1.4	
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	0.42	W
Pulsed Drain Current	$t_p = 10\ \mu\text{s}$	$I_{DM}$	-10	A
ESD HBM, JESD22-A114 (Note 3)	$V_{ESD}$	1000	V	
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	-1.1	A	
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	175	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 10\text{ s}$ (Note 1)	$R_{\theta JA}$	155	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	301	

1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 727 mm sq., 1 oz).
2. Surface-mounted on FR4 board using minimum pad size (Cu area = 3.8 mm sq., 1 oz).
3. ESD Rating: HBM Class 1C

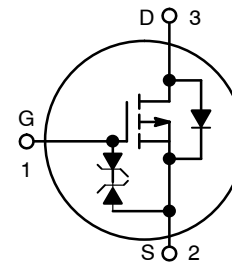


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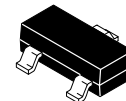
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$V_{(BR)DSS}$	$R_{DS(on)}$ Max	$I_D$ MAX
-20 V	77 m $\Omega$ @ -4.5 V	-2.7 A
	105 m $\Omega$ @ -2.5 V	
	160 m $\Omega$ @ -1.8 V	

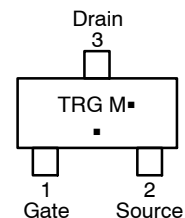
### P-Channel MOSFET



### MARKING DIAGRAM & PIN ASSIGNMENT



SOT-23  
CASE 318  
STYLE 21



TRG = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
NTR3A085PZT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTR3A085PZ

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	I <sub>D</sub> = -250 μA, ref to 25°C		22		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -20 V	T <sub>J</sub> = 25°C		-1	μA
			T <sub>J</sub> = 125°C		-100	μA
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±8 V			±10	μA

## ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-0.4		-1.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			3.0		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -1.6 A		54	77	mΩ
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -1.3 A		67	105	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -0.9 A		87	160	
		V <sub>GS</sub> = -1.5 V, I <sub>D</sub> = -0.3 A		110		
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -5 V, I <sub>D</sub> = -2.3 A		12		S

## CHARGES AND CAPACITANCES

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = -10 V		586		pF
Output Capacitance	C <sub>oss</sub>			81		
Reverse Transfer Capacitance	C <sub>rss</sub>			72		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.6 A		6.9		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			0.5		
Gate-to-Source Charge	Q <sub>GS</sub>			0.8		
Gate-to-Drain Charge	Q <sub>GD</sub>			1.6		

## SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.6 A, R <sub>G</sub> = 6.0 Ω		6.8		ns
Rise Time	t <sub>r</sub>			11		
Turn-Off Delay Time	t <sub>d(off)</sub>			32		
Fall Time	t <sub>f</sub>			23		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -1.1 A	T <sub>J</sub> = 25°C	-0.7	-1.2	V
			T <sub>J</sub> = 125°C	-0.6		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>SD</sub> /dt = 100 A/μs, I <sub>S</sub> = -1.6 A		11		ns
Charge Time	t <sub>a</sub>			6.0		
Discharge Time	t <sub>b</sub>			5.0		
Reverse Recovery Charge	Q <sub>RR</sub>			3.6		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 ms, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

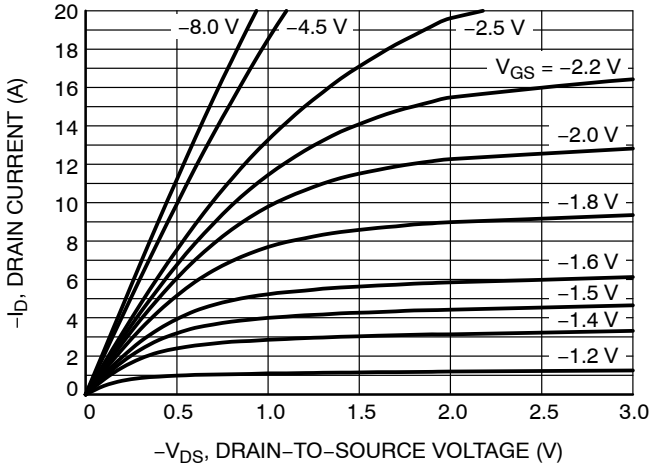


Figure 1. On-Region Characteristics

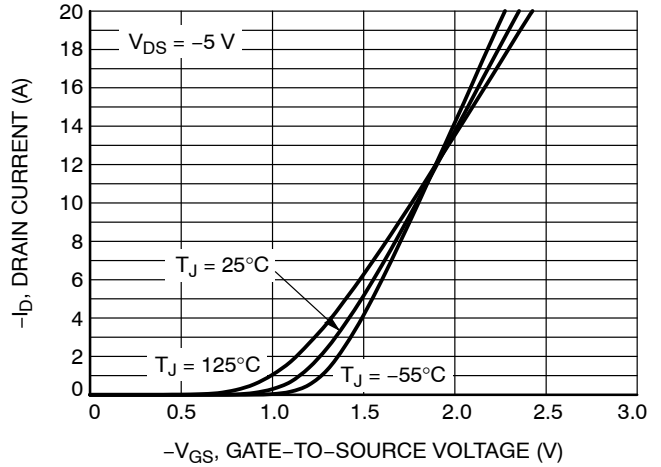


Figure 2. Transfer Characteristics

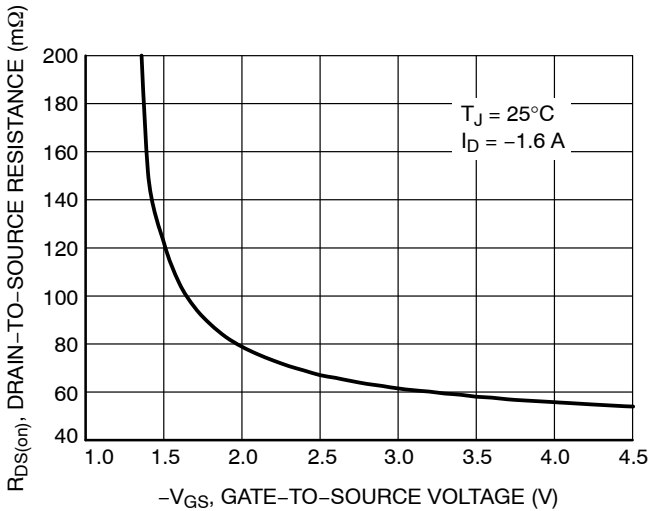


Figure 3. On-Resistance vs. Gate-to-Source Voltage

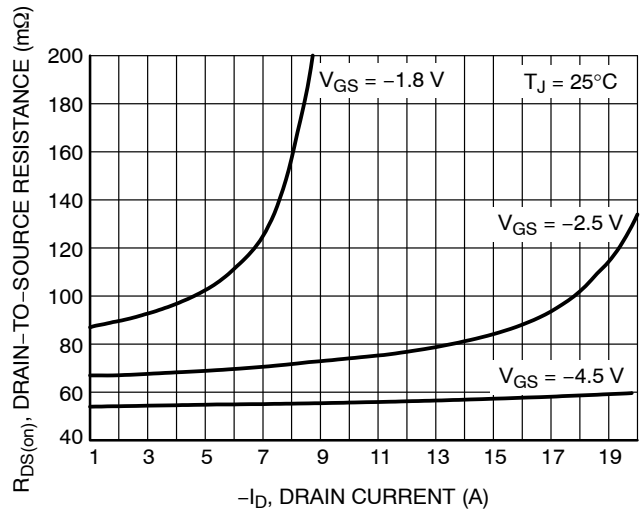


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

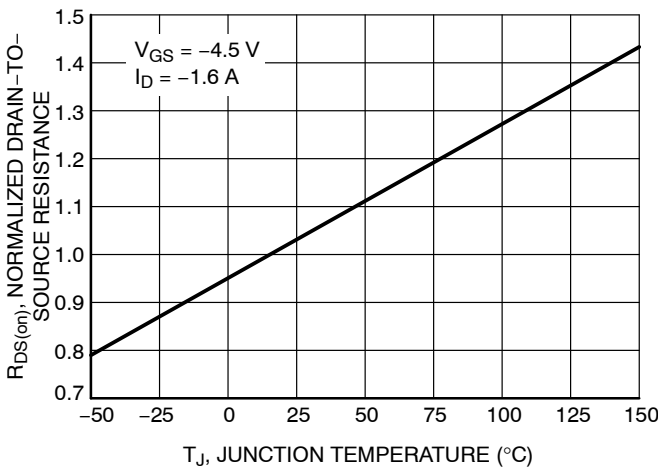


Figure 5. On-Resistance Variation with Temperature

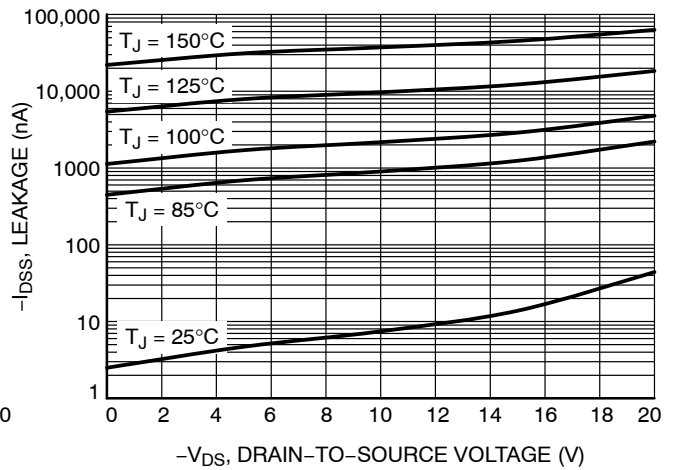


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTR3A085PZ

## TYPICAL CHARACTERISTICS

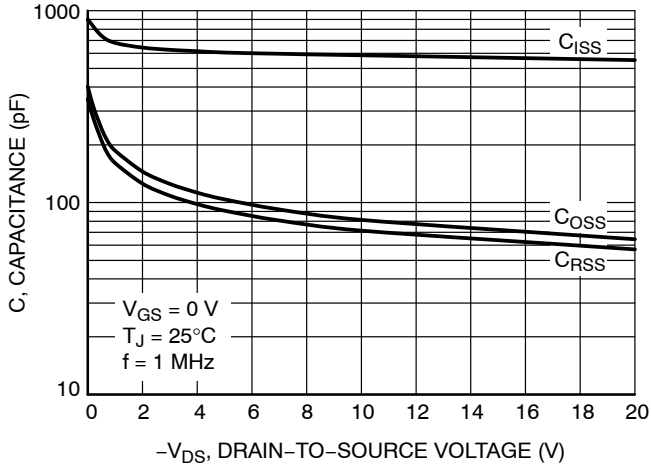


Figure 7. Capacitance Variation

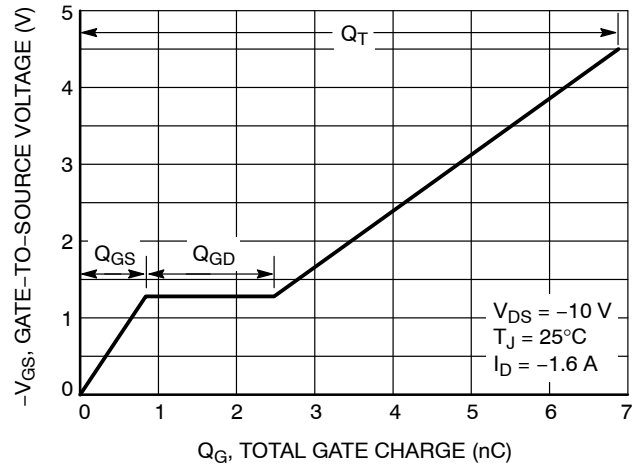


Figure 8. Gate-to-Source vs. Total Charge

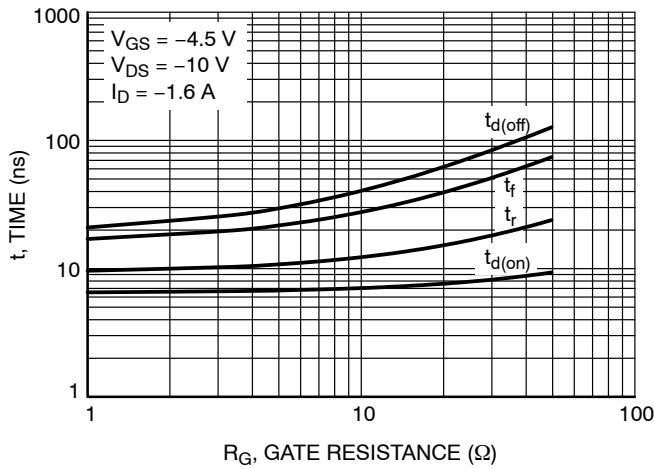


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

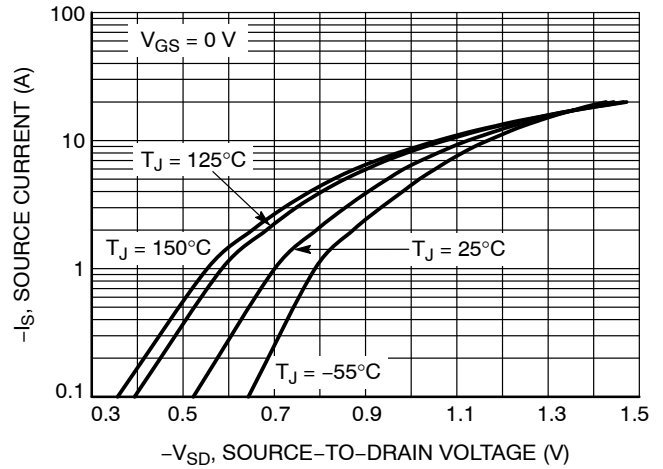


Figure 10. Diode Forward Voltage vs. Current

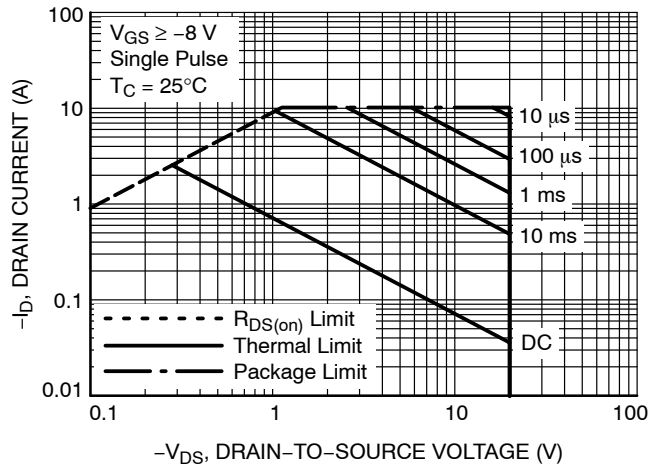


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NTR3A085PZ

## TYPICAL CHARACTERISTICS

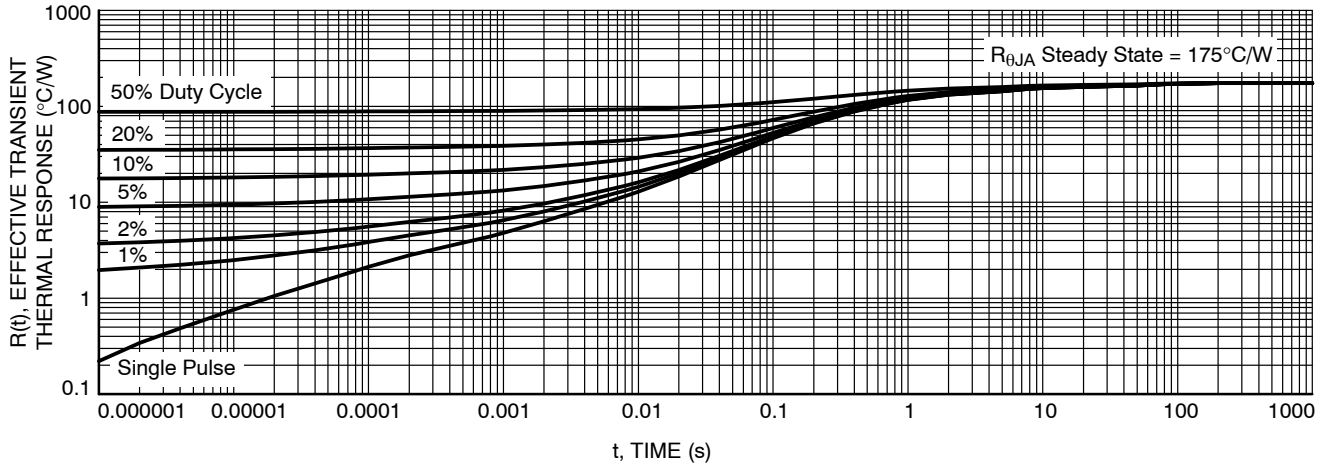
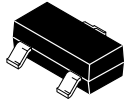


Figure 12. Thermal Impedance (Junction-to-Ambient)

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**SOT-23 (TO-236)**  
CASE 318  
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

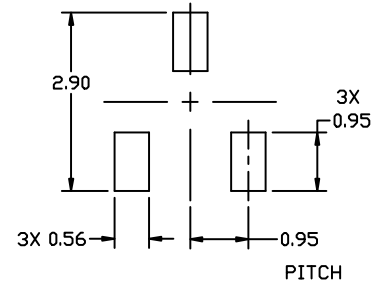
DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H <sub>E</sub>	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

**GENERIC MARKING DIAGRAM\***



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



**RECOMMENDED MOUNTING FOOTPRINT**

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

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**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**



**SOT-23 (TO-236)**  
**CASE 318**  
**ISSUE AT**

DATE 01 MAR 2023

- |   |   |   |   |   |   |
|---|---|---|---|---|---|
| STYLE 1 THRU 5:<br>CANCELLED                            | STYLE 6:<br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR | STYLE 7:<br>PIN 1. EMITTER<br>2. BASE<br>3. COLLECTOR       | STYLE 8:<br>PIN 1. ANODE<br>2. NO CONNECTION<br>3. CATHODE  |   |   |
| STYLE 9:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE      | STYLE 10:<br>PIN 1. DRAIN<br>2. SOURCE<br>3. GATE     | STYLE 11:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE-ANODE | STYLE 12:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. ANODE       | STYLE 13:<br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE           | STYLE 14:<br>PIN 1. CATHODE<br>2. GATE<br>3. ANODE          |
| STYLE 15:<br>PIN 1. GATE<br>2. CATHODE<br>3. ANODE      | STYLE 16:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE | STYLE 17:<br>PIN 1. NO CONNECTION<br>2. ANODE<br>3. CATHODE | STYLE 18:<br>PIN 1. NO CONNECTION<br>2. CATHODE<br>3. ANODE | STYLE 19:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE-ANODE | STYLE 20:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE          |
| STYLE 21:<br>PIN 1. GATE<br>2. SOURCE<br>3. DRAIN       | STYLE 22:<br>PIN 1. RETURN<br>2. OUTPUT<br>3. INPUT   | STYLE 23:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE         | STYLE 24:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE           | STYLE 25:<br>PIN 1. ANODE<br>2. CATHODE<br>3. GATE          | STYLE 26:<br>PIN 1. CATHODE<br>2. ANODE<br>3. NO CONNECTION |
| STYLE 27:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. CATHODE | STYLE 28:<br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE     |   |   |   |   |

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