4550 Group

SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER for INFRARED REMOTE CONTROL TRANSMITTER

DESCRIPTION

The 4550 Group is a 4-bit single chip microcomputer designed with CMOS technology for remote controller. Its CPU is that of 4500 series using a simple, high-speed instruction set. The computer is equipped with a remote control carrier wave output circuit and an LCD control circuit, and is suitable for remote control transmitters designed for VCR_S and air conditioners.

The various microcomputers in the 4550 Group include variations of the built-in memory type and package as shown the table below.

APPLICATION

Various remote control transmitters

FEATURES

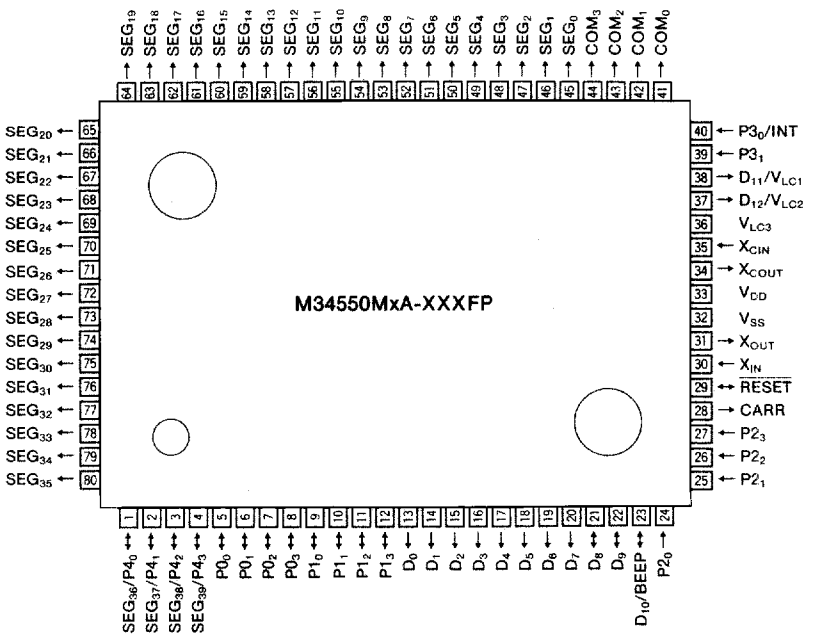
- Number of basic instructions 100
- Minimum instruction execution time ..... 1.875μs (at 1.6MHz system clock frequency)
- Supply voltage ..... 2.2V to 3.6V (2.5V to 3.6V at built-in PROM versions)
- Timers
  - Timer 1 ..... 9-bit timer with a reload register
  - Timer 2 ..... 4-bit×2 (fixed dividing frequency)
  - Timer 3 ..... 8-bit timer with a reload register
- Interrupt function ..... 3 sources
- Clock generating circuit
  - Main clock (X_{IN}) : a ceramic resonator or external clock input
  - Sub-clock (X_{CIN}) : a quartz-crystal oscillator (32kHz)
- Remote control carrier wave output function
- Built-in LCD controller/driver
  - Segment output 40
  - Common output 4

Product	ROM (PROM) size (×10 bits)	RAM size (×4 bits)	Package outline	ROM type
M34550M4A-XXXFP	4096 words	368 words	80P6N-A	Mask ROM
M34550M6A-XXXFP	6144 words			
M34550M8A-XXXFP	8192 words			
M34550E8-XXXFP				One Time PROM
M34550E8FP *				
M34550E8FS **			80D0	EPROM

* : Shipped in blank

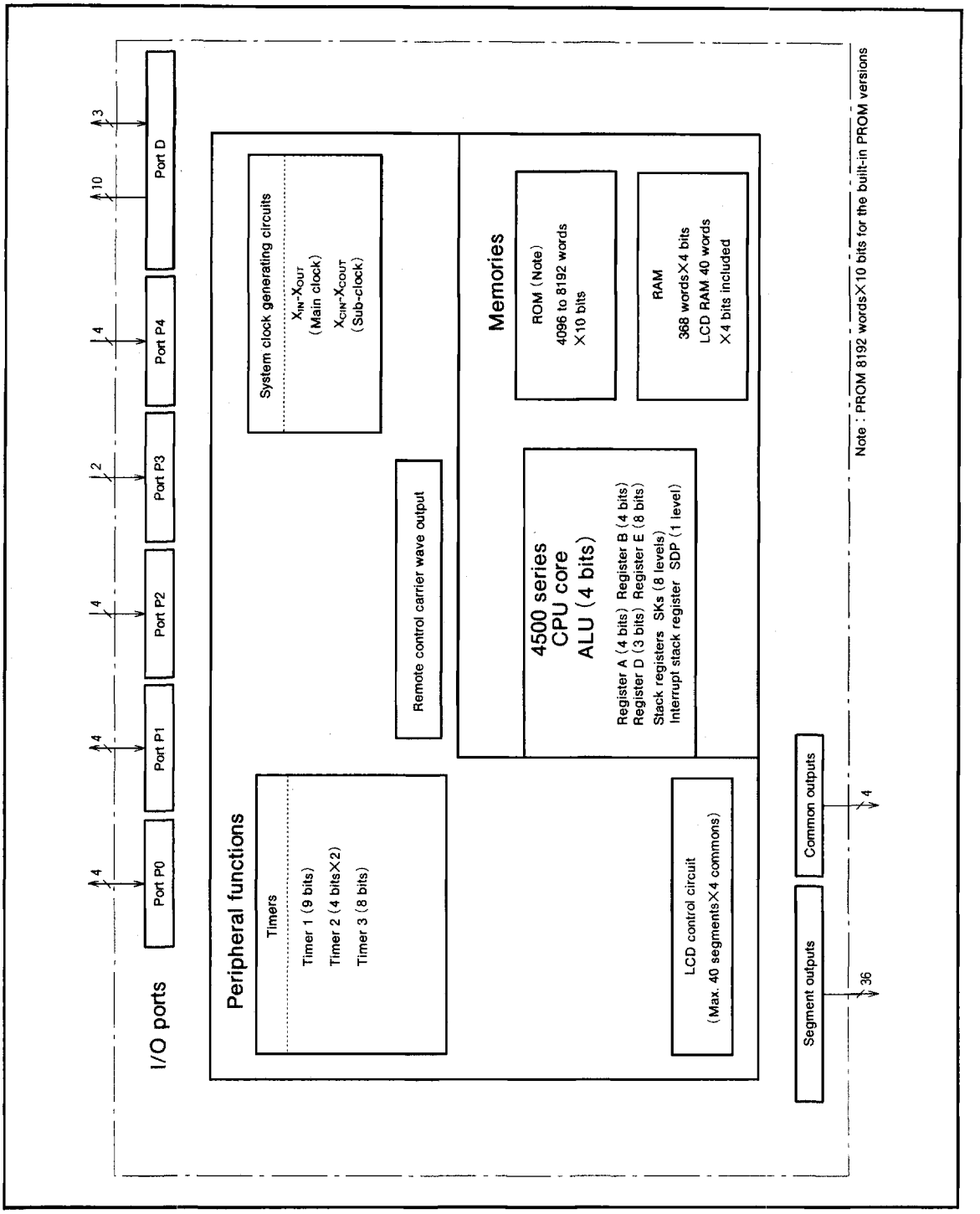
** : For program development only

PIN CONFIGURATION (TOP VIEW)



Outline 80P6N-A

BLOCK DIAGRAM



PERFORMANCE OVERVIEW

Parameter			Function
Number of basic instructions			100
Minimum instruction execution time			1.875μs (at 1.6MHz system clock frequency)
System clock frequencies	Main clock		1.6MHz
	Sub-clock		32kHz
Memory sizes	ROM	M34550M4A	4096 words×10 bits
		M34550M6A	6144 words×10 bits
		M34550M8A	8192 words×10 bits
	RAM		368 words×4 bits (LCD RAM 40 words×4 bits included)
Input/Output pins	D_0—D_7 D_{11}, D_{12}	Output	Ten independent output ports; D_{11} and D_{12} are also used as the LCD power supply input pins V_{LC1} and V_{LC2}, respectively.
	D_8—D_{10}	I/O	Three independent I/O ports; D_{10} pin is also used as the buzzer output pin BEEP.
	$P0_0$—$P0_3$	I/O	4-bit I/O port; each pin is equipped with a pull-up function and a key-on wakeup function (both programmable).
	$P1_0$—$P1_3$	I/O	4-bit I/O port; each pin is equipped with a pull-up function and a key-on wakeup function (both programmable).
	$P2_0$—$P2_3$	Input	4-bit input port; pins $P2_0$ and $P2_1$ are equipped with a key-on wakeup function, respectively.
	$P3_0$, $P3_1$	Input	2-bit input port; each pin is equipped with a pull-up function. $P3_0$ pin is also used as the interrupt input pin INT, and is equipped with a key-on wakeup function.
	$P4_0$—$P4_3$	Input	4-bit input port; these pins are also used as pins SEG_{36}—SEG_{39} respectively with software.
Carrier wave	Output structure		Variable period carrier wave output (software carrier output enabled)
	Output frequency (Variable period carrier wave output used)		26.57kHz to 400kHz (at 1.6MHz system clock frequency)
Timers	Timer 1		9-bit programmable timer with a reload register
	Timer 2		4-bit fixed dividing frequency ×2
	Timer 3		8-bit programmable timer with a reload register
Interrupt	Source		3 (one for both edges sense external, two for timer)
	Nesting		1 level
Subroutine nesting			8 levels
LCD	Selective bias value		1/2, 1/3 bias
	Selective duty value		2, 3, 4 duty
	Common output		4
	Segment output		40
	Internal resistor for power supply		200kΩ (typical value) ×3
Device structure			CMOS silicon gate
Package			80-pin plastic molded QFP
Operating temperature range			−20℃ to 70℃
Supply voltage			2.2V to 3.6V (2.5V to 3.6V at built-in PROM version)
Power dissipation (typical value)	Active mode		1mA (f(X_{IN})=910kHz, V_{DD}=3V, output transistors in the cut-off state)
			0.5mA (f(X_{IN})=455kHz, V_{DD}=3V, output transistors in the cut-off state)
	Power down 1 mode		4μA (f(X_{CIN})=32kHz, V_{DD}=3V, output transistors in the cut-off state)
	Power down 2 mode		0.1μA (at room temperature, V_{DD}=3V, output transistors in the cut-off state)

PIN DESCRIPTION

Pin	Name	Input/Output	Function
V_{DD}	Power supply	—	Connected to a plus power supply
V_{SS}	Ground	—	Connected to a 0V power supply
$\overline{RESET}$	Reset I/O	I/O	An N-channel open-drain I/O pin for a system reset. When the watchdog timer causes the system to be reset, the $\overline{RESET}$ pin outputs "L" level.
X_{IN}	Main clock input	Input	I/O pins of the main clock generating circuit. X_{IN} and X_{OUT} can be connected to a ceramic resonator. A feedback resistor is built-in between them.
X_{OUT}	Main clock output	Output	
X_{CIN}	Sub-clock input	Input	I/O pins of the sub-clock generating circuit. X_{CIN} and X_{COUT} are connected to a 32.768kHz quarts-crystal oscillator. A feedback resistor is built-in between them.
X_{COUT}	Sub-clock output	Output	
D_0—D_7 D_{11}/V_{LC1} D_{12}/V_{LC2}	Output port D	Output	Each pin has an independent 1-bit wide output function for instructions SD and RD. Each bit is designated for independent use by register Y of the data pointer. Each pin has an output latch. All latches on port D can be set to "1" with the CLD instruction.
D_8—D_{10}	I/O port D	I/O	Each pin has an independent 1-bit wide I/O function for instructions SZD, SD, and RD. Each bit is designated for independent use by register Y of the data pointer. Each pin has an output latch. For input use, set the latch of the specified bit to "1". All latches on port D can be set to "1" with the CLD instruction.
$P0_0$—$P0_3$	I/O port P0	I/O	Each of ports P0 and P1 serves as a 4-bit I/O port, and it can be used as inputs when the output latch is set to "1". Every pin of the ports has a key-on wakeup function and a pull-up function.
$P1_0$—$P1_3$	I/O port P1		
$P2_0$—$P2_3$	Input port P2	Input	4-bit input port. Pins $P2_0$ and $P2_1$ have a key-on wakeup function, respectively.
$P3_0$/INT $P3_1$	Input port P3	Input	2-bit input port. Each pin is provided with a pull-up function which can be turned on or off with software. $P3_0$ pin is also used as the interrupt input pin INT and has a key-on wakeup function which can be initiated with software.
$SEG_{36}/P4_0$ —$SEG_{39}/P4_3$	Input port P4	Input	4-bit input port. $P4_0$—$P4_3$ are also used as SEG_{36}—SEG_{39} respectively with software.
CARR	Carrier output	Output	Remote control carrier wave output pin. C4 flag (1 bit) can be also used to control the carrier wave in addition to hardware carrier method using an exclusive hardware.
V_{LC1}—V_{LC3}	LCD power input	Input	LCD power supply input pins. Connect V_{LC3} pin to V_{DD} pin when an internal resistor is used (connect to V_{DD} through a resistor if brightness control is necessary). Apply voltage such that $0 \leq V_{LC1} \leq V_{LC2} \leq V_{LC3} \leq V_{DD}$ when external power is used.
SEG_0—SEG_{39}	Segment output	Output	LCD segment output pins
COM_0—COM_3	Common output	Output	LCD common output pins. Pins COM_0 and COM_1 are used at 1/2 duty, pins COM_0—COM_2 are used at 1/3 duty, and pins COM_0—COM_3 are used at 1/4 duty.

CONNECTIONS OF UNUSED PINS

Pin	Connection	Pin	Connection
X_{OUT}	Open (when using an external clock)	$P2_0$—$P2_3$	Connect to V_{DD} (Note 2)
X_{CIN}	Connect to V_{SS}	$P3_0$, $P3_1$	Connect to V_{DD}
X_{COUT}	Open	$SEG_{36}/P4_0$—$SEG_{39}/P4_3$	When selecting SEG pin function, open (Note 3)
D_0—D_7, D_{11}/V_{LC1}, D_{12}/V_{LC2}	Connect to V_{SS}, or set the output latch to "0" and open. (Note 1)	CARR	Open
		V_{LC3}	When not using LCD, connect to V_{DD} (Note 4)
D_8—D_{10}	Connect to V_{SS}, or set the output latch to "0" and open.	SEG_0—SEG_{35}	Open
$P0_0$—$P0_3$	Open	COM_0—COM_3	Open
$P1_0$—$P1_3$	Open		

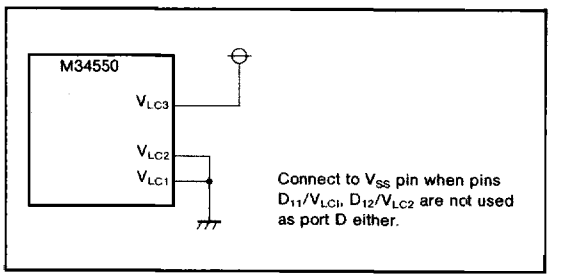
Notes : 1. Pins D_{11} and D_{12} are also used as pins V_{LC1} and V_{LC2}, respectively. When not using, clear the LCD control register (L3) to "0_2" and disconnect from the internal LCD power supply (register L3="0_2" at reset).
2. When not using the $P2_3$ pin of M34550E8, connect to V_{SS} through a 5kΩ resistor at the shortest distance.
3. The segment output pin function is selected at reset.
4. When not using LCD, clear the LCD control register (L1) to "0000_2" and turn off the LCD (register L1="0000_2" at reset).

(Note when the output latch is set to "0" and pins are open)

- After reset is released, port is in a high-impedance state until it is switched to an output enabled state. Accordingly, the voltage level of pins is undefined and the excess of the supply current may occur while the port is in a high-impedance state.
- To set the output latch periodically by a program is recommended because the value of output latch may change by noise or program run-away (caused by noise).

(Note when connecting to V_{DD} and V_{SS})

- Connect the unused pins to V_{DD} or V_{SS} using the thickest wire at the shortest distance.

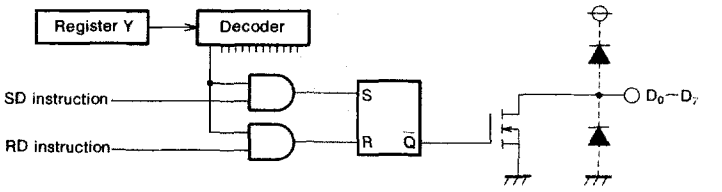


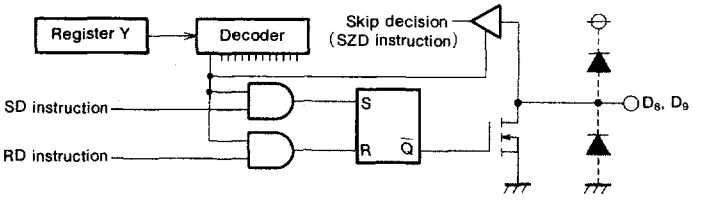
Handling of unused LCD power supply input pins

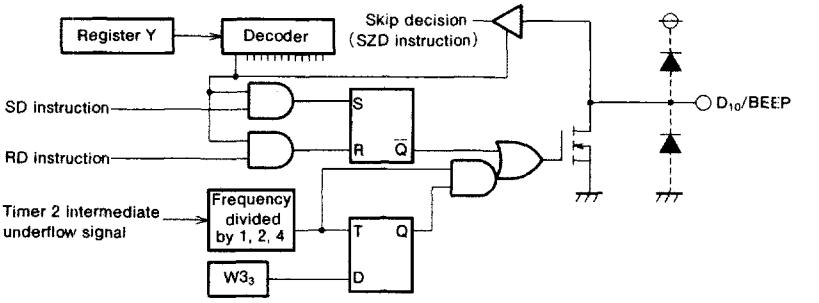
PORT FUNCTION

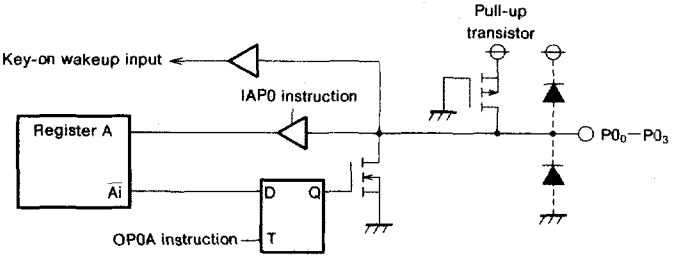
Port	Pin	Input/ Output	Output structure	Control bits	Control instructions	Multifunction	Control registers	Remark
Port D	D_0—D_7	Output (10)	N-channel open-drain	1	SD, RD, CLD			
	D_{11}/V_{LC1}					V_{LC1}	L1, L3	
	D_{12}/V_{LC2}					V_{LC2}		
	D_8, D_9	I/O (3)			SZD			
	D_{10}/BEEP					BEEP	W3	
Port P0	$P0_0$—$P0_3$	I/O (4)	N-channel open-drain	4	OP0A, IAP0	Key-on wakeup		Built-in a pull-up transistor
Port P1	$P1_0$—$P1_3$	I/O (4)	N-channel open-drain	4	OP1A, IAP1	Key-on wakeup		Built-in a pull-up transistor
Port P2	$P2_0$, $P2_1$	Input (4)		4	IAP2	Key-on wakeup		
	$P2_2$, $P2_3$							
Port P3	$P3_0$/INT	Input (2)		2	IAP3	INT Key-on wakeup	I1	Built-in a programmable pull-up transistor
	$P3_1$							
Port P4	$SEG_{36}/P4_0$—$SEG_{39}/P4_3$	Input (4)		4	IAP4	SEG_{36}—SEG_{39}	L2	
Port CARR	CARR	Output (1)	CMOS	1	SC3, RC3 SC4, RC4		C1, C2, PA	

PORT BLOCK DIAGRAMS









This symbol represents a parasitic diode on the port.
i represents 0, 1, 2, or 3.

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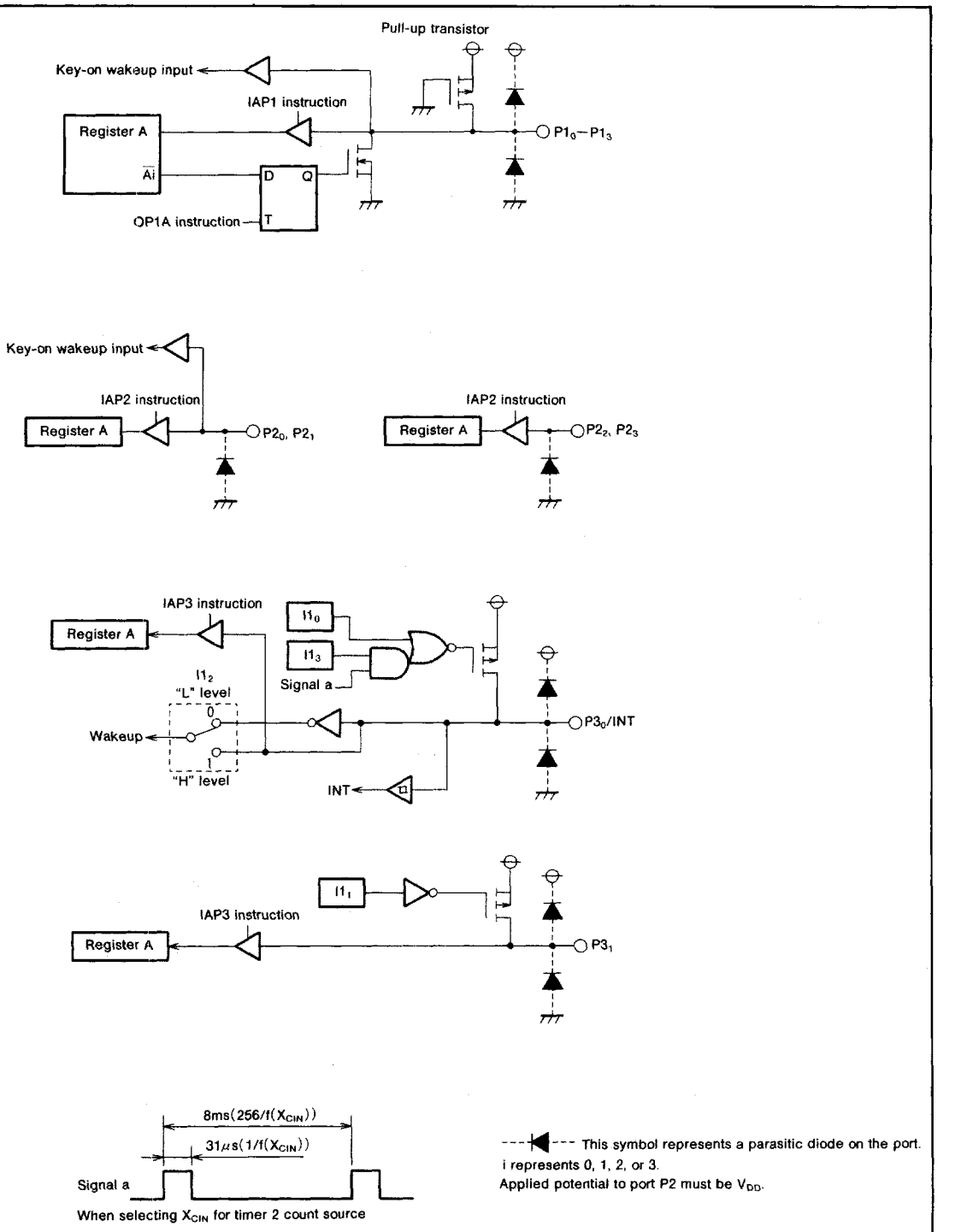
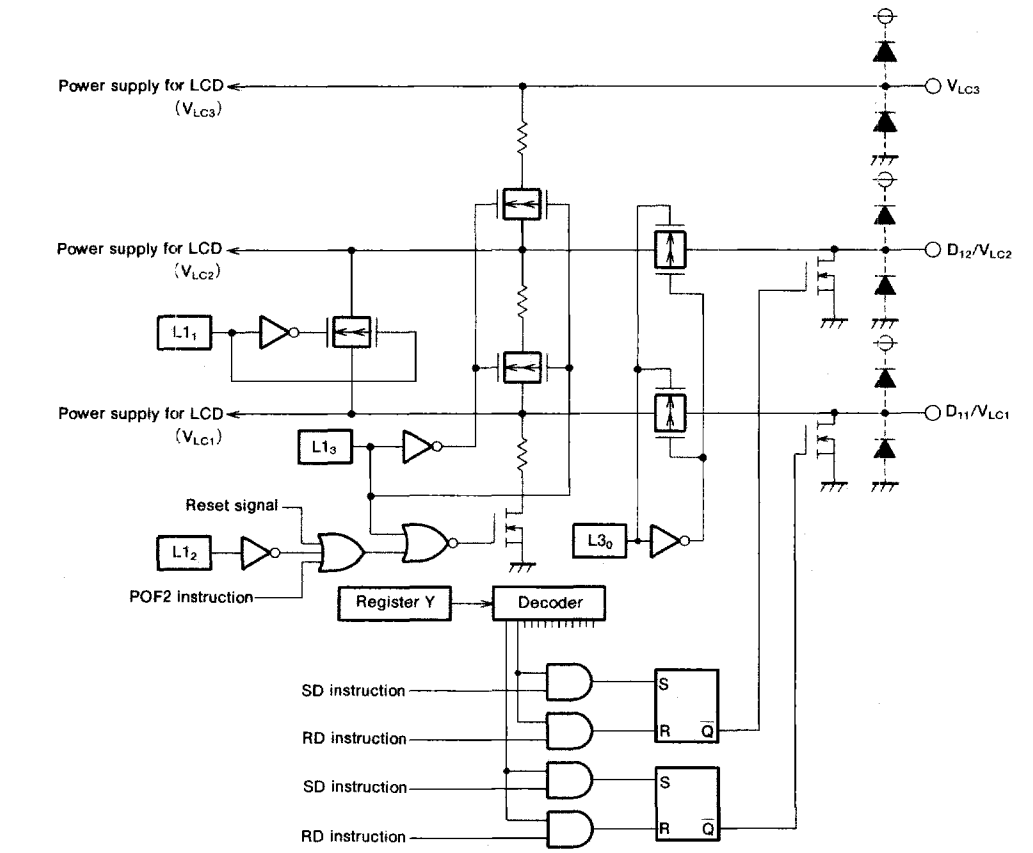
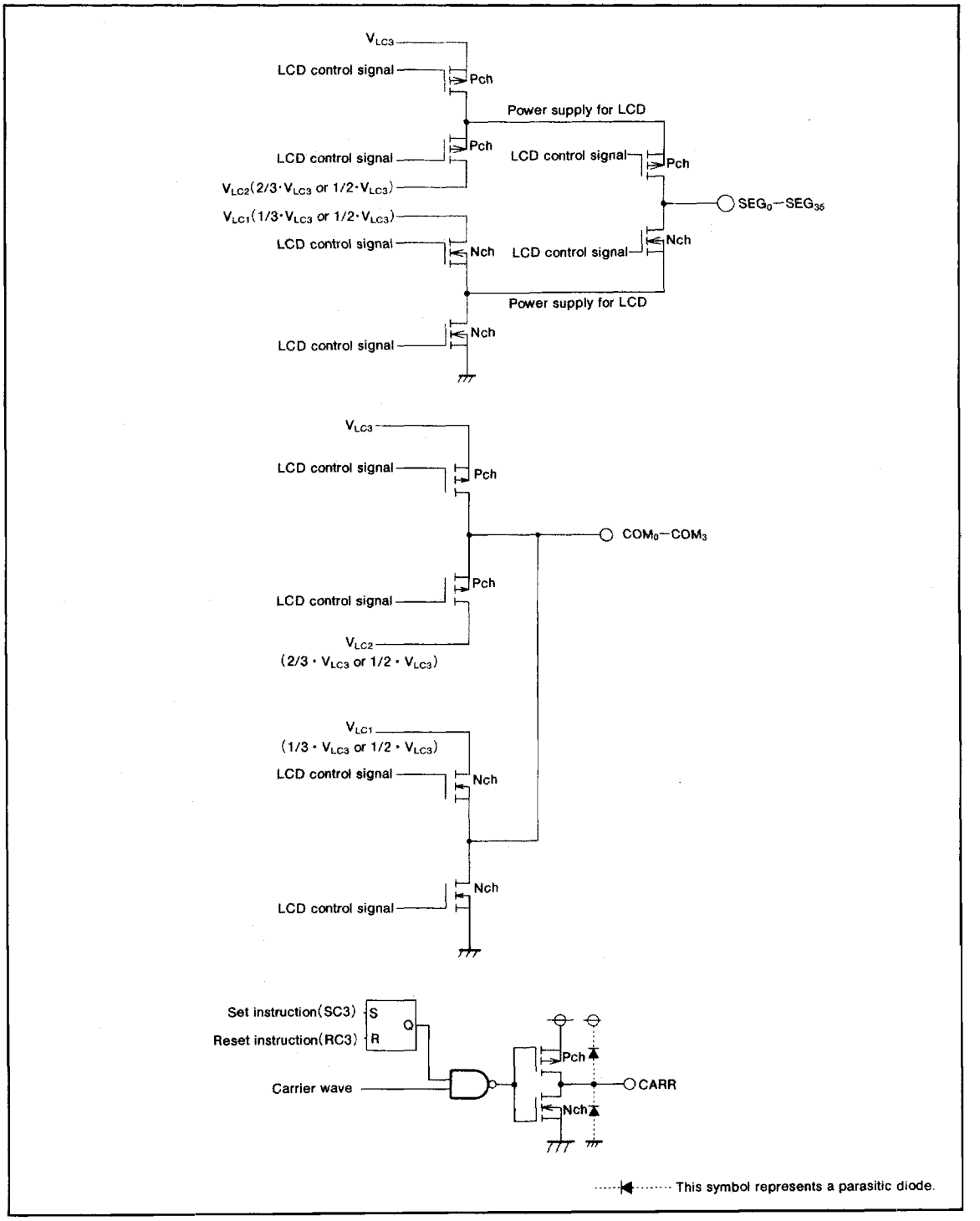
PORT BLOCK DIAGRAMS (continued)



PORT BLOCK DIAGRAMS (continued)



PORT BLOCK DIAGRAMS (continued)



FUNCTION BLOCK OPERATIONS

ARITHMETIC LOGIC UNIT (ALU)

The arithmetic logic unit ALU performs 4-bit arithmetic such as 4-bit data addition, comparison, AND operation, OR operation, and bit manipulation.

REGISTER A AND CARRY FLAG

Register A is a 4-bit register used for arithmetic, transfer, exchange, and I/O operation.

Carry flag CY is a 1-bit flag that is set to "1" when there is a carry with the AMC instruction (it is unchanged with both A n instruction and AM instruction). The value of A_0 is stored in the carry flag CY with the RAR instruction.

Carry flag CY can be set to "1" with the SC instruction and cleared to "0" with the RC instruction.

REGISTERS B and E

Register B is a 4-bit register used for temporary storage of 4-bit data, and for 8-bit data transfer together with register A.

Register E is an 8-bit register. It can be used for 8-bit data transfer with register B used as the high-order 4 bits and register A as the low-order 4 bits.

REGISTER D

Register D is a 3-bit register. It is used to store a 7-bit ROM address together with register A and is used as a pointer within the specified page when the TABP p, BLA p, or BMLA p instruction is executed.

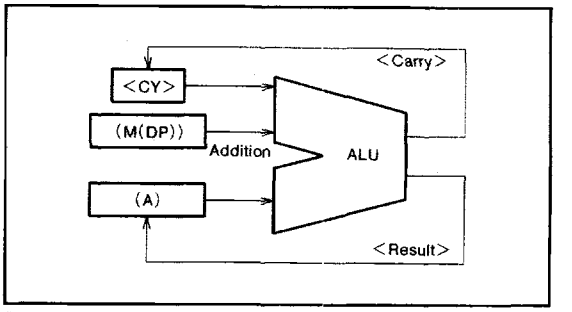


Fig. 1 AMC instruction execution example

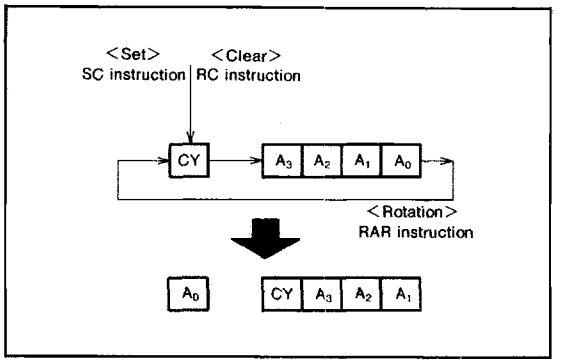


Fig. 2 RAR instruction execution example

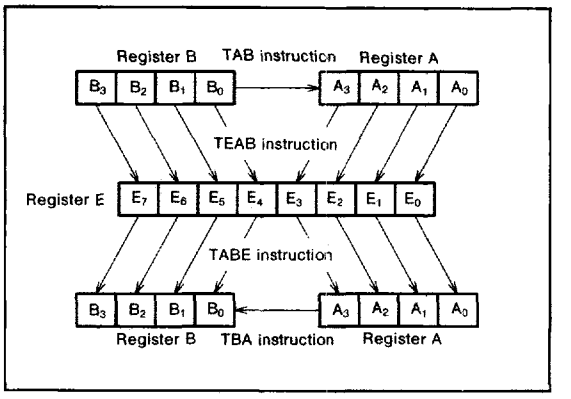


Fig. 3 Registers A, B and register E

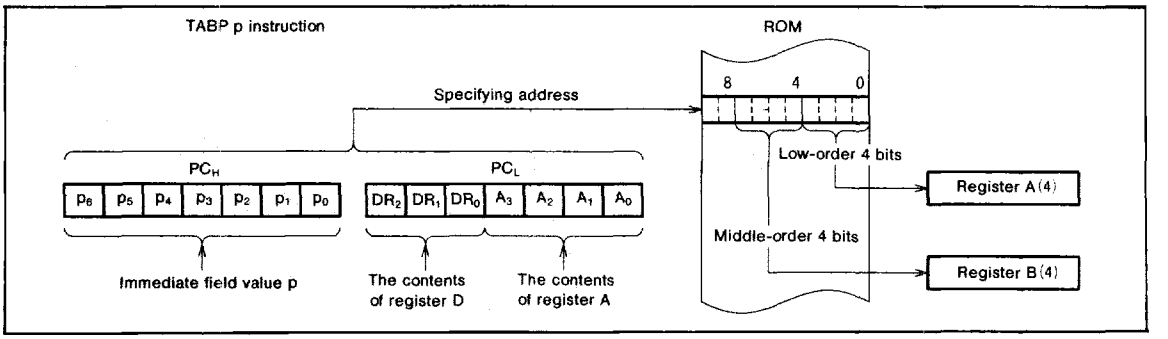


Fig. 4 TABP p instruction execution example

STACK REGISTERS (SKs)

Stack registers (SKs) are used to temporarily store the contents of program counter (PC) just before branching until returning to the original routine when;

- branching to an interrupt service routine (referred to as an interrupt service routine),
- performing a subroutine call, or
- executing the table reference instruction (TABP p).

Stack registers (SKs) are eight identical registers, so that subroutines can be nested up to 8 levels. However, one of stack registers is used respectively when using an interrupt service routine and when executing a table reference instruction. Accordingly, be careful not to over the stack when performing these operations together. The contents of registers SKs are destroyed when 8 levels are exceeded.

The register SK nesting level is pointed automatically by 3-bit stack pointer (SP). The contents of the stack pointer (SP) can be transferred to register A with the TASP instruction.

INTERRUPT STACK REGISTER (SDP)

Interrupt stack register (SDP) is a 1-stage register. When an interrupt occurs, this register (SDP) is used to temporarily store the contents of data pointer, carry flag, skip flag, register A, and register B just before an interrupt until returning to the original routine.

Unlike the stack registers (SKs), this register (SDP) is not used when executing the subroutine call instruction and the table reference instruction.

SKIP FLAG

Skip flag controls skip decision for the conditional skip instructions and continuous described skip instructions. When an interrupt occurs, the contents of skip flag is stored automatically in the interrupt stack register (SDP) and the skip condition is retained.

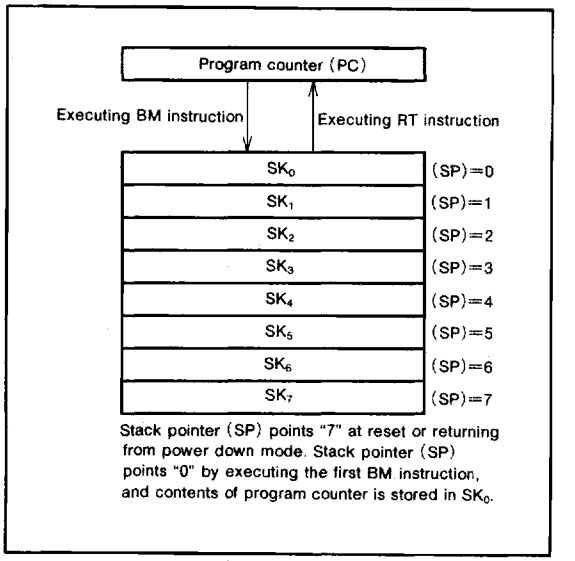


Fig. 5 Stack register (SK) structure

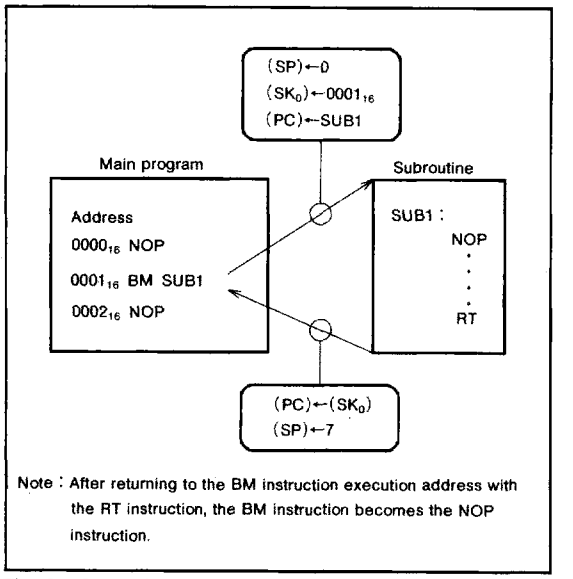


Fig. 6 Operation at subroutine call

PROGRAM MEMORY (ROM)

The program memory is the mask ROM. 1 word of ROM is composed of 10 bits. ROM is separated every 128 words by the unit of page (addresses 0 to 127).

Table 1 ROM size and pages

Product	ROM size (×10 bits)	Pages
M34550M4A	4096 words	32 (0 to 31)
M34550M6A	6144 words	48 (0 to 47)
M34550M8A/E8	8192 words	64 (0 to 63)

A part of page 1 (addresses 0080_{16} to $00FF_{16}$) is reserved for interrupt addresses. When an interrupt occurs, the address (interrupt address) corresponding to each interrupt is set in the program counter, and the instruction at the interrupt address is executed. When using an interrupt service routine, write the instruction generating the branch to that routine at an interrupt address.

Page 2 (addresses 0100_{16} to $017F_{16}$) is the special page for subroutine calls. Subroutines written in this page can be called from any page with the 1-word instruction (BM). Subroutines extending from page 2 to another page can also be called with the BM instruction when it starts on page 2.

All pages can be used as data areas with the TABP p instruction.

PROGRAM COUNTER (PC)

Program counter (PC) is used to specify a ROM address (page and address). It determines a sequence in which the instructions stored in ROM are read. It is a binary counter that increments the number of instruction bytes each time an instruction is executed. However, the value changes to a specified address when branch instructions, subroutine call instructions, return instructions, or the table reference instruction (TABP p) is executed.

Program counter consists of PC_H (most significant bit to bit 7) which specifies a ROM page and PC_L (bits 6 to 0) which specifies an address within a page. After it reaches the last address (address 127) of a page, it specifies address 0 of the next page.

Make sure that the PC_H does not specify after the last page of the built-in ROM.

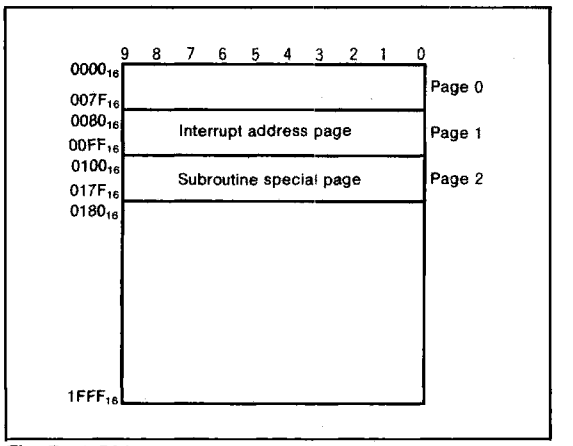


Fig. 7 ROM map of M34550M8A-XXXFP

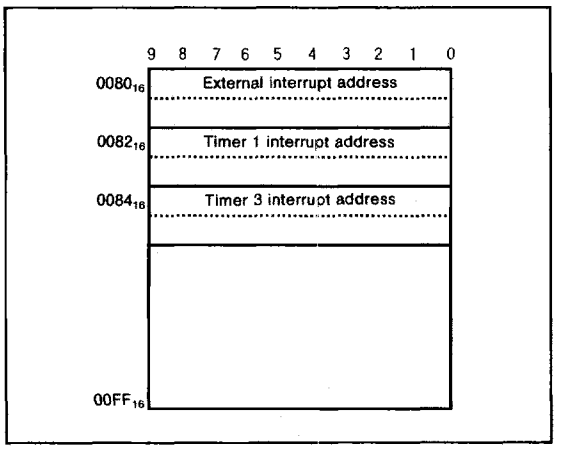


Fig. 8 Page 1 structure

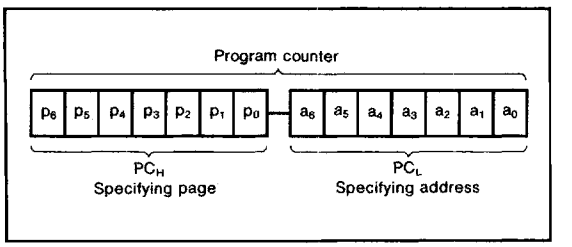


Fig. 9 Program counter structure

DATA MEMORY (RAM)

1 word of RAM is composed of 4 bits, but 1-bit manipulation (with the SB j, RB j, and SZB j instructions) is enabled for the entire memory area. A RAM address is specified by a data pointer. The data pointer consists of registers Z, X, and Y. Set a value to the data pointer certainly when executing an instruction to access RAM.

Table 2 RAM size

Product	RAM size
M34550M4A	368 words×4 bits (1472 bits)
M34550M6A	
M34550M8A/E8	

The RAM includes the area corresponding to the LCD. A segment is turned on automatically when "1" is written in the bit corresponding to the segment.

DATA POINTER (DP)

Data pointer (DP) is used to specify a RAM address and consists of registers Z, X, and Y. Register Z specifies a RAM file group, register X specifies a file, and register Y specifies a RAM digit.

Register Y is also used to specify the port D bit position. Set the value to register Y certainly when using port D.

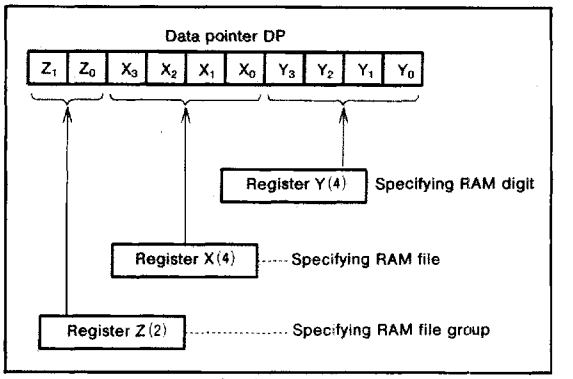


Fig. 10 Data pointer (DP) structure

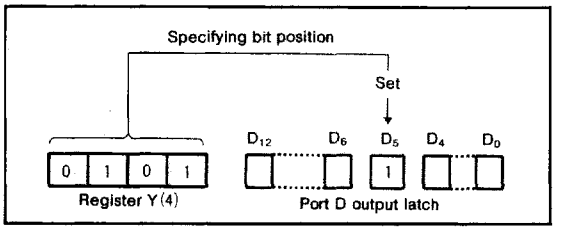


Fig. 11 SD instruction execution example

RAM 368 words×4 bits (1472 bits)

	Register Z	0				1								
	Register X	0	1	···	15	0	···	3	4	5	6	7	8	9
Register Y	0								—	—	—	—	—	—
	1								—	—	—	—	—	—
	2								—	—	—	—	—	—
	3								—	—	—	—	—	—
	4								—	—	—	—	—	—
	5								—	—	—	—	—	—
	6								—	—	—	—	—	—
	7								—	—	—	—	—	—
	8								0	8	16	24	32	
	9								1	9	17	25	33	
	10								2	10	18	26	34	
	11								3	11	19	27	35	
	12								4	12	20	28	36	
	13								5	13	21	29	37	
	14								6	14	22	30	38	
	15								7	15	23	31	39	

Notes 1. The area marked "—" (Z=1, X=4 to 9, Y=0 to 7) is not a memory area.
2. The numbers in the shaded area represent the corresponding segment output pin numbers.

Fig. 12 RAM map

INTERRUPT FUNCTION

The interrupt type is a vectored interrupt branching to an individual address (interrupt address) according to each interrupt source. An interrupt occurs when the following 3 conditions are satisfied.

- An interrupt activated condition is satisfied (interrupt request flag="1")
- Interrupt enable bit is enabled ("1")
- Interrupt enable flag is enabled (INTE="1").

Table 3 shows the interrupt sources. (Refer to each interrupt request flag for details of activated conditions.)

(1) Interrupt enable flag (INTE)

The interrupt enable flag (INTE) controls whether the every interrupt enable/disable. Interrupts are enabled when INTE flag is set to "1" with the EI instruction and disabled when INTE flag is cleared to "0" with the DI instruction. When any interrupt occurs, the INTE flag is automatically cleared to "0", so that other interrupts are disabled until the EI instruction is executed.

(2) Interrupt enable bit

Occurrence of each interrupt can be controlled with software. When an interrupt is not used, its corresponding skip instruction examines whether the interrupt activated condition is satisfied (whether the interrupt request flag="1") or not. Use an interrupt enable bit to select the corresponding interrupt or skip instruction.

(3) Interrupt request flag

When the activated condition for each interrupt is satisfied, the corresponding interrupt request flag is set to "1". Each interrupt request flag is cleared to "0" when either;

- an interrupt occurs, or
- the next instruction is skipped with a skip instruction.

Each interrupt request flag is set when the activated condition is satisfied even if the interrupt is disabled by the interrupt enable flag (INTE) or its interrupt enable bit. Once set, the interrupt request flag retains set until a reset condition is satisfied.

Accordingly, an interrupt occurs when the interrupt disable state is released while the interrupt request flag is set. If more than one interrupt request flag is set when interrupt disable state is released, the interrupt priority level is as follows shown in Table 3.

Table 3 Interrupt sources

Priority level	Interrupt name	Activated condition	Interrupt address
1	External interrupt	Level change of INT pin ("H"→"L" and "L"→"H")	Address 0 in page 1
2	Timer 1 interrupt	Timer 1 underflow	Address 2 in page 1
3	Timer 3 interrupt	Timer 3 underflow	Address 4 in page 1

Table 4 Interrupt enable bit and skip instruction

Interrupt name	Request flag	Enable bit	Skip instruction
External interrupt	EXF0	$V1_0$	SNZ0
Timer 1 interrupt	T1F	$V1_1$	SNZT1
Timer 3 interrupt	T3F	$V1_2$	SNZT3

Table 5 Interrupt enable bit function

Interrupt enable bit	Occurrence of interrupt	Skip instruction
1	Enabled	Invalid
0	Disabled	Valid

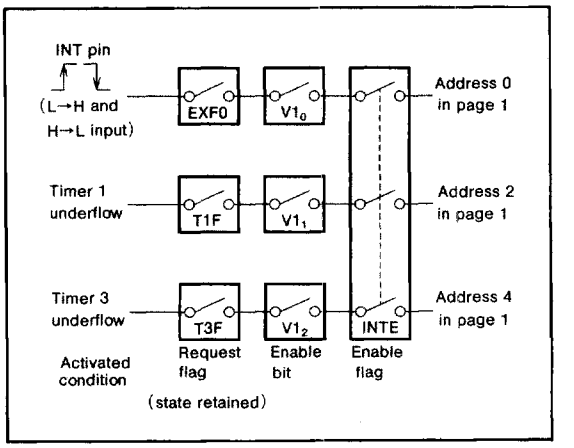


Fig. 13 Interrupt system diagram

(4) Internal state during an interrupt

The internal state of the microcomputer during an interrupt is as follows.

- Program counter (PC)
  An interrupt address is set in program counter. The address to be executed when returning to the main routine is automatically stored in the stack register (SK).
- Interrupt enable flag (INTE)
  INTE flag is cleared to "0" so that interrupts are disabled.
- Interrupt request flag
  Only the request flag for the current interrupt source is cleared to "0".
- Data pointer, carry flag, skip flag, registers A and B
  The contents of these registers and flags are stored in the interrupt stack register (SDP).

(5) External interrupt request flag (EXF0)

EXF0 flag is set to "1" when either a rising edge ("L"→"H") or a falling edge ("H"→"L") is input to $P3_0$/INT pin. However, both levels before the change and after of an waveform for an interrupt activated condition must be retained 4 periods or more (2.5μs at 1.6MHz system clock frequency) of a signal used as the system clock in order for an interrupt activated condition to be satisfied. (Refer to Fig.15)

The state of EXF0 flag can be examined with the skip instruction (SNZ0). Use the interrupt control register (V1) to select the interrupt or the skip instruction. This flag is cleared to "0" when the interrupt occurs or when the next instruction is skipped with the skip instruction.

$P3_0$/INT pin need not be selected the input port $P3_0$ function or an external interrupt input pin INT function. However, EXF0 flag is set to "1" when a condition for setting EXF0 flag is satisfied (waveform which is the external interrupt activated condition is input) even if this pin is used as the input port $P3_0$.

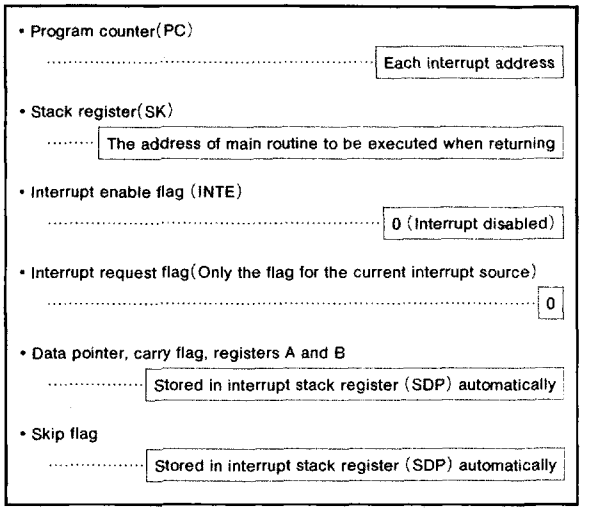
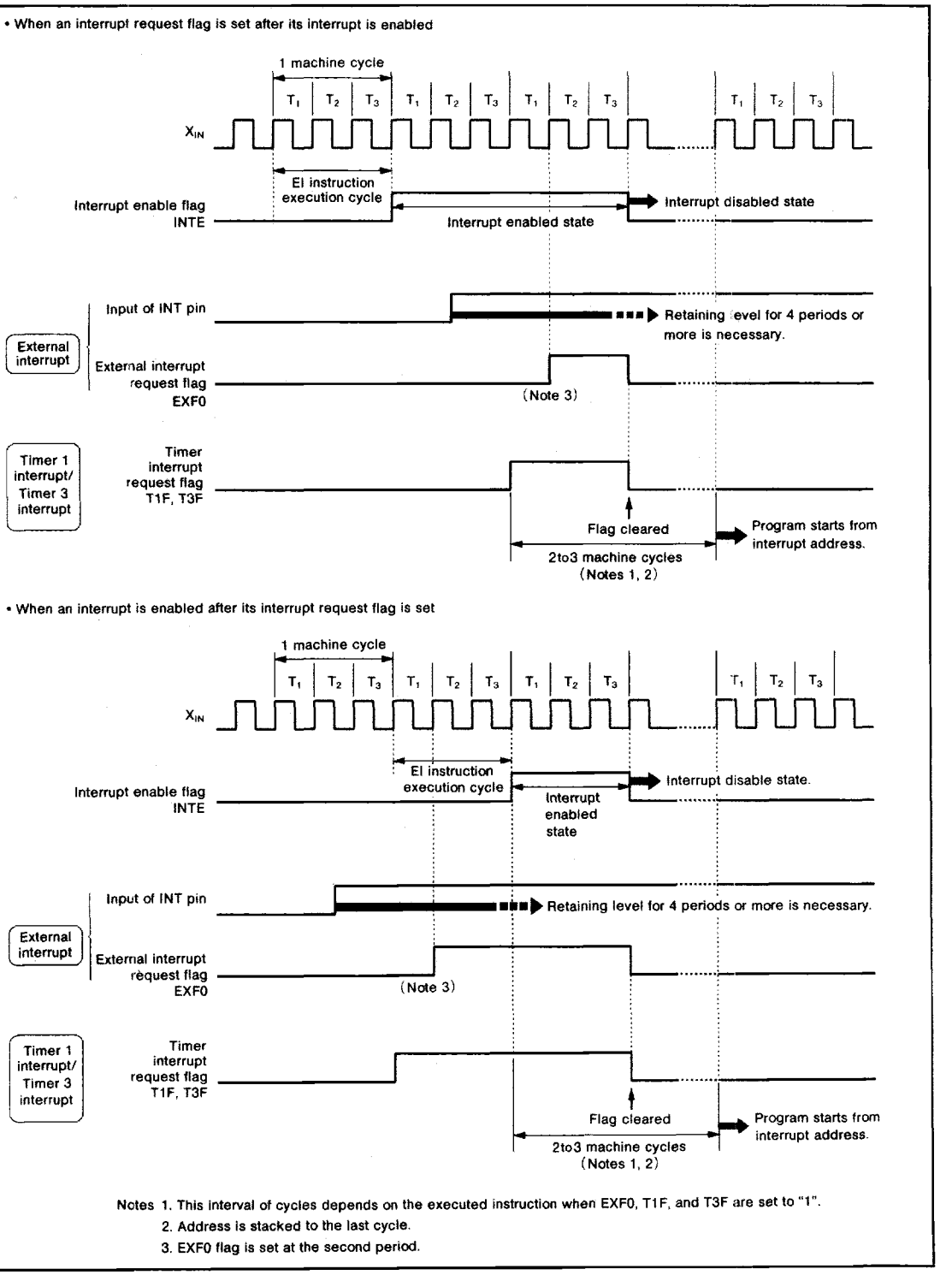


Fig. 14 Internal state when interrupt occurs



Notes 1. This interval of cycles depends on the executed instruction when EXF0, T1F, and T3F are set to "1".
2. Address is stacked to the last cycle.
3. EXF0 flag is set at the second period.

Fig. 15 Interrupt sequence

(6) Interrupt control register

• Interrupt control register (V1)

The interrupt enable bit is assigned to register V1. Set the contents of this register through register A with the TV1A instruction. The TAV1 instruction can be used to transfer the contents of register V1 to register A.

(7) Interrupt processing

When an interrupt occurs, a program at an interrupt address is executed after branching a data store sequence to stack register. Write the branch instruction to an interrupt service routine at an interrupt address.

Use the RTI instruction to return from an interrupt service routine. Interrupt enabled by executing the EI instruction is performed after executing 1 instruction (just after the next instruction is executed). Accordingly, when the EI instruction is executed just before the RTI instruction, interrupts are enabled just after returning the main routine. (Refer to Fig.16)

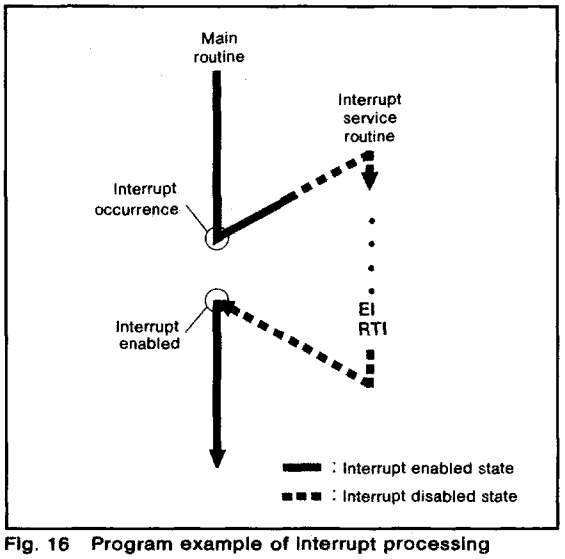


Fig. 16 Program example of interrupt processing

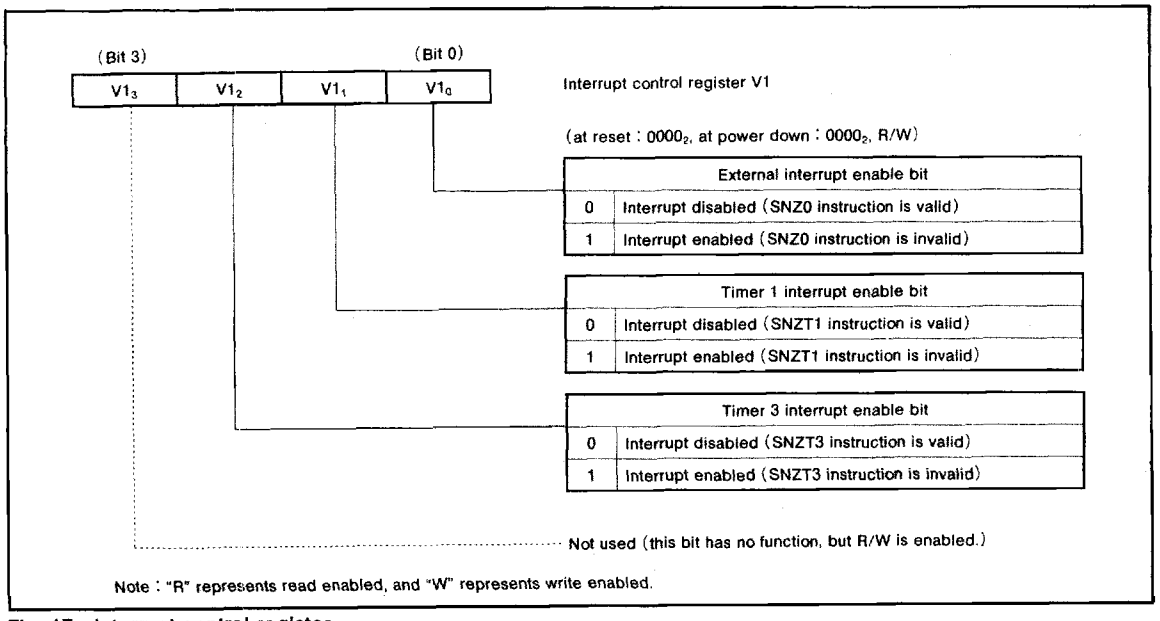


Fig. 17 Interrupt control register

TIMERS

The 4550 Group has 2-type timers. One is a programmable timer, and the other is a fixed dividing frequency timer.

- Programmable timer

  The programmable timer has a reload register and enables the frequency dividing ratio to be set. It is decremented from the setting value n. When it underflows (count to n+1), a timer interrupt request flag is set to "1", new data is loaded from the reload register, and count continues (auto-reload function).

- Fixed dividing frequency timer

  A fixed dividing frequency timer has a fixed frequency dividing ratio (n). The underflow flag is set to "1" after every n count of the count pulse.

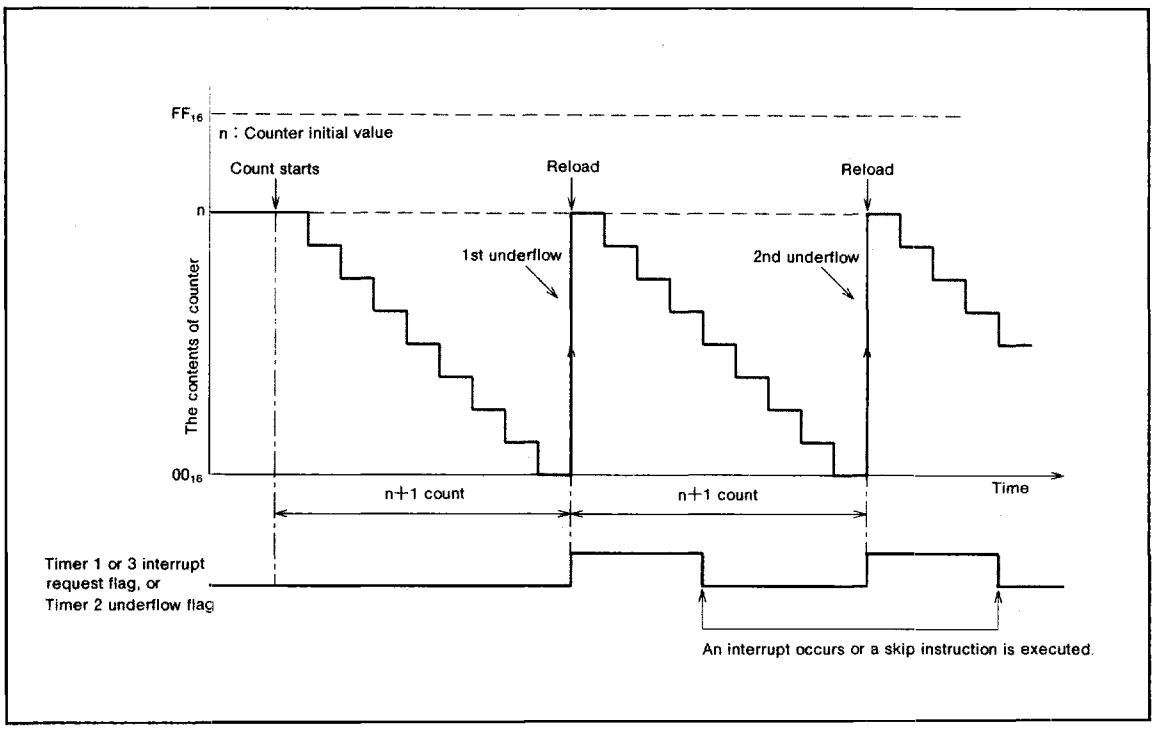


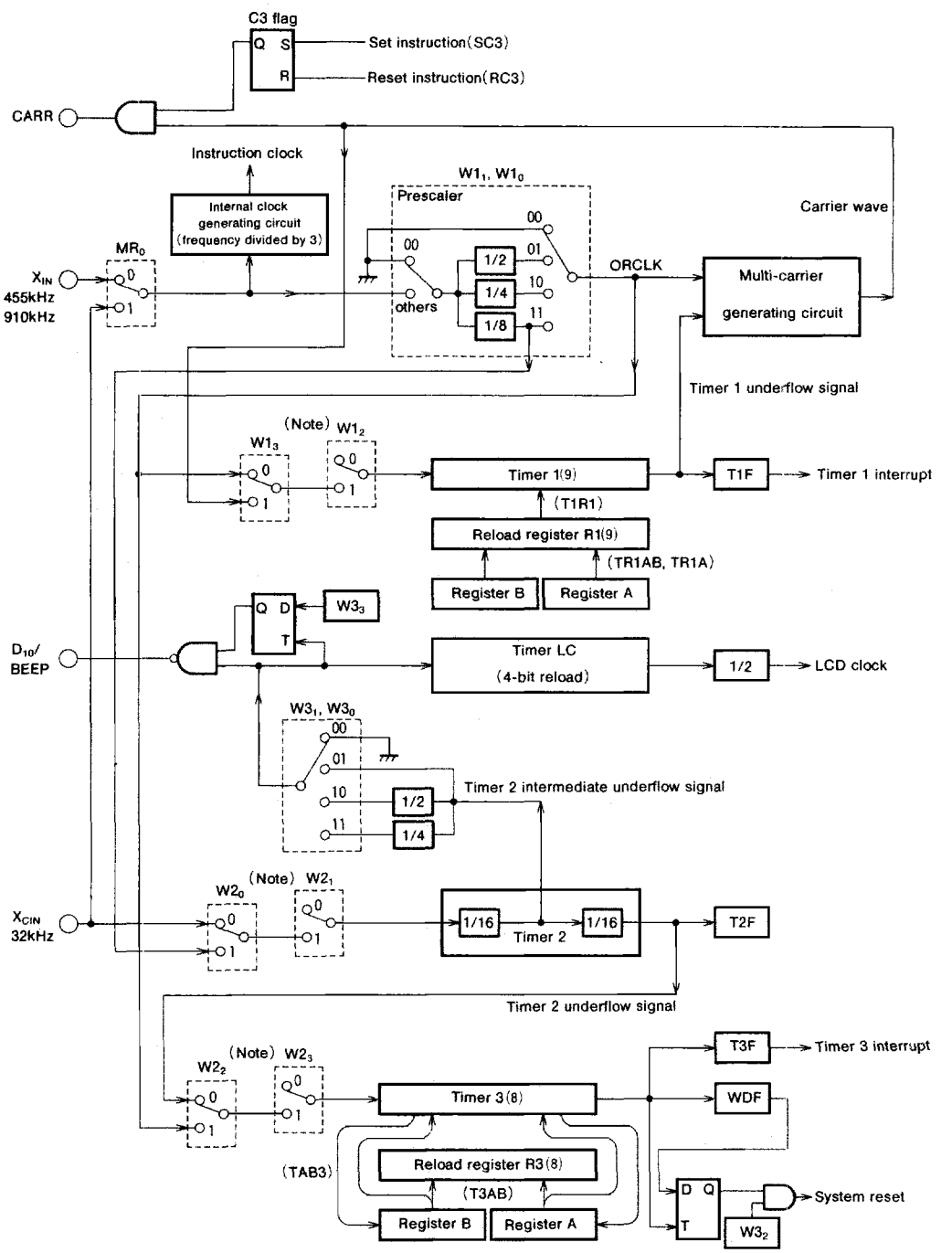
Fig. 18 Auto-reload function

The 4550 Group timer consists of the following circuits.
- Prescaler : frequency divider
- Timer 1 : 9-bit programmable timer (with interrupt function)
- Timer 2 : 8-bit fixed dividing frequency timer
- Timer 3 : 8-bit programmable timer (with interrupt function)
- Watchdog timer
- Buzzer drive output
- Frequency divider for LCD

These timers can be controlled with the timer control registers (W1 to W3). Each function is described below.

Table 6 Function related timers

Circuit	Structure	Count source	Frequency dividing ratio	Use of output signal	control
Prescaler	Frequency divider	• $f(X_{IN})$ or $f(X_{CIN})$	2, 4, 8	• Timer 1 and 3 count sources • Multi-carrier generating circuit	W1
	(Frequency divider (divide by 8))		(8)	• Timer 2 count source	
Timer 1	9-bit programmable binary down counter	• Prescaler output (ORCLK) • Multi-carrier output (CARR)	1 to 512	• Multi-carrier generating circuit • Timer 1 interrupt	
Timer 2	8-bit fixed dividing frequency binary down counter	• $f(X_{CIN})$ • Prescaler output (Frequency divided by 8 output)	256	• Timer 3 count source	W2
	(Frequency divider (divide by 16))		(16)	• Buzzer drive output • Frequency divider for LCD	
Timer 3	8-bit programmable binary down counter	• Timer 2 underflow • Prescaler output (ORCLK)	1 to 256	• Watchdog timer • Power down 1 return • Timer 3 interrupt	
Watchdog timer	Timer 3	• Timer 3 underflow		• System reset	W3
Buzzer drive output	Frequency divider	• Timer 2 intermediate underflow (Frequency divided by 16 output)	1, 2, 4		
Frequency divider for LCD	Frequency divider (divide by 1, 2, 4) +4-bit counter +frequency divider (divide by 2)	• Timer 2 intermediate underflow (Frequency divided by 16 output)	2(n+1), 4(n+1), 8(n+1) [n=0 to 15]	• LCD controller/driver	



Note : The count source stops by setting to "0".

Fig. 19 Timers structure

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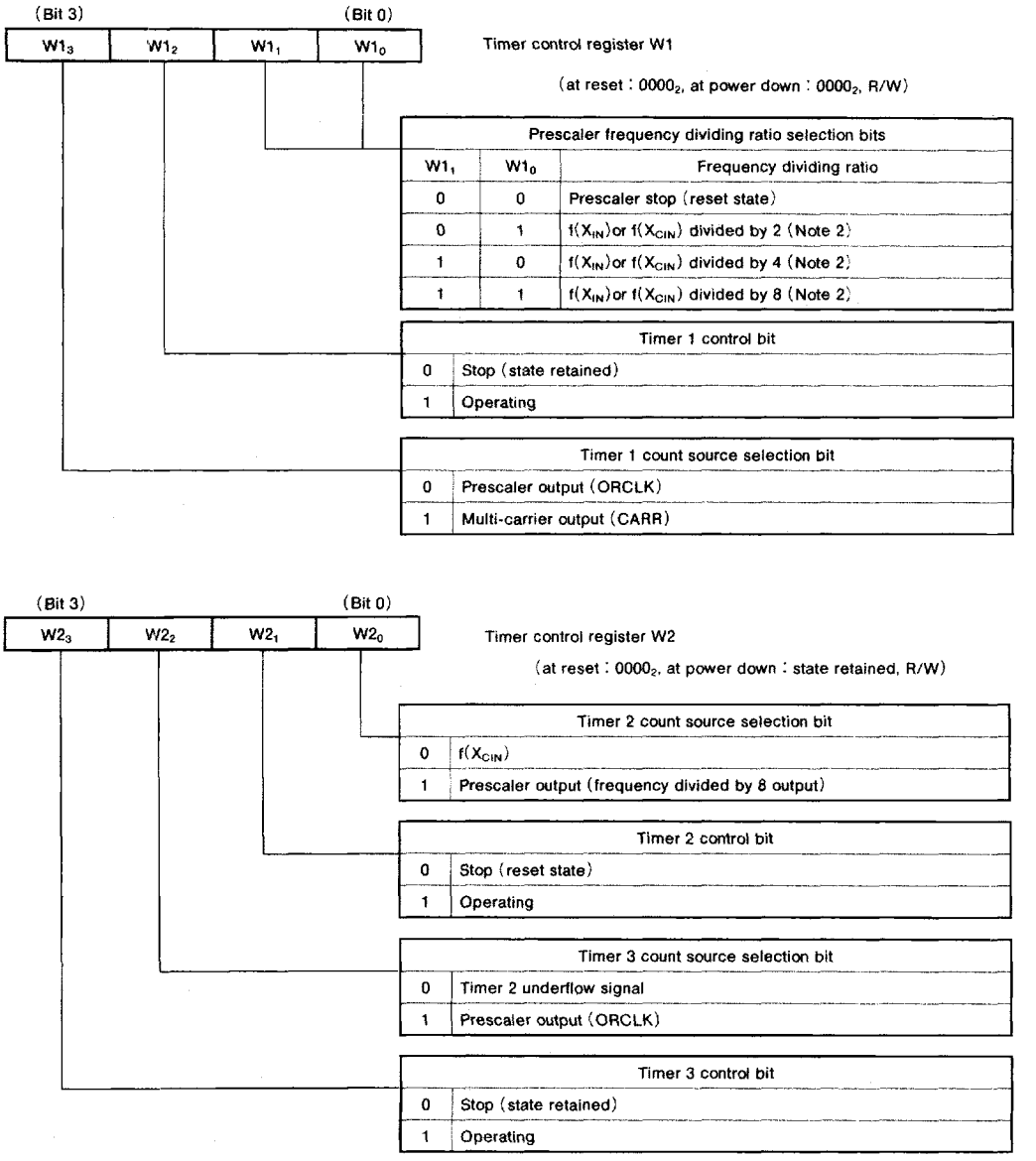
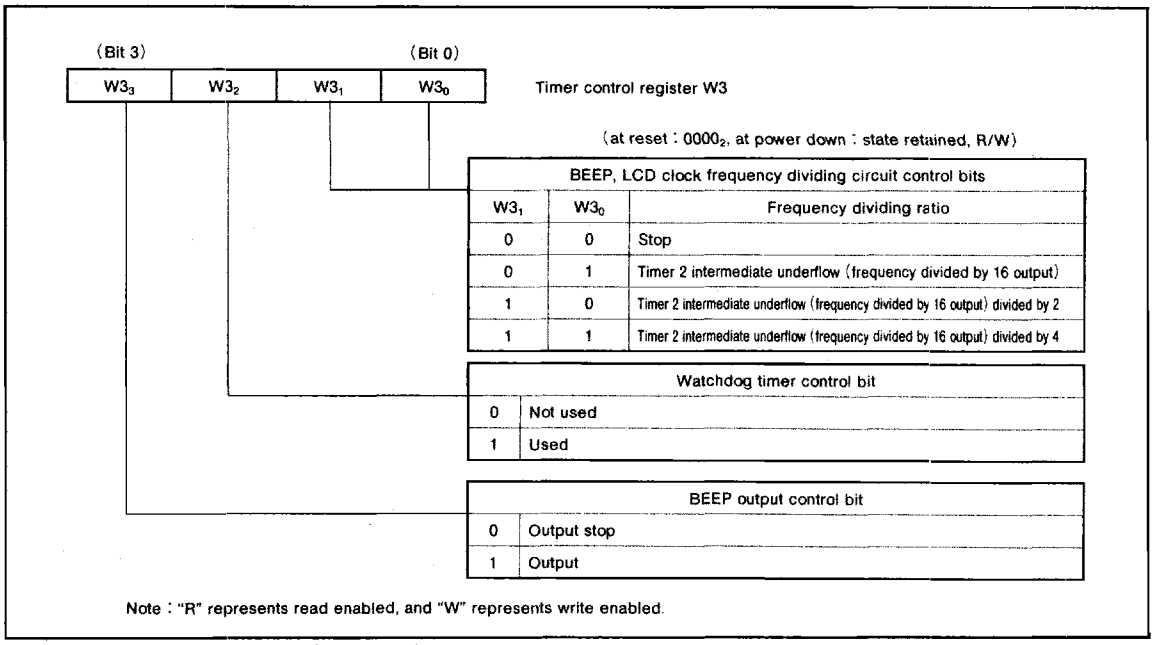


Notes 1. "R" represents read enabled, and "W" represents write enabled.
2. The signal in f(XIN) or f(XCIN) selected as a system clock is used.

Fig. 20 Timer control register



Note : "R" represents read enabled, and "W" represents write enabled.

Fig. 21 Timer control register (continued)

(1) Prescaler

Prescaler is a frequency divider. Its frequency dividing ratio can be selected. Prescaler outputs 2 signals (ORCLK and frequency divided by 8 as signal). Prescaler count source is $f(X_{IN})$ or $f(X_{CIN})$ which is a signal selected as a system clock with the register MR.

Use bits 0 and 1 of the register W1 to select the prescaler dividing ratio and to start and stop its operation. Prescaler is reset state, and the ORCLK and frequency divided by 8 as signal output stop when both bits 0 and 1 of the register W1 are cleared to "0".

(2) Timer 1 (with the interrupt function)

Timer 1 is a 9-bit binary down counter with timer 1 reload register (R1). To set data in timer 1, first set data in reload register R1 (TR1AB instruction, TR1A instruction) and then transfer it from the reload register R1 to timer 1 (T1R1 instruction). Timer 1 starts counting when data is set in timer 1, count source is selected with bit 3 of the register W1, and bit 2 is set to "1".

Once count is started, when timer 1 underflows (the next count pulse is input after the contents of timer 1 becomes "0"), the timer 1 interrupt request flag (T1F) is set to "1", new data is loaded from the reload register R1, and count continues (auto-reload function). When the value set in reload register R1 is n, timer 1 divides the count source signal by n+1 (n=0 to 511).

When writing data to reload register R1, be sure the timing when timer 1 does not underflow.

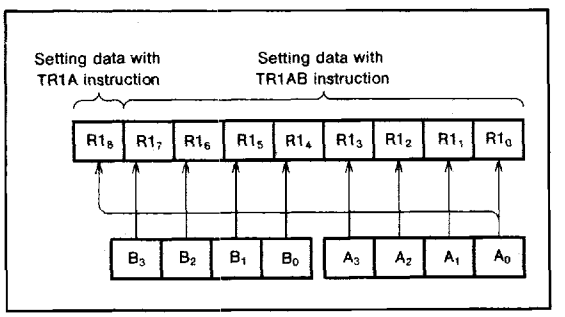


Fig. 22 Setting example of register R1

(3) Timer 2

Timer 2 is an 8-bit binary down counter. Timer 2 starts counting when the count source is selected with bit 0 of the register W2 and bit 1 is set to "1". The timer 2 underflow flag (T2F) is set to "1" at every 256 count of the count source.

Timer 2 outputs both count source divided by 16 (intermediate underflow) as a signal and count source divided by 256 (underflow) as a signal. Timer 2 is cleared and both count source divided by 16 and 256 outputs stop when bit 1 of the register W2 is cleared to "0".

Timer 2 can be used as clock counter during power down 1 state (executing the POF instruction).

(4) Timer 3 (with the interrupt function)

Timer 3 is an 8-bit binary down counter with timer 3 reload register (R3). Data can be set simultaneously in reload register R3 and timer 3 with the T3AB instruction. Timer 3 starts counting when data is set in timer 3, count source is selected with bit 2 of the register W2, and bit 3 is set to "1".

Once count is started, when timer 3 underflows (the next count pulse is input after the contents of timer 3 becomes "0"), the timer 3 interrupt request flag (T3F) is set to "1", new data is loaded from the reload register R3, and count continues (auto-reload function). When the value set in reload register R3 is n, timer 3 divides the count source signal by n+1 (n=0 to 255).

The TAB3 instruction can be used to read the data in timer 3. Stop the counter before executing the TAB3 instruction to read the data. Timer 3 can be used as the clock counter during power down 1 state (executing the POF instruction).

(5) Watchdog timer

Watchdog timer provides a method to reset the system when a program runs wild. The watchdog timer consists of timer 3 and watchdog timer flag (WDF). When a timer 3 underflow signal occurs, the WDF flag is set to "1". When the timer 3 underflows once more while the WDF flag is set, the watchdog timer forces a system reset (operationally the same that power-on reset). Whether to use watchdog timer or not can be set with the bit 2 of the register W3. When using the watchdog timer, be sure to clear the WDF flag to "0" with the WRST instruction with a program before timer 3 underflows again. In order to effectively use watchdog timer, do not execute the WRST instruction during timer 3 interrupt.

(6) Buzzer drive output

The D_{10}/BEEP pin has a buzzer drive output function. The output signal can be selected from the timer 2 intermediate underflow signal (frequency divided by 16 output) undivided, divided by 2 or 4. Select the frequency dividing ratio with bits 0 and 1 of the register W3. Signal start/stop can be controlled with bit 3 of the register W3.

When using the D_{10}/BEEP pin as buzzer drive output, set the D_{10} output latch to "1".

(7) Frequency divider for LCD

The frequency divider for the LCD consists of timer LC and frequency divider (divide by 2). Timer LC is a 4-bit programmable timer with reload latch. Data can be set simultaneously in the reload latch and timer LC with the TLCA instruction. The timer LC count source can be selected from the timer 2 intermediate underflow signal (frequency divided by 16 output) undivided, divided by 2 or 4.

Timer LC starts counting when data is set in timer LC and the count source is selected with bits 0 and 1 of the register W3. When it underflows, data is loaded from the reload latch and count continues. When the value set in timer LC is n, the count source is divided by n+1 (n=0 to 15).

The timer LC underflow signal divided by 2 becomes the standard clock of the LCD.

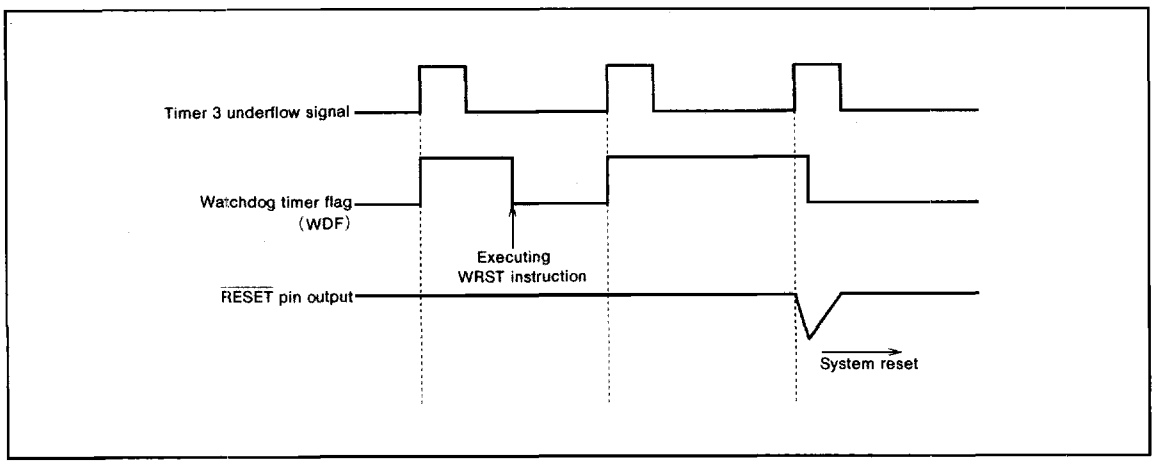


Fig. 23 Watchdog timer function

(8) Timer interrupt request flags (T1F and T3F)

The timer 1 interrupt request flag (T1F) is set to "1" when timer 1 underflows, and the timer 3 interrupt request flag (T3F) is set to "1" when timer 3 underflows. The states of these flags can be examined with the skip instructions (SNZT1 and SNZT3). Use the interrupt control register (V1) to select an interrupt or a skip instruction.

An interrupt request flag is cleared to "0" when an interrupt occurs or when the next instruction is skipped with a skip instruction.

(9) Underflow flag (T2F)

The timer 2 underflow flag (T2F) is set to "1" each time timer 2 underflows (every 256 count). The state of this flag can be examined with the skip instruction (SNZT2 instruction). The T2F flag is cleared to "0" only when the next instruction is skipped with the skip instruction.

(10) Timer control registers

- Timer control register (W1)

Register W1 controls the prescaler, the count operation and count source for timer 1. Set the contents of this register with the TW1A instruction through register A. The TAW1 instruction can be used to transfer the contents of register W1 to register A.

- Timer control register (W2)

Register W2 controls the count operations and count sources for timer 2 and timer 3. Set the contents of this register with the TW2A instruction through register A. The TAW2 instruction can be used to transfer the contents of register W2 to register A.

- Timer control register (W3)

Register W3 controls the watchdog timer, buzzer drive output, and the frequency divider for the LCD. Set the contents of this register with the TW3A instruction through register A. The TAW3 instruction can be used to transfer the contents of register W3 to register A.

(11) Precautions

Note the following when using a timer.

- Prescaler precautions

Stop the prescaler to change its frequency dividing ratio.

- Timer precautions

Stop timer 1, 2, or 3 counting to change its count source, as well as to execute the TAB3 instruction for reading the data (from timer 3).

- D_{10}/BEEP pin precautions

To use the buzzer drive output function, set the frequency (bits 0 and 1 of the register W3) and then start output. When changing the buzzer drive output frequency or switching this pin as port D_{10} function, first stop the buzzer drive output, wait for 1 cycle of the buzzer drive output, and then set the frequency or start using as port D_{10}.

MULTI-CARRIER GENERATING CIRCUIT

The 4550 Group is equipped with the multi-carrier generating circuit to generate transmission waves for the remote control carrier wave. This circuit automatically generates a carrier wave compensated at constant period by setting data in the carrier wave data control register (C1), carrier wave compensation control register (C2), preset register (PA_0—PA_3), and compensation control timer (PT). When a waveform not obtainable with this method is necessary, the "H" or "L" interval of the carrier wave and the compensation can be controlled at your option by generating the wait interval until the set instruction and reset instruction (SC4, RC4) are executed with software.

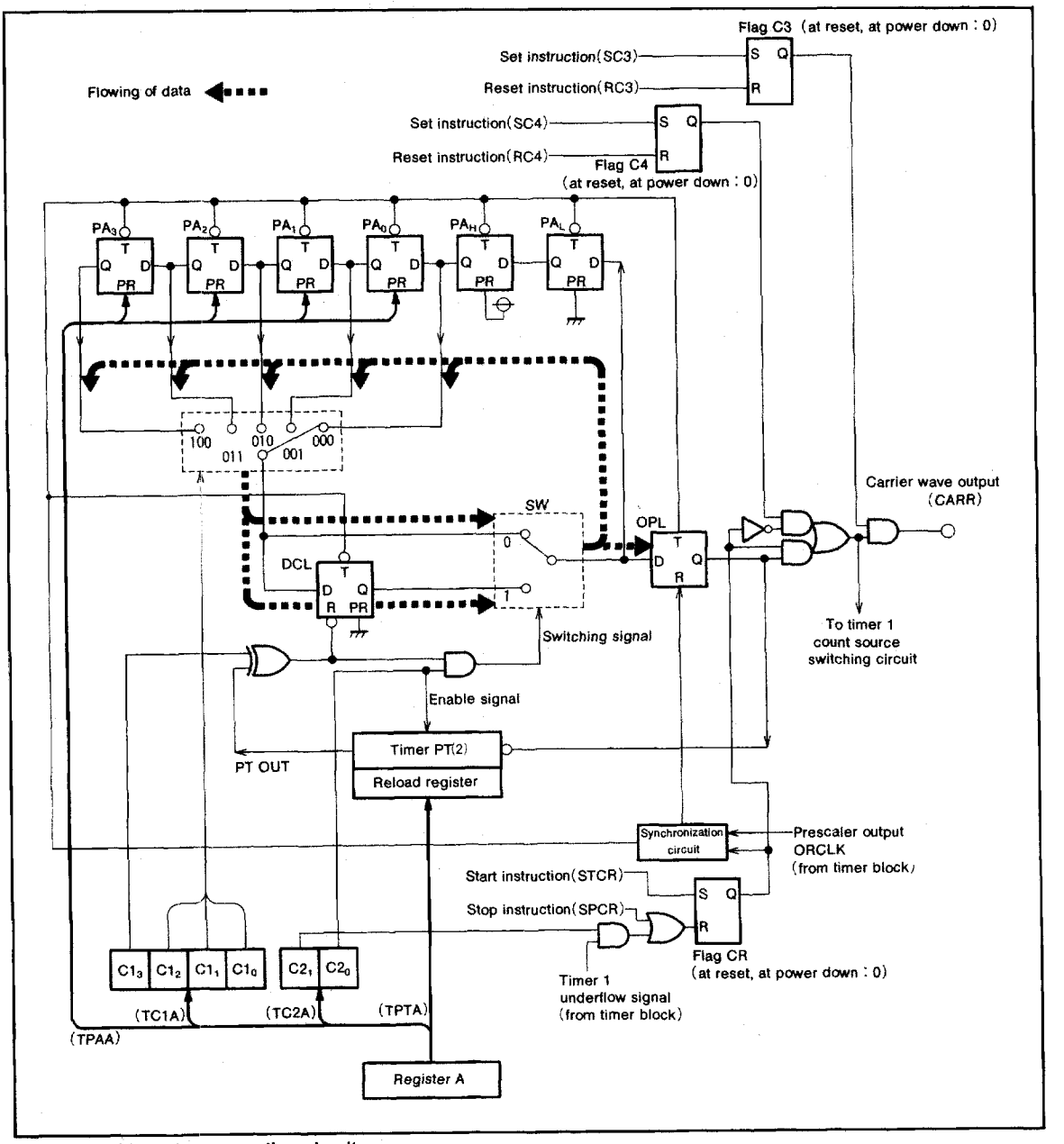
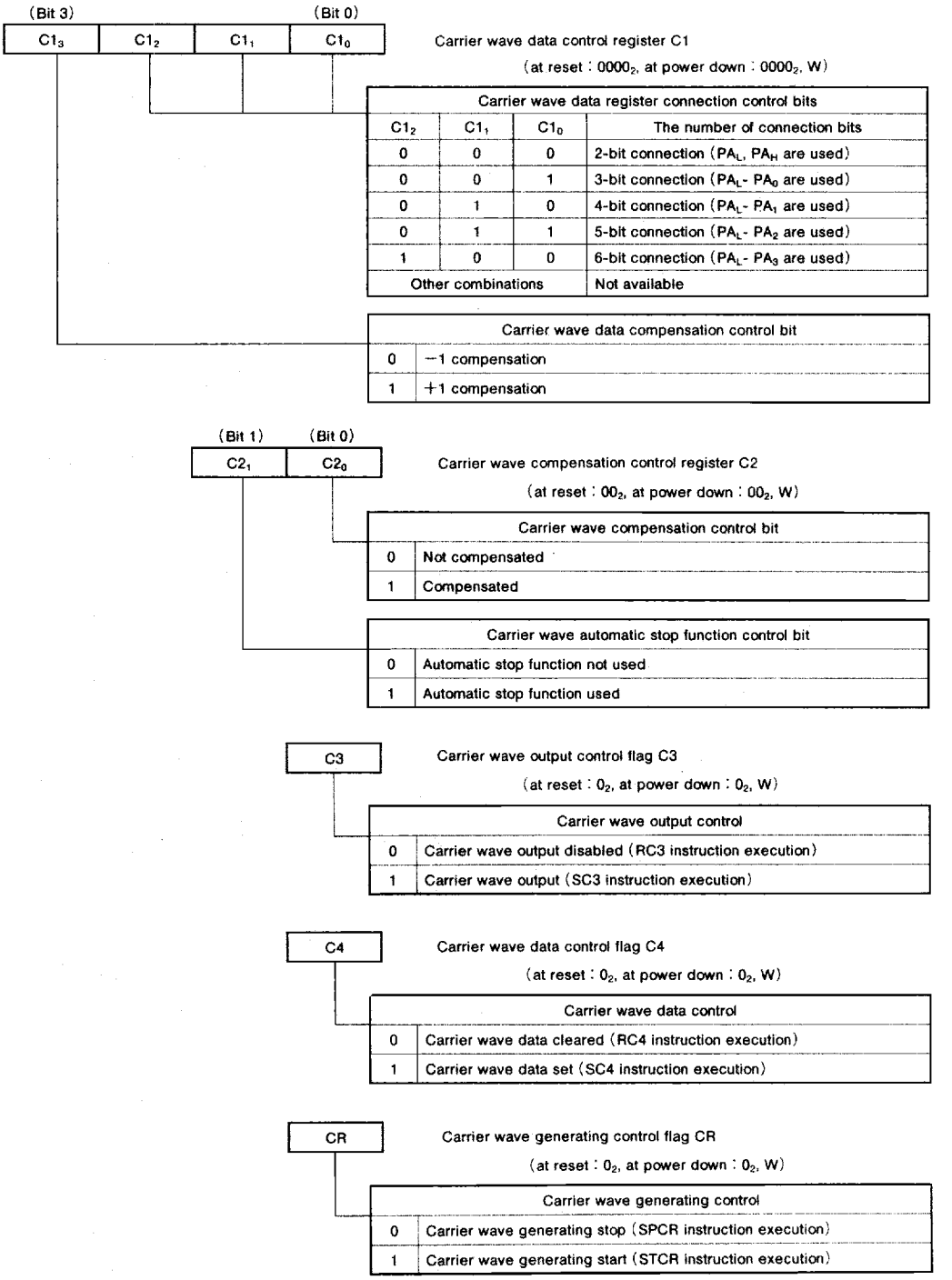


Fig. 24 Multi-carrier generating circuit



Note : "W" represents write enabled.

Fig. 25 Multi-carrier generating circuit control register and control flag

(1) Multi-carrier generating circuit operation

The carrier wave is compensated by +1 compensation or −1 compensation. Assuming the interval between the rise of the reference clock (ORCLK) input through the synchronization circuit and the next rise is 1T :

+1 compensation : extends the "L" interval by 1T at constant period.

−1 compensation : reduces the "L" interval by 1T at constant period.

The operation of the multi-carrier generating circuit is described below with examples for +1 compensation and −1 compensation (refer to Fig. 24).

●+1 compensation example

[Output waveform]

- Basic waveform : "H" interval=2T
  "L" interval=2T
- Compensation period : once every 2 period (+1 compensation)

[Initial setting value]

- Carrier wave data control register
  $C1_3$−$C1_0$=$(1010)_2$
- Carrier wave compensation control register
  $C2_1$, $C2_0$=$(01)_2$
- Preset register PA_3−PA_0
  Initial value=$(XX01)_2$
- Compensation control timer PT
  Initial value=$(1)_{16}$

X : Set the arbitrary value (this bit is not related the waveform setting in this example).

In this case, the shift operation is PA_L→PA_H→PA_0→PA_1 because the carrier wave data register (PA) is set to 4-bit connection. In addition, the data compensation latch (DCL) stops at reset state when the timer PT output (PT OUT) is "H" and operates when it is "L" because $C1_3$ is set to "1".

ORCLK is input to the multi-carrier generating circuit with the STCR instruction and register PA shift operation starts. At this time, DCL stops at reset state and disconnected from register PA because timer PT outputs initial level "H". Accordingly, PA_1 output is input to output latch (OPL) and is output as the carrier wave (CARR) after T/2. This is the basic waveform.

When timer PT underflows and PT OUT changes to "L", DCL reset is released and connected to the top bit of register PA. This causes the shift operation PA_L→PA_H→PA_0→PA_1→DCL. Accordingly, the DCL output is input to OPL and the "L" interval becomes longer than the basic waveform by 1T. This is the waveform of compensated period.

When the next fall of the carrier wave occurs, PT OUT returns to "H", DCL is disconnected, and a basic waveform is output. The carrier waveform is stopped with the SPCR instruction because $C2_1$ is cleared to "0".

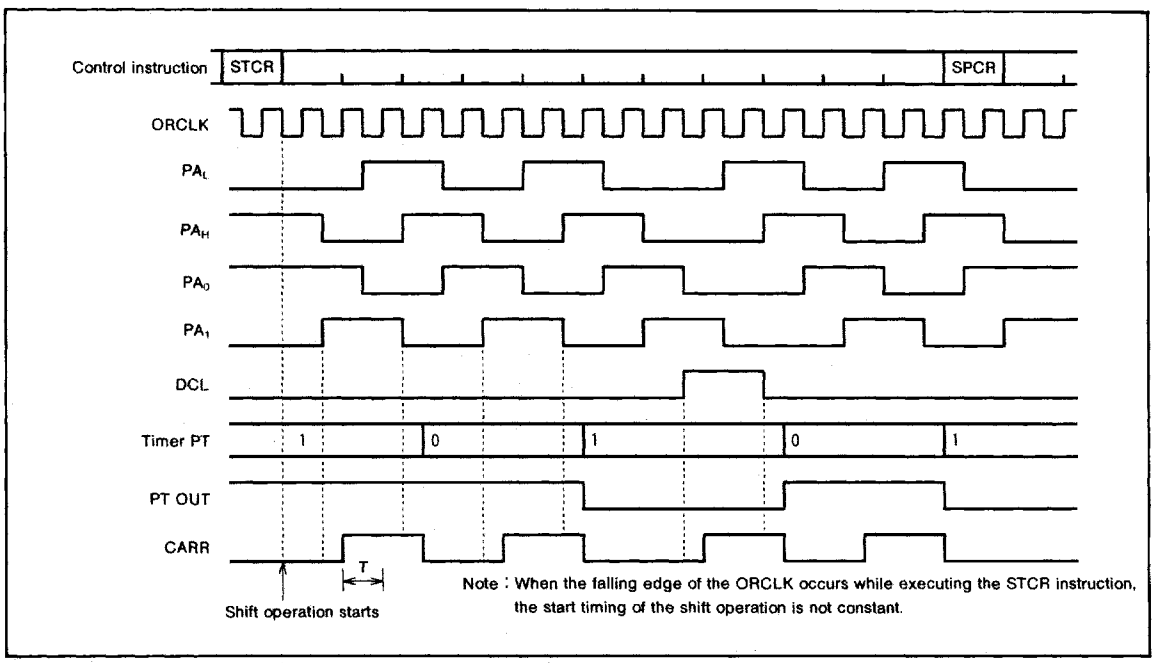


Fig. 26 Timing diagram at +1 compensation

● −1 compensation example

[Output waveform]

- Basic waveform : "H" interval=2T
  "L" interval=2T
- Compensation period : once every 2 period
  (−1 compensation)

[Initial setting value]

- Carrier wave data control register
  $C1_3$−$C1_0$=$(0001)_2$
- Carrier wave compensation control register
  $C2_1$, $C2_0$=$(01)_2$
- Preset register PA_3−PA_0
  Initial value=$(XXX1)_2$
- Compensation control timer PT
  Initial value=$(1)_{16}$

X : Set the arbitray value (this bit is not related the waveform setting in this example).

In this case, the shift operation is PA_L→PA_H→PA_0 because the carrier wave data register (PA) is set to 3-bit connection. In addition, the data compensation latch (DCL) operates when the timer PT output (PT OUT) is "H" and stops at reset state when it is "L" because $C1_3$ is cleared to "0".

ORCLK is input to the multi-carrier generating circuit with the STCR instruction and register PA shift operation starts. At this time, DCL operates and is connected to the top bit of register PA because timer PT outputs initial level "H". Accordingly, DCL output is input to output latch (OPL) and is output as the carrier wave (CARR) after T/2 because shift operation PA_L→PA_H→PA_0→DCL is performed. This is the basic waveform.

When timer PT underflows and PT OUT changes to "L", DCL stops at reset state and is disconnected from register PA opposite of +1 compensation. Accordingly, the PA_0 output is input to OPL and the "L" interval becomes shorter than the basic waveform by 1T. This is the waveform of compensated period.

When the next fall of the carrier wave occurs, PT OUT becomes "H" and the basic waveform is output. The carrier waveform is stopped with the SPCR instruction because $C2_1$ is cleared to "0".

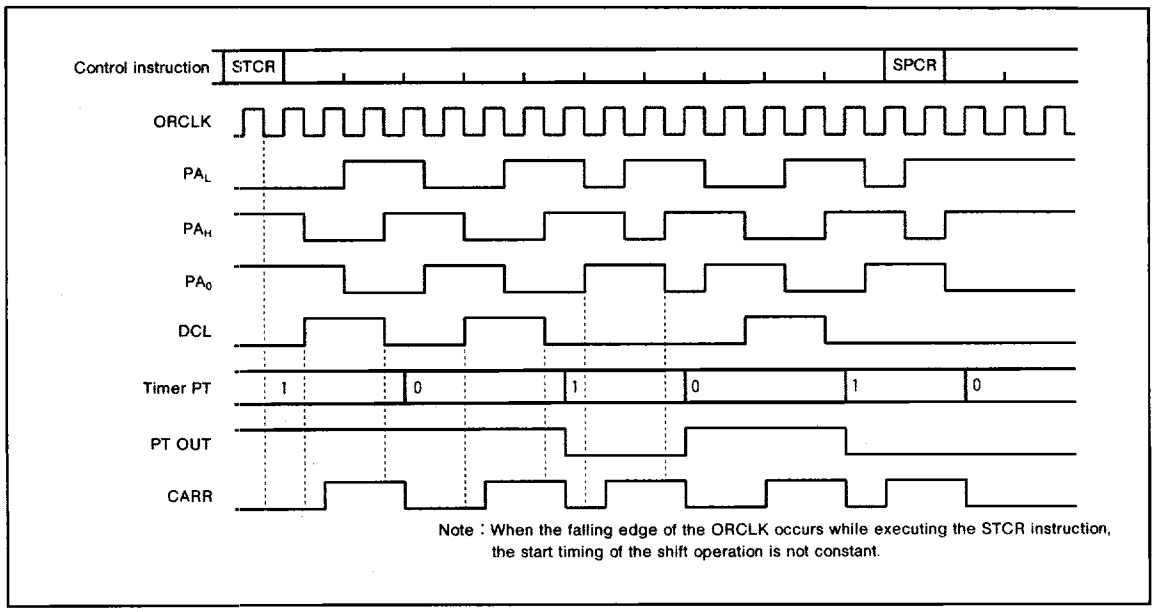


Fig. 27 Timing diagram at −1 compensation

(2) Preset register (PA_0—PA_3)

Preset register is the top 4 bits of the carrier wave data register (PA) which consists of a 6-bit shift register. The waveform of the carrier wave is determined by the number of connection bits of this register and the preset value.

Set the number of connection bits of preset register with bits 0 to 2 of the carrier wave data control register (C1), and the preset value with the TPAA instruction through register A. Set so that the waveform generated by the carrier wave data register (PA) is 1 period (both "H" and "L" are one interval).

(3) Compensation control timer (PT)

Timer PT is a 2-bit programmable timer and is used to determine the compensation period of the carrier wave. The initial level of the timer PT output (PT OUT) is "H". Timer PT down counts the fall of the carrier wave ("H" → "L"). An underflow occurs and PT OUT changes to "L" at the fall of the carrier wave after it becomes "0". Then the initial value is reloaded into timer PT and count continues. The output returns to "H" next time the carrier wave falls.

The carrier wave is compensated while this PT OUT is "L" (carrier wave compensation interval). Accordingly, when the value set in timer PT is n, the carrier wave is compensated every n + 1 period. Data can be set simultaneously in timer PT and the reload register with the TPTA instruction.

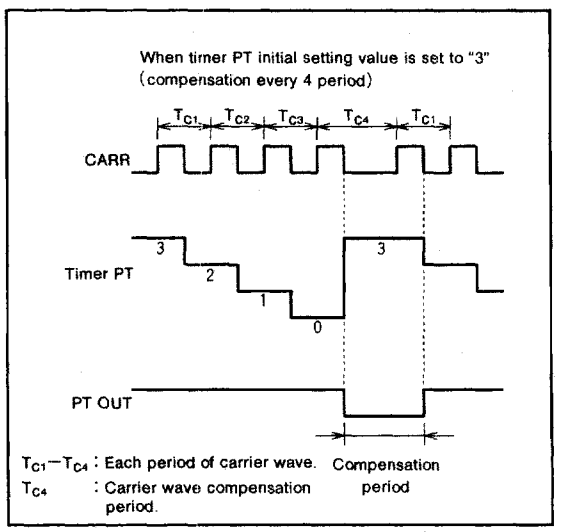


Fig. 28 Timer PT operation example

(4) Data compensation latch (DCL)

Data compensation latch is a 1-bit latch with the preset value fixed to "0". The "L" interval of the carrier wave changes depending on whether or not this latch is connected to the top bit of the shift register (register PA). The connection/disconnection of DCL is automatically controlled by timer PT output value (PT OUT).

Table 7 Timer PT output value and DCL connection state

		$C1_3$="0"	$C1_3$="1"
PT OUT	"H"	Connection	Disconnection
	"L"	Disconnection	Connection

Note : $C2_0$ is set to "1" in this table.

(5) Carrier wave control instruction

The carrier wave generation is controlled with the STCR instruction (generation start) and the SPCR instruction (generation stop). Whether to output the generated carrier wave from the CARR pin can be controlled by the SC3 instruction (output) and the RC3 instruction (output disabled).

(6) Multi-carrier generating circuit control registers and control flags

- Carrier wave data control register (C1)

Register C1 controls the number of connection bits to the carrier wave data register (PA), and the carrier wave compensation method. Set the contents of this register with the TC1A instruction through register A.

- Carrier wave compensation control register (C2)

Register C2 controls the carrier wave compensation function and the automatic stop function (stop with timer 1 underflow flag). Set the contents of this register with the TC2A instruction through register A.

- Carrier wave output control flag (C3)

C3 flag controls whether to output the generated carrier wave from the CARR pin. C3 flag is cleared to "0" and the carrier wave output is disabled when the RC3 instruction is executed, and C3 flag is set to "1" and carrier wave output is enabled when the SC3 instruction is executed.

Even if output is disabled with this flag, the carrier wave output stop interval can be counted by using timer 1 because the carrier wave generation is possible. This flag is cleared to "0" at system reset.

• Carrier wave data control flag (C4)
C4 flag controls the generation of the carrier wave which cannot be generated with the multi-carrier generating circuit. C4 flag is cleared to "0" and "L" interval of carrier wave is generated when the RC4 instruction is executed. C4 flag is set to "1" and "H" interval of carrier wave is generated when the SC4 instruction is executed. The "H" or "L" interval of the carrier wave and the compensation can be controlled at your option by generating the wait interval until the SC4 instruction and the RC4 instruction are executed with software. Stop the multi-carrier generating circuit (CR flag="0") when the carrier wave is generated by C4 flag. This flag is cleared to "0" at system reset.

• Carrier wave generating control flag (CR)
CR flag controls the operation to generate the carrier wave at the multi-carrier generating circuit. CR flag is cleared to "0" and generating the carrier wave is stopped when the SPCR instruction is executed or timer 1 underflow occurs (when $C2_1$ is set to "1"), and CR flag is set to "1" and generating the carrier wave is started when the STCR instruction is executed. This flag is cleared to "0" at system reset.

(7) Precautions
Note the following when using the multi-carrier generating circuit.

• Precaution when starting carrier wave (CARR) generation
The shift operation of the multi-carrier generating circuit starts in synchronization with the falling edge ("H" → "L") of ORCLK. However, the shift operation start timing after executing the carrier wave generation start instruction (STCR) is not constant because the instruction cycle does not match the ORCLK period.
In addition, when the falling edge of ORCLK occurs during the STCR instruction execution cycle, whether register PA starts shift operation or not is undefined. When the shift operation is not started, it is started at the falling edge of the next ORCLK. The carrier wave output timing after starting shift operation depends on the initial setting value as described in the carrier wave compensation example.

• Precaution when stopping carrier wave (CARR) generation
The carrier wave is stopped at the fall of the carrier wave. However, the carrier wave stop timing after executing the carrier wave stop instruction (SPCR) is not constant because the instruction cycle does not match the carrier wave period.
In addition, when the fall of the carrier wave occurs during the SPCR instruction execution cycle, whether the carrier wave is stopped or not is undefined. When the carrier wave is not stopped, it is stopped at the fall of the next carrier wave.
When the prescaler is to be stopped after stopping the carrier wave, wait for 1 period of ORCLK after the carrier wave has stopped, and then stop the prescaler.

• Precaution when restarting carrier wave (CARR) generation
When carrier wave generation is restarted after stopping, timer PT retains the previous value without initializing. Accordingly, be sure to set again timer PT (with the TPTA instruction) before restarting carrier wave generation (with the STCR instruction).

• Precaution when using the carrier wave (CARR) automatic stop function
Carrier wave generation can be stopped ($C2_1$ = "1") with the timer 1 underflow signal using the carrier wave as the timer 1 count source ($W1_3$="1"). In this case, it is necessary to set again timer 1 (with the T1R1 instruction) when carrier wave generation is to be restarted (with the STCR instruction) after stopping it with a timer 1 underflow signal.

LCD FUNCTION

The 4550 Group has a built-in LCD (Liquid Crystal Display) controller/driver. When proper voltage is applied to the LCD power supply input pins, and data is set in timer control registers (W2, W3), timer LC, LCD control registers (L1 to L3), and LCD RAM, the controller/driver automatically reads the display data, controls the LCD display by setting duty and bias.

4 common signal output pins and 40 segment signal output pins can be used to drive the LCD to control the display of up to 160 segments (when 1/4 duty and 1/3 bias are selected). When the required number of segment pins is 40 or less, SEG_{36}—SEG_{39} can be used as input ports $P4_0$—$P4_3$.

(1) Duty and bias

There are three combinations of duty and bias for displaying data on the LCD. Use bits 0 and 1 of the LCD control register (L1) to select the proper display method for the LCD panel being used.

- 1/2 duty, 1/2 bias
- 1/3 duty, 1/3 bias
- 1/4 duty, 1/3 bias

Table 8 Duty and maximum number of displayed pixels

Duty	Maximum number of displayed pixels	Used COM pins
1/2	80 segments	COM_0, COM_1 (Note)
1/3	120 segments	COM_0—COM_2 (Note)
1/4	160 segments	COM_0—COM_3

Note : Leave unused COM pins open.

(2) LCD clock control

The LCD clock is determined by the setting values of the timer 2 count source selection bit ($W2_0$), LCD clock frequency dividing circuit control bits ($W3_0$, $W3_1$), and timer LC. Accordingly, the frequency (F) of the LCD clock is obtained by the following formula. The number (① to ⑥) shown under formula corresponds to Fig.29

- When using the prescaler output (frequency divided by 8 output)as timer 2 count source ($W2_0$=1)

$$F=\underbrace{\frac{\text{System clock frequency}}{8}}_{①②}\times\underbrace{\frac{1}{16}}_{③}\times\underbrace{\frac{1}{m}}_{④}\times\underbrace{\frac{1}{LC+1}}_{⑤}\times\underbrace{\frac{1}{2}}_{⑥}$$

- When using $f(X_{CIN})$ as timer 2 count source ($W2_0$=0)

$$F=f(X_{CIN})\times\underbrace{\frac{1}{16}}_{③}\times\underbrace{\frac{1}{m}}_{④}\times\underbrace{\frac{1}{LC+1}}_{⑤}\times\underbrace{\frac{1}{2}}_{⑥}$$

[System clock frequency : $f(X_{IN})$ or $f(X_{CIN})$
m : 1, 2, 4
LC : 0 to 15]

The frame frequency and frame period for each display method can be obtained by the following formula :

$$\text{Frame frequency}=\frac{F}{n}(\text{Hz})$$

$$\text{Frame period}=\frac{n}{F}(\text{s})$$

[F : LCD clock frequency
1/n : Duty]

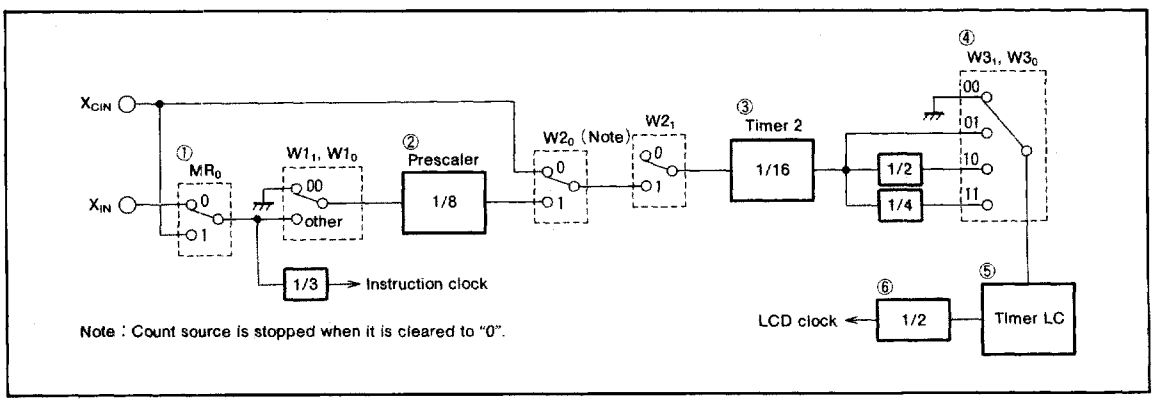


Fig. 29 LCD clock control circuit

MITSUBISHI ELECTRIC

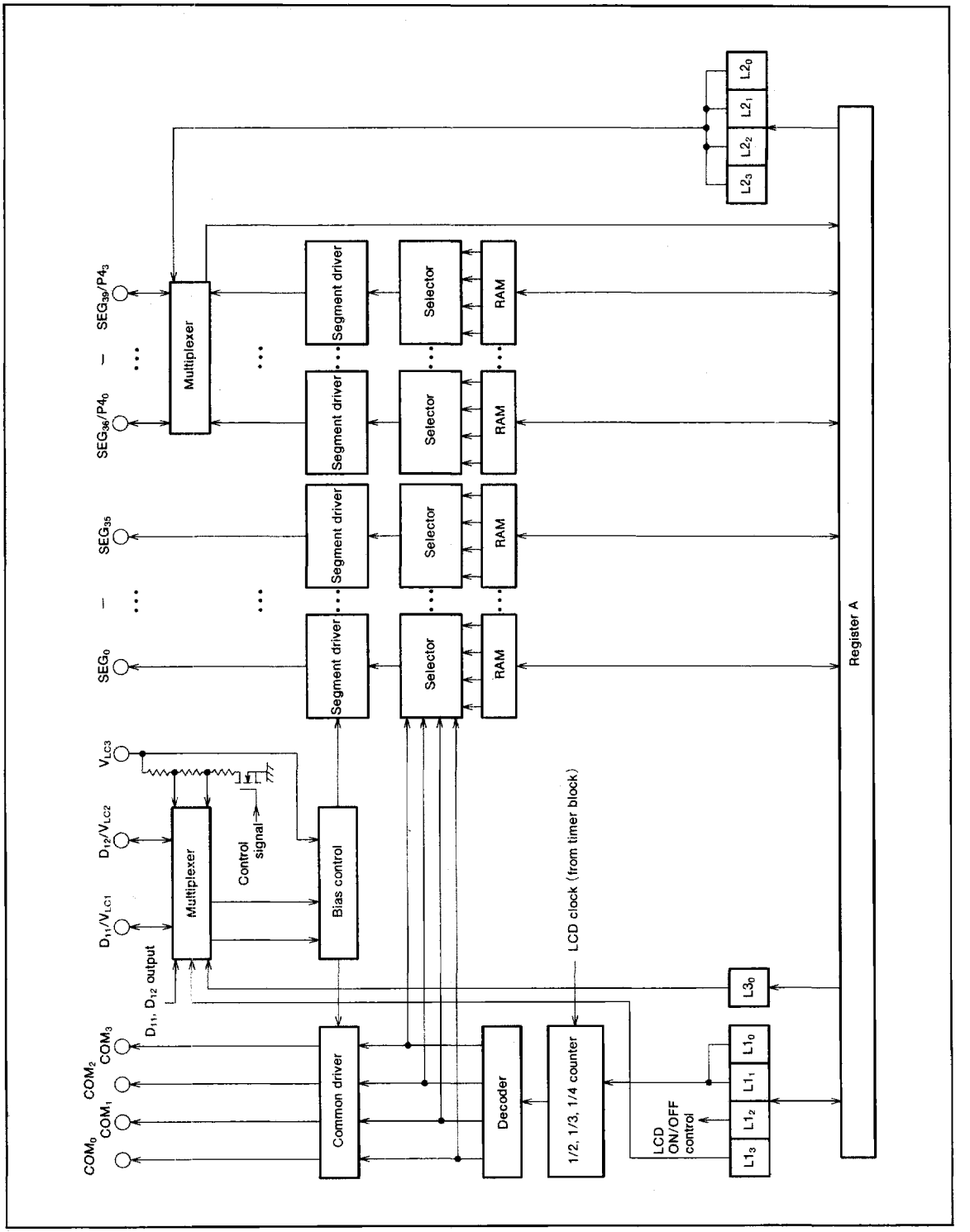
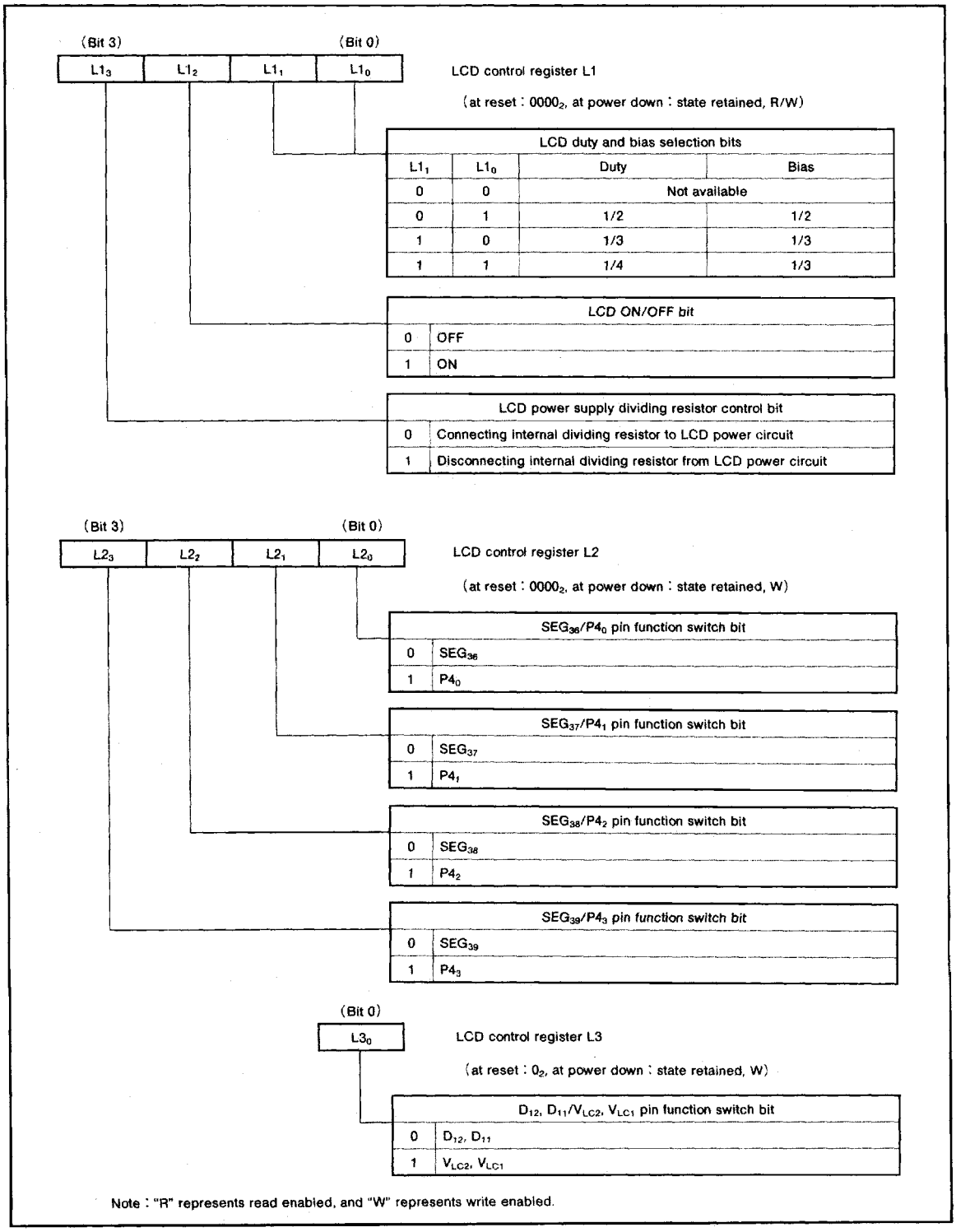


Fig. 30 LCD controller/driver structure



Note : "R" represents read enabled, and "W" represents write enabled.

Fig. 31 LCD control register

(3) LCD RAM

The RAM contains areas corresponding to the liquid crystal display. When "1" is written to this LCD RAM, the display pixel corresponding to the bit is displayed automatically.

Z	1											
X	4				5				6			
Y \ Bit	3	2	1	0	3	2	1	0	3	2	1	0
8	SEG_0	SEG_0	SEG_0	SEG_0	SEG_8	SEG_8	SEG_8	SEG_8	SEG_{16}	SEG_{16}	SEG_{16}	SEG_{16}
9	SEG_1	SEG_1	SEG_1	SEG_1	SEG_9	SEG_9	SEG_9	SEG_9	SEG_{17}	SEG_{17}	SEG_{17}	SEG_{17}
10	SEG_2	SEG_2	SEG_2	SEG_2	SEG_{10}	SEG_{10}	SEG_{10}	SEG_{10}	SEG_{18}	SEG_{18}	SEG_{18}	SEG_{18}
11	SEG_3	SEG_3	SEG_3	SEG_3	SEG_{11}	SEG_{11}	SEG_{11}	SEG_{11}	SEG_{19}	SEG_{19}	SEG_{19}	SEG_{19}
12	SEG_4	SEG_4	SEG_4	SEG_4	SEG_{12}	SEG_{12}	SEG_{12}	SEG_{12}	SEG_{20}	SEG_{20}	SEG_{20}	SEG_{20}
13	SEG_5	SEG_5	SEG_5	SEG_5	SEG_{13}	SEG_{13}	SEG_{13}	SEG_{13}	SEG_{21}	SEG_{21}	SEG_{21}	SEG_{21}
14	SEG_6	SEG_6	SEG_6	SEG_6	SEG_{14}	SEG_{14}	SEG_{14}	SEG_{14}	SEG_{22}	SEG_{22}	SEG_{22}	SEG_{22}
15	SEG_7	SEG_7	SEG_7	SEG_7	SEG_{15}	SEG_{15}	SEG_{15}	SEG_{15}	SEG_{23}	SEG_{23}	SEG_{23}	SEG_{23}
COM	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0

Z	1							
X	7				8			
Y \ Bit	3	2	1	0	3	2	1	0
8	SEG_{24}	SEG_{24}	SEG_{24}	SEG_{24}	SEG_{32}	SEG_{32}	SEG_{32}	SEG_{32}
9	SEG_{25}	SEG_{25}	SEG_{25}	SEG_{25}	SEG_{33}	SEG_{33}	SEG_{33}	SEG_{33}
10	SEG_{26}	SEG_{26}	SEG_{26}	SEG_{26}	SEG_{34}	SEG_{34}	SEG_{34}	SEG_{34}
11	SEG_{27}	SEG_{27}	SEG_{27}	SEG_{27}	SEG_{35}	SEG_{35}	SEG_{35}	SEG_{35}
12	SEG_{28}	SEG_{28}	SEG_{28}	SEG_{28}	SEG_{36}	SEG_{36}	SEG_{36}	SEG_{36}
13	SEG_{29}	SEG_{29}	SEG_{29}	SEG_{29}	SEG_{37}	SEG_{37}	SEG_{37}	SEG_{37}
14	SEG_{30}	SEG_{30}	SEG_{30}	SEG_{30}	SEG_{38}	SEG_{38}	SEG_{38}	SEG_{38}
15	SEG_{31}	SEG_{31}	SEG_{31}	SEG_{31}	SEG_{39}	SEG_{39}	SEG_{39}	SEG_{39}
COM	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0

Fig. 32 LCD RAM map

(4) LCD control register

- LCD control register (L1)

Register L1 controls the combinations of duty and bias, LCD on/off, and internal dividing resistor connection. Set the contents of this register with the TL1A instruction through register A. The TAL1 instruction can also be used to transfer the contents of register L1 to register A.

- LCD control register (L2)

Register L2 controls pins $SEG_{36}/P4_0 - SEG_{39}/P4_3$ function. Set the contents of this register with the TL2A instruction through register A.

- LCD control register (L3)

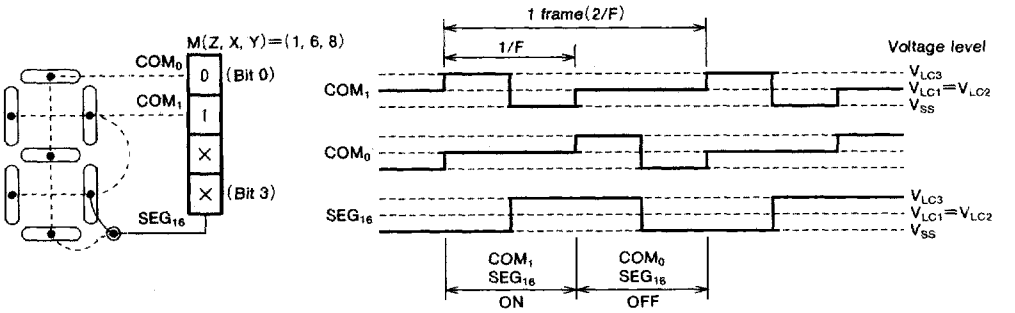
Register L3 controls pins D_{11}/V_{LC1} and D_{12}/V_{LC2} function. Set the contents of this register with the TL3A instruction through register A.

(5) LCD drive waveform

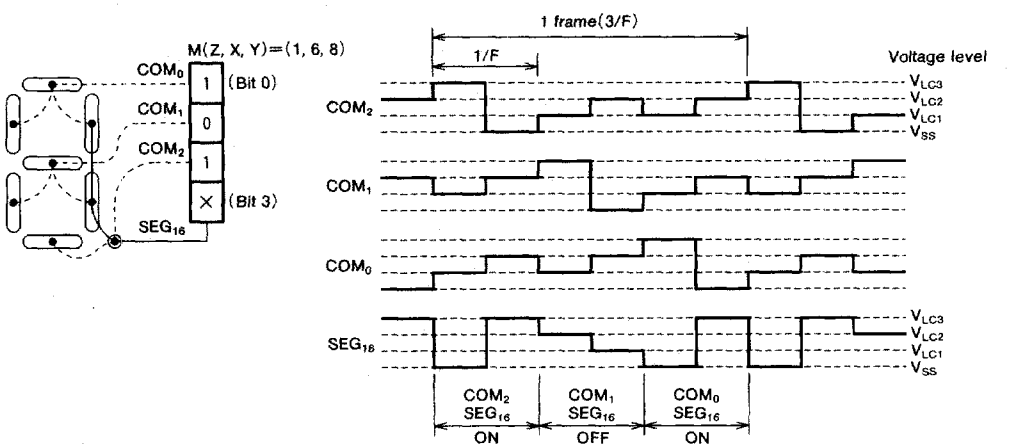
Fig. 33 shows the drive waveform example for each display method. When "1" is written in the LCD RAM data, the voltage difference between the corresponding common pin and segment pin becomes $|V_{LC3}|$ automatically and the display pixel at the cross section turns on.

When returning from reset and being the power down 2 state, display pixel turns off because every segment output pin and common output pin becomes V_{LC3} level.

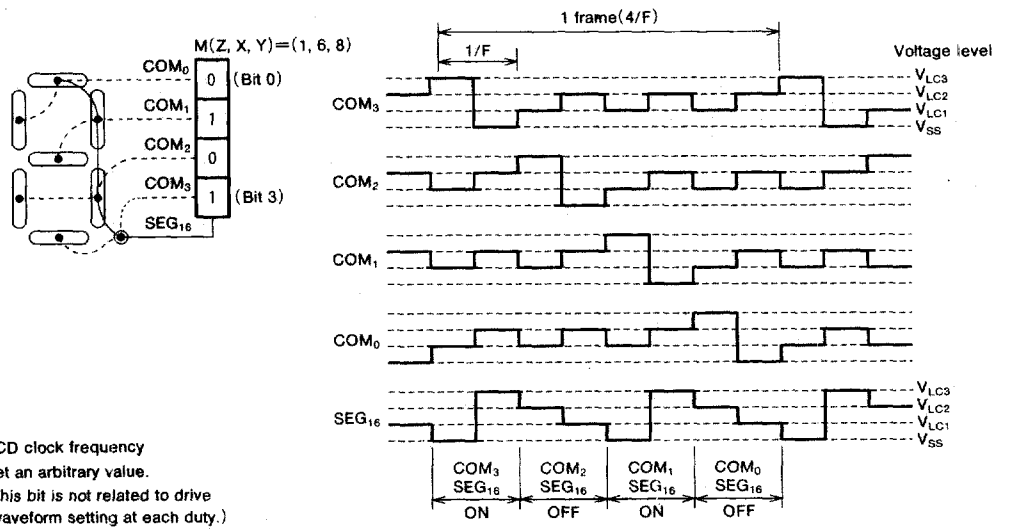
1/2 duty, 1/2 bias : When writing $(XX10)_2$ to address M(Z, X, Y)=(1, 6, 8) in RAM



1/3 duty, 1/3 bias : When writing $(X101)_2$ to address M(Z, X, Y)=(1, 6, 8) in RAM



1/4 duty, 1/3 bias : When writing $(1010)_2$ to address M(Z, X, Y)=(1, 6, 8) in RAM



F : LCD clock frequency
X : Set an arbitrary value.
(This bit is not related to drive waveform setting at each duty.)

Fig. 33 Drive wave example

(6) LCD power supply

The 4550 Group has the built-in LCD dividing resistor that can be disconnected with software. Select whether to connect this internal dividing resistor or not, and select the LCD power supply circuit appropriate for the LCD panel being used according to the combination of 3 items in the following Table 9. LCD power supply control.

Table 9 LCD power supply control

Control Item	Control Bit	
Connect/disconnect internal dividing resistor to/from LCD power supply.	$L1_3$	
	Connecting	0
	Disconnecting	1
Connect/disconnect pins D_{11}/V_{LC1} and D_{12}/V_{LC2} to/from LCD power supply.	$L3_0$	
	Disconnecting	0
	Connecting	1
Use 1/2 or 1/3 bias.	$L1_1$	
	1/2 bias	0
	1/3 bias	1

- *When connecting the internal dividing resistor and disconnecting pins D_{11}/V_{LC1} and D_{12}/V_{LC2}*
  $[L1_3=0, L3_0=0]$
  In this case, 0 to V_{LC3} (V) voltage is applied to the LCD panel. Apply voltage between 2.2V and V_{DD} to the V_{LC3} pin. (circuit example a)
- When connecting the internal dividing resistor and connecting pins D_{11}/V_{LC1} and D_{12}/V_{LC2} $[L1_3=0, L3_0=1]$
  In this case, internally generated divided voltage is output from pins D_{11}/V_{LC1} and D_{12}/V_{LC2}. Accordingly, the impedance of the LCD power can be reduced by externally connecting a capacitor to the pins D_{11}/V_{LC1} and D_{12}/V_{LC2}. Apply voltage between 2.2V and V_{DD} to the V_{LC3} pin.
  (1/3 bias : circuit example b, 1/2 bias : circuit example c)
- When disconnecting the internal dividing resistor and connecting pins D_{11}/V_{LC1} and D_{12}/V_{LC2}
  $[L1_3=1, L3_0=1]$
  This is the external power input mode. Apply the following voltage to each LCD power supply input pins.
  When using 1/3 bias : $(2.2V \leq V_{LC3} \leq V_{DD})$
  $V_{LC2}=\frac{2}{3}V_{LC3}$, $V_{LC1}=\frac{1}{3}V_{LC3}$
  When using 1/2 bias : $(2.2V \leq V_{LC3} \leq V_{DD})$
  $V_{LC2}=V_{LC1}=\frac{1}{2}V_{LC3}$
  (1/3 bias : circuit example d, 1/2 bias : circuit example e)

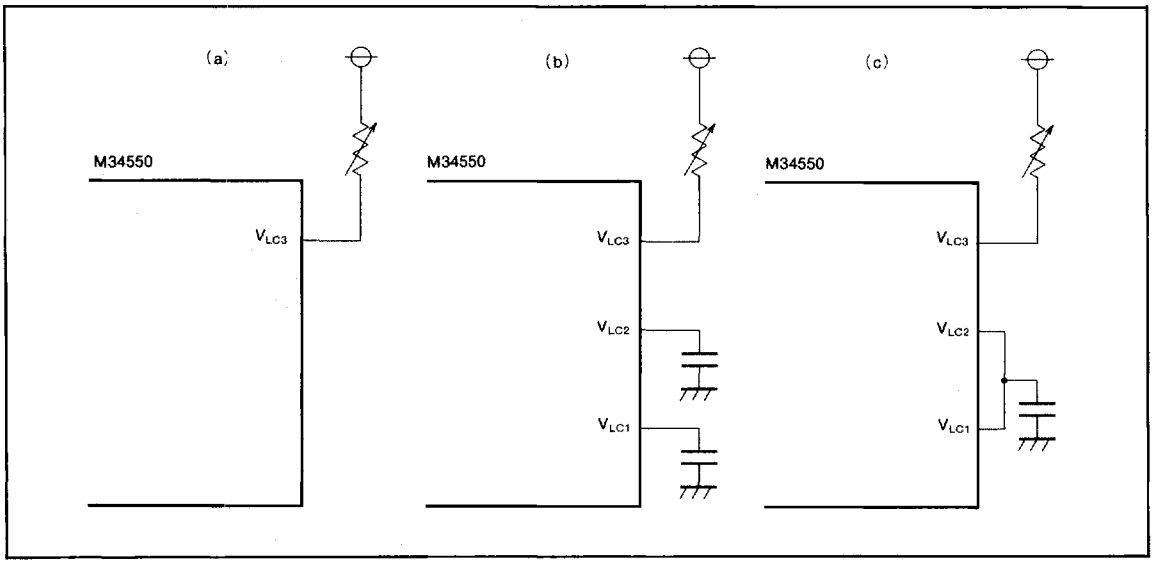


Fig. 34 LCD power circuit example

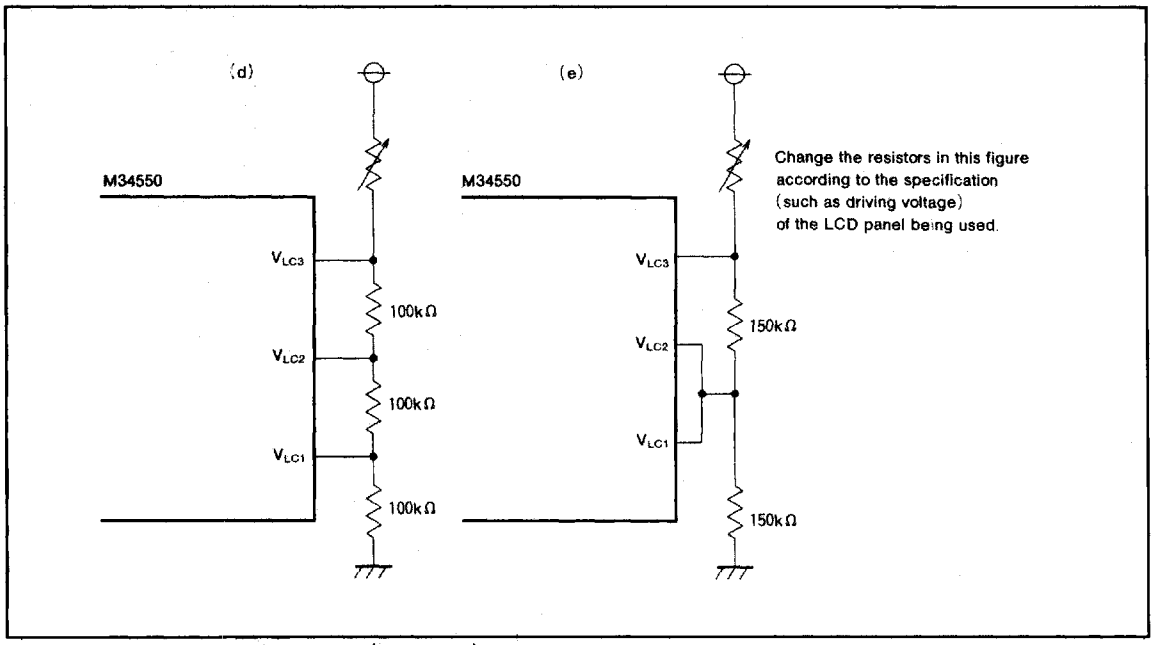


Fig. 35 LCD power circuit example (continued)

(7) LCD display method

The connection example in Fig. 36 shows the display method, how to set the LCD control register, and the drive waveform when displaying the character "9".

1. Select the duty and bias combinations with bits 0 and 1 of the register L1.
2. Set the internal resistor with bit 3 of the register L1, and register L3.
3. Switch pins $SEG_{36}/P4_0$ and $SEG_{37}/P4_1$ to segment output ports with bits 0 and 1 of the register L2.
4. Write $(1011)_2$ and $(0111)_2$ to addresses M(Z, X, Y) = (1, 8, 12) and M(Z, X, Y) = (1, 8, 13) in RAM as shown in Fig. 38.
5. Character "9" is displayed by setting bit 2 of the register L1 to "1".

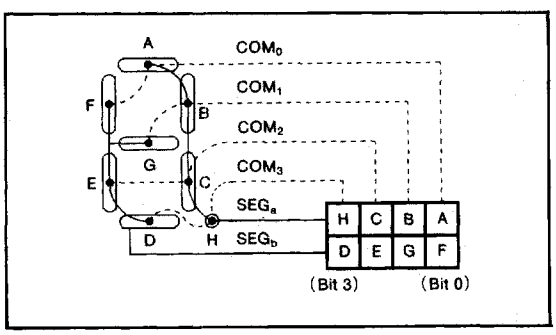


Fig. 36 LCD connection example

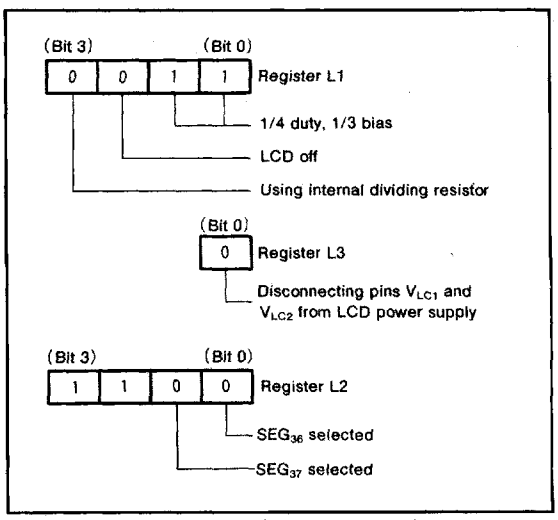


Fig. 37 Setting registers (before LCD on)

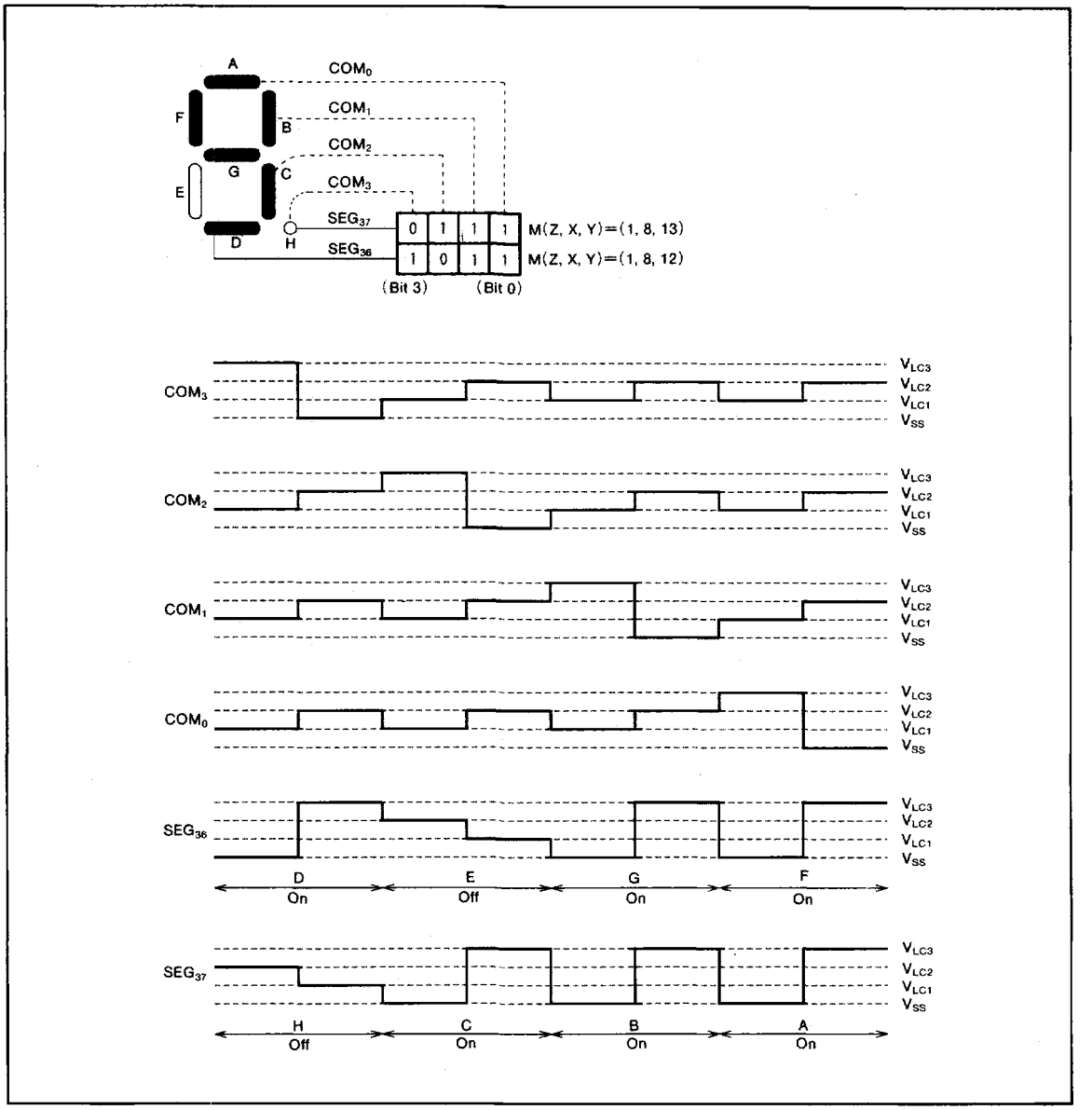


Fig. 38 Display pattern example and drive waveform example

RESET FUNCTION

System reset is performed by applying "L" level to the $\overline{\text{RESET}}$ pin for 1 machine cycle or more when the following 2 conditions are satisfied;

- the value of supply voltage is the minimum value or more of the recommended operating conditions, and
- the oscillation is stabilized.

Then when "H" level is applied to the $\overline{\text{RESET}}$ pin, the program starts from address 0 in page 0.

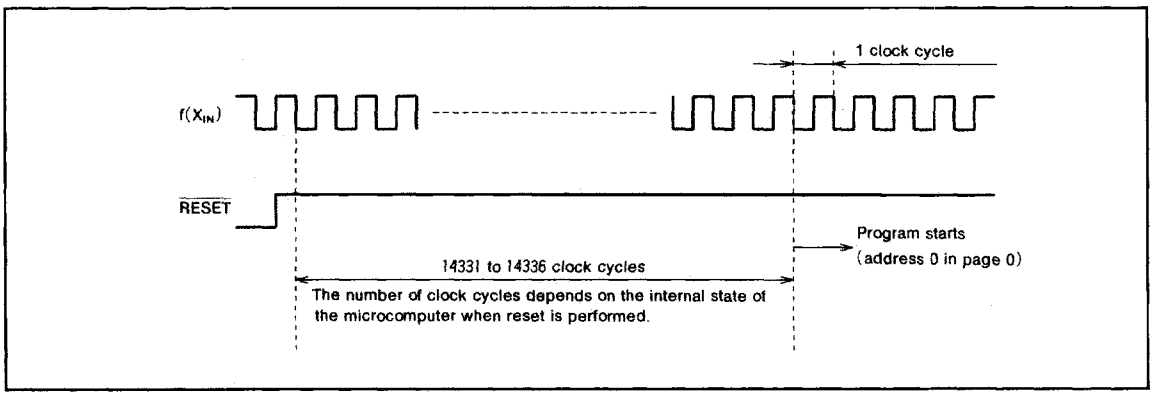


Fig. 39 Reset release timing

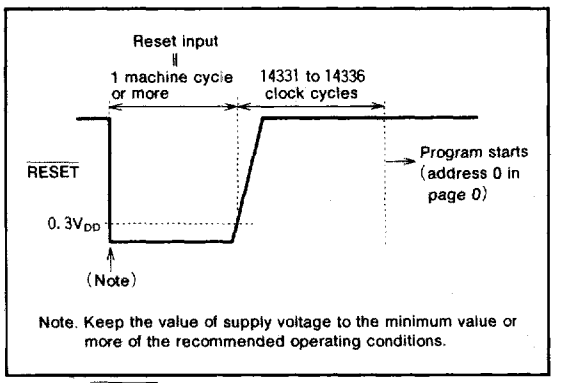


Fig. 40 $\overline{\text{RESET}}$ pin input waveform and reset operation

(1) Power-on reset

Reset can be performed automatically at power on (power-on reset) by connecting resistors, a diode, and a capacitor to the $\overline{\text{RESET}}$ pin. Connect the $\overline{\text{RESET}}$ pin and the external circuit at the shortest distance.

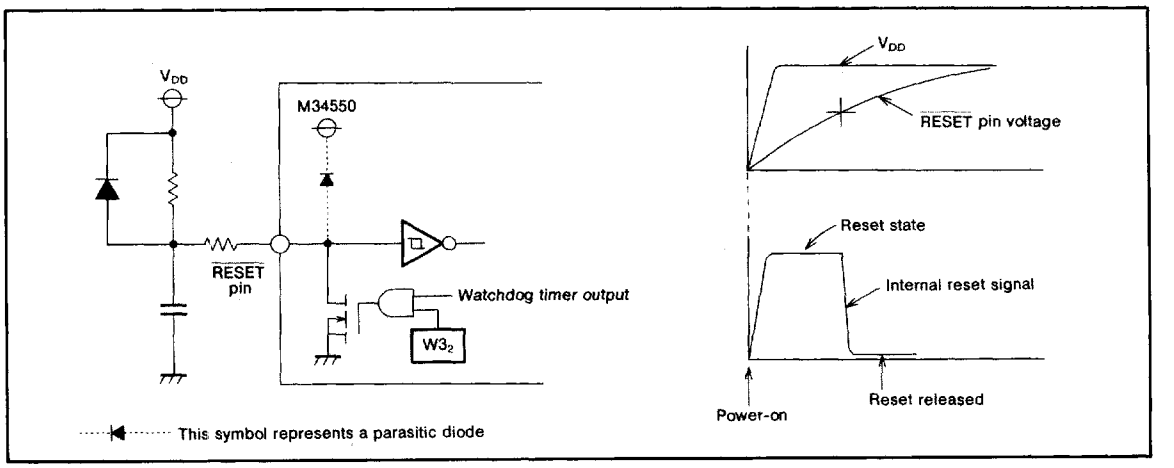


Fig. 41 Power-on reset circuit example

(2) Internal state at reset

Fig. 42 shows the internal state and port state at reset (they are the same after reset is released).

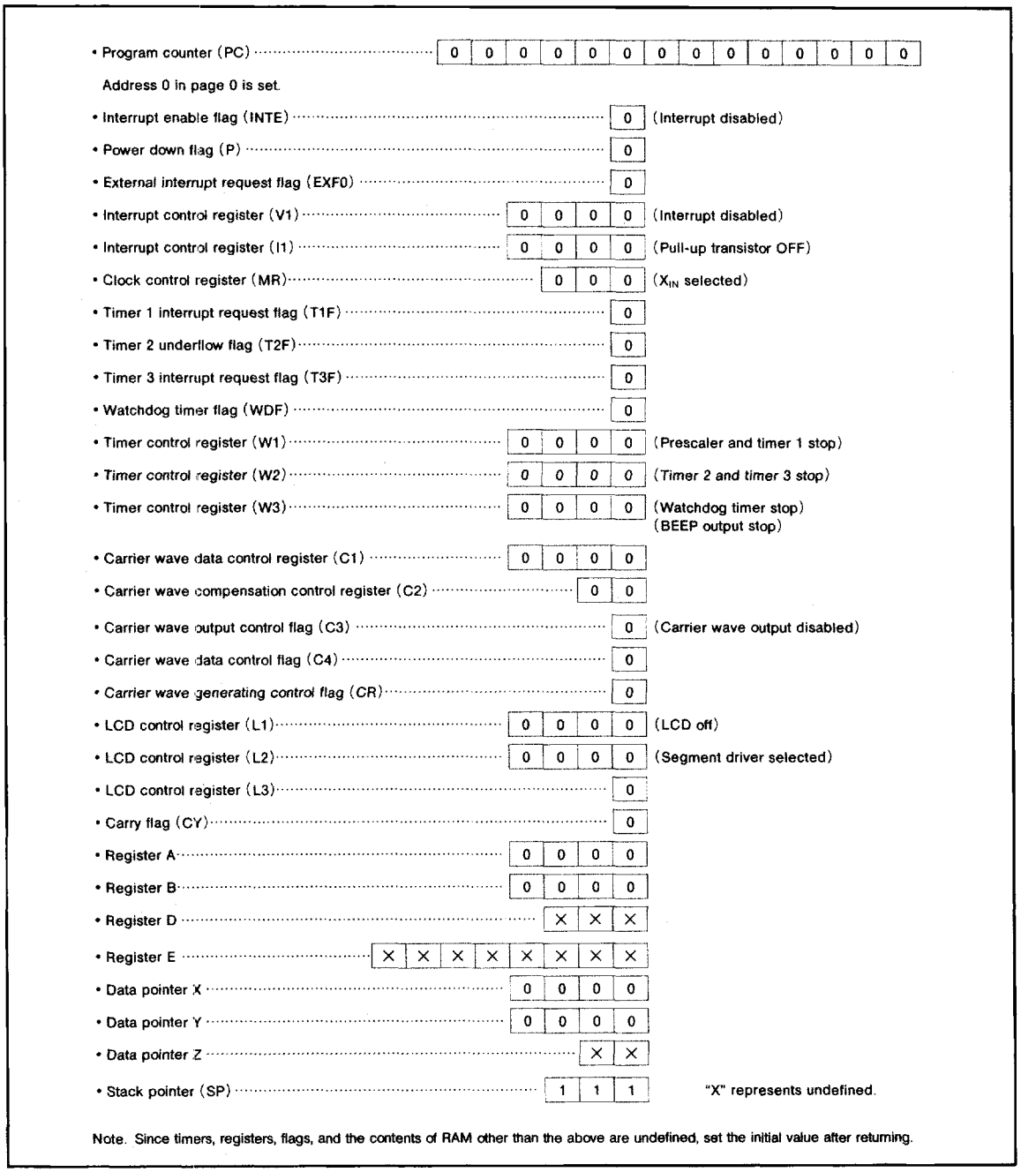


Fig. 42 Internal state at reset

Table 10 Port state at reset

Name	Function at reset	State at reset
D_0—D_7	D_0—D_7	High impedance (Note 1)
D_8, D_9	D_8, D_9	
D_{10}/BEEP	D_{10}/BEEP	
D_{11}/V_{LC1}, D_{12}/V_{LC2}	D_{11}, D_{12}	
$P0_0$—$P0_3$	$P0_0$—$P0_3$	"H" (V_{DD}) level (Note 1)
$P1_0$—$P1_3$	$P1_0$—$P1_3$	
$P2_0$—$P2_3$	$P2_0$—$P2_3$	High impedance
$P3_0$/INT	$P3_0$	High impedance (Note 2)
$P3_1$	$P3_1$	
$SEG_{36}/P4_0$—$SEG_{39}/P4_3$	SEG_{36}—SEG_{39}	V_{LC3} level
SEG_0—SEG_{35}	SEG_0—SEG_{35}	
COM_0—COM_3	COM_0—COM_3	
CARR	CARR	"L" (V_{SS}) level

Notes 1. Output latch is set to "1".
2. Pull-up transistor is turned off.

POWER DOWN FUNCTION

The 4550 Group has 2-type power down functions.

- Power down 1 (clock operating mode)
  ..... POF instruction
- Power down 2 (RAM back-up mode)
  ..... POF2 instruction

Note : be sure to disable interrupts by executing the DI instruction before the POF (power down 1) or POF2 (power down 2) instruction is executed.

Power down is performed by executing each instruction. The start condition is different between these power downs and normal reset.

- Return from power-down state
  ..... Warm start condition
- Return from reset state
  ..... Cold start codition

(1) Power down 1 (clock operating mode)

The following functions and states are retained at a power down with the POF instruction.

- RAM
- Reset circuit
- $X_{CIN}-X_{COUT}$ oscillation
- LCD display
- Timer 2, timer 3

(2) Power down 2 (RAM back-up mode)

The following functions and states are retained at a power down with the POF2 instruction.

- RAM
- Reset circuit

Unlike power down 1, all oscillations stop with power down 2.

(3) Warm start condition

The system returns from the power-down state when :

- external wakeup signal is input, or
- timer 3 interrupt request flag is set in power down 1 state, or when :
- external wakeup signal is input in power down 2 state. In either case, the CPU starts executing the program from address 0 in page 0 after returning. In this case, the P flag is set to "1".

(4) Cold start condition

The CPU starts executing the program from address 0 in page 0 when :

- reset pulse is input, or
- reset by watchdog timer.

In this case, the P flag is cleared to "0".

Table 11 Functions and states retained at power down

Function	Power down	
	Mode 1	Mode 2
Registers A, B Program counter (PC) Stack pointer (SP) (Note 2) Carry flag (CY)	×	×
Contents of RAM	○	○
Port level	○	○
Clock control register (MR)	○	○
Timer control register (W1)	×	×
Timer control registers (W2, W3)	○	○
Interrupt control register (V1)	×	×
Interrupt control register (I1)	○	○
Multi-carrier generating circuit control registers and flags (C1, C2, C3, C4, CR)	×	×
LCD display function	○	(Note 3)
LCD control registers (L1, L2, L3)	○	○
Timer LC	○	(Note 4)
Timer 2 function	○	(Note 4)
Timer 3 function	○	(Note 4)
External interrupt request flag (EXF0)	×	×
Timer 2 underflow flag (T2F)	○	(Note 4)
Timer 3 interrupt request flag (T3F)	○	(Note 4)
Watchdog timer flag (WDF)	○	(Note 4) (Note 5)
Interrupt enable flag	×	×

Notes 1. "O" represents that the function can be retained, and "X" represents that the function is initialized.
Timers, registers and flags other than the above are undefined at power down, and set the initial value after returning.
2. The stack pointer (SP) points the level of the stack register and is initialized to "7" at power down.
3. The LCD is turned off.
4. The state of the timer is undefined.
5. Stop the watchdog timer with software, and then execute the POF2 instruction.

(5) Identification of the start condition

The start condition (warm start or cold start) can be identified by examining the state of P flag with the SNZP instruction. The warm start condition (timer 3 or external wakeup signal) can be identified by examining the state of the T3F flag.

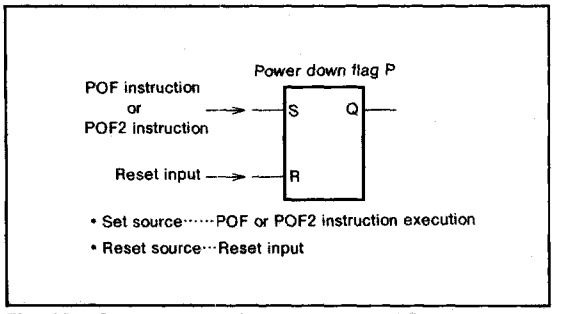


Fig. 43. Set source and reset source of P flag

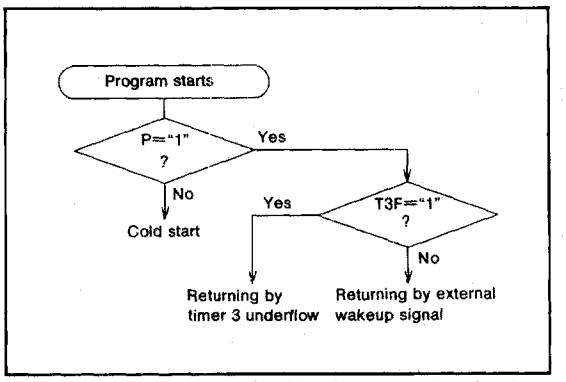


Fig. 44 Start condition identification example with the SNZP instruction

(6) State transition

State transition is described using Fig. 45.

1. Cold start (Return from reset state)

   The state is A after a cold start from the reset state. In state A, bit 0 (MR_0) and bit 1 (MR_1) of the clock control register are both "0", and $f(X_{IN})$ is selected as the system clock.

2. Transition from state A to low-speed mode state C

   First set MR_0 to "1" (state B) to switch the system clock and then set MR_1 to "1" (state C) to stop $f(X_{IN})$ oscillation.

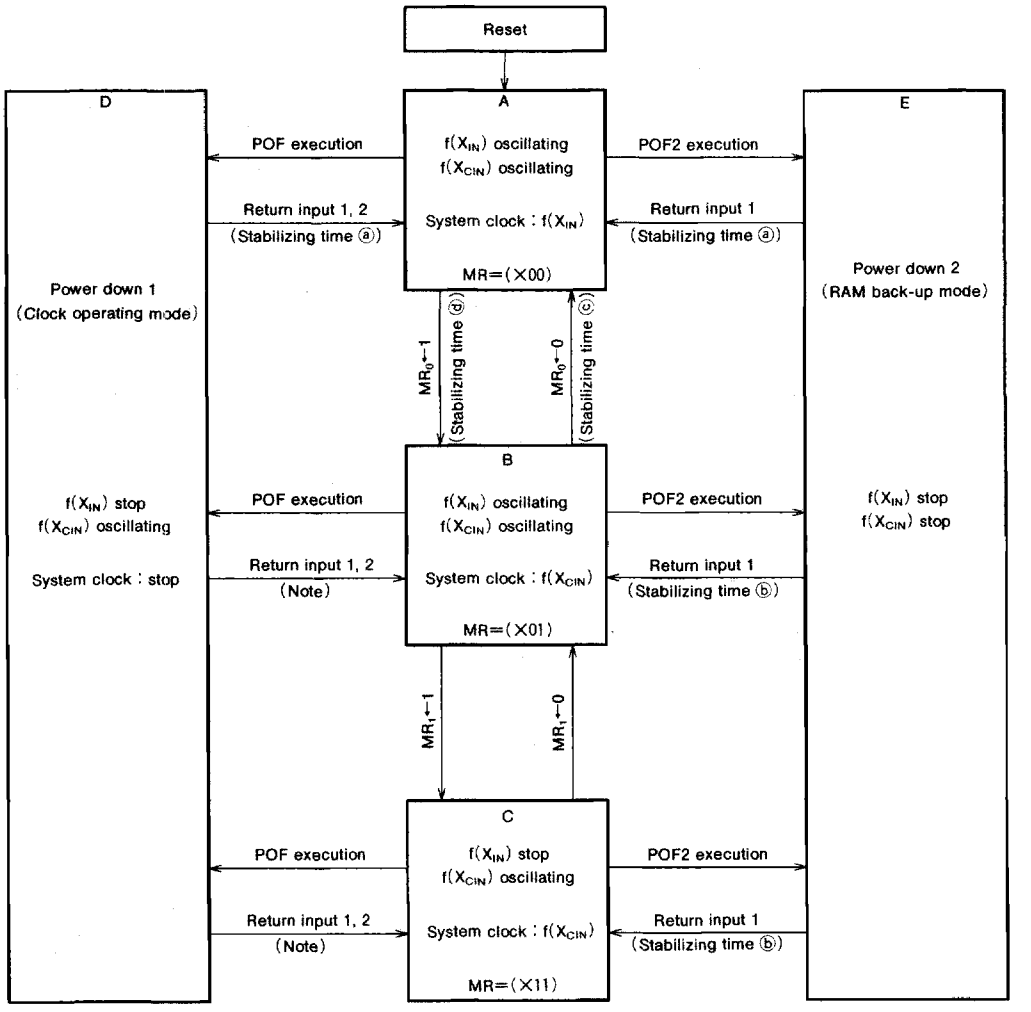
   However, after a cold start, do not use $f(X_{CIN})$ as system clock and count source until $f(X_{CIN})$ oscillation sufficiently stabilizes (same as when returning from state E to state A).

3. Transition from state D (power down 1) or state E (power down 2)

   The power down 1 (state D) or power down 2 (state E) state can be entered from state A, B, or C with the POF or POF2 instruction. When returning, the state returns to the state before executing the POF or POF2 instruction, but stabilizing time is generated automatically according to the state as shown in Fig. 45 because the oscillation stabilizing time depends on the state of $f(X_{IN})$ or $f(X_{CIN})$.

4. Transition from state C to state A

   First clear MR_1 to "0" to go to state B, generate sufficient time for $f(X_{IN})$ oscillation to stabilize with software, and then clear MR_0 to "0" to go to state A. Also generate sufficient time for $f(X_{IN})$ oscillation to stabilize with software, and then clear MR_0 to "0" to go to state A from state B after the transition to state D from state B with the POF instruction (State transition : B→D→B→A).



Stabilizing time ⓐ : Microcomputer starts its operation after counting the f(X_{IN}) clock signal 14331 to 14336 times with hardware to stabilize the f(X_{IN}) oscillation.

Stabilizing time ⓑ : Microcomputer starts its operation after counting the f(X_{CIN}) clock signal 14331 to 14336 times with hardware to stabilize the f(X_{CIN}) oscillation.

Stabilizing time ⓒ : Generate an interval required to stabilize the f(X_{IN}) oscillation in state B with software at the transition C→B→A or D→B→A.

Stabilizing time ⓓ : Generate an interval required to stabilize the f(X_{CIN}) oscillation in state A with software since the f(X_{CIN}) oscillation may be unstable immediately after cold starting or the return from power down 2.

Returning input 1 : External wakeup signal ($P0_0$–$P0_3$, $P1_0$–$P1_3$, $P2_0$, $P2_1$, $P3_0$)

Returning input 2 : Timer 3 interrupt request flag

X : Not used (this bit has no function)

Note : The microcomputer starts its operation after counting f(X_{CIN}) oscillation 27 to 34 times.

Fig. 45 State transition diagram

(7) Return signal

An external wakeup signal or the timer 3 interrupt request flag is used to return from power down 1. External wakeup signal is used to return from power down 2 because the oscillation is stopped. Table 12 shows the return condition each return source.

Table 12 Return source and condition

Return Source		Return Condition	Remarks
External wakeup signals	Ports P0, P1	Return by external falling edge input ("H"→"L").	Set ports P0 and P1 to "H" level before going into power down state because the falling edge detection circuit is also used as ports P0 and P1.
	Ports $P2_0$, $P2_1$	Return by external falling edge input ("H"→"L").	Set both ports $P2_0$ and $P2_1$ to "H" level before going into power down state because the falling edge detection circuit is also used as ports $P2_0$ and $P2_1$.
	Port $P3_0$/INT (Note 1)	Return by external "H" level or "L" level input. In this case, EXF0 flag is not set.	Select the return level ("L" level or "H" level) with bit 2 of the interrupt control register (I1) according to the external state before going into power down state.
Timer 3 interrupt request flag		Return when timer 3 underflows and T3F flag is set to "1".	Allowed only when returning from power down 1 (executing POF instruction). However, when the POF or POF2 instruction is executed with T3F="1", return condition is recognized and return is performed.

Notes 1 : The $P3_0$/INT pin has a built-in pull-up transistor that can be turned ON/OFF by program. When going into power down state with the $P3_0$/INT pin externally set to "L" level, current flows from the $P3_0$/INT pin if this pull-up transistor is turned ON. Accordingly, systems that required power consumption to be kept low should turn off this pull-up transistor by program ($I1_0$="0") before going into power down state. However, when pull-up transistor is necessary to obtain the return level "H", pull-up transistor can be temporarily turned ON by using timer 2 output signal (dynamic pull-up function: $I1_0$="0", $I1_3$="1")

2 : When the POF or POF2 instruction is executed with T3F=1, return condition is recognized and return is immediately performed after going into power down state.

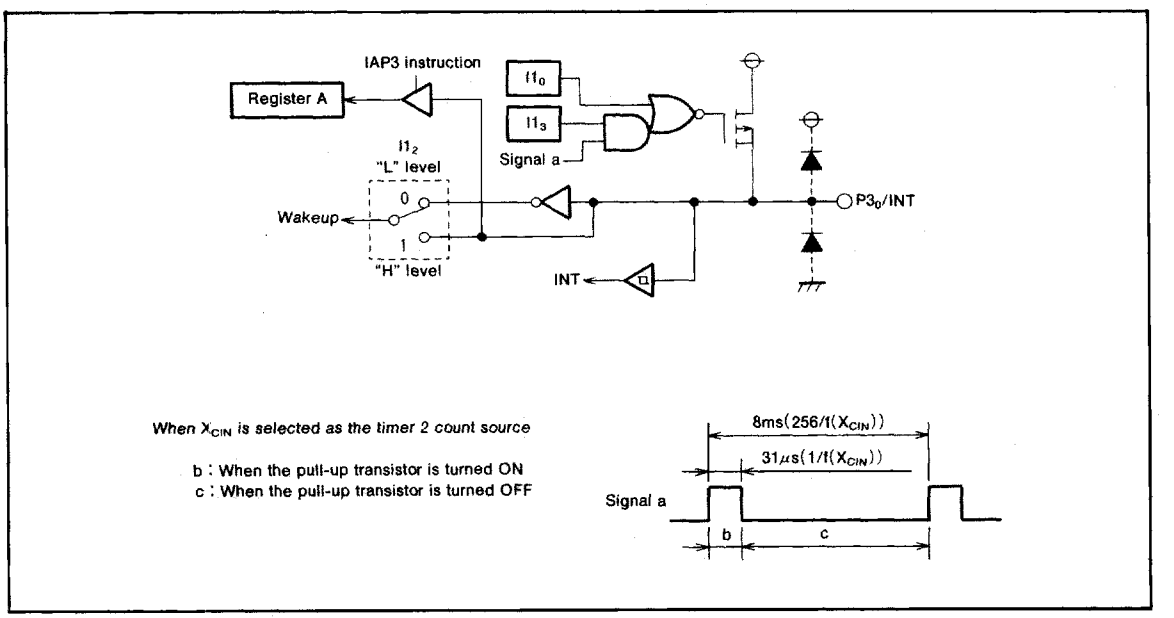


Fig. 46 $P3_0$/INT pin block diagram

(8) Power down function control register

• Interrupt control register (I1)

Register I1 controls pins $P3_0$/INT and $P3_1$ pull-up transistors ON/OFF and controls the return signal level of the $P3_0$/INT pin from power down state. Set the contents of this register with the TI1A instruction through register A. The TAI1 instruction can also be used to transfer the contents of register I1 to register A.

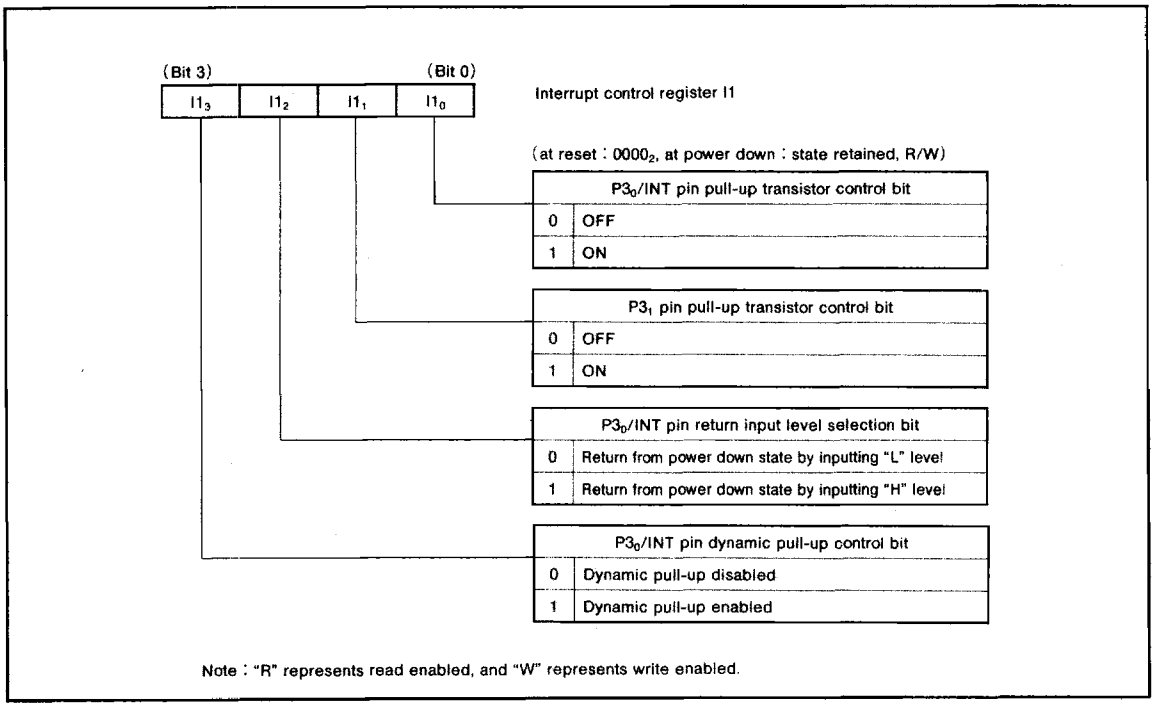


Fig. 47 Power down function control register

CLOCK CONTROL

The clock control circuit consists of the following circuits.

- $f(X_{IN})$ clock generating circuit
- $f(X_{CIN})$ clock generating circuit
- Control circuit to stop the clock oscillation
- Control circuit to return from power down state

System clock selection and clock oscillation start/stop are controlled with the clock control register (MR). The $f(X_{IN})$ clock is selected just after a cold start. The instruction clock can be switched to the $f(X_{CIN})$ clock with the system clock selection bit (MR_0). At a warm start, the clock selected just before power down is used. The instruction clock is the signal divided by 3 of the selected clock ($f(X_{IN})/3$ or $f(X_{CIN})/3$).

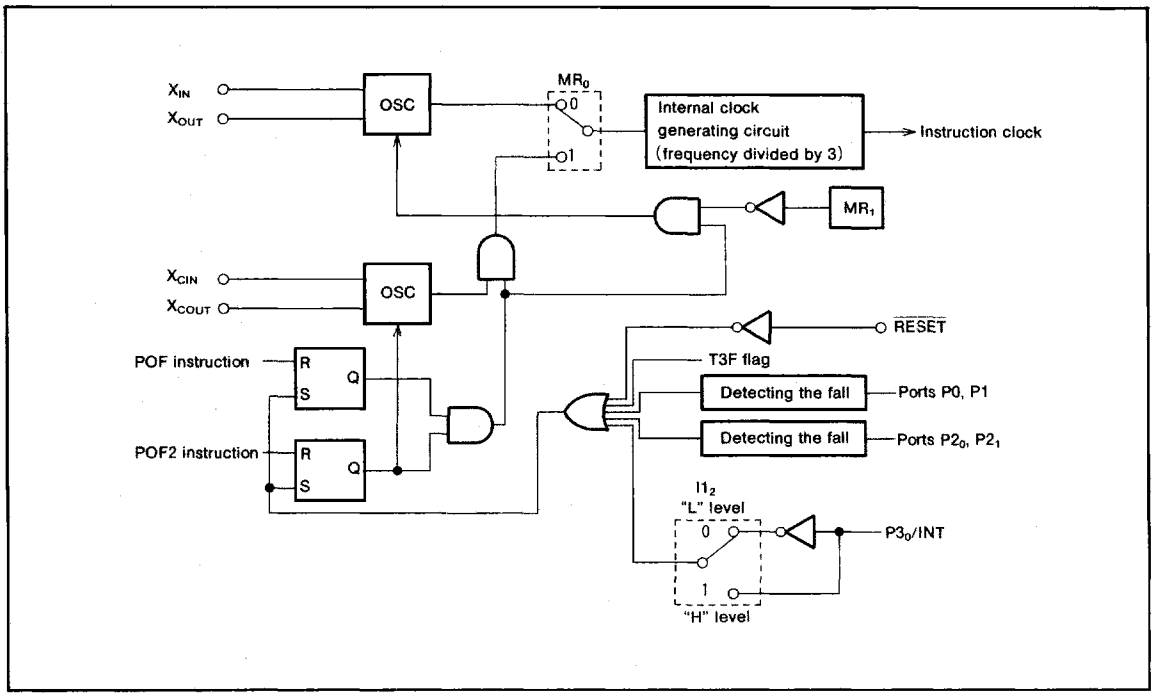


Fig. 48 Clock control circuit structure

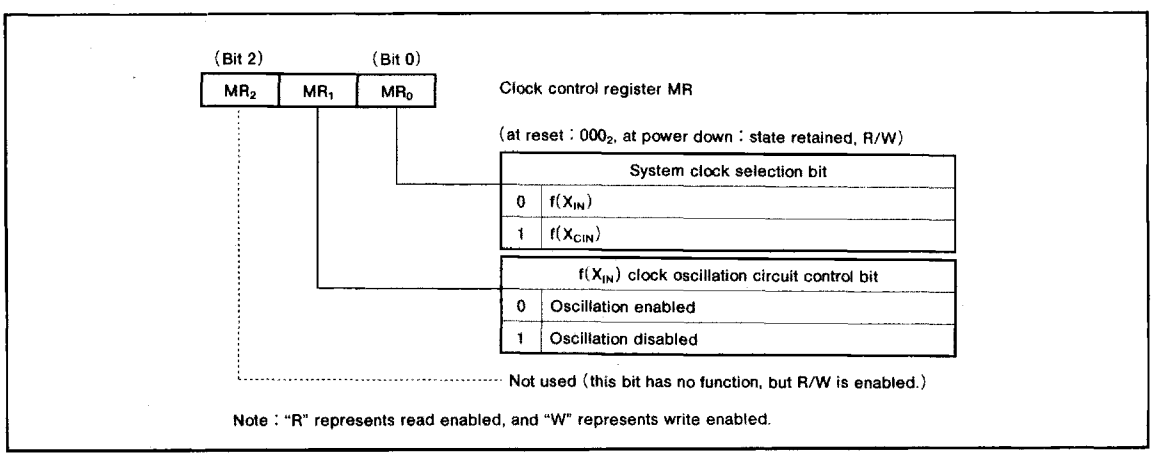


Fig. 49 Registers related clock control

(1) Clock control register MR
Register MR controls the system clock. Set the contents of this register with the TMRA instruction through register A. The TAMR instruction can also be used to transfer the contents of register MR to register A. After executing the TAMR instruction, "0" is stored in bit 3 of register A.

(2) $f(X_{IN})$ clock generating circuit
Clock oscillation ($f(X_{IN})$) is obtained by externally connecting a ceramic resonator. Connect this external circuit to pins X_{IN} and X_{OUT} at the shortest distance. A feedback resistor is built-in between pins X_{IN} and X_{OUT}. When external clock signal is input, connect the clock source to X_{IN} and leave X_{OUT} open. When using an external clock, the maximum clock system clock frequency is 800kHz. Use the external clock at 30% to 70% duty ratio.

(3) $f(X_{CIN})$ clock generating circuit
Clock oscillation ($f(X_{CIN})$) is obtained by externally connecting a quartz-crystal oscillator. Connect this external circuit to pins X_{CIN} and X_{COUT} at the shortest distance. A feedback resistor is built-in between pins X_{CIN} and X_{COUT}.
Unlike the $f(X_{IN})$ clock generating circuit, the external clock signal cannot be used for this circuit.

ROM ordering method
Please submit the information described below when ordering Mask ROM.

(1) M34550M4A-XXXFP ROM Order Confirmation Form, M34550M6A-XXXFP ROM Order Confirmation Form, or M34550M8A-XXXFP ROM Order Confirmation Form ··· 1
(2) Data to be written into mask ROM ····· EPROM (three sets containing the identical data)
(3) Mark Specification Form ····· 1

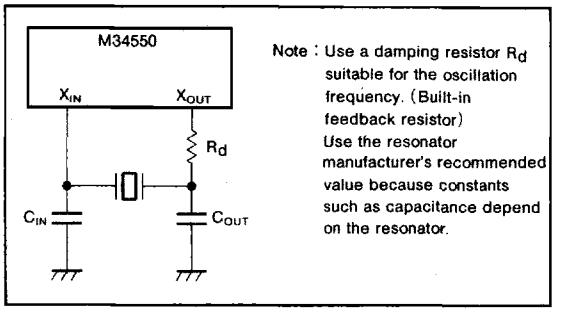


Fig. 50 Ceramic resonator external circuit

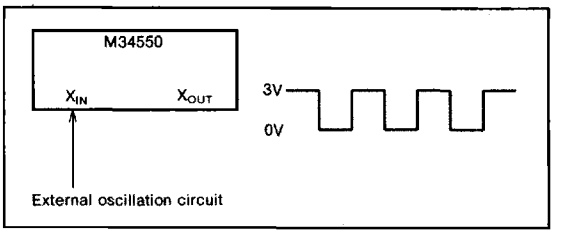


Fig. 51 External clock input circuit

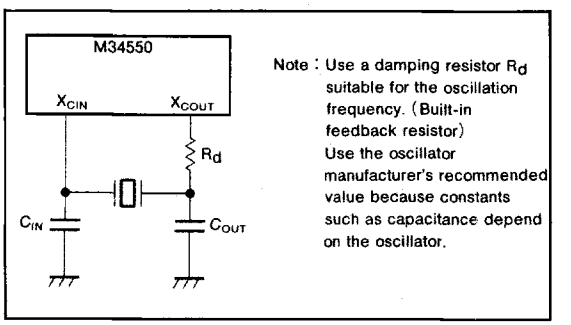


Fig. 52 Quartz-crystal oscillator external circuit

LIST OF PRECAUTIONS

(1) Noise and latch-up prevention

Connect a capacitor (approx. 0.1μF) between pins V_{DD} and V_{SS} using the thickest wire and equalizing its wiring in width and length at the shortest distance in order to prevent noise and latch up.

In the built-in PROM version, $P2_3$ pin is also used as V_{PP} pin. Accordingly, when using this pin, use this pin through a resistor about 5kΩ in series at the shortest distance.

When not using this pin, connect to V_{SS} through a 5kΩ resistor at the shortest distance.

(2) Prescaler

Stop the prescaler to change its frequency dividing ratio.

(3) Timer 1, 2, 3

Stop timer 1, 2, or 3 counting to change its count source, as well as to execute the TAB3 instruction for reading the data (from timer 3).

(4) D_{10}/BEEP pin

To use the buzzer drive output function, set the frequency (bits 0 and 1 of the register W3) and then start output. When changing the buzzer drive output frequency or switching this pin as port D_{10} function, first stop the buzzer drive output, wait for 1 cycle of the buzzer drive output, and then set the frequency or start using as port D_{10}.

(5) Multi-carrier generating circuit

- Precaution when starting carrier wave (CARR) generation

The shift operation of the multi-carrier generating circuit starts in synchronization with the falling edge ("H" → "L") of ORCLK. However, the shift operation start timing after executing the carrier wave generation start instruction (STCR) is not constant because the instruction cycle does not match the ORCLK period.

In addition, when the falling edge of ORCLK occurs during the STCR instruction execution cycle, whether register PA starts shift operation or not is undefined. When the shift operation is not started, it is started at the falling edge of the next ORCLK. The carrier wave output timing after starting shift operation depends on the initial setting value as described in the carrier wave compensation example.

- Precaution when stopping carrier wave (CARR) generation

The carrier wave is stopped at the fall of the carrier wave. However, the carrier wave stop timing after executing the carrier wave stop instruction (SPCR) is not constant because the instruction cycle does not match the carrier wave period.

In addition, when the fall of the carrier wave occurs during the SPCR instruction execution cycle, whether the carrier wave is stopped or not is undefined. When the carrier wave is not stopped, it is stopped at the fall of the next carrier wave.

When the prescaler is to be stopped after stopping the carrier wave, wait for 1 period of ORCLK after the carrier wave has stopped, and then stop the prescaler.

- Precaution when restarting carrier wave (CARR) generation

When carrier wave generation is restarted after stopping, timer PT retains the previous value without initializing. Accordingly, be sure to set again timer PT (with the TPTA instruction) before restarting carrier wave generation (with the STCR instruction).

- Precaution when using the carrier wave (CARR) automatic stop function

Carrier wave generation can be stopped ($C2_1$ = "1") with the timer 1 underflow signal using the carrier wave as the timer 1 count source ($W1_3$="1"). In this case, it is necessary to set again timer 1 (with the T1R1 instruction) when carrier wave generation is to be restarted (with the STCR instruction) after stopping it with a timer 1 underflow signal.

(6) Built-in PROM version precautions

The operating power voltage of the built-in EPROM version (M34550E8FS) and the One Time PROM version (M34550E8-XXXFP, M34550E8FP) is 2.5V to 3.6V.

The operating power voltage of the mask ROM version (M34550M8A-XXXFP) is 2.2V to 3.6V.

(7) Notes on power down function

Be sure to disable interrupts by executing the DI instruction before the POF (power down 1) or POF2 (power down 2) instruction is executed.

(8) Note on program counter

Make sure that the PC_H does not specify after the last page of the built-in ROM.

(9) Note on LCD

The 4550 Group has the LCD dividing resistor that can be disconnected by software. Select whether to connect this internal dividing resistor or not, the LCD power supply circuit appropriate for the LCD panel being used, and test sufficiently.

SYMBOL

The symbols shown are used in the following instruction function table and instruction list.

Symbol	Contents	Symbol	Contents
A	Register A (4 bits)	T1F	Timer 1 interrupt request flag
B	Register B (4 bits)	T2F	Timer 2 underflow flag
DR	Register D (3 bits)	T3F	Timer 3 interrupt request flag
E	Register E (8 bits)	INTE	Interrupt enable flag
C1	Carrier wave data control register C1 (4 bits)	EXF0	External interrupt request flag
C2	Carrier wave compensation control register C2 (2 bits)	P	Power down flag
C3	Carrier wave output control flag C3	WDF	Watchdog timer flag WDF
C4	Carrier wave data control flag C4		
CR	Carrier wave generating control flag CR	D	Port D (13 bits)
PA	Preset register PA (4 bits)	P0	Port P0 (4 bits)
L1	LCD control register L1 (4 bits)	P1	Port P1 (4 bits)
L2	LCD control register L2 (4 bits)	P2	Port P2 (4 bits)
L3	LCD control register L3 (1 bit)	P3	Port P3 (2 bits)
MR	Clock control register MR (3 bits)	P4	Port P4 (4 bits)
V1	Interrupt control register V1 (4 bits)		
I1	Interrupt control register I1 (4 bits)	x	Hexadecimal variable
W1	Timer control register W1 (4 bits)	y	Hexadecimal variable
W2	Timer control register W2 (4 bits)	z	Hexadecimal variable
W3	Timer control register W3 (4 bits)	p	Hexadecimal variable
		n	Hexadecimal constant
X	Register X (4 bits)	i	Hexadecimal constant
Y	Register Y (4 bits)	j	Hexadecimal constant
Z	Register Z (2 bits)	$A_3A_2A_1A_0$	Binary notation of hexadecimal variable A
DP	Data pointer (10 bits)		(same for others)
	(It consists of registers X, Y and Z)		
PC	Program counter (14 bits)	←	Direction of data movement
PC_H	High-order 7 bits of program counter	( )	Contents of registers and memories
PC_L	Low-order 7 bits of program counter	—	Negate, Flag unchanged after executing instruction
SK	Stack register (14 bits×8)	M(DP)	RAM address specified by the data pointer
SP	Stack pointer (3 bits)	a	Label indicating address $a_6\ a_5\ a_4\ a_3\ a_2\ a_1\ a_0$
CY	Carry flag	p, a	Label indicating address $a_6\ a_5\ a_4\ a_3\ a_2\ a_1\ a_0$ in page $p_5\ p_4$ $p_3\ p_2\ p_1\ p_0$
T1	Timer 1		
T2	Timer 2		
T3	Timer 3	C	Hex. C + Hex. number × (also same for others)
R1	Timer 1 reload register	+	
R2	Timer 2 reload register	×	
R3	Timer 3 reload register		

Note : The 4550 Group just invalidates the next instruction when a skip is performed. The contents of program counter is not increased by 2. Accordingly, the number of cycles does not change even if a skip is not performed. However, the cycle count becomes "1" when the TABP $_p$, RT, or RTS instruction is skipped.

LIST OF INSTRUCTION FUNCTION

Grouping	Mnemonic	Function
Register to register transfer	TAB	(A)←(B)
	TBA	(B)←(A)
	TAY	(A)←(Y)
	TYA	(Y)←(A)
	TEAB	(E_7—E_4)←(B) (E_3—E_0)←(A)
	TABE	(B)←(E_7—E_4) (A)←(E_3—E_0)
	TDA	(DR_2—DR_0)←(A_2—A_0)
	TAD	(A_2—A_0)←(DR_2—DR_0) (A_3)←0
	TAZ	(A_1, A_0)←(Z_1, D_0) (A_3, A_2)←0
	TAX	(A)←(X)
	TASP	(A_2—A_0)←(SP_2—SP_0) (A_3)←0
RAM addresses	LXY x, y	(X)←x, x=0 to 15 (Y)←y, y=0 to 15
	LZ z	(Z)←z, z=0 to 3
	INY	(Y)←(Y)+1
	DEY	(Y)←(Y)−1
RAM to register transfer	TAM j	(A)←(M(DP)) (X)←(X)EXOR(j) j=0 to 15
	XAM j	(A)←→(M(DP)) (X)←(X)EXOR(j) j=0 to 15
	XAMD j	(A)←→(M(DP)) (X)←(X)EXOR(j) j=0 to 15 (Y)←(Y)−1
RAM to register transfer	XAMI j	(A)←→(M(DP)) (X)←(X)EXOR(j) j=0 to 15 (Y)←(Y)+1
	TMA j	(M(DP))←(A) (X)←(X)EXOR(j) j=0 to 15
Arithmetic operation	LA n	(A)←n However, n=0 to 15
	TABP p	(SP)←(SP)+1 (SK(SP))←(PC) (PC_H)←p (PC_L)←(DR_2—DR_0, A_3—A_0) (B)←(ROM(PC))$_{7\ to\ 4}$ (A)←(ROM(PC))$_{3\ to\ 0}$ (PC)←(SK(SP)) (SP)←(SP)−1
	AM	(A)←(A)+(M(DP))
	AMC	(A)←(A)+(M(DP))+(CY) (CY)←Carry
	A n	(A)←(A)+n However, n=0 to 15
	AND	(A)←(A)AND(M(DP))
	OR	(A)←(A)OR(M(DP))
	SC	(CY)←1
	RC	(CY)←0
	SZC	(CY)=0?
	CMA	(A)←($\overline{A}$)
	RAR	CY → $A_3A_2A_1A_0$
Bit operation	SB j	(Mj(DP))←1 j=0 to 3
	RB j	(Mj(DP))←0 j=0 to 3
Bit operation	SZB j	(Mj(DP))←0? j=0 to 3
Comparison operation	SEAM	(A)=(M(DP))?
	SEA n	(A)=n? However, n=0 to 15
Branch operation	B a	(PC_L)←a_6—a_0
	BL p, a	(PC_H)←p (PC_L)←a_6—a_0
	BLA p	(PC_H)←p (PC_L)←(DR_2—DR_0, A_3—A_0)
Subroutine operation	BM a	(SP)←(SP)+1 (SK(SP))←(PC) (PC_H)←2 (PC_L)←a_6—a_0
	BML p, a	(SP)←(SP)+1 (SK(SP))←(PC) (PC_H)←p (PC_L)←a_6—a_0
	BMLA p	(SP)←(SP)+1 (SK(SP))←(PC) (PC_H)←p (PC_L)←(DR_2—DR_0, A_3—A_0)
Return operation	RTI	(PC)←(SK(SP)) (SP)←(SP)−1
	RT	(PC)←(SK(SP)) (SP)←(SP)−1
	RTS	(PC)←(SK(SP)) (SP)←(SP)−1

MITSUBISHI ELECTRIC

Grouping	Mnemonic	Function
Interrupt operation	DI	(INTE)←0
	EI	(INTE)←1
	SNZ0	(EXF0)=1? After skipping, (EXF0)←0
	TV1A	(V1)←(A)
	TI1A	(I1)←(A)
	TAV1	(A)←(V1)
	TAI1	(A)←(I1)
Timer operation	TW1A	(W1)←(A)
	TW2A	(W2)←(A)
	TW3A	(W3)←(A)
	TAW1	(A)←(W1)
	TAW2	(A)←(W2)
	TAW3	(A)←(W3)
	T3AB	($R3_7$—$R3_4$)←(B) ($T3_7$—$T3_4$)←(B) ($R3_3$—$R3_0$)←(A) ($T3_3$—$T3_0$)←(A)
	T1R1	(T1)←(R1)
	TR1AB	($R1_7$—$R1_4$)←(B) ($R1_3$—$R1_0$)←(A)
	TR1A	($R1_8$)←(A_0)
	TAB3	(B)←($T3_7$—$T3_4$) (A)←($T3_3$—$T3_0$)
	SNZT1	(T1F)=1? After skipping, (T1F)←0
	SNZT2	(T2F)=1? After skipping, (T2F)←0
Timer operation	SNZT3	(T3F)=1?
Input/Output operation	IAP0	(A)←(P0)
	IAP1	(A)←(P1)
	IAP2	(A)←(P2)
	IAP3	(A_1, A_0)←($P3_1$, $P3_0$) (A_3, A_2)←0
	IAP4	(A)←(P4)
	CLD	(D)←1
	RD	(D(Y))←0 (Y)=0 to 12
	SD	(D(Y))←1 (Y)=0 to 12
	SZD	(D(Y))=0? (Y)=8 to 10
	OP0A	(P0)←(A)
	OP1A	(P1)←(A)
LCD control operation	TL1A	(L1)←(A)
	TAL1	(A)←(L1)
	TL2A	(L2)←(A)
	TL3A	(L3)←(A_0)
	TLCA	(LC)←(A)
Multi-carrier generating circuit operation	TPTA	(PT)←(A_1, A_0)
	TC1A	(C1)←(A)
	TPAA	(PA)←(A)
	RC3	(C3)←0
	SC3	(C3)←1
	RC4	(C4)←0
Multi-carrier generating circuit operation	SC4	(C4)←1
	STCR	Carrier wave generating starts
	SPCR	Carrier wave generating stops
	TC2A	(C2)←(A_1, A_0)
Other operation	NOP	(PC)←(PC)+1
	POF	Power down 1
	POF2	Power down 2
	SNZP	(P)=1?
	TMRA	(MR_2—MR_0)←(A_2—A_0)
	TAMR	(A_2—A_0)←(MR_2—MR_0) (A_3)←0
	WRST	(WDF)←0

INSTRUCTION CODE TABLE

D_3–D_0 \ D_9–D_4	Hexadecimal notation	000000	000001	000010	000011	000100	000101	000110	000111	001000	001001	001010	001011	001100	001101	001110	001111	010000 | 010111	011000 | 011111
		00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10 to 17	18 to 1F
0000	0	NOP	BLA	SZB 0	BMLA	—	TASP	A 0	LA 0	TABP 0	TABP 16	TABP 32**	TABP 48*	BML	BML	BL	BL	BM	B
0001	1	—	CLD	SZB 1	—	—	TAD	A 1	LA 1	TABP 1	TABP 17	TABP 33**	TABP 49*	BML	BML	BL	BL	BM	B
0010	2	POF	—	SZB 2	—	—	TAX	A 2	LA 2	TABP 2	TABP 18	TABP 34**	TABP 50*	BML	BML	BL	BL	BM	B
0011	3	SNZP	INY	SZB 3	—	—	TAZ	A 3	LA 3	TABP 3	TABP 19	TABP 35**	TABP 51*	BML	BML	BL	BL	BM	B
0100	4	DI	RD	SZD	—	RT	TAV1	A 4	LA 4	TABP 4	TABP 20	TABP 36**	TABP 52*	BML	BML	BL	BL	BM	B
0101	5	EI	SD	SEAn	—	RTS	—	A 5	LA 5	TABP 5	TABP 21	TABP 37**	TABP 53*	BML	BML	BL	BL	BM	B
0110	6	RC	—	SEAM	—	RTI	—	A 6	LA 6	TABP 6	TABP 22	TABP 38**	TABP 54*	BML	BML	BL	BL	BM	B
0111	7	SC	DEY	—	—	—	—	A 7	LA 7	TABP 7	TABP 23	TABP 39**	TABP 55*	BML	BML	BL	BL	BM	B
1000	8	POF2	AND	—	SNZ0	LZ 0	—	A 8	LA 8	TABP 8	TABP 24	TABP 40**	TABP 56*	BML	BML	BL	BL	BM	B
1001	9	—	OR	TDA	—	LZ 1	—	A 9	LA 9	TABP 9	TABP 25	TABP 41**	TABP 57*	BML	BML	BL	BL	BM	B
1010	A	AM	TEAB	TABE	—	LZ 2	—	A 10	LA 10	TABP 10	TABP 26	TABP 42**	TABP 58*	BML	BML	BL	BL	BM	B
1011	B	AMC	—	—	—	LZ 3	—	A 11	LA 11	TABP 11	TABP 27	TABP 43**	TABP 59*	BML	BML	BL	BL	BM	B
1100	C	TYA	CMA	—	—	RB 0	SB 0	A 12	LA 12	TABP 12	TABP 28	TABP 44**	TABP 60*	BML	BML	BL	BL	BM	B
1101	D	—	RAR	—	—	RB 1	SB 1	A 13	LA 13	TABP 13	TABP 29	TABP 45**	TABP 61*	BML	BML	BL	BL	BM	B
1110	E	TBA	TAB	—	—	RB 2	SB 2	A 14	LA 14	TABP 14	TABP 30	TABP 46**	TABP 62*	BML	BML	BL	BL	BM	B
1111	F	—	TAY	SZC	TV1A	RB 3	SB 3	A 15	LA 15	TABP 15	TABP 31	TABP 47**	TABP 63*	BML	BML	BL	BL	BM	B

The above table shows the relationship between machine language codes and machine language instructions. D_3–D_0 show the low-order 4 bits of the machine language code, and D_9–D_4 show the high-order 6 bits of the machine language code. The hexadecimal representation of the code is also provided. There are one-word instructions and two-word instructions, but only the first word of each instruction is shown. Do not use the code marked "—".

The codes for the second word of a two-word instruction are described below.

	The second word
BL	1 0 p a a a a a a a
BML	1 0 p a a a a a a a
BLA	1 0 p p p 0 0 p p p p
BMLA	1 0 p p p 0 0 p p p p
SEA	0 0 0 1 1 1 n n n n
SZD	0 0 0 0 1 0 1 0 1 1

** and * cannot be used at M34550M4A-XXXFP.
* cannot be used at M34550M6A-XXXFP.

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D_3—D_0 \ D_9—D_4	Hexadecimal notation	100000	100001	100010	100011	100100	100101	100110	100111	101000	101001	101010	101011	101100	101101	101110	101111	110000 111111
		20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30 to 3F
0000	0	—	TW3A	OP0A	—	—	—	IAP0	—	SNZT 1	—	WRST	TMA 0	TAM 0	XAM 0	XAMI 0	XAMD 0	LXY
0001	1	—	—	OP1A	—	—	—	IAP1	—	SNZT 2	—	—	TMA 1	TAM 1	XAM 1	XAMI 1	XAMD 1	LXY
0010	2	—	—	—	T3AB	—	TAMR	IAP2	TAB3	SNZT 3	—	—	TMA 2	TAM 2	XAM 2	XAMI 2	XAMD 2	LXY
0011	3	—	—	—	—	—	TAI1	IAP3	—	—	—	—	TMA 3	TAM 3	XAM 3	XAMI 3	XAMD 3	LXY
0100	4	—	—	—	—	—	—	IAP4	—	—	—	—	TMA 4	TAM 4	XAM 4	XAMI 4	XAMD 4	LXY
0101	5	—	—	—	—	—	—	—	—	—	—	TPTA	TMA 5	TAM 5	XAM 5	XAMI 5	XAMD 5	LXY
0110	6	—	TMRA	—	—	—	—	—	—	—	—	TR1A	TMA 6	TAM 6	XAM 6	XAMI 6	XAMD 6	LXY
0111	7	—	TI1A	—	—	—	—	—	—	—	—	—	TMA 7	TAM 7	XAM 7	XAMI 7	XAMD 7	LXY
1000	8	—	—	—	—	—	—	—	—	—	STCR	TC1A	TMA 8	TAM 8	XAM 8	XAMI 8	XAMD 8	LXY
1001	9	—	—	—	—	—	—	—	—	—	SPCR	TC2A	TMA 9	TAM 9	XAM 9	XAMI 9	XAMD 9	LXY
1010	A	TL1A	—	—	—	TAL1	—	—	—	—	—	TPAA	TMA 10	TAM 10	XAM 10	XAMI 10	XAMD 10	LXY
1011	B	TL2A	—	—	—	TAW1	—	—	—	—	—	T1R1	TMA 11	TAM 11	XAM 11	XAMI 11	XAMD 11	LXY
1100	C	TL3A	—	—	—	TAW2	—	—	—	—	—	RC3	TMA 12	TAM 12	XAM 12	XAMI 12	XAMD 12	LXY
1101	D	TLCA	—	—	—	TAW3	—	—	—	—	—	SC3	TMA 13	TAM 13	XAM 13	XAMI 13	XAMD 13	LXY
1110	E	TW1A	—	—	—	—	—	—	—	—	—	RC4	TMA 14	TAM 14	XAM 14	XAMI 14	XAMD 14	LXY
1111	F	TW2A	—	—	TR1AB	—	—	—	—	—	—	SC4	TMA 15	TAM 15	XAM 15	XAMI 15	XAMD 15	LXY

The above table shows the relationship between machine language codes and machine language instructions. D_3—D_0 show the low-order 4 bits of the machine language code, and D_9—D_4 show the high-order 6 bits of the machine language code. The hexadecimal representation of the code is also provided. There are one-word instructions and two-word instructions, but only the first word of each instruction is shown. Do not use the code marked "—".

The codes for the second word of a two-word instruction are described below.

	The second word
BL	1 0 P a a a a a a a a
BML	1 0 P a a a a a a a a
BLA	1 0 P P 0 0 P P P P
BMLA	1 0 P P 0 0 P P P P
SEA	0 0 0 1 1 1 n n n n
SZD	0 0 0 0 1 0 1 0 1 1

MACHINE INSTRUCTIONS

Type of instructions	Mnemonic	Instruction code D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal notation			Number of words	Number of cycles	Functions
Register to register transfer	TAB	0	0	0	0	0	1	1	1	1	0	0	1	E	1	1	(A)←(B)
	TBA	0	0	0	0	0	0	1	1	1	0	0	0	E	1	1	(B)←(A)
	TAY	0	0	0	0	0	1	1	1	1	1	0	1	F	1	1	(A)←(Y)
	TYA	0	0	0	0	0	0	1	1	0	0	0	0	C	1	1	(Y)←(A)
	TEAB	0	0	0	0	0	1	1	0	1	0	0	1	A	1	1	$(E_7-E_4)\leftarrow(B)$, $(E_3-E_0)\leftarrow(A)$
	TABE	0	0	0	0	1	0	1	0	1	0	0	2	A	1	1	$(B)\leftarrow(E_7-E_4)$, $(A)\leftarrow(E_3-E_0)$
	TDA	0	0	0	0	1	0	1	0	0	1	0	2	9	1	1	$(DR_2-DR_0)\leftarrow(A_2-A_0)$
	TAD	0	0	0	1	0	1	0	0	0	1	0	5	1	1	1	$(A_2-A_0)\leftarrow(DR_2-DR_0)$, $(A_3)\leftarrow 0$
	TAZ	0	0	0	1	0	1	0	0	1	1	0	5	3	1	1	$(A_1, A_0)\leftarrow(Z_1, Z_0)$ $(A_3, A_2)\leftarrow 0$
	TAX	0	0	0	1	0	1	0	0	1	0	0	5	2	1	1	(A)←(X)
	TASP	0	0	0	1	0	1	0	0	0	0	0	5	0	1	1	$(A_2-A_0)\leftarrow(SP_2-SP_0)$ $(A_3)\leftarrow 0$
RAM addresses	LXY x, y	1	1	x_3	x_2	x_1	x_0	y_3	y_2	y_1	y_0	3	x	y	1	1	(X)←x, x= 0 to 15 (Y)←y, y= 0 to 15
	LZ z	0	0	0	1	0	0	1	0	z_1	z_0	0	4	8+z	1	1	(Z)←z, z= 0 to 3
	INY	0	0	0	0	0	1	0	0	1	1	0	1	3	1	1	(Y)←(Y)+1
	DEY	0	0	0	0	0	1	0	1	1	1	0	1	7	1	1	(Y)←(Y)−1
RAM to register transfer	TAM j	1	0	1	1	0	0	j	j	j	j	2	C	j	1	1	(A)←(M(DP)) (X)←(X)EXOR(j), j= 0 to 15
	XAM j	1	0	1	1	0	1	j	j	j	j	2	D	j	1	1	(A)⟷(M(DP)) (X)←(X)EXOR(j), j= 0 to 15
	XAMD j	1	0	1	1	1	1	j	j	j	j	2	F	j	1	1	(A)⟷(M(DP)) (X)←(X)EXOR(j), j= 0 to 15 (Y)←(Y)−1
	XAMI j	1	0	1	1	1	0	j	j	j	j	2	E	j	1	1	(A)⟷(M(DP)) (X)←(X)EXOR(j), j= 0 to 15 (Y)←(Y)+1
	TMA j	1	0	1	0	1	1	j	j	j	j	2	B	j	1	1	(M(DP))←(A) (X)←(X)EXOR(j), j= 0 to 15
Arithmetic operation	LA n	0	0	0	1	1	1	n	n	n	n	0	7	n	1	1	(A)←n, However, n= 0 to 15
	TABP p	0	0	1	0	p_5	p_4	p_3	p_2	p_1	p_0	0	8	p+p	1	3	(SP)←(SP)+1 (SK(SP))←(PC) $(PC_H)\leftarrow p$ $(PC_L)\leftarrow(DR_2-DR_0, A_3-A_0)$ $(B)\leftarrow(ROM(PC))_{7\text{ to }4}$ $(A)\leftarrow(ROM(PC))_{3\text{ to }0}$ (PC)←(SK(SP)) (SP)←(SP)−1 (Note)
	AM	0	0	0	0	0	0	1	0	1	0	0	0	A	1	1	(A)←(A)+(M(DP))

Note : p is 0 to 63 for M34550M8A.
p is 0 to 47 for M34550M6A.
p is 0 to 31 for M34550M4A.

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Skip condition	Carry flag CY	Detailed description
—	—	Transfers the contents of register B to register A.
—	—	Transfers the contents of register A to register B.
—	—	Transfers the contents of register Y to register A.
—	—	Transfers the contents of register A to register Y.
—	—	Transfers the contents of registers A and B to register E.
—	—	Transfers the contents of register E to registers A and B.
—	—	Transfers the contents of register A to register D.
—	—	Transfers the contents of register D to register A.
—	—	Transfers the contents of register Z to register A.
—	—	Transfers the contents of register X to register A.
—	—	Transfers the contents of stack pointer (SP) to register A.
Continuous description	—	Loads the value x in the immediate field to register X, and the value y in the immediate field to register Y. When the LXY instructions are continuously coded and executed, only the first LXY instruction is executed and other LXY instructions coded continuously are skipped.
—	—	Loads the value z in the immediate field to register Z.
(Y) = 0	—	Adds 1 to the contents of register Y. As a result of addition, when the contents of register Y is 0, the next instruction is skipped.
(Y) = 15	—	Subtracts 1 from the contents of register Y. As a result of subtraction, when the contents of register Y is 15, the next instruction is skipped.
—	—	After transferring the contents of M(DP) to register A, an exclusive OR operation is performed between register X and the value j in the immediate field, and stores the result in register X.
—	—	After exchanging the contents of M(DP) with the contents of register A, an exclusive OR operation is performed between register X and the value j in the immediate field, and stores the result in register X.
(Y) = 15	—	After exchanging the contents of M(DP) with the contents of register A, an exclusive OR operation is performed between register X and the value j in the immediate field, and stores the result in register X. Subtracts 1 from the contents of register Y. As a result of subtraction, when the contents of register Y is 15, the next instruction is skipped.
(Y) = 0	—	After exchanging the contents of M(DP) with the contents of register A, an exclusive OR operation is performed between register X and the value j in the immediate field, and stores the result in register X. Adds 1 to the contents of register Y. As a result of addition, when the contents of register Y is 0, the next instruction is skipped.
—	—	After transferring the contents of register A to M(DP), an exclusive OR operation is performed between register X and the value j in the immediate field, and stores the result in register X.
Continuous description	—	Loads the value n in the immediate field to the register A. When the LA instructions are continuously coded and executed, only the first LA instruction is executed and other LA instructions coded continuously are skipped.
—	—	Transfers bits 7 to 4 to register B and bits 3 to 0 to register A. These bits 7 to 0 are the ROM pattern in address (DR_2 DR_1 DR_0 A_3 A_2 A_1 A_0) specified by registers A and D in page p. When this instruction is executed, 1 stage of stack register is used.
—	—	Adds the contents of M(DP) to register A. Stores the result in register A. The contents of carry flag CY remains unchanged.

Type of instructions \ Parameter	Mnemonic	Instruction code D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal notation			Number of words	Number of cycles	Functions
Arithmetic operation	AMC	0	0	0	0	0	0	1	0	1	1	0	0	B	1	1	(A)←(A)+(M(DP))+(CY) (CY)←Carry
	An	0	0	0	1	1	0	n	n	n	n	0	6	n	1	1	(A)←(A)+n However, n= 0 to 15
	AND	0	0	0	0	0	1	1	0	0	0	0	1	8	1	1	(A)←(A) AND (M(DP))
	OR	0	0	0	0	0	1	1	0	0	1	0	1	9	1	1	(A)←(A) OR (M(DP))
	SC	0	0	0	0	0	0	0	1	1	1	0	0	7	1	1	(CY)←1
	RC	0	0	0	0	0	0	0	1	1	0	0	0	6	1	1	(CY)←0
	SZC	0	0	0	0	1	0	1	1	1	1	0	2	F	1	1	(CY)=0 ?
	CMA	0	0	0	0	0	1	1	1	0	0	0	1	C	1	1	(A)←($\overline{A}$)
	RAR	0	0	0	0	0	1	1	1	0	1	0	1	D	1	1	CY → $A_3A_2A_1A_0$
Bit operation	SB j	0	0	0	1	0	1	1	1	j	j	0	5	C+j	1	1	(Mj(DP))←1 j= 0 to 3
	RB j	0	0	0	1	0	0	1	1	j	j	0	4	C+j	1	1	(Mj(DP))←0 j= 0 to 3
	SZB j	0	0	0	0	1	0	0	0	j	j	0	2	j	1	1	(Mj(DP))= 0 ? j= 0 to 3
Comparison operation	SEAM	0	0	0	0	1	0	0	1	1	0	0	2	6	1	1	(A)=(M(DP)) ?
	SEA n	0	0	0	0	1	0	0	1	0	1	0	2	5	2	2	(A)=n ?
		0	0	0	1	1	1	n	n	n	n	0	7	n			However, n= 0 to 15
Branch operation	Ba	0	1	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	1	8	a+a	1	1	(PC_L)←a_6–a_0
	BL p, a	0	0	1	1	1	p_4	p_3	p_2	p_1	p_0	0	E	p+p	2	2	(PC_H)←p (PC_L)←a_6–a_0 (Note)
		1	0	p_5	a_6	a_5	a_4	a_3	a_2	a_1	a_0	2	p	a+a			
	BLA p	0	0	0	0	0	1	0	0	0	0	0	1	0	2	2	(PC_H)←p (PC_L)←(DR_2–DR_0, A_3–A_0) (Note)
		1	0	p_5	p_4	0	0	p_3	p_2	p_1	p_0	2	p	p			
Subroutine operation	BM a	0	1	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	1	a	a	1	1	(SP)←(SP)+1 (SK(SP))←(PC) (PC_H)←2, (PC_L)←a_6–a_0
	BML p, a	0	0	1	1	0	p_4	p_3	p_2	p_1	p_0	0	C	p+p	2	2	(SP)←(SP)+1 (SK(SP))←(PC) (PC_H)←p, (PC_L)←a_6–a_0 (Note)
		1	0	p_5	a_6	a_5	a_4	a_3	a_2	a_1	a_0	2	p	a+a			
	BMLA p	0	0	0	0	1	1	0	0	0	0	0	3	0	2	2	(SP)←(SP)+1 (SK(SP))←(PC)
		1	0	p_5	p_4	0	0	p_3	p_2	p_1	p_0	2	p	p			(PC_H)←p (PC_L)←(DR_2–DR_0, A_3–A_0) (Note)

Note : p is 0 to 63 for M34550M8A.
p is 0 to 47 for M34550M6A.
p is 0 to 31 for M34550M4A.

Skip condition	Carry flag CY	Detailed description
—	0/1	Adds the contents of M(DP) and the contents of carry flag CY to register A. Stores the result in register A and carry flag CY.
Overflow= 0	—	Adds the value n in the immediate field to register A. The contents of carry flag CY remains unchanged. Skips the next instruction when there is no overflow as the result of operation.
—	—	Takes the AND operation between the contents of register A and the contents of M(DP), and stores the result in register A.
—	—	Takes the OR operation between the contents of register A and the contents of M(DP), and stores the result in register A.
—	1	Carry flag CY is set to 1.
—	0	Carry flag CY is cleared to 0.
(CY)= 0	—	Skips the next instruction when the contents of carry flag CY is 0.
—	—	Stores the one's complement for register A's contents in register A.
—	0/1	Rotates 1 bit of the contents of register A including the contents of the carry flag CY to the right.
—	—	Sets (1) to the contents of bit j (bit specified by the value j in the immediate field) of M(DP).
—	—	Clears (0) the contents of bit j (bit specified by the value j in the immediate field) of M(DP).
(Mj(DP))= 0 , j= 0 to 3	—	Skips the next instruction when the contents of bit j (bit specified by the value j in the immediate field) of M(DP) is "0".
(A)=(M(DP))	—	Skips the next instruction when the contents of register A is equal to the contents of M(DP).
(A)=n	—	Skips the next instruction when the contents of register A is equal to the value n in the immediate field.
—	—	Branch within a page : Branches to address a in the identical page.
—	—	Branch out of a page : Branches to address a in page p.
—	—	Branch out of a page : Branches to address (address DR_2 DR_1 DR_0 A_3 A_2 A_1 $A_0)_2$ specified by registers D and A in page p.
—	—	Call the subroutine in page 2 : Calls the subroutine at address a in page 2.
—	—	Call the subroutine : Calls the subroutine at address a in page p.
—	—	Call the subroutine : Calls the subroutine at address (address DR_2 DR_1 DR_0 A_3 A_2 A_1 $A_0)_2$ specified by registers A and D in page p.

Type of instruction	Mnemonic	Instruction code D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal notation	Number of words	Number of cycles	Functions
Return operation	RTI	0	0	0	1	0	0	0	1	1	0	0 4 6	1	1	(PC)←(SK(SP)) (SP)←(SP)−1
	RT	0	0	0	1	0	0	0	1	0	0	0 4 4	1	2	(PC)←(SK(SP)) (SP)←(SP)−1
	RTS	0	0	0	1	0	0	0	1	0	1	0 4 5	1	2	(PC)←(SK(SP)) (SP)←(SP)−1
Interrupt operation	DI	0	0	0	0	0	0	0	1	0	0	0 0 4	1	1	(INTE)←0
	EI	0	0	0	0	0	0	0	1	0	1	0 0 5	1	1	(INTE)←1
	SNZ0	0	0	0	0	1	1	1	0	0	0	0 3 8	1	1	(EXF0)=1 ? After skipping (EXF0)←0
	TV1A	0	0	0	0	1	1	1	1	1	1	0 3 F	1	1	(V1)←(A)
	TI1A	1	0	0	0	0	1	0	1	1	1	2 1 7	1	1	(I1)←(A)
	TAV1	0	0	0	1	0	1	0	1	0	0	0 5 4	1	1	(A)←(V1)
	TAI1	1	0	0	1	0	1	0	0	1	1	2 5 3	1	1	(A)←(I1)
Timer operation	TW1A	1	0	0	0	0	0	1	1	1	0	2 0 E	1	1	(W1)←(A)
	TW2A	1	0	0	0	0	0	1	1	1	1	2 0 F	1	1	(W2)←(A)
	TW3A	1	0	0	0	0	1	0	0	0	0	2 1 0	1	1	(W3)←(A)
	TAW1	1	0	0	1	0	0	1	0	1	1	2 4 B	1	1	(A)←(W1)
	TAW2	1	0	0	1	0	0	1	1	0	0	2 4 C	1	1	(A)←(W2)
	TAW3	1	0	0	1	0	0	1	1	0	1	2 4 D	1	1	(A)←(W3)
	T3AB	1	0	0	0	1	1	0	0	1	0	2 3 2	1	1	($R3_7$—$R3_4$)←(B), ($T3_7$—$T3_4$)←(B) ($R3_3$—$R3_0$)←(A), ($T3_3$—$T3_0$)←(A)
	T1R1	1	0	1	0	1	0	1	0	1	1	2 A B	1	1	(T1)←(R1)
	TR1AB	1	0	0	0	1	1	1	1	1	1	2 3 F	1	1	($R1_7$—$R1_4$)←(B), ($R1_3$—$R1_0$)←(A)
	TR1A	1	0	1	0	1	0	0	1	1	0	2 A 6	1	1	($R1_8$)←(A_0)
	TAB3	1	0	0	1	1	1	0	0	1	0	2 7 2	1	1	(B)←($T3_7$—$T3_4$), (A)←($T3_3$—$T3_0$)
	SNZT1	1	0	1	0	0	0	0	0	0	0	2 8 0	1	1	(T1F)=1 ? After skipping (T1F)←0
	SNZT2	1	0	1	0	0	0	0	0	0	1	2 8 1	1	1	(T2F)=1 ? After skipping (T2F)←0
	SNZT3	1	0	1	0	0	0	0	0	1	0	2 8 2	1	1	(T3F)=1 ? After skipping (T3F)←0
Input/Output operation	IAP0	1	0	0	1	1	0	0	0	0	0	2 6 0	1	1	(A)←(P0)
	IAP1	1	0	0	1	1	0	0	0	0	1	2 6 1	1	1	(A)←(P1)
	IAP2	1	0	0	1	1	0	0	0	1	0	2 6 2	1	1	(A)←(P2)
	IAP3	1	0	0	1	1	0	0	0	1	1	2 6 3	1	1	(A_1, A_0)←($P3_1$, $P3_0$) (A_3, A_2)←0
	IAP4	1	0	0	1	1	0	0	1	0	0	2 6 4	1	1	(A)←(P4)
	CLD	0	0	0	0	0	1	0	0	0	1	0 1 1	1	1	(D)←1
	RD	0	0	0	0	0	1	0	1	0	0	0 1 4	1	1	(D(Y))←0 (Y)=0 to 12
	SD	0	0	0	0	0	1	0	1	0	1	0 1 5	1	1	(D(Y))←1 (Y)=0 to 12
	SZD	0	0	0	0	1	0	0	1	0	0	0 2 4	2	2	(D(Y))=0 ? (Y)=8 to 10
		0	0	0	0	1	0	1	0	1	1	0 2 B			(P0)←(A)
	OP0A	1	0	0	0	1	0	0	0	0	0	2 2 0	1	1	(P1)←(A)
	OP1A	1	0	0	0	1	0	0	0	0	1	2 2 1	1	1	

Skip condition	Carry flag CY	Detailed description
—	—	Returns from interrupt service routine to main routine.
		Returns each value of data pointer (X, Y, Z), carry flag, skip status, NOP mode status by the continuous description of the LA/LXY instruction, registers A and B to the states just before interrupt.
—	—	Returns from subroutine to the routine called the subroutine.
Skip at uncondition	—	Returns from subroutine to the routine called the subroutine, and skips the next instruction at uncondition.
—	—	Clears (0) to the interrupt enable flag INTE, and disables the interrupt.
—	—	Sets (1) to the interrupt enable flag INTE, and enables the interrupt.
(EXF0) = 1	—	Skips the next instruction when the contents of EXF0 flag is "1".
		After skipping, clears the EXF0 flag.
—	—	Transfers the contents of register A to interrupt control register V1.
—	—	Transfers the contents of register A to interrupt control register I1.
—	—	Transfers the contents of interrupt control register V1 to register A.
—	—	Transfers the contents of interrupt control register I1 to register A.
—	—	Transfers the contents of register A to timer control register W1.
—	—	Transfers the contents of register A to timer control register W2.
—	—	Transfers the contents of register A to timer control register W3.
—	—	Transfers the contents of timer control register W1 to register A.
—	—	Transfers the contents of timer control register W2 to register A.
—	—	Transfers the contents of timer control register W3 to register A.
—	—	Transfers the contents of registers A and B to timer 3 and the reload register R3.
—	—	Transfers the reload register value to timer 1.
—	—	Transfers the contents of registers A and B to reload register R1.
—	—	Transfers the contents of register A to reload register R1.
—	—	Transfers the contents of timer 3 to registers A and B.
(T1F) = 1	—	Skips the next instruction when the contents of T1F flag is "1". Clears the T1F flag after skipping.
(T2F) = 1	—	Skips the next instruction when the contents of T2F flag is "1". Clears the T2F flag after skipping.
(T3F) = 1	—	Skips the next instruction when the contents of T3F flag is "1". Clears the T3F flag after skipping.
—	—	Transfers input to port P0 to register A.
—	—	Transfers input to port P1 to register A.
—	—	Transfers input to port P2 to register A.
—	—	Transfers input to port P3 to register A.
—	—	Transfers input to port P4 to register A.
—	—	Sets (1) port D.
—	—	Clears (0) to a bit of port D specified by register Y.
—	—	Sets (1) a bit of port D specified by register Y.
(D(Y)) = 0, (Y) = 8 to 10	—	When the contents of a bit of port D specified by register Y is "0", skips the next instruction.
—	—	Outputs the contents of register A to port P0.
—	—	Outputs the contents of register A to port P1.

Parameter / Type of instructions	Mnemonic	Instruction code										Hexadecimal notation			Number of words	Number of cycles	Functions
		D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0						
LCD control operation	TL1A	1	0	0	0	0	0	1	0	1	0	2	0	A	1	1	(L1)←(A)
	TAL1	1	0	0	1	0	0	1	0	1	0	2	4	A	1	1	(A)←(L1)
	TL2A	1	0	0	0	0	0	1	0	1	1	2	0	B	1	1	(L2)←(A)
	TL3A	1	0	0	0	0	0	1	1	0	0	2	0	C	1	1	(L3)←(A_0)
	TLCA	1	0	0	0	0	0	1	1	0	1	2	0	D	1	1	(LC)←(A)
Multi-carrier generating circuit operation	TPTA	1	0	1	0	1	0	0	1	0	1	2	A	5	1	1	(PT)←(A_1, A_0)
	TC1A	1	0	1	0	1	0	1	0	0	0	2	A	8	1	1	(C1)←(A)
	TPAA	1	0	1	0	1	0	1	0	1	0	2	A	A	1	1	(PA)←(A)
	RC3	1	0	1	0	1	0	1	1	0	0	2	A	C	1	1	(C3)←0
	SC3	1	0	1	0	1	0	1	1	0	1	2	A	D	1	1	(C3)←1
	RC4	1	0	1	0	1	0	1	1	1	0	2	A	E	1	1	(C4)←0
	SC4	1	0	1	0	1	0	1	1	1	1	2	A	F	1	1	(C4)←1
	STCR	1	0	1	0	0	1	1	0	0	0	2	9	8	1	1	Carrier wave generating start
	SPCR	1	0	1	0	0	1	1	0	0	1	2	9	9	1	1	Carrier wave generating stop
	TC2A	1	0	1	0	1	0	1	0	0	1	2	A	9	1	1	(C2)←(A_1, A_0)
Other operation	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	(PC)←(PC)+1
	POF	0	0	0	0	0	0	0	0	1	0	0	0	2	1	1	Power down 1
	POF2	0	0	0	0	0	0	1	0	0	0	0	0	8	1	1	Power down 2
	SNZP	0	0	0	0	0	0	0	0	1	1	0	0	3	1	1	(P)=1 ?
	TMRA	1	0	0	0	0	1	0	1	1	0	2	1	6	1	1	(MR_2—MR_0)←(A_2—A_0)
	TAMR	1	0	0	1	0	1	0	0	1	0	2	5	2	1	1	(A_2—A_0)←(MR_2—MR_0), (A_3)←0
	WRST	1	0	1	0	1	0	0	0	0	0	2	A	0	1	1	(WDF)←0

Skip condition	Carry flag CY	Detailed description
—	—	Transfers the contents of register A to LCD control register L1.
—	—	Transfers the contents of LCD control register L1 to register A.
—	—	Transfers the contents of register A to LCD control register L2.
—	—	Transfers the contents of register A to LCD control register L3.
—	—	Transfers the contents of register A to LC counter and reload register.
—	—	Transfers the contents of register A to compensation control timer PT.
—	—	Transfers the contents of register A to data control register C1.
—	—	Transfers the contents of register A to preset register PA.
—	—	Clears (0) the output control flag C3 and disables carrier wave output.
—	—	Sets (1) the output control flag C3 and enables carrier wave output.
—	—	Clears (0) to data of data control flag C4.
—	—	Sets (1) to data of data control flag C4.
—	—	Starts generating of carrier wave.
—	—	Stops generating of carrier wave.
—	—	Transfers the contents of register A to compensation control register C2.
—	—	No operation
—	—	Puts the system in power down 1 state (clock operating mode) f(X_{CIN}) oscillation, LCD, timer 2 and timer 3 can be used.
—	—	Puts the system in power down 2 state (RAM back-up mode). Oscillations are all stopped.
(P)= 1	—	Skips the next instruction when the contents of P flag is "1". After skipping, the contents of P flag remains unchanged.
—	—	Transfers the contents of register A to clock control register MR.
—	—	Transfers the contents of clock control register MR to register A.
—	—	Clears watchdog flag WDF.

CONTROL REGISTERS

Interrupt control register V1		at reset : 0000_2	at power down : 0000_2	R/W
$V1_3$	Not used	0 / 1	This bit has no function, but R/W is enabled.	
$V1_2$	Timer 3 interrupt enable bit	0	Interrupt disabled (SNZT3 instruction is valid)	
		1	Interrupt enabled (SNZT3 instruction is invalid)	
$V1_1$	Timer 1 interrupt enable bit	0	Interrupt disabled (SNZT1 instruction is valid)	
		1	Interrupt enabled (SNZT1 instruction is invalid)	
$V1_0$	External interrupt enable bit	0	Interrupt disabled (SNZ0 instruction is valid)	
		1	Interrupt enabled (SNZ0 instruction is invalid)	

Interrupt control register I1		at reset : 0000_2	at power down : state retained	R/W
$I1_3$	$P3_0$/INT pin dynamic pull-up control bit	0	Dynamic pull-up disabled	
		1	Dynamic pull-up enabled	
$I1_2$	$P3_0$/INT pin return input level selection bit	0	Return from power down state by inputting "L" level	
		1	Return from power down state by inputting "H" level	
$I1_1$	$P3_1$ pin pull-up transistor control bit	0	OFF	
		1	ON	
$I1_0$	$P3_0$/INT pin pull-up transistor control bit	0	OFF	
		1	ON	

Clock control register MR		at reset : 000_2	at power down : state retained	R/W
MR_2	Not used	0 / 1	This bit has no function, but R/W is enabled.	
MR_1	$f(X_{IN})$ clock oscillation circuit control bit	0	Oscillation enabled	
		1	Oscillation disabled	
MR_0	*System clock selection bit*	0	$f(X_{IN})$	
		1	$f(X_{CIN})$	

Timer control register W1		at reset : 0000_2	at power down : 0000_2	R/W
$W1_3$	Timer 1 count source selection bit	0	Prescaler output (ORCLK)	
		1	Multi-carrier output (CARR)	
$W1_2$	Timer 1 control bit	0	Stop (state retained)	
		1	Operating	
$W1_1$ / $W1_0$	Prescaler frequency dividing ratio selection bits	$W1_1$ $W1_0$	Frequency dividing ratio	
		0 0	Prescaler stop (reset state)	
		0 1	$f(X_{IN})$ or $f(X_{CIN})$ divided by 2 (Note 2)	
		1 0	$f(X_{IN})$ or $f(X_{CIN})$ divided by 4 (Note 2)	
		1 1	$f(X_{IN})$ or $f(X_{CIN})$ divided by 8 (Note 2)	

Notes 1. "R" represents read enabled, and "W" represents write enabled.
2. The signal in $f(X_{IN})$ or $f(X_{CIN})$ selected as system clock is used.

Timer control register W2		at reset : 0000_2		at power down : state retained	R/W
$W2_3$	Timer 3 control bit	0	Stop (state retained)		
		1	Operating		
$W2_2$	Timer 3 count source selection bit	0	Timer 2 underflow signal		
		1	Prescaler output (ORCLK)		
$W2_1$	Timer 2 control bit	0	Stop (reset state)		
		1	Operating		
$W2_0$	Timer 2 count source selection bit	0	$f(X_{CIN})$		
		1	Prescaler output (frequency divided by 8 output)		

Timer control register W3		at reset : 0000_2		at power down : state retained	R/W
$W3_3$	BEEP output control bit	0	Output stop		
		1	Output		
$W3_2$	Watchdog timer control bit	0	Not used		
		1	Used		
$W3_1$	BEEP, LCD clock frequency dividing circuit control bits	$W3_1$ $W3_0$	Frequency dividing ratio		
$W3_0$		0 0	Stop		
		0 1	Timer 2 intermediate underflow (frequency divided by 16 output)		
		1 0	Timer 2 intermediate underflow (frequency divided by 16 output) divided by 2		
		1 1	Timer 2 intermediate underflow (frequency divided by 16 output) divided by 4		

Carrier wave data control register C1		at reset : 0000_2		at power down : 0000_2	W
$C1_3$	Carrier wave data compensation control bit	0	−1 compensation		
		1	+1 compensation		
$C1_2$	Carrier wave data register connection control bits	$C1_2$ $C1_1$ $C1_0$	The number of connection bits		
$C1_1$		0 0 0	2-bit connection (PA_L, PA_H are used)		
		0 0 1	3-bit connection (PA_L-PA_0 are used)		
$C1_0$		0 1 0	4-bit connection (PA_L-PA_1 are used)		
		0 1 1	5-bit connection (PA_L-PA_2 are used)		
		1 0 0	6-bit connection (PA_L-PA_3 are used)		
		Other combinations	Not available		

Carrier wave compensation control register C2		at reset : 00_2		at power down : 00_2	W
$C2_1$	Carrier wave automatic stop function control bit	0	Automatic stop function not used		
		1	Automatic stop function used		
$C2_0$	Carrier wave compensation control bit	0	Not compensated		
		1	Compensated		

Carrier wave output control flag C3		at reset : 0_2		at power down : 0_2	W
C3	(Carrier wave output control)	0	Carrier wave output disabled (RC3 instruction execution)		
		1	Carrier wave output (SC3 instruction execution)		

Carrier wave data control flag C4		at reset : 0_2		at power down : 0_2	W
C4	Carrier wave data control	0	Carrier wave data cleared (RC4 instruction execution)		
		1	Carrier wave data set (SC4 instruction execution)		

Carrier wave generating control flag CR		at reset : 0_2		at power down : 0_2	W
CR	Carrier wave generating control	0	Carrier wave generating stop (SPCR instruction execution)		
		1	Carrier wave generating start (STCR instruction execution)		

Note "R" represents read enabled, and "W" represents write enabled.

LCD control register L1		at reset : 0000_2	at power down : state retained	R/W
$L1_3$	LCD power supply dividing resistor control bit	0	Connecting internal dividing resistor to LCD power circuit	
		1	Disconnecting internal dividing resistor from LCD power circuit	
$L1_2$	LCD ON/OFF bit	0	OFF	
		1	ON	
$L1_1$	LCD duty and bias selection bits	$L1_1$ $L1_0$	Duty	Bias
		0 0	Not available.	
$L1_0$		0 1	1/2	1/2
		1 0	1/3	1/3
		1 1	1/4	1/3

LCD control register L2		at reset : 0000_2	at power down : state retained	W
$L2_3$	$SEG_{39}/P4_3$ pin function switch bit	0	SEG_{39}	
		1	$P4_3$	
$L2_2$	$SEG_{38}/P4_2$ pin function switch bit	0	SEG_{38}	
		1	$P4_2$	
$L2_1$	$SEG_{37}/P4_1$ pin function switch bit	0	SEG_{37}	
		1	$P4_1$	
$L2_0$	$SEG_{36}/P4_0$ pin function switch bit	0	SEG_{36}	
		1	$P4_0$	

LCD control register L3		at reset : 0_2	at power down : state retained	W
L3	D_{12}, D_{11}/V_{LC2}, V_{LC1} pin function switch bit	0	D_{12}, D_{11}	
		1	V_{LC2}, V_{LC1}	

Note "R" represents read enabled, and "W" represents write enabled.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Rating	Unit
V_{DD}	Supply voltage		−0.3 to 7	V
V_I	Input voltage P0, P1, P2, D_8−D_{10}, P3, P4, $\overline{RESET}$, X_{IN}, X_{CIN}		−0.3 to V_{DD}+0.3	V
V_I	Input voltage V_{LC1}, V_{LC2}, V_{LC3}		−0.3 to V_{DD}+0.3	V
V_O	Output voltage P0, P1, D, $\overline{RESET}$	Output transistors in the cut-off state	−0.3 to V_{DD}+0.3	V
V_O	Output voltage CARR, X_{OUT}, X_{COUT}		−0.3 to V_{DD}+0.3	V
V_O	Output voltage SEG, COM		−0.3 to V_{LC3}+0.3	V
P_d	Power dissipation		300	mW
Topr	Operating temperature range		−20 to 70	℃
Tstg	Storage temperature range		−40 to 125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20℃ to 70℃, V_{DD}=2.2V to 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	f(X_{IN})=1.6MHz	2.2		3.6	V
V_{RAM}	RAM back-up voltage (at RAM back-up mode)		2.0		3.6	V
V_{SS}	Supply voltage			0		V
V_{LC3}	Supply voltage for LCD (Note 1)		2.2		3.6	V
V_{IH}	"H" level input voltage P0, P1, P2, P3, P4, D_8−D_{10}	V_{DD}=3.0V	0.8V_{DD}		V_{DD}	V
V_{IH}	"H" level input voltage X_{IN}		0.7V_{DD}		V_{DD}	V
V_{IH}	"H" level input voltage $\overline{RESET}$		0.85V_{DD}		V_{DD}	V
V_{IH}	"H" level input voltage INT		0.8V_{DD}		V_{DD}	V
V_{IL}	"L" level input voltage P0, P1, P2, P3, P4, D_8−D_{10}		0		0.3V_{DD}	V
V_{IL}	"L" level input voltage X_{IN}		0		0.3V_{DD}	V
V_{IL}	"L" level input voltage $\overline{RESET}$		0		0.3V_{DD}	V
V_{IL}	"L" level input voltage INT		0		0.2V_{DD}	V
$I_{OL(peak)}$	"L" level peak output current P0, P1, D_0−D_7, D_{10}−D_{12}, CARR, $\overline{RESET}$				4	mA
$I_{OL(peak)}$	"L" level peak output current D_8, D_9				24	mA
$I_{OL(avg)}$	"L" level average output current P0, P1, D_0−D_7, D_{10}−D_{12}, CARR, $\overline{RESET}$				2	mA
$I_{OL(avg)}$	"L" level average output current D_8, D_9				12	mA
$I_{OH(peak)}$	"H" level peak output current CARR		−30			mA
$I_{OH(avg)}$	"H" level average output current CARR		−15			mA
f(X_{IN})	f(X_{IN}) clock frequency	with a ceramic resonator			1.6	MHz
f(X_{IN})	f(X_{IN}) clock frequency (Note 2)	with external clock input			800	kHz
f(X_{CIN})	f(X_{CIN}) clock frequency (Note 3)	with a quartz-crystal oscillator	32		50	kHz

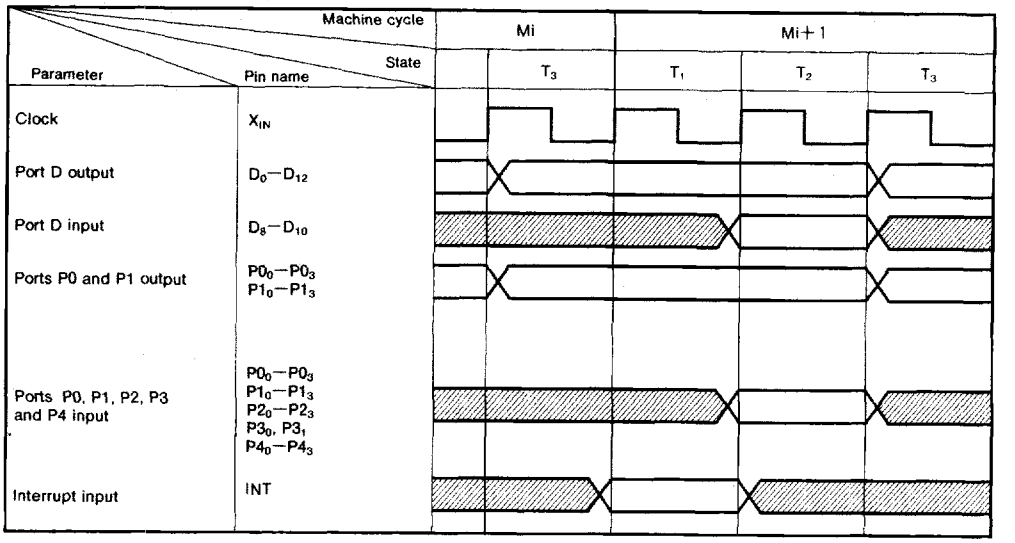
Note 1. at 1/2 bias : V_{LC1}=V_{LC2}=1/2 · V_{LC3}
at 1/3 bias : V_{LC1}=1/3 · V_{LC3}, V_{LC2}=2/3 · V_{LC3}
2. External clock duty is 30% to 70%.
3. External clock cannot be used as f(X_{CIN}) clock.

ELECTRICAL CHARACTERISTICS (T_a=−20℃ to 70℃, V_{DD}=3V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OL}	"L" level output voltage P0, P1, D_0–D_7, D_{10}–D_{12}, CARR, $\overline{RESET}$		I_{OL}=2mA			0.9	V
V_{OL}	"L" level output voltage D_8, D_9		I_{OL}=12mA			1.5	V
V_{OH}	"H" level output voltage CARR		I_{OH}=−7mA	1.0			V
I_{IH}	"H" level input current P0, P1, P2, P3, P4, D_8–D_{10}, $\overline{RESET}$		V_I=V_{DD} (Note 1)			1	μA
I_{IL}	"L" level input current P2, P3, P4, D_8–D_{10}, $\overline{RESET}$		V_I=0V (Note 1)	−1			μA
I_{OZ}	Output current at off-state D_0–D_7		V_O=V_{DD}			1	μA
I_{DD}	Supply current	at active high-speed mode	f(X_{IN})=1MHz f(X_{CIN})=32kHz		1	2	mA
			f(X_{IN})=500kHz f(X_{CIN})=32kHz		0.5	1.0	mA
		at active low-speed mode	f(X_{IN})=Stop f(X_{CIN})=32kHz		20	50	μA
		at power down 1 mode (LCD operation)	f(X_{IN})=Stop f(X_{CIN})=32kHz T_a=25℃		4	10	μA
			f(X_{IN})=Stop f(X_{CIN})=32kHz			15	μA
		at power down 2 mode	f(X_{IN})=Stop f(X_{CIN})=Stop T_a=25℃		0.1	1.0	μA
			f(X_{IN})=Stop f(X_{CIN})=Stop			10	μA
R_{PU}	Pull-up resistor value P0, P1, and P3		V_{DD}=3V V_I=0V	40	100	250	kΩ
V_{T+} − V_{T-}	Hysteresis INT				0.4		V
V_{T+} − V_{T-}	Hysteresis $\overline{RESET}$				0.7		V
R_{COM}	COM output impedance		(Note 2)		2	10	kΩ
R_{SEG}	SEG output impedance		(Note 2)		3	15	kΩ
R_{VLC}	Internal resistor value for LCD power (impedance between V_{LC3} and V_{SS})		T_a=25℃	300	600	1200	kΩ

Notes 1. In this case, port P4 is selected as input port with software.
2. External power is used for LCD power and measurement is performed with all pins freed except the measurement pin.

BASIC TIMING DIAGRAM



BUILT-IN PROM VERSION

In addition to the mask ROM versions, the 4550 Group has three programmable ROM versions software compatible with the Mask ROM. One is the window-type EPROM version supplied with a built-in EPROM which can be written to and erased. Others are the One Time PROM versions whose PROMs can only be written to and not be erased. Since the functions of the built-in EPROM and One Time PROM versions are exactly the same, except erasure, all of them are referred to as built-in PROM versions in this explanation, unless otherwise noted.

The built-in PROM versions have functions similar to those of the mask ROM versions, but they have PROM mode that enables writing to built-in PROM.

Table 13 shows the product of built-in PROM version.

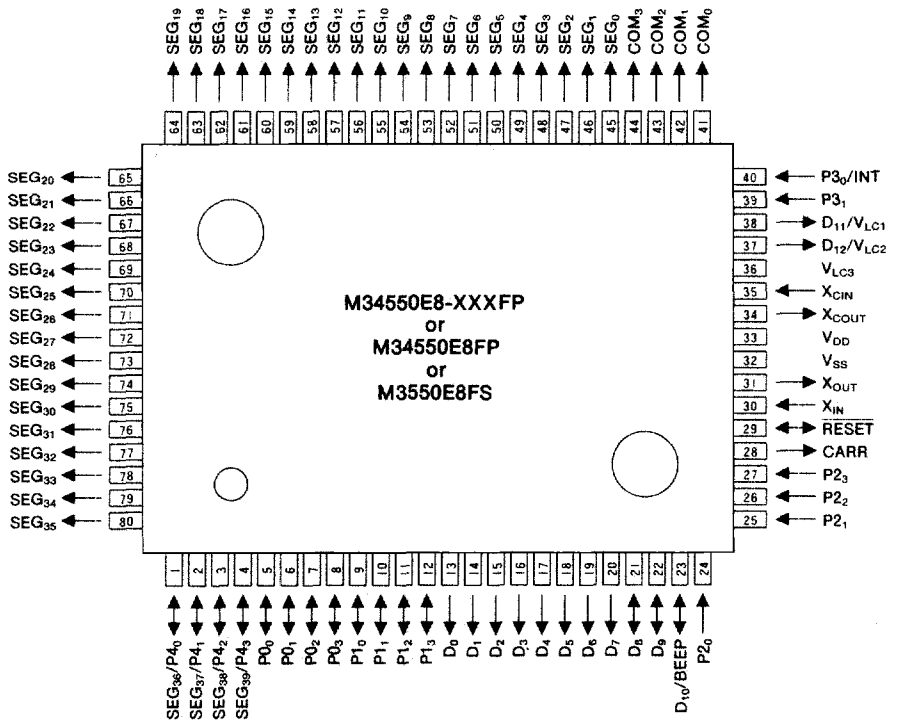
The One Time PROM versions have pin-compatibility with the mask ROM version. The built-in EPROM version has different outline.

Table 13 Product of built-in PROM version

Product	PROM size (×10 bits)	RAM size (×4 bits)	Package	Remarks
M34550E8-XXXFP	8192 words	368 words	80P6N-A	One Time PROM version (shipped after writing) (Shipping after writing and testing in factory)
M34550E8FP				One Time PROM version (shipped in blank)
M34550E8FS *			80D0	Built-in EPROM version

* : For program development only

PIN CONFIGURATION (TOP VIEW)



Outline 80P6N-A (One Time PROM version)
80D0 (Built-in EPROM version)

Fig. 53 Pin configuration of built-in PROM version

(1) PROM mode

Each built-in PROM version has a PROM mode in addition to a normal operation mode. The PROM mode is used to write to and read from the built-in PROM.

In the PROM mode, the programming adapter can be used with a general-purpose PROM programmer to write to or read from the built-in PROM as if it were M5M27C256K. Programming adapters are listed in table 14.

- Writing and reading of built-in PROM

  Programming voltage is 12.5V. Write the program in the PROM of the built-in PROM version as shown in Fig. 54.

- Erasing

  Only the built-in EPROM (M34550E8FS) version has a transparent window for erasing on the top surface of the package. The EPROM is erased when it is exposed to ultraviolet light with a wavelength of 2537Å to an integrated dose of 15W·s/cm^2 or more through the window.

(2) Notes on handling

① Sunlight and fluorescent lamp contain light that can erase written information. Be sure to cover the transparent glass portion with a seal or other similar materials except when erasing.

② Mitsubishi Electric corp. provides the seal for covering the transparent glass. Take care that the seal does not touch the lead pins.

③ Clean the transparent glass before erasing. Fingers' fat and paste disturb the passage of ultraviolet light and may affect badly the erasure capability.

④ A high voltage is used for writing. Take care that overvoltage is not applied. Take care especially at turning on the power.

⑤ For the One Time PROM version shipped in blank, Mitsubishi Electric corp. does not perform PROM writing test and screening in the assembly process and following processes. In order to improve reliability after writing, performing writing and test according to the flow shown in Fig. 55 before using is recommended. (Products shipped in blank : PROM contens is not written in factory when shipped)

Table 14 Programming adapters

Microcomputer	Programming adapter
M34550E8-XXXFP, M34550E8FP	PCA4745
M34550E8FS	PCA4746

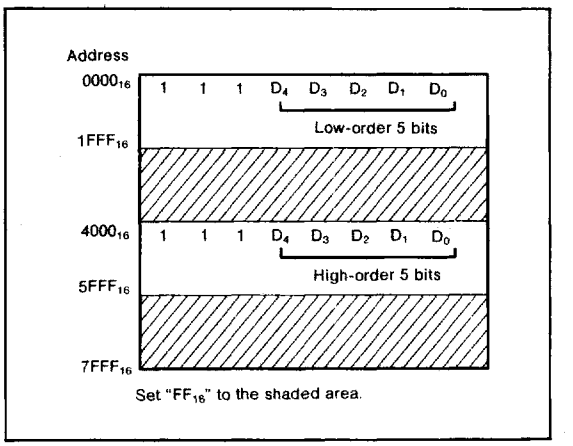


Fig. 54 PROM memory map

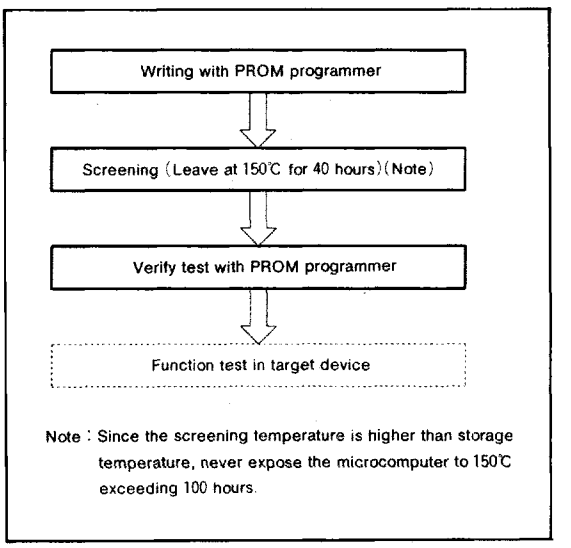


Fig. 55 Flow of writing and testing for products shipped in blank

ABSOLUTE MAXIMUM RATINGS FOR BUILT-IN PROM VERSION

Symbol	Parameter	Conditions	Rating	Unit
V_{DD}	Supply voltage		−0.3 to 7	V
V_I	Input voltage P0, P1, P2, D_8−D_{10}, P3, P4, $\overline{RESET}$, X_{IN}, X_{CIN}		−0.3 to V_{DD}+0.3	V
V_I	Input voltage V_{LC1}, V_{LC2}, V_{LC3}		−0.3 to V_{DD}+0.3	V
V_O	Output voltage P0, P1, D, $\overline{RESET}$	Output transistors in the cut-off state	−0.3 to V_{DD}+0.3	V
V_O	Output voltage CARR, X_{OUT}, X_{COUT}		−0.3 to V_{DD}+0.3	V
V_O	Output voltage SEG, COM		−0.3 to V_{LC3}+0.3	V
Pd	Power dissipation		300	mW
Topr	Operating temperature range		−20 to 70	℃
Tstg	Storage temperature range		−40 to 125	℃

RECOMMENDED OPERATING CONDITIONS FOR BUILT-IN PROM VERSION

(T_a=−20℃ to 70℃, V_{DD}=2.5V to 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	f(X_{IN})=1.6MHz	2.5		3.6	V
V_{RAM}	RAM back-up voltage (at RAM back-up mode)		2.0		3.6	V
V_{SS}	Supply voltage			0		V
V_{LC3}	Supply voltage for LCD (Note 1)		2.5		3.6	V
V_{IH}	"H" level input voltage P0, P1, P2, P3, P4, D_8−D_{10}	V_{DD}=3.0V	0.8V_{DD}		V_{DD}	V
V_{IH}	"H" level input voltage X_{IN}		0.7V_{DD}		V_{DD}	V
V_{IH}	"H" level input voltage $\overline{RESET}$		0.85V_{DD}		V_{DD}	V
V_{IH}	"H" level input voltage INT		0.8V_{DD}		V_{DD}	V
V_{IL}	"L" level input voltage P0, P1, P2, P3, P4, D_8−D_{10}		0		0.3V_{DD}	V
V_{IL}	"L" level input voltage X_{IN}		0		0.3V_{DD}	V
V_{IL}	"L" level input voltage $\overline{RESET}$		0		0.3V_{DD}	V
V_{IL}	"L" level input voltage INT		0		0.2V_{DD}	V
$I_{OL(peak)}$	"L" level peak output current P0, P1, D_0−D_7, D_{10}−D_{12}, CARR, $\overline{RESET}$				4	mA
$I_{OL(peak)}$	"L" level peak output current D_8, D_9				24	mA
$I_{OL(avg)}$	"L" level average output current P0, P1, D_0−D_7, D_{10}−D_{12}, CARR, $\overline{RESET}$				2	mA
$I_{OL(avg)}$	"L" level average output current D_8, D_9				12	mA
$I_{OH(peak)}$	"H" level peak output current CARR		−30			mA
$I_{OH(avg)}$	"H" level average output current CARR		−15			mA
f(X_{IN})	f(X_{IN}) clock frequency	with a ceramic resonator			1.6	MHz
f(X_{IN})	f(X_{IN}) clock frequency (Note 2)	with external clock input			800	kHz
f(X_{CIN})	f(X_{CIN}) clock frequency (Note 3)	with a quartz-crystal oscillator	32		50	kHz

Note 1. at 1/2 bias : V_{LC1}=V_{LC2}=1/2・V_{LC3}
at 1/3 bias : V_{LC1}=1/3・V_{LC3}, V_{LC2}=2/3・V_{LC3}
2. External clock duty is 30% to 70%.
3. External clock cannot be used as f(X_{CIN}) clock.

ELECTRICAL CHARACTERISTICS FOR BUILT-IN PROM VERSION

(T_a=−20℃ to 70℃, V_{DD}=3V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OL}	"L" level output voltage P0, P1, D_0−D_7, D_{10}−D_{12}, CARR, $\overline{RESET}$		I_{OL}=2mA			0.9	V
V_{OL}	"L" level output voltage D_8, D_9		I_{OL}=12mA			1.5	V
V_{OH}	"H" level output voltage CARR		I_{OH}=−7mA	1.0			V
I_{IH}	"H" level input current P0, P1, P2, P3, P4, D_8−D_{10}, $\overline{RESET}$		V_I=V_{DD} (Note 1)			1	μA
I_{IL}	"L" level input current P2, P3, P4, D_8−D_{10}, $\overline{RESET}$		V_I=0V (Note 1)	−1			μA
I_{OZ}	OFF-state output current D_0−D_7		V_O=V_{DD}			1	μA
I_{DD}	Supply current	at active high-speed mode	f(X_{IN})=1MHz f(X_{CIN})=32kHz		1	2	mA
			f(X_{IN})=500kHz f(X_{CIN})=32kHz		0.5	1.0	mA
		at active low-speed mode	f(X_{IN})=Stop f(X_{CIN})=32kHz		20	50	μA
		at power down 1 mode (LCD operation)	f(X_{IN})=Stop f(X_{CIN})=32kHz T_a=25℃		4	10	μA
			f(X_{IN})=Stop f(X_{CIN})=32kHz			15	μA
		at power down 2 mode	f(X_{IN})=Stop f(X_{CIN})=Stop T_a=25℃		0.1	1.0	μA
			f(X_{IN})=Stop f(X_{CIN})=Stop			10	μA
R_{PU}	Pull-up resistor value P0, P1, and P3		V_{DD}=3V V_I=0V	40	100	250	kΩ
V_{T+} − V_{T-}	Hysteresis INT				0.4		V
V_{T+} − V_{T-}	Hysteresis $\overline{RESET}$				0.7		V
R_{COM}	COM output impedance		(Note 2)		2	10	kΩ
R_{SEG}	SEG output impedance		(Note 2)		3	15	kΩ
R_{VLC}	Internal resistor value for LCD power (impedance between V_{LC3} and V_{SS})		T_a=25℃	300	600	1200	kΩ

Notes 1. In this case, port P4 is selected as input port with software.
2. External power is used for LCD power and measurement is performed with all pins freed except the measurement pin.