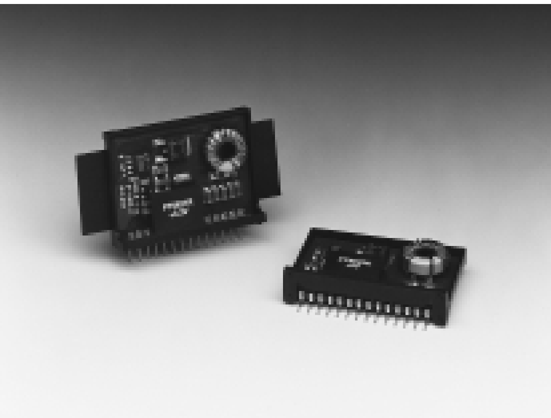


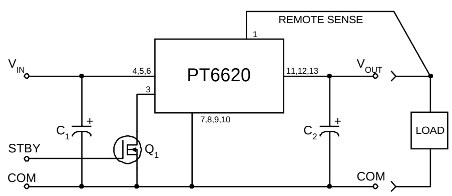
Features

- Single Device: 6-A Output
- Input Voltage Range: 9 V to 16 V
- Adjustable Output Voltage
- 83 % Efficiency
- Remote Sense Capability
- Standby Function
- Over-Temperature Protection
- 16-pin Mount Option (Suffixes L, M, Q, & F)

Description

The PT6620 series is a line of 12-V input Integrated Switching Regulators (ISRs). These regulators are designed for stand-alone operation in applications requiring as much as 6 A of output current. The PT6620 series is packaged in a 14-Pin SIP (Single In-line Package), which is available in either a vertical or horizontal configurations, including surface mount.

Standard Application



C_1 = Required 330µF electrolytic (1)
C_2 = Required 330µF electrolytic (1)
Q_1 = Optional N-Channel MOSFET

Pin Configuration

Pin	Function
1	V_o Sense
2	Do Not Connect
3	STBY*
4	V_{in}
5	V_{in}
6	V_{in}
7	GND
8	GND
9	GND
10	GND
11	V_{out}
12	V_{out}
13	V_{out}
14	V_o Adjust

Ordering Information

PT6621☐ =3.3 Volts
PT6622☐ =1.5 Volts
PT6623☐ =2.5 Volts
PT6624☐ =3.6 Volts
PT6625☐ =5.0 Volts
PT6626☐ =9.0 Volts
PT6627☐ =1.8 Volts

PT Series Suffix (PT1234 x)

Case/Pin Configuration	Order Suffix	Package Code *
Vertical	P	(EED)
Horiz	D	(EEA)
SMD	E	(EEC)
Horiz, 2-Pin Tab	M	(EEM)
SMD, 2-Pin Tab	L	(EEL)
Horiz, 2-Pin Ext Tab	Q	(EEQ)
SMD, 2-Pin Ext Tab	F	(EEF)
Vertical, Side Tab	R	(EEE)
Horiz, Side Tab	G	(EEG)
SMD, Side Tab	B	(EEK)

** Previously known as package styles 400/410.*

(Reference the applicable package code drawing for the dimensions and PC board layout)

Specifications

Unless otherwise stated, T_a =25 °C, C_2 =330 µF, V_{in} =12 V, I_o =$I_o$max

Characteristics	Symbols	Conditions		PT6620 SERIES Min	Typ	Max	Units
Output Current	I_o	T_a = 60 °C, 200 LFM, pkg P T_a = 25 °C, natural convection		0.1 (2) 0.1 (2)	— —	6 6	A
Input Voltage Range	V_{in}	0.1 A ≤ I_o ≤ 6 A	V_o ≤ 5 V 6 V ≤ V_o ≤ 9 V	9 V_o + 3	— —	16 16	V
Output Voltage Tolerance	ΔV_o	T_a = 0 to 60 °C		V_o – 0.1	—	V_o + 0.1	V
Output Voltage Adjust Range	$V_o$adj	Pin 14 to V_o or ground	V_o = 3.3 V V_o = 1.5 V V_o = 2.5 V V_o = 3.6 V V_o = 5 V V_o = 9 V	2.3 1.4 1.9 2.5 2.9 5.2	— — — — — —	4.5 2.6 3.7 4.8 6.5 10	V
Line Regulation	Reg_{line}	V_{in}(min) ≤ V_{in} ≤ V_{in}(max)		—	±0.5	±1	%V_o
Load Regulation	Reg_{load}	0.1 ≤ I_o ≤ 6 A		—	±0.5	±1	%V_o
V_o Ripple (pk-pk)	V_r	20 MHz bandwidth,	V_o ≤ 6 V V_o > 6 V	— —	50 1	— —	mVpp %V_o
Transient Response	t_{tr} ΔV_{tr}	1 A/µs load step, 50 to 100% I_o max Recovery time V_o over/undershoot		— —	100 150	— —	µSec mV
Efficiency	η	I_o =3 A	V_o=3.3/3.6 V V_o = .5 V V_o =2.5 V V_o =5.0 V V_o =9.0 V	— — — — —	84 68 76 86 93	— — — — —	%
		I_o =6 A	V_o=3.3/3.6 V V_o =1.5 V V_o =2.5 V V_o =5.0 V V_o =9.0 V	— — — — —	83 66 75 85 92	— — — — —	%
Switching Frequency	f_s	V_{in}(min) ≤ V_{in} ≤ V_{in}(max)	PT6622	500	550	600	kHz
		0.1 A ≤ I_o ≤ 6 A	Except PT6622	550	650	750	kHz

Continued

Specifications *(continued)*

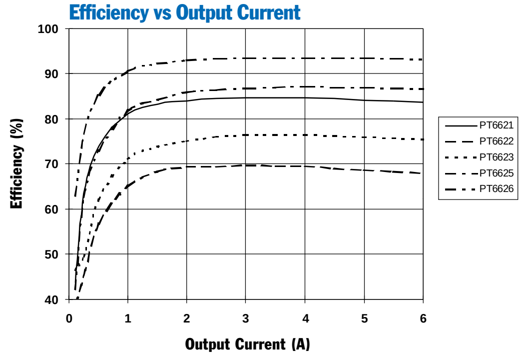
Characteristics	Symbols	Conditions	PT6620 SERIES Min	Typ	Max	Units
Operating Temperature Range	T_a	Over V_{in} range	–40	—	+85 (3)	°C
Storage Temperature	T_s	—	–40	—	+125	°C
Mechanical Shock	—	Per Mil-STD-883D, Method 2002.3	—	500	—	G's
Mechanical Vibration	—	Per Mil-STD-883D, Method 2007.2, 20–2000 Hz, soldered in a PC board	—	7.5	—	G's
Weight	—	—	—	14	—	grams

Notes: (1) *The PT6620 Series requires a 330 µF(output) and 100 µF(input) electrolytic capacitors for proper operation in all applications.*
(2) *ISR will operate down to no load with reduced specifications*
(3) *See safe Operating Area curves or contact the factory for the appropriate derating.*

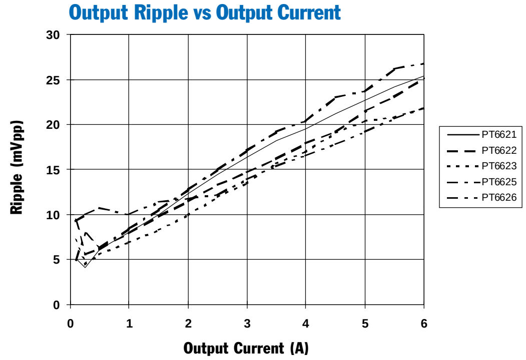
TYPICAL CHARACTERISTICS

PT6620 Series @V_{in}=12 V (See Note A)

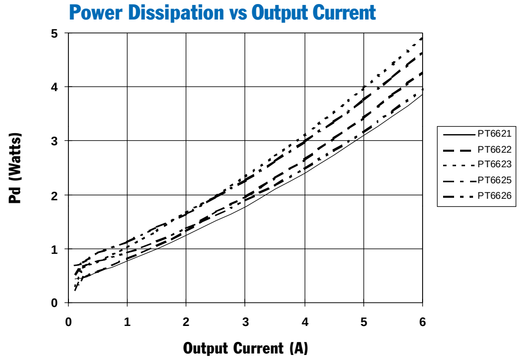
Efficiency vs Output Current



Output Ripple vs Output Current

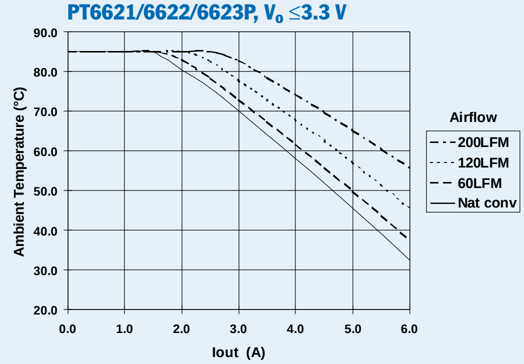


Power Dissipation vs Output Current

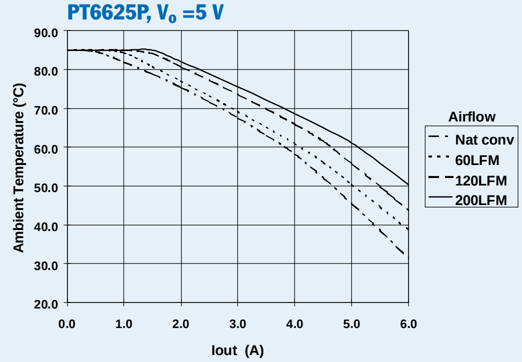


Safe Operating Area, V_{in} =12 V (See Note B)

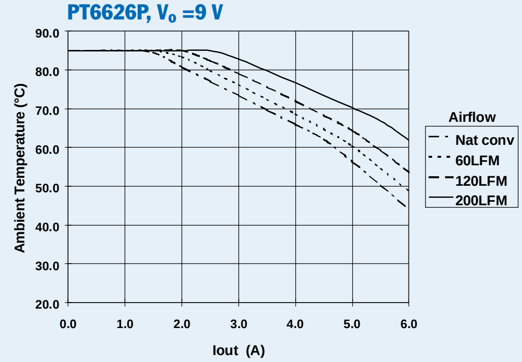
PT6621/6622/6623P, V_o ≤3.3 V



PT6625P, V_o =5 V



PT6626P, V_o =9 V



Note A: *All characteristic data in the above graphs has been develped from actual products tested at 25 °C. This data is considered typical for the ISR.*
Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

Adjusting the Output Voltage of the PT6620 6 A, 12-V Bus Converter Series

The output voltage of the Power Trends PT6620 Series ISRs may be adjusted higher or lower than the factory trimmed pre-set voltage with the addition of a single external resistor. Table 1 accordingly gives the allowable adjustment range for each model in the series as V_a (min) and V_a (max).

Adjust Up: An increase in the output voltage is obtained by adding a resistor R_2, between V_o *Adjust* (pin 14) and *GND* (pins 7-10).

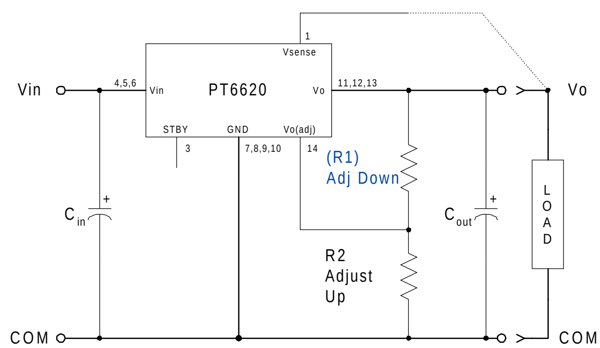
Adjust Down: Add a resistor (R_1), between V_o *Adjust* (pin 14) and V_{out} (pins 11-13).

Refer to Figure 1 and Table 2 for both the placement and value of the required resistor, either (R_1) or R_2 as appropriate.

Notes:

1. Use only a single 1% resistor in either the (R_1) or R_2 location. Place the resistor as close to the ISR as possible.
2. Never connect capacitors from V_o Adjust to either GND, V_{out}, or the Remote Sense pin. Any capacitance added to the V_o adjust pin will affect the stability of the ISR.
3. If the Remote Sense feature is being used, connecting the resistor (R_1) between V_o Adjust (pin 14) and Remote Sense (pin 1) can benefit load regulation.
4. The minimum input voltage required by the part is V_{out} + 3, or 9 V, whichever is higher.

Figure 1



The values of (R_1) [adjust down], and R_2 [adjust up], can also be calculated using the following formulae.

$$(R_1) = \frac{R_o (V_a - 1.25)}{(V_o - V_a)} - R_s \quad k\Omega$$

$$R_2 = \frac{1.25 R_o}{V_a - V_o} - R_s \quad k\Omega$$

Where: V_o = Original output voltage
V_a = Adjusted output voltage
R_o = The resistance value in Table 1
R_s = The series resistance from Table 1

Table 1

PT6620 ADJUSTMENT AND FORMULA PARAMETERS

Series Pt #	PT6622	PT6623	PT6621	PT6624	PT6625	PT6626
V_o (nom)	1.5 V	2.5 V	3.3 V	3.6 V	5 V	9.0 V
V_a (min)	1.4 V	1.9 V	2.3 V	2.5 V	2.9 V	5.2 V
V_a (max)	2.7 V	3.7 V	4.5 V	4.8 V	6.5 V	10 V
R_o (kΩ)	4.99	10.0	12.1	12.1	16.2	12.1
R_s (kΩ)	2.49	4.99	12.1	12.1	12.1	12.1

Table 2

PT6620 ADJUSTMENT RESISTOR VALUES

Series Pt #	PT6622	PT6623	PT6621	PT6624	PT6625
V_o (nom)	1.5 V	2.5 V	3.3 V	3.6 V	5 V
V_a (req'd)					
1.4	(5.0) kΩ				
1.5					
1.6	59.9 kΩ				
1.7	28.7 kΩ				
1.8	18.3 kΩ				
1.9	13.1 kΩ	(5.8) kΩ			
2.0	10.0 kΩ	(10.0) kΩ			
2.1	7.9 kΩ	(16.3) kΩ			
2.2	6.4 kΩ	(26.7) kΩ			
2.3	5.3 kΩ	(47.5) kΩ	(0.6) kΩ		
2.4	4.4 kΩ	(110.0) kΩ	(3.4) kΩ		
2.5	3.8 kΩ		(6.8) kΩ	(1.7) kΩ	
2.6	3.2 kΩ	120.0 kΩ	(11.2) kΩ	(4.2) kΩ	
2.7		57.5 kΩ	(17.1) kΩ	(7.4) kΩ	
2.8		36.7 kΩ	(25.4) kΩ	(11.3) kΩ	
2.9		26.3 kΩ	(37.8) kΩ	(16.4) kΩ	(0.6) kΩ
3.0		20.0 kΩ	(58.5) kΩ	(23.2) kΩ	(2.1) kΩ
3.1		15.8 kΩ	(99.8) kΩ	(32.7) kΩ	(3.7) kΩ
3.2		12.9 kΩ	(224.0)kΩ	(46.9) kΩ	(5.5) kΩ
3.3		10.6 kΩ		(70.6) kΩ	(7.4) kΩ
3.4		8.9 kΩ	139.0 kΩ	(118.0) kΩ	(9.7) kΩ
3.5		7.5 kΩ	63.5 kΩ	(260.0) kΩ	(12.2) kΩ
3.6		6.4 kΩ	38.3 kΩ		(15.1) kΩ
3.7		5.4 kΩ	25.7 kΩ	139.0 kΩ	(18.4) kΩ
3.8			18.2 kΩ	63.5 kΩ	(22.3) kΩ
3.9			13.1 kΩ	38.3 kΩ	(26.9) kΩ
4.0			9.5 kΩ	25.7 kΩ	(32.5) kΩ
4.1			6.8 kΩ	18.2 kΩ	(39.2) kΩ
4.2			4.7 kΩ	13.1 kΩ	(47.6) kΩ
4.3			3.0 kΩ	9.5 kΩ	(58.5) kΩ
4.4			1.7 kΩ	6.8 kΩ	(73.0) kΩ
4.5			0.5 kΩ	4.7 kΩ	(93.2) kΩ
4.6				3.0 kΩ	(124.0) kΩ
4.7				1.7 kΩ	(174.0) kΩ
4.8				0.5 kΩ	(275.0) kΩ
4.9					(579.0) kΩ
5.0					
5.1					190.0 kΩ

Series Pt #	PT6625	PT6626
V_o (nom)	5 V	9 V
V_a (req'd)		
5.2	89.1 kΩ	(0.5) kΩ
5.3	55.4 kΩ	(1.1) kΩ
5.4	38.5 kΩ	(1.9) kΩ
5.5	28.4 kΩ	(2.6) kΩ
5.6	21.7 kΩ	(3.4) kΩ
5.7	16.8 kΩ	(4.2) kΩ
5.8	13.2 kΩ	(5.1) kΩ
5.9	10.4 kΩ	(6.1) kΩ
6.0	8.2 kΩ	(7.1) kΩ
6.1	6.3 kΩ	(8.1) kΩ
6.2	4.8 kΩ	(9.3) kΩ
6.3	3.5 kΩ	(10.5) kΩ
6.4	2.4 kΩ	(11.9) kΩ
6.5	1.4 kΩ	(13.3) kΩ
6.6		(14.9) kΩ
6.7		(16.6) kΩ
6.8		(18.4) kΩ
6.9		(20.5) kΩ
7.0		(22.7) kΩ
7.1		(25.2) kΩ
7.2		(27.9) kΩ
7.3		(31.0) kΩ
7.4		(34.4) kΩ
7.5		(38.3) kΩ
7.6		(42.8) kΩ
7.8		(53.9) kΩ
8.0		(69.6) kΩ
8.2		(93.0) kΩ
8.4		(132.0) kΩ
8.6		(210.0) kΩ
8.8		(445.0) kΩ
9.0		
9.2		63.5 kΩ
9.4		25.7 kΩ
9.6		13.1 kΩ
9.8		6.8 kΩ
10.0		3.0 kΩ

R_1 = (Blue) R_2 = Black

Using the Standby Function on the PT6620 Series of 12-V Bus Converters

For applications requiring output voltage On/Off control, the 14-pin PT6620 ISR series incorporates a standby function. This feature may be used for power-up/shut-down sequencing, and wherever there is a requirement for the output status of the module to be controlled by external circuitry.

The standby function is provided by the *STBY** control, pin 3. If pin 3 is left open-circuit the regulator operates normally, providing a regulated output whenever a valid supply voltage is applied to V_{in} (pins 4, 5, & 6) with respect to *GND* (pins 7-10). Connecting pin 3 to ground [1] will disable the regulator output and reduce the input current to less than 30 mA [3]. Grounding the standby control will also hold-off the regulator output during the period that input power is applied.

The standby input is ideally controlled with an open-collector (or open-drain) discrete transistor (See Figure 1). It can also be driven directly from a dedicated TTL [2] compatible gate. Table 1 provides details of the threshold requirements.

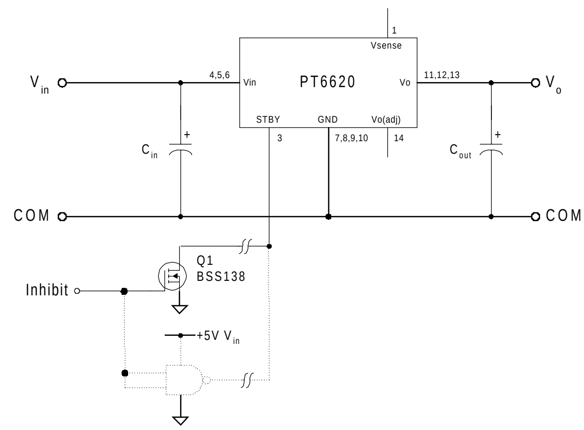
Table 1 Inhibit Control Thresholds [1,2]

Parameter	Min	Max
Enable (V_{IH})	1 V	5 V
Disable (V_{IL})	–0.1V	0.3V

Notes:

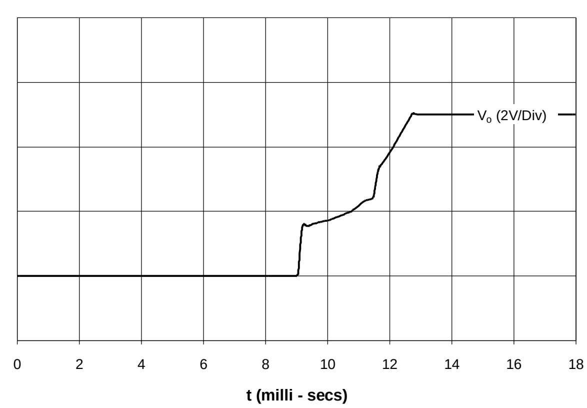
1. The Standby input on the PT6620 regulator series may be controlled using either an open-collector (or open-drain) discrete transistor, or a device with a totem-pole output. A pull-up resistor is not necessary. The control input has an open-circuit voltage of about 1.5 Vdc. To disable the regulator output, the control pin must be “pulled” to less than 0.3 Vdc with a low-level 0.25 mA max. sink to ground.
2. The Standby input on the PT6620 series is also compatible with TTL logic. A standard TTL logic gate will meet the 0.3 V V_{IL}(max) requirement (Table 1) at 0.25 mA sink current. *Do not* drive the Standby control input above 5 Vdc.
3. When the regulator output is disabled the current drawn from the input source is reduced to approximately 15 mA (30 mA maximum).
4. The turn-off time of Q_1, or rise time of the standby input is not critical on the PT6620 series. Turning Q_1 off slowly, over periods up to 100 ms, will not damage the regulator. However, a slow turn-off time will increase both the initial delay and rate-of-rise of the output voltage.

Figure 1



Turn-On Time: Turning Q_1 in Figure 1 off, removes the low-voltage signal at pin 3 and enables the output. The PT6620 series of regulators will provide a fully regulated output voltage within 20ms. The actual turn-on time may vary with load and the total amount of output capacitance. Figure 2 shows the typical output voltage waveform of a PT6625 (5 V) following the prompt turn off of Q_1 at time t =0 secs. The waveform was measured with a 12-V input voltage, and 5-A resistive load.

Figure 2



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PT6621B	LIFEBUY	SIP MODULE	EEK	14		TBD	Call TI	Call TI	-40 to 85		
PT6621E	OBSOLETE	SIP MODULE	EEC	14		TBD	Call TI	Call TI	-40 to 85		
PT6621F	LIFEBUY	SIP MODULE	EEF	14		TBD	Call TI	Call TI	-40 to 85		
PT6621L	LIFEBUY	SIP MODULE	EEL	14		TBD	Call TI	Call TI	-40 to 85		
PT6621M	LIFEBUY	SIP MODULE	EEM	14		TBD	Call TI	Call TI	-40 to 85		
PT6621Q	LIFEBUY	SIP MODULE	EEQ	14		TBD	Call TI	Call TI	-40 to 85		
PT6622B	LIFEBUY	SIP MODULE	EEK	14		TBD	Call TI	Call TI	-40 to 85		
PT6622E	LIFEBUY	SIP MODULE	EEC	14		TBD	Call TI	Call TI	-40 to 85		
PT6622F	LIFEBUY	SIP MODULE	EEF	14		TBD	Call TI	Call TI	-40 to 85		
PT6622G	LIFEBUY	SIP MODULE	EEG	14		TBD	Call TI	Call TI	-40 to 85		
PT6622L	LIFEBUY	SIP MODULE	EEL	14		TBD	Call TI	Call TI	-40 to 85		
PT6622M	LIFEBUY	SIP MODULE	EEM	14		TBD	Call TI	Call TI	-40 to 85		
PT6622Q	LIFEBUY	SIP MODULE	EEQ	14		TBD	Call TI	Call TI	-40 to 85		
PT6622R	LIFEBUY	SIP MODULE	EEE	14		TBD	Call TI	Call TI	-40 to 85		
PT6623B	NRND	SIP MODULE	EEK	14		TBD	Call TI	Call TI	-40 to 85		
PT6623D	NRND	SIP MODULE	EEA	14		TBD	Call TI	Call TI	-40 to 85		
PT6623E	NRND	SIP MODULE	EEC	14		TBD	Call TI	Call TI	-40 to 85		
PT6623G	NRND	SIP MODULE	EEG	14		TBD	Call TI	Call TI	-40 to 85		
PT6623L	NRND	SIP MODULE	EEL	14		TBD	Call TI	Call TI	-40 to 85		
PT6623M	NRND	SIP MODULE	EEM	14		TBD	Call TI	Call TI	-40 to 85		
PT6623Q	NRND	SIP MODULE	EEQ	14		TBD	Call TI	Call TI	-40 to 85		
PT6623R	NRND	SIP MODULE	EEE	14		TBD	Call TI	Call TI	-40 to 85		
PT6624B	NRND	SIP MODULE	EEK	14		TBD	Call TI	Call TI	-40 to 85		
PT6624E	NRND	SIP MODULE	EEC	14		TBD	Call TI	Call TI	-40 to 85		
PT6624F	NRND	SIP MODULE	EEF	14		TBD	Call TI	Call TI	-40 to 85		
PT6624G	NRND	SIP MODULE	EEG	14		TBD	Call TI	Call TI	-40 to 85		
PT6624L	NRND	SIP MODULE	EEL	14		TBD	Call TI	Call TI	-40 to 85		
PT6624M	NRND	SIP MODULE	EEM	14		TBD	Call TI	Call TI	-40 to 85		
PT6624P	NRND	SIP MODULE	EED	14		TBD	Call TI	Call TI	-40 to 85		
PT6624Q	NRND	SIP MODULE	EEQ	14		TBD	Call TI	Call TI	-40 to 85		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PT6624R	NRND	SIP MODULE	EEE	14		TBD	Call TI	Call TI	-40 to 85		
PT6625F	LIFEBUY	SIP MODULE	EEF	14		TBD	Call TI	Call TI	-40 to 85		
PT6625L	LIFEBUY	SIP MODULE	EEL	14		TBD	Call TI	Call TI	-40 to 85		
PT6625M	LIFEBUY	SIP MODULE	EEM	14		TBD	Call TI	Call TI	-40 to 85		
PT6625Q	LIFEBUY	SIP MODULE	EEQ	14		TBD	Call TI	Call TI	-40 to 85		
PT6626B	LIFEBUY	SIP MODULE	EEK	14		TBD	Call TI	Call TI	-40 to 85		
PT6626E	LIFEBUY	SIP MODULE	EEC	14		TBD	Call TI	Call TI	-40 to 85		
PT6626F	LIFEBUY	SIP MODULE	EEF	14		TBD	Call TI	Call TI	-40 to 85		
PT6626G	OBSOLETE	SIP MODULE	EEG	14		TBD	Call TI	Call TI	-40 to 85		
PT6626L	LIFEBUY	SIP MODULE	EEL	14		TBD	Call TI	Call TI	-40 to 85		
PT6626M	LIFEBUY	SIP MODULE	EEM	14		TBD	Call TI	Call TI	-40 to 85		
PT6626Q	LIFEBUY	SIP MODULE	EEQ	14		TBD	Call TI	Call TI	-40 to 85		
PT6627D	NRND	SIP MODULE	EEA	14		TBD	Call TI	Call TI			
PT6627E	NRND	SIP MODULE	EEC	14		TBD	Call TI	Call TI			
PT6627F	NRND	SIP MODULE	EEF	14		TBD	Call TI	Call TI			
PT6627G	NRND	SIP MODULE	EEG	14		TBD	Call TI	Call TI			
PT6627L	NRND	SIP MODULE	EEL	14		TBD	Call TI	Call TI			
PT6627M	NRND	SIP MODULE	EEM	14		TBD	Call TI	Call TI			
PT6627P	NRND	SIP MODULE	EED	14		TBD	Call TI	Call TI			
PT6627Q	NRND	SIP MODULE	EEQ	14		TBD	Call TI	Call TI			
PT6627R	NRND	SIP MODULE	EEE	14		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

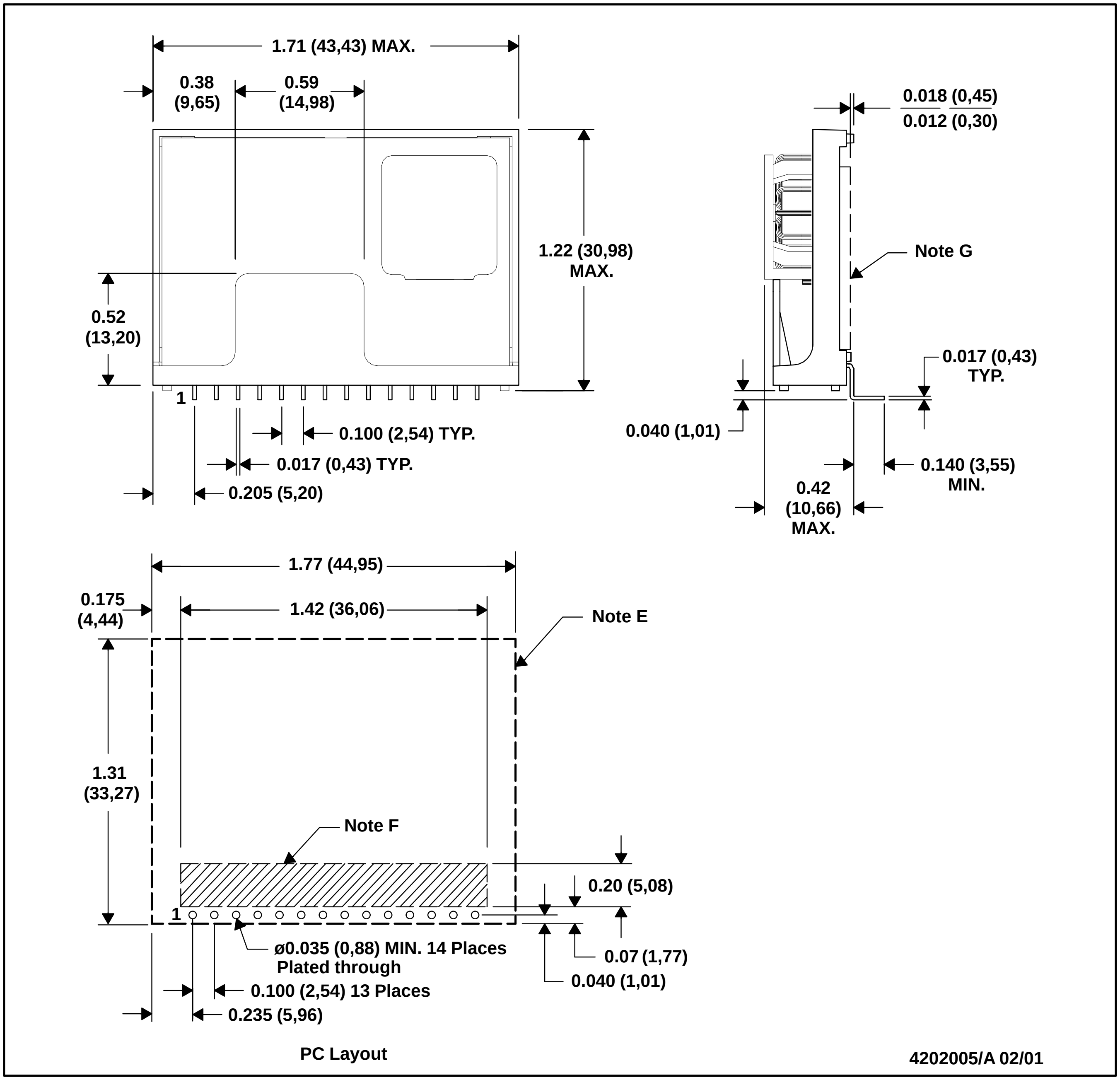
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

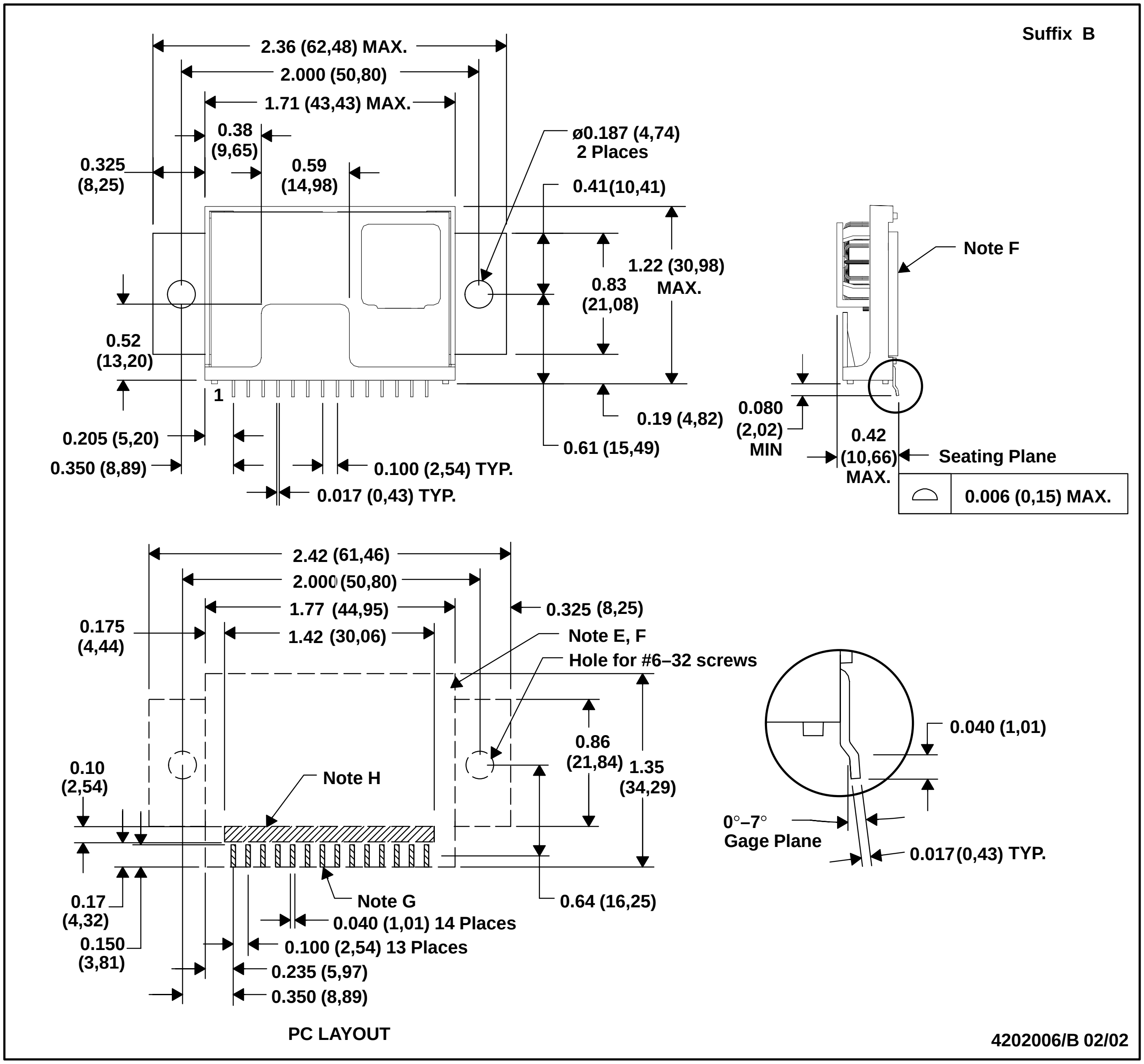
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

EEA (R–PSIP–T14) **PLASTIC SINGLE-IN-LINE MODULE**



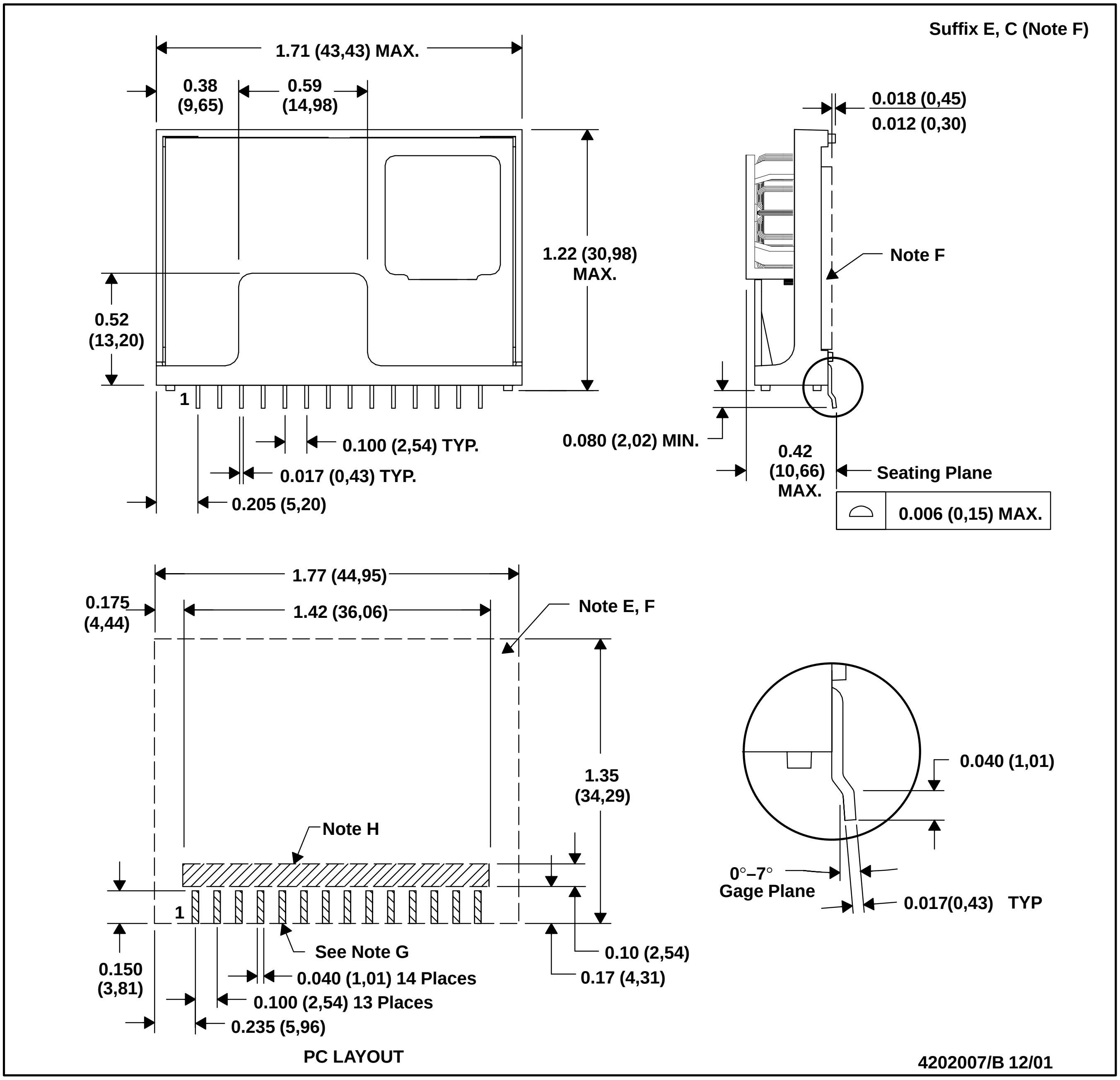
NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2-place decimals are ± 0.030 (± 0, 76 mm).
- D. 3-place decimals are ± 0.010 (± 0, 25 mm).
- E. Recommended mechanical keep-out area.
- F. No copper, power or signal traces in this area.
- G. D-suffix parts include a metal heat spreader. No signal traces are allowed under the heat spreader area. A solid copper island is recommended, which may be grounded. A-suffix does not include a metal heat spreader.

EEK (R–PSIP–G14) **PLASTIC SINGLE-IN-LINE MODULE**



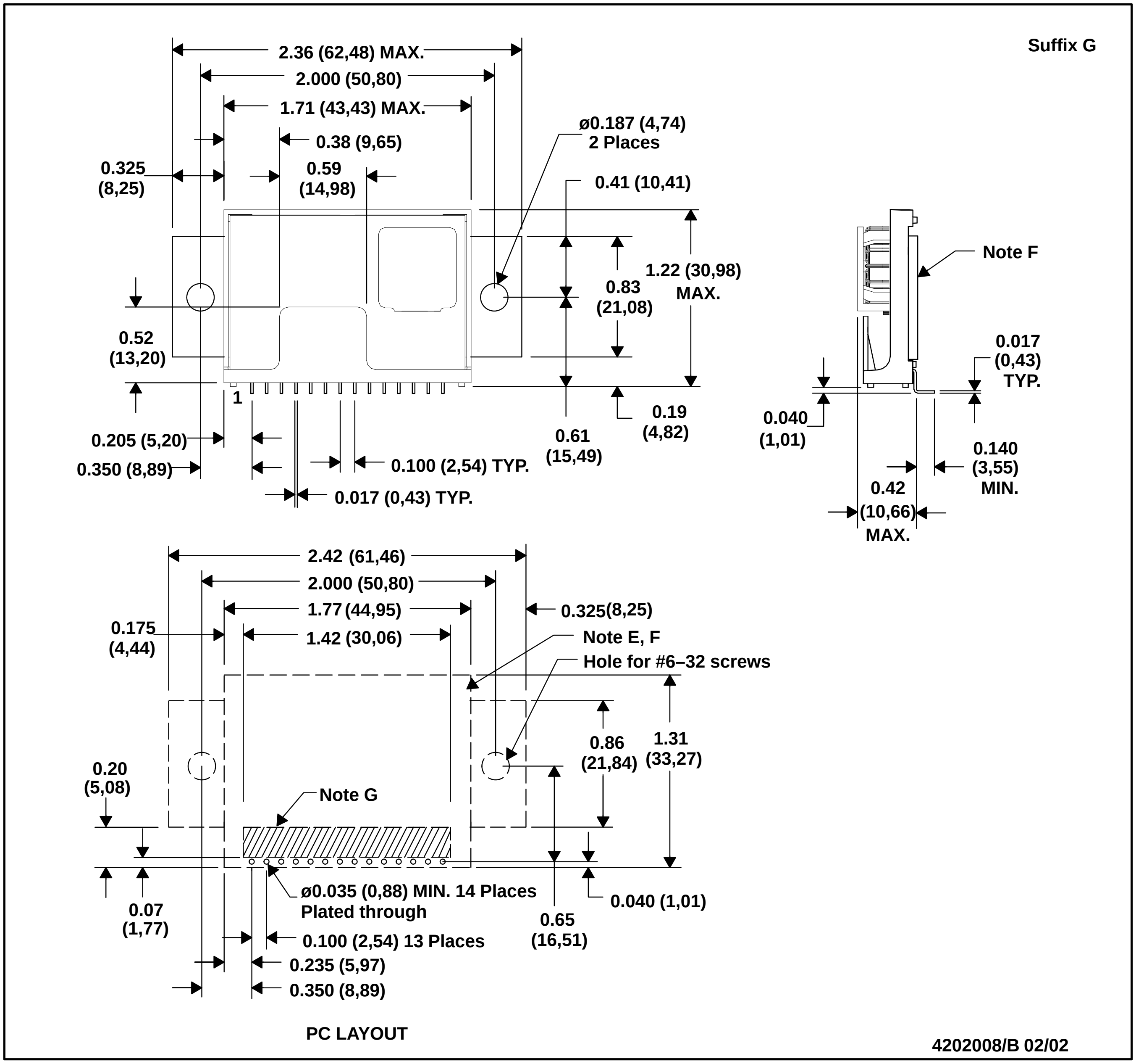
NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2–place decimals are ± 0.030 (± 0, 76 mm).
- D. 3–place decimals are ± 0.010 (± 0, 25 mm).
- E. Recommended mechanical keep-out area.
- F. The metal tab is isolated but electrically conductive. No signal traces are allowed under the metal tab area. A solid copper island is recommended, which may be grounded.
- G. Power pin connections should utilize two or more vias per input, ground and output pin.
- H. No copper, power or signal traces in this area.

EEC (R–PSIP–G14) **PLASTIC SINGLE-IN-LINE MODULE**



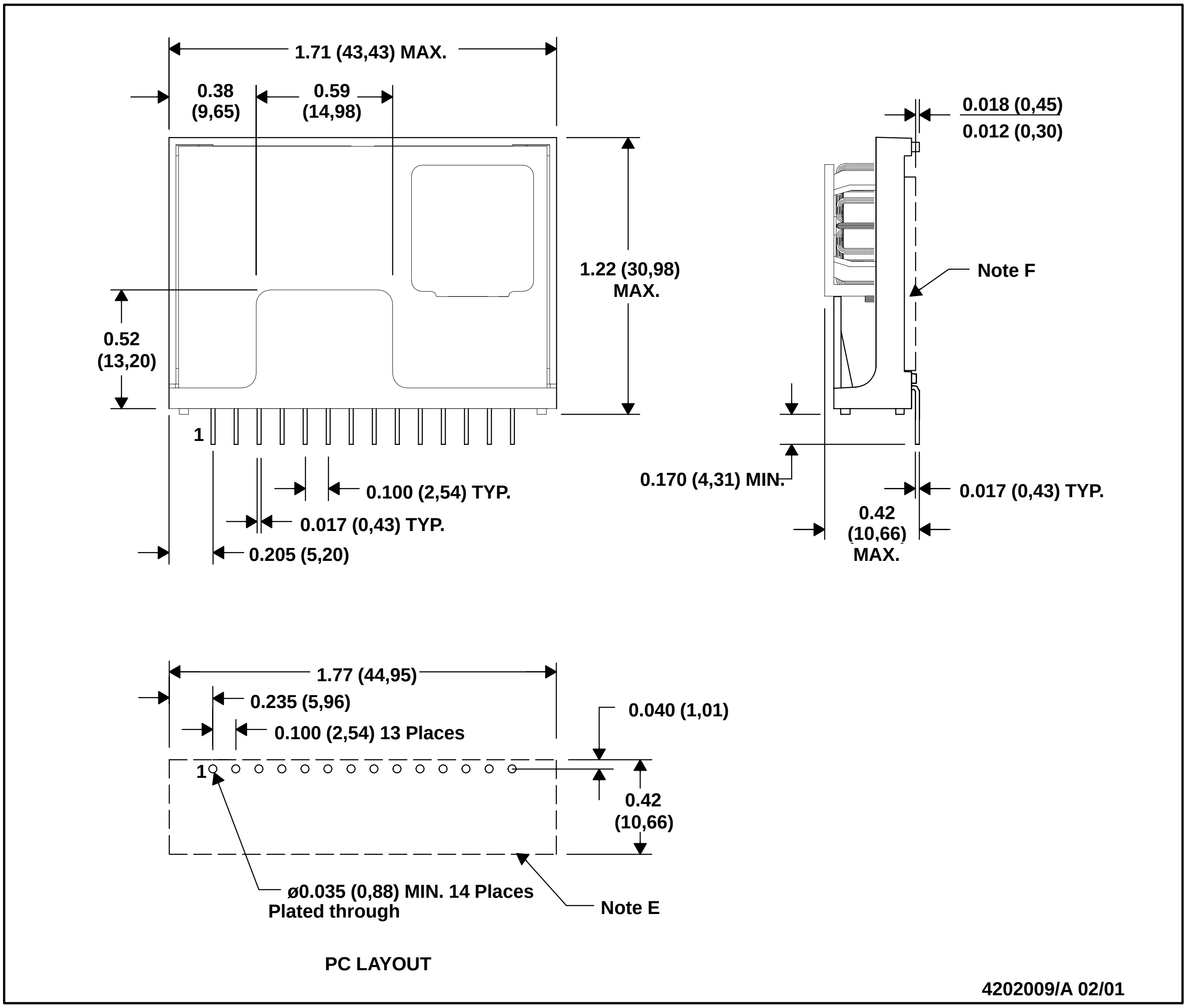
NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2–place decimals are ± 0.030 (± 0, 76 mm).
- D. 3–place decimals are ± 0.010 (± 0, 25 mm).
- E. Recommended mechanical keep-out area.
- F. E-suffix parts include a metal heat spreader. No signal traces are allowed under the heat spreader area. A solid copper island is recommended, which may be grounded. C-suffix does not include a metal heat spreader.
- G. Power pin connections should utilize two or more vias per input, ground and output pin.
- H. No copper, power or signal traces in this area.

EEG (R–PSIP–T14) **PLASTIC SINGLE-IN-LINE MODULE**



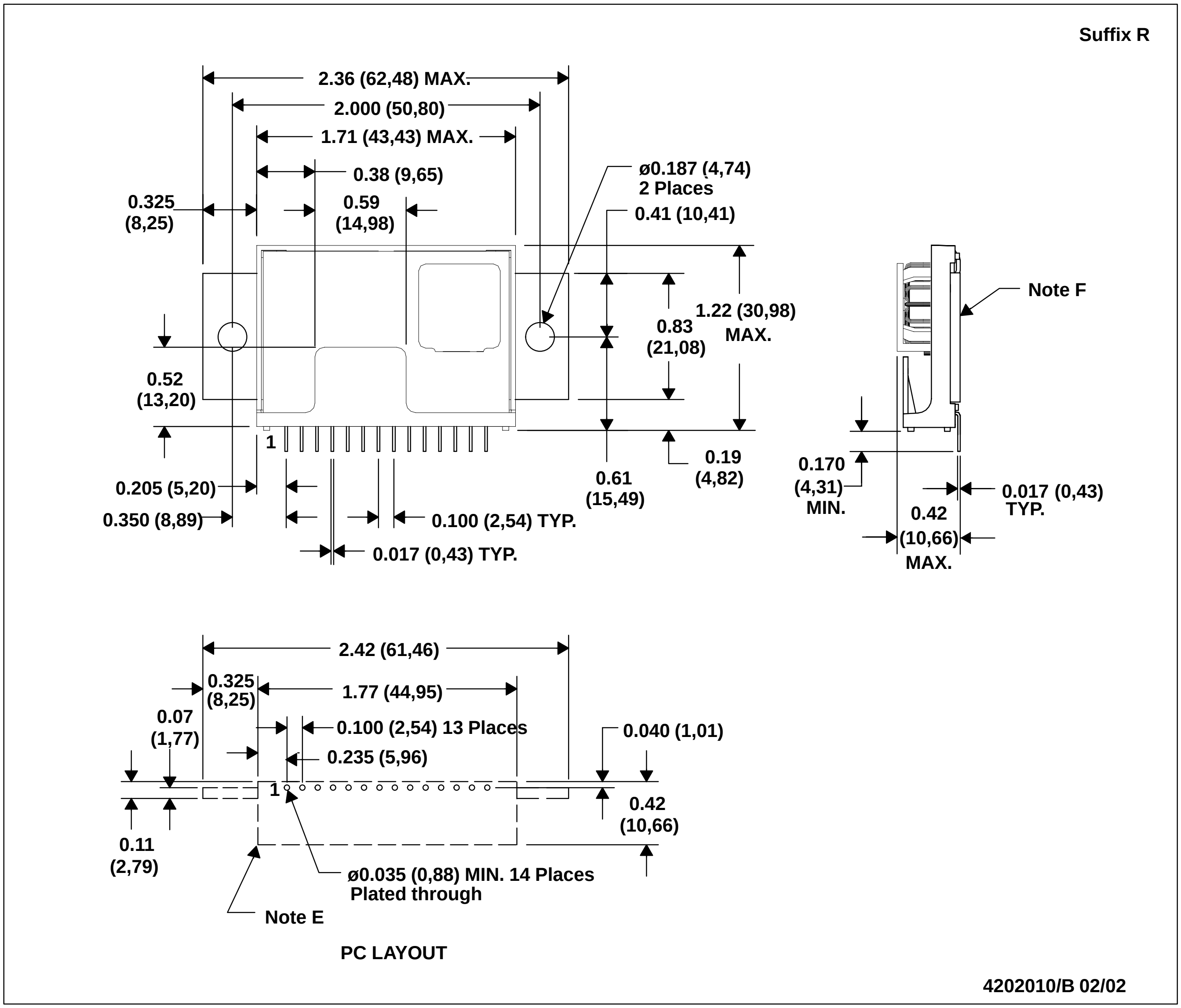
NOTES: A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2-place decimals are ± 0.030 (± 0,76 mm).
D. 3-place decimals are ± 0.010 (± 0,25 mm).
E. Recommended mechanical keep-out area.
F. The metal tab is isolated but electrically conductive.
No signal traces are allowed under the metal tab area.
A solid copper island is recommended, which may be grounded.
G. No copper, power or signal traces in this area.

EED (R–PSIP–T14) PLASTIC SINGLE-IN-LINE MODULE



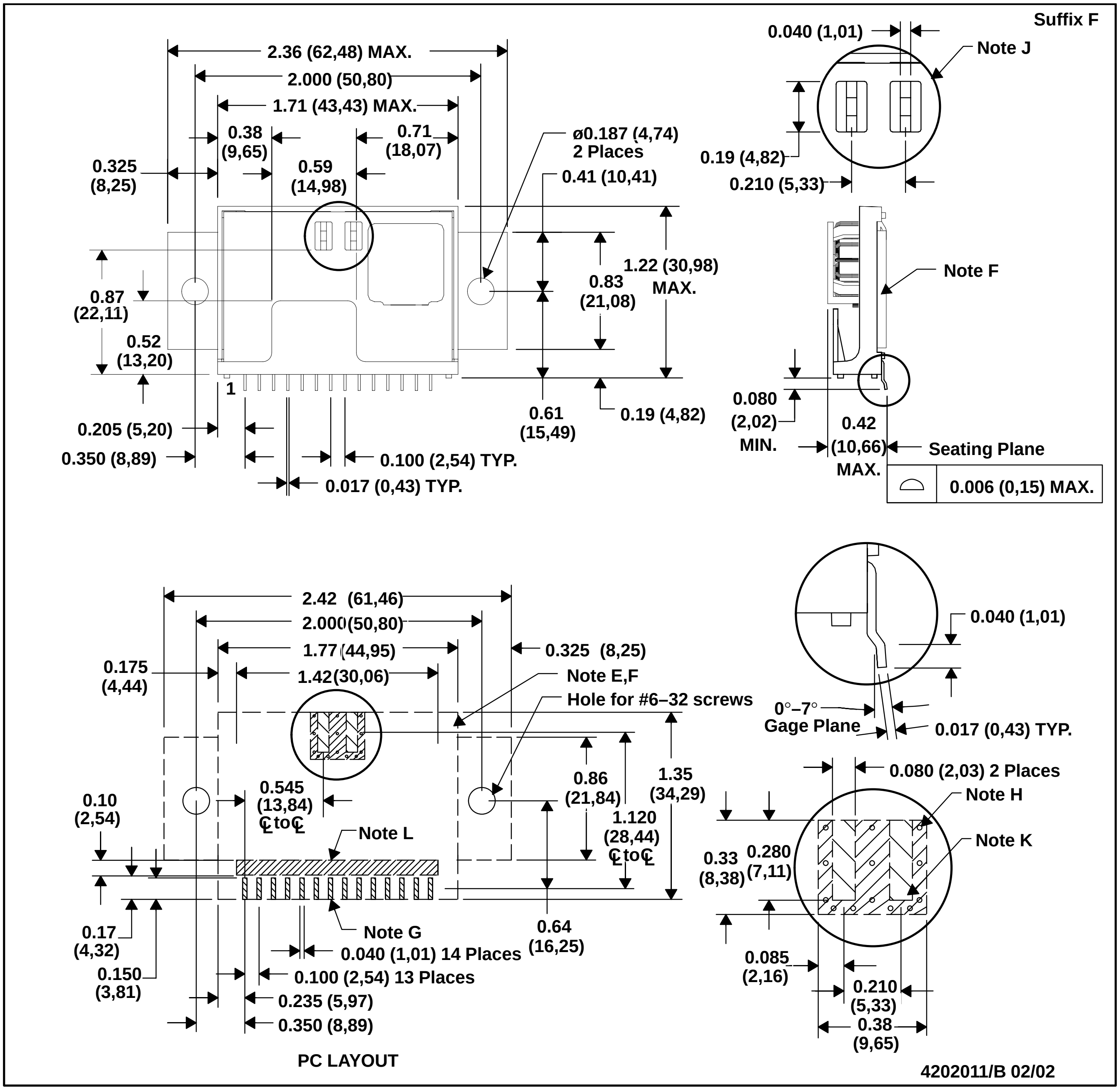
NOTES: A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2-place decimals are ± 0.030 (± 0, 76 mm).
D. 3-place decimals are ± 0.010 (± 0, 25 mm).
E. Recommended mechanical keep-out area.
F. P-suffix parts include a metal heat spreader. The heat spreader is isolated but electrically conductive, it can be grounded. N-suffix does not include a metal heat spreader.

EEE (R–PSIP–T14) **PLASTIC SINGLE-IN-LINE MODULE**



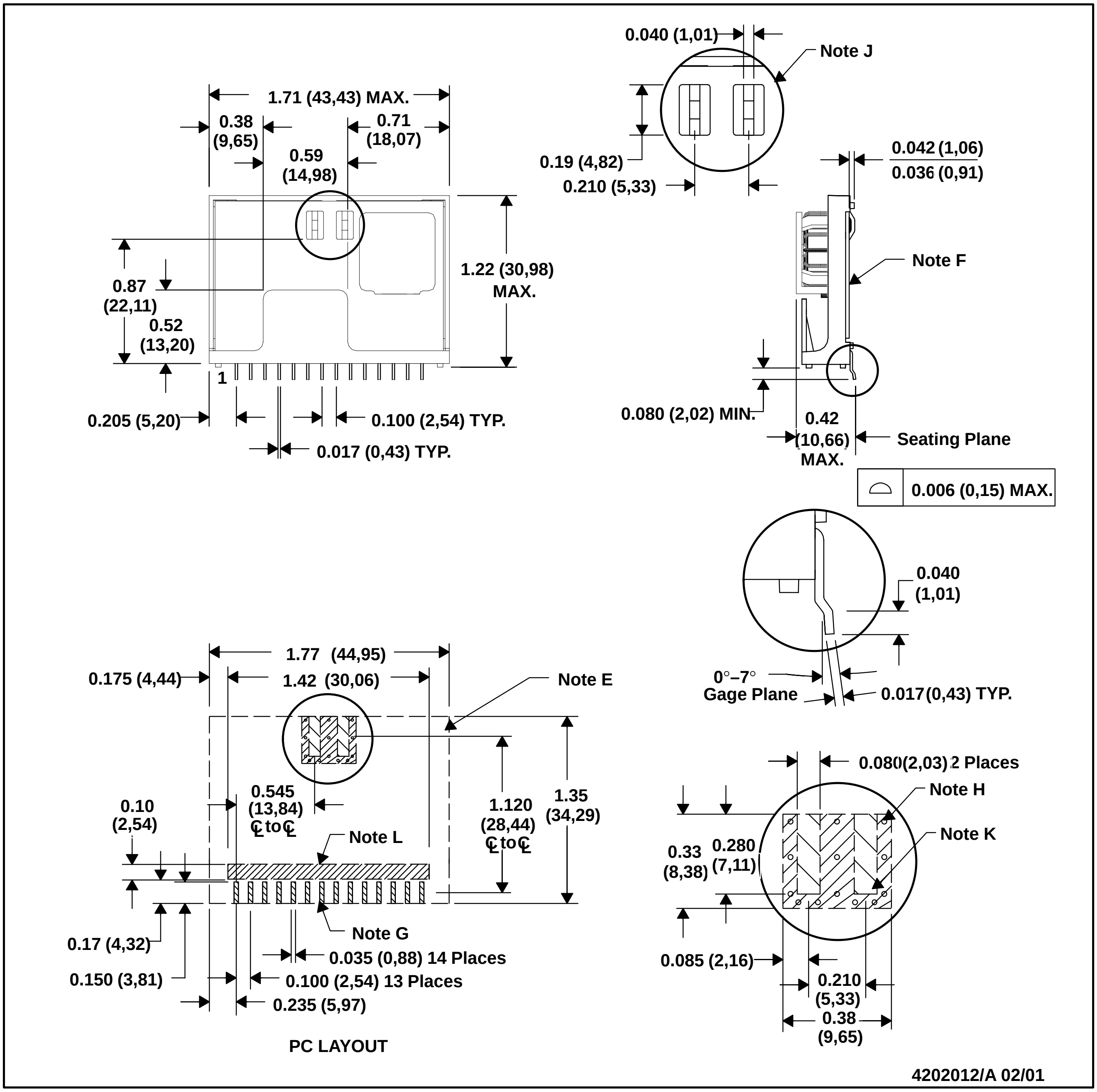
NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2-place decimals are ± 0.030 (± 0,76 mm).
D. 3-place decimals are ± 0.010 (± 0,25 mm).
E. Recommended mechanical keep-out area.
F. The metal tab is isolated but electrically conductive, it can be grounded.

EEF (R–PSIP–G14) **PLASTIC SINGLE-IN-LINE MODULE**



NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2-place decimals are ± 0.030 (± 0,76 mm).
- D. 3–place decimal are ± 0.010 (± 0,25 mm).
- E. Recommended mechanical keep-out area.
- F. The metal tab is isolated but electrically conductive. No signal traces are allowed under the metal tab area. A solid copper island is recommended, which may be grounded.
- G. Power pin connections should utilize two or more vias per input, ground and output pin.
- H. Minimum copper land area required for solder tab. Vias are recommended to improve copper adhesion or connect land to other ground area.
- J. Underside solder tabs detail.
- K. Solder mask openings to copper island for solder joints to mechanical pins.
- L. No copper, power or signal traces in this area.

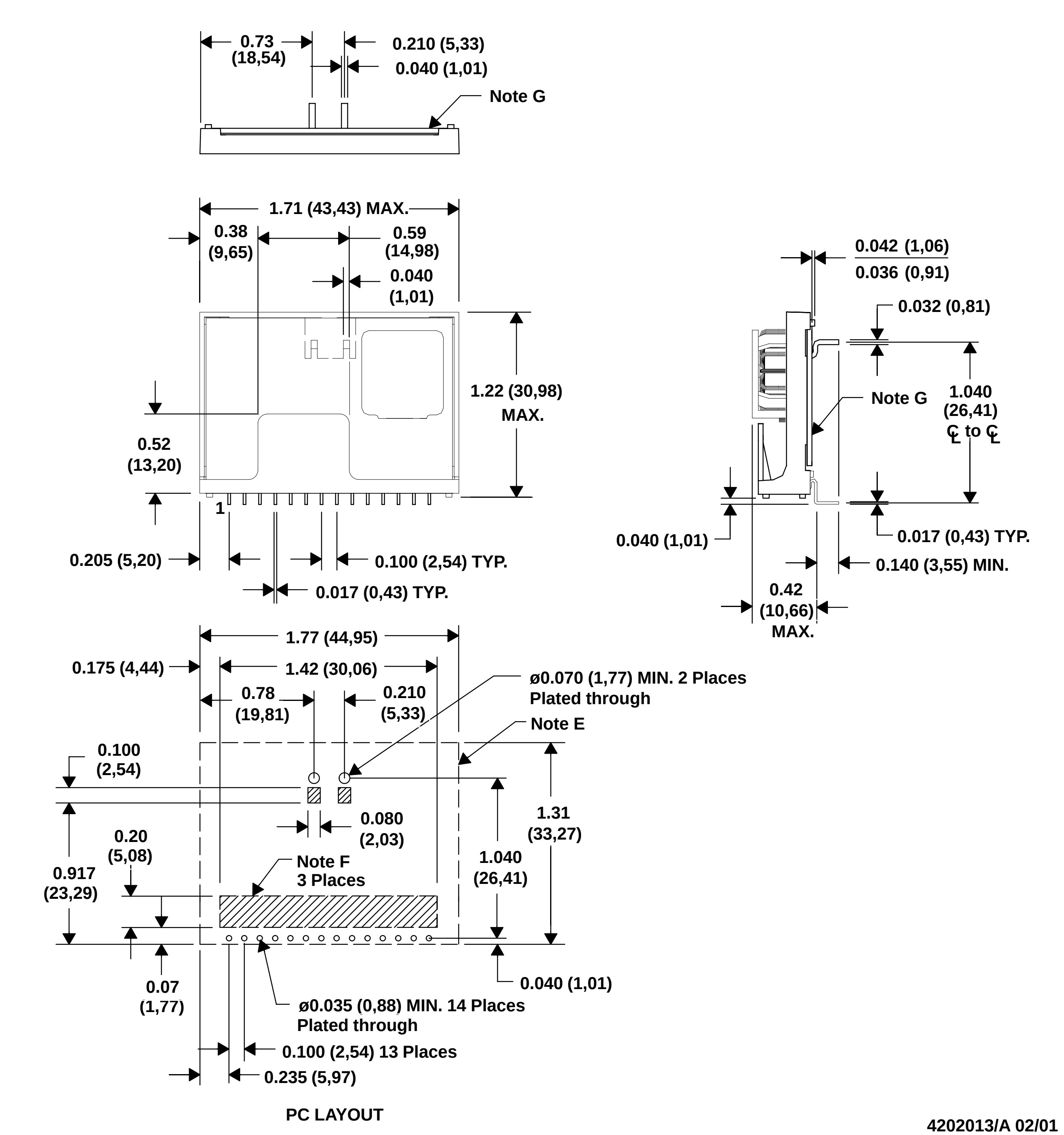
EEL (R–PSIP–G14) **PLASTIC SINGLE-IN-LINE MODULE**



NOTES:

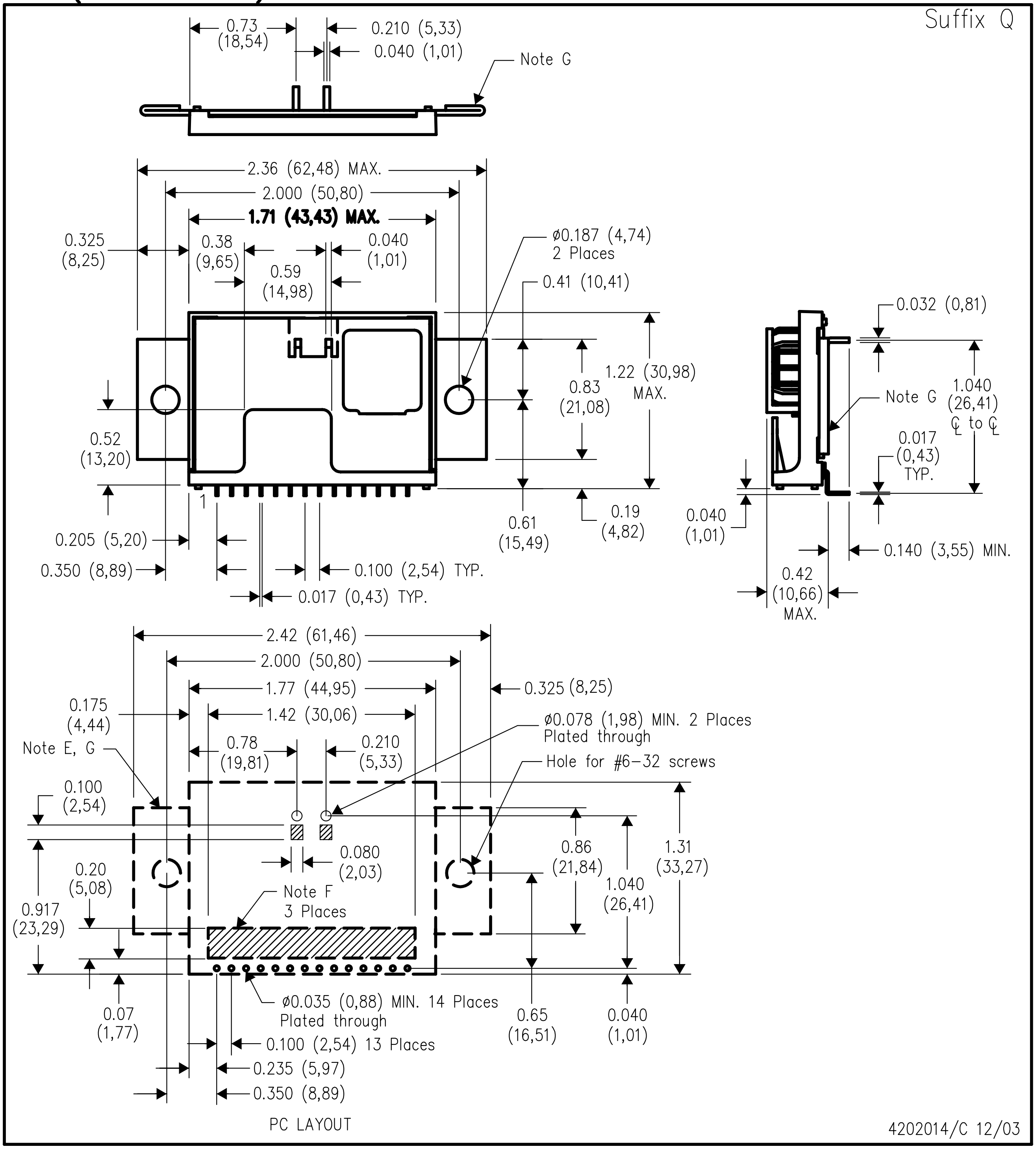
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2–place decimals are ± 0.030 (± 0, 76 mm).
D. 3–place decimals are ± 0.010 (± 0, 25 mm).
E. Recommended mechanical keep-out area.
F. The metal tab is isolated but electrically conductive. No signal traces are allowed under the metal tab area. A solid copper island is recommended, which may be grounded.
G. Power pin connections should utilize two or more vias per input, ground and output pin.
H. Minimum copper land area required for solder tab. Vias are recommended to improve copper adhesion or connect land to other ground area.
J. Underside solder tabs detail
K. Solder mask openings to copper island for solder joints to mechanical pins.
L. No copper, power or signal traces in this area.

EEM (R–PSIP–T14) **PLASTIC SINGLE-IN-LINE MODULE**



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2-place decimals are ± 0.030 (± 0, 76 mm).
D. 3-place deciamals are ± 0.010 (± 0, 25 mm).
E. Recommended mechanical keep-out area.
F. No copper, power or signal traces in this area.
G. The metal tab is isolated but electrically conductive. No signal traces are allowed under the metal tab area. A solid copper island is recommended, which may be grounded to the two underside pins.

EEQ (R-PSIP-T14) PLASTIC SINGLE-IN-LINE MODULE



NOTES:

A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended mechanical keep out area.
F. No copper, power or signal traces in this area.
G. The metal tab is isolated but electrically conductive. No signal traces are allowed under the metal tab area. A solid copper island is recommended, which may be grounded to the two underside pins.