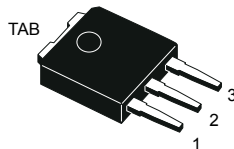
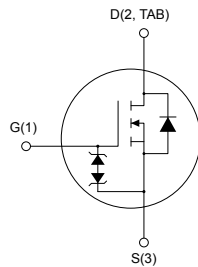


N-channel 700 V, 1.2 Ω typ., 3.5 A MDmesh™ M6 Power MOSFET in a short IPAK package



Short IPAK



AM01475V1

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STU5N70M6-S	700 V	1.4 Ω	3.5 A

- Reduced switching losses
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

Product status link

[STU5N70M6-S](#)

Product summary

Order code	STU5N70M6-S
Marking	5N70M6
Package	Short IPAK
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	3.5	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	2.2	A
$I_{DM}^{(1)}$	Drain current pulsed	8	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	45	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_j	Operating junction temperature range	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature range		

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 3.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$, $V_{DD} = 100\text{ V}$
3. $V_{DS} \leq 560\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.78	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	100	$^\circ\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1	A
E_{AS}	Single-pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	77	mJ

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified

Table 4. On-/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	700			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 700\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 700\text{ V}$ $T_C = 125\text{ }^\circ\text{C}^{(1)}$			100	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.25	3	3.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 1.75\text{ A}$		1.2	1.4	Ω

1. Defined by design, no subject to production test.

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	-	170	-	pF
C_{oss}	Output capacitance		-	15	-	pF
C_{riss}	Reverse transfer capacitance		-	1	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }560\text{ V}, V_{GS} = 0\text{ V}$	-	70	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}, \text{ open drain}$	-	5	-	Ω
Q_g	Total gate charge	$V_{DD} = 350\text{ V}, I_D = 1\text{ A}$	-	5.1	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$	-	0.85	-	nC
Q_{gd}	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	2.6	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 350\text{ V}, I_D = 1.75\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	5.8	-	ns
t_r	Rise time		-	6.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	17	-	ns
t_f	Fall time		-	27.5	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		8	A
$V_{SD}^{(2)}$	Forward on-voltage	$I_{SD} = 3.5 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 3.5 \text{ A}$, $V_{DD} = 60 \text{ V}$, $di/dt = 100 \text{ A}/\mu\text{s}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	230		ns
Q_{rr}	Reverse recovery charge		-	1.25		μC
I_{RRM}	Reverse recovery current	$I_{SD} = 3.5 \text{ A}$, $V_{DD} = 60 \text{ V}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	11		A
t_{rr}	Reverse recovery time		-	277		ns
Q_{rr}	Reverse recovery charge		-	1.4		μC
I_{RRM}	Reverse recovery current		-	10		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

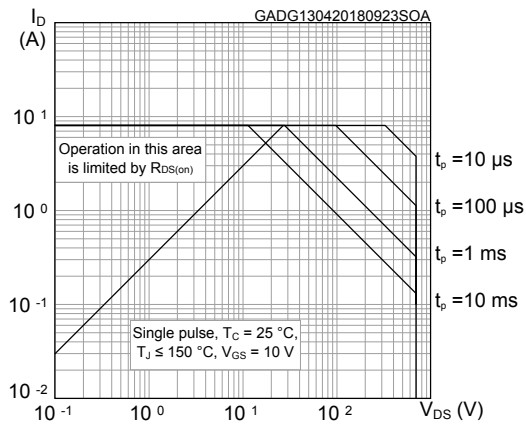


Figure 2. Thermal impedance

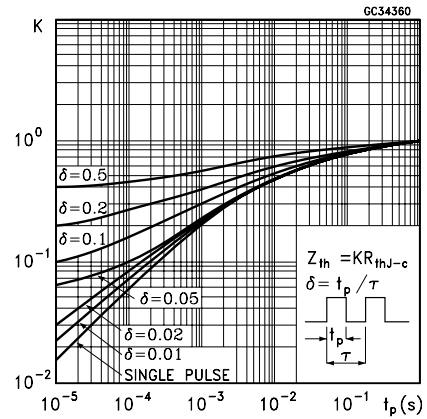


Figure 3. Output characteristics

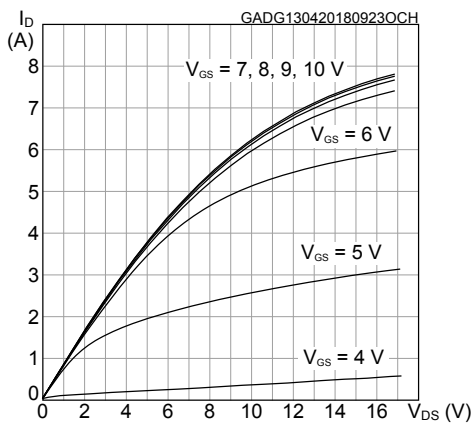


Figure 4. Transfer characteristics

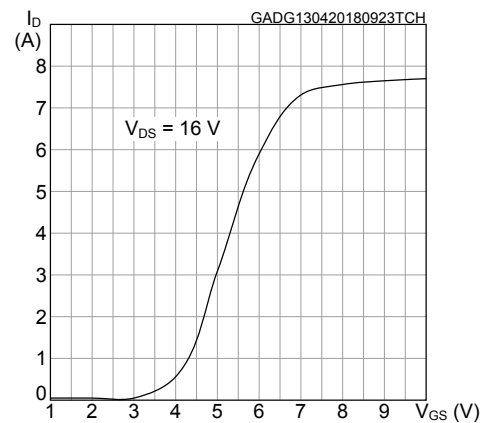


Figure 5. Gate charge vs gate-source voltage

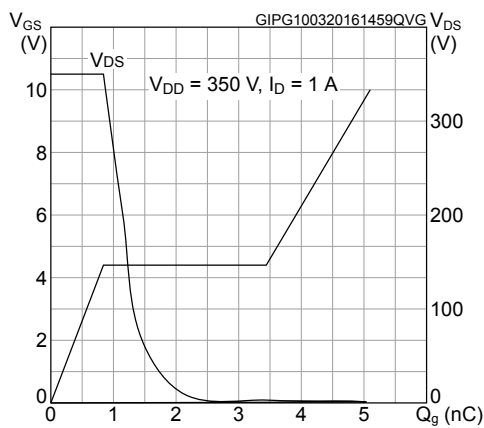


Figure 6. Static drain-source on-resistance

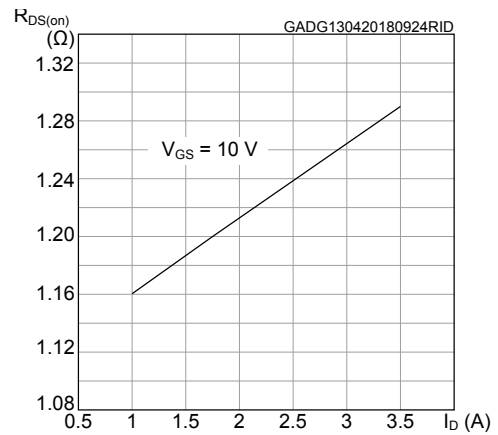


Figure 7. Capacitance variations

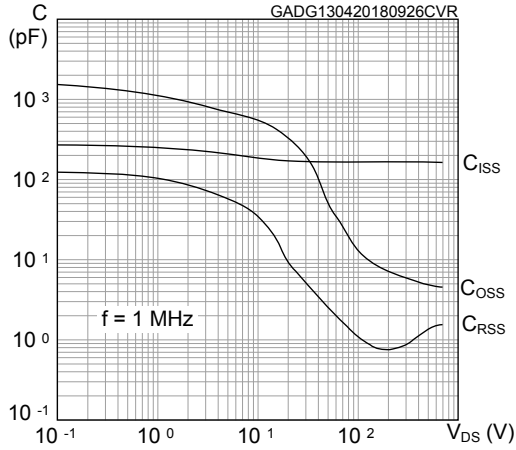


Figure 8. Normalized gate threshold voltage vs temperature

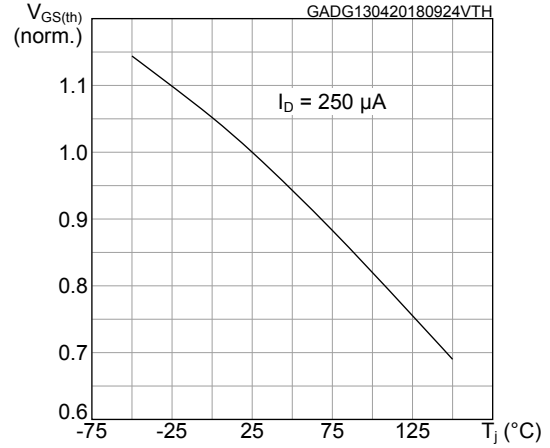


Figure 9. Normalized on-resistance vs temperature

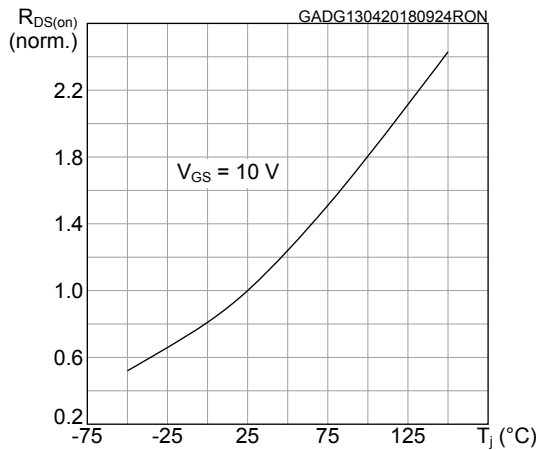


Figure 10. Normalized V_(BR)DSS vs temperature

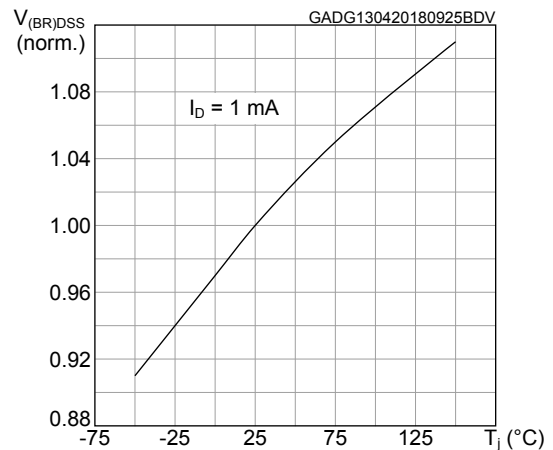


Figure 11. Output capacitance stored energy

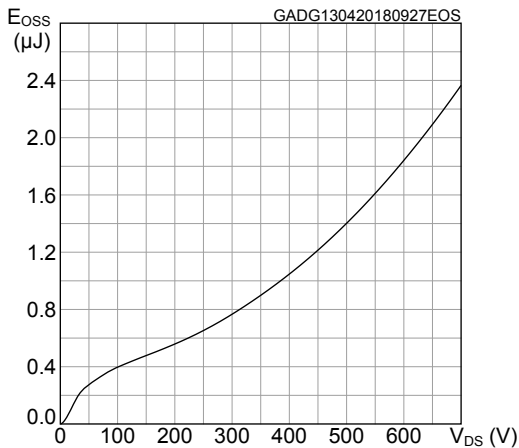
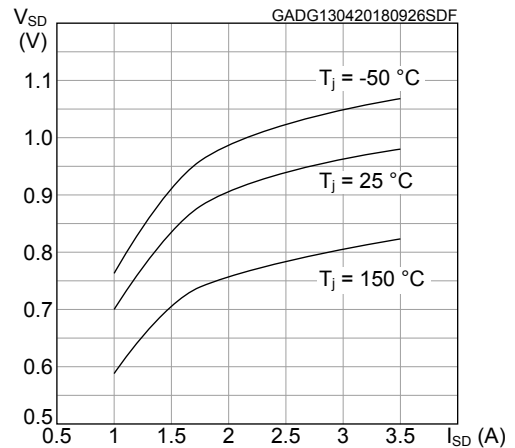
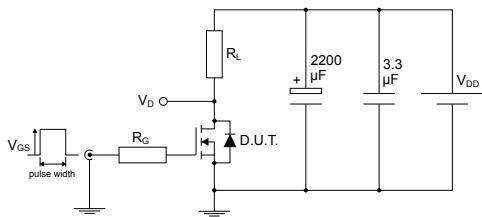


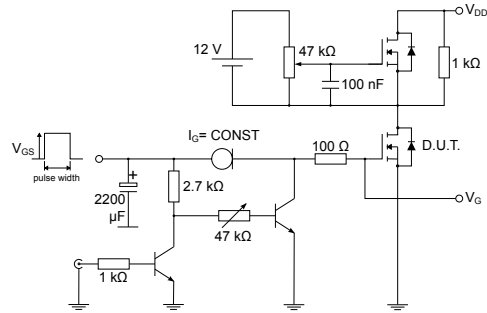
Figure 12. Source-drain forward characteristics



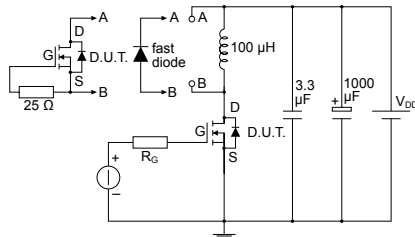
3 Test circuits

Figure 13. Test circuit for resistive load switching times


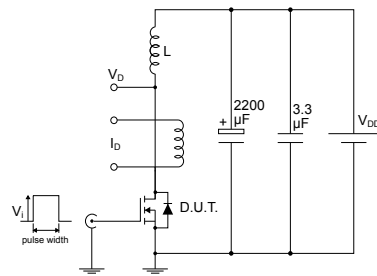
AM01468v1

Figure 14. Test circuit for gate charge behavior


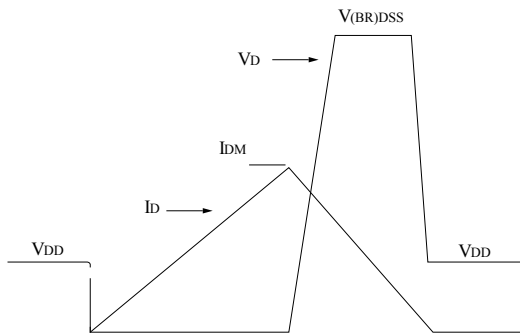
AM01469v1

Figure 15. Test circuit for inductive load switching and diode recovery times


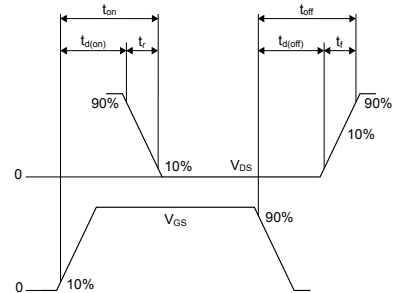
AM01470v1

Figure 16. Unclamped inductive load test circuit


AM01471v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 Short IPAK package information

Figure 19. Short IPAK package outline

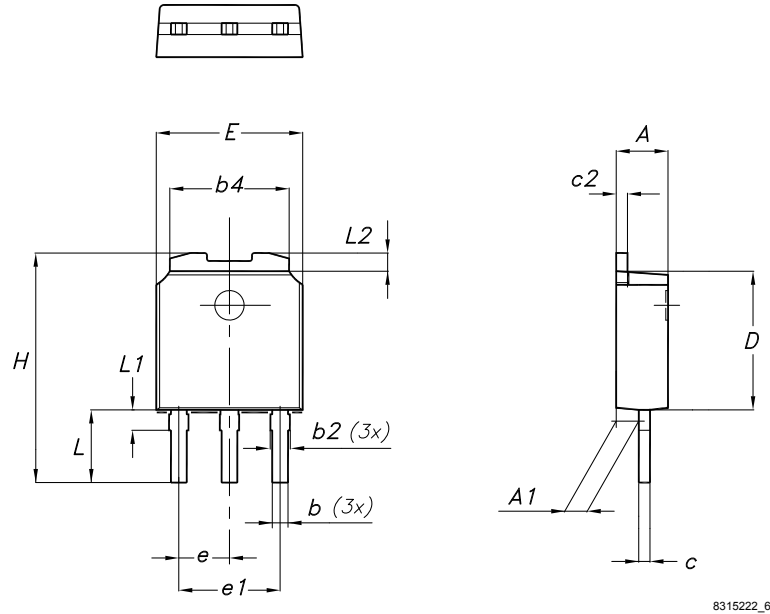


Table 8. Short IPAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.35
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.15
E	6.40		6.55
e		2.25	
e1	4.40		4.60
H	9.80		10.40
L	3.00		3.40
L1	0.80		1.20
L2		0.80	1.00

Revision history

Table 9. Document revision history

Date	Version	Changes
09-May-2018	1	Initial release. The document status is production data.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	7
4	Package information	8
4.1	Short IPAK package information	9
	Revision history	10

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved