

±270V Common Mode Voltage Difference Amplifier

FEATURES

- ±270V Common Mode Voltage Range
- 97dB Minimum CMRR (LT6375A)
- 0.0035% (35ppm) Maximum Gain Error (LT6375A)
- 1ppm/°C Maximum Gain Error Drift
- 2ppm Maximum Gain Nonlinearity
- Wide Supply Voltage Range: 3.3V to 50V
- Rail-to-Rail Output
- 350μA Supply Current
- Selectable Internal Resistor Divider Ratio
- 300μV Maximum Offset Voltage (LT6375A)
- 575kHz –3dB Bandwidth (Resistor Divider = 7)
- 375kHz –3dB Bandwidth (Resistor Divider = 20)
- –40°C to 125°C Specified Temperature Range
- Low Power Shutdown: 20μA (DFN Package Only)
- Space-Saving MSOP and DFN Packages

APPLICATIONS

- High Side or Low Side Current Sensing
- Bidirectional Wide Common Mode Range Current Sensing
- High Voltage to Low Voltage Level Translation
- Precision Difference Amplifier
- Industrial Data-Acquisition Front-Ends
- Replacement for Isolation Circuits

DESCRIPTION

The **LT®6375** is a unity-gain difference amplifier which combines excellent DC precision, a very high input common mode range and a wide supply voltage range. It includes a precision op amp and a highly-matched thin film resistor network. It features excellent CMRR, extremely low gain error and extremely low gain drift.

Comparing the LT6375 to existing difference amplifiers with high common mode voltage range, the selectable resistor divider ratios of the LT6375 offer superior system performance by allowing the user to achieve maximum SNR, precision and speed for a specific input common mode voltage range.

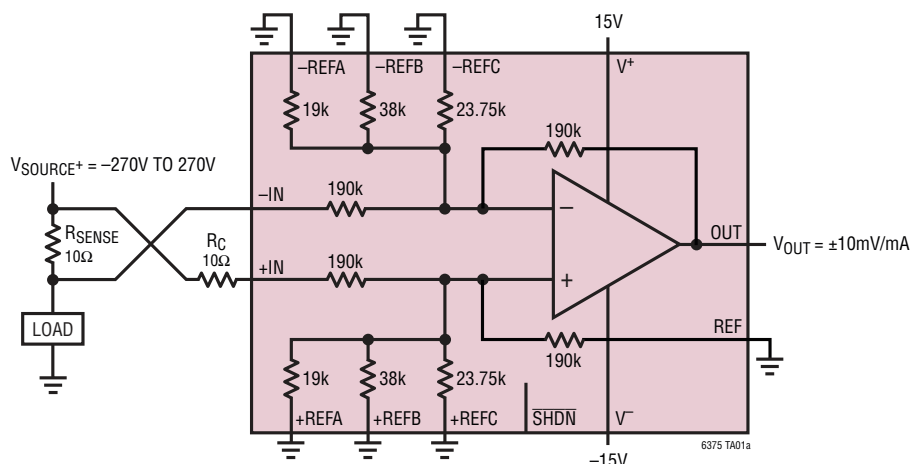
The op amp at the core of the LT6375 has Over-The-Top® protected inputs which allow for robust operation in environments with unpredictable voltage conditions. See the Applications Information section for more details.

The LT6375 is specified over the –40°C to 125°C temperature range and is available in space-saving MSOP16 and DFN14 packages.

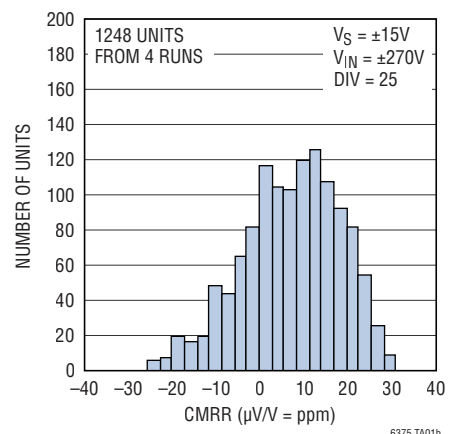
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TYPICAL APPLICATION

Precision Wide Voltage Range, Bidirectional Current Monitor



Typical Distribution of CMRR



6375fa

LT6375

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages

(V^+ to V^-)60V

+IN, -IN, (Note 2)

Each Input.....±270V

Differential±540V

+REFA, -REFA, +REFB, -REFB, +REFC, -REFC,
REF, $\overline{\text{SHDN}}$ (Note 2) ($V^+ + 0.3\text{V}$) to ($V^- - 0.3\text{V}$)

Output Current (Continuous) (Note 6)50mA

Output Short-Circuit Duration (Note 3) Thermally Limited
Temperature Range (Notes 4, 5)

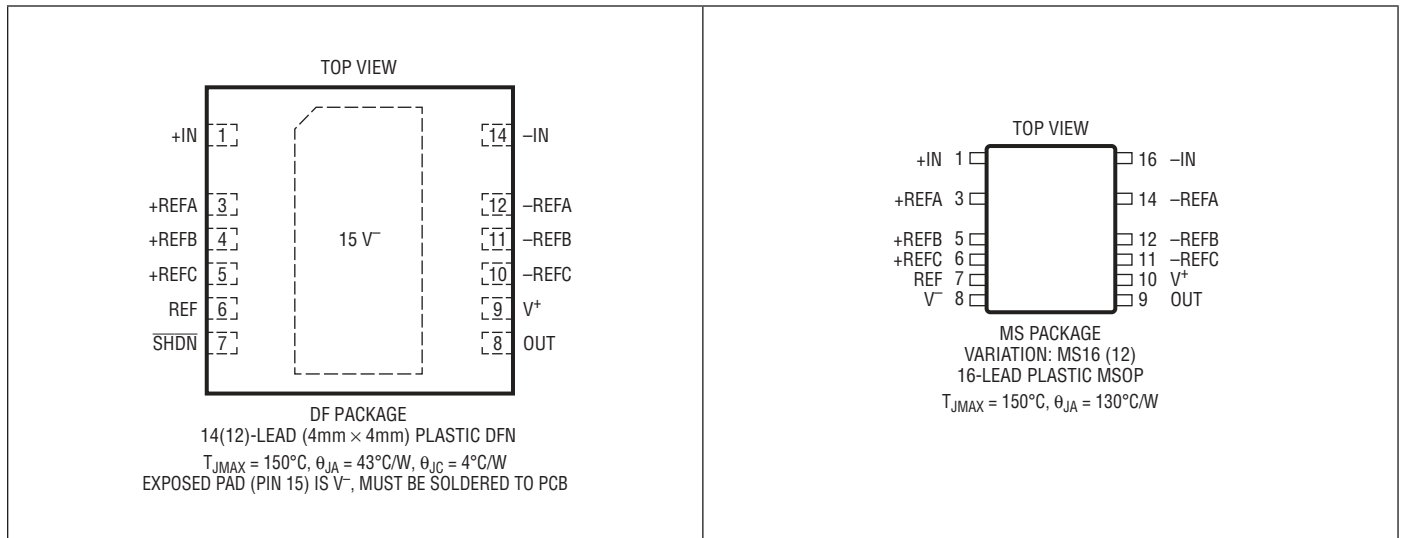
LT6375I.....-40°C to 85°C

LT6375H-40°C to 125°C

Storage Temperature Range-65°C to 150°C

MSOP Lead Temperature (Soldering, 10 sec).....300°C

PIN CONFIGURATION



ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|------------------|------------------|---------------|---------------------------------|-------------------|
| LT6375IDF#PBF | LT6375IDF#TRPBF | 6375 | 14-Lead (4mm × 4mm) Plastic DFN | -40°C to 85°C |
| LT6375HDF#PBF | LT6375HDF#TRPBF | 6375 | 14-Lead (4mm × 4mm) Plastic DFN | -40°C to 125°C |
| LT6375AHDF#PBF | LT6375AHDF#TRPBF | 6375 | 14-Lead (4mm × 4mm) Plastic DFN | -40°C to 125°C |
| LT6375IMS#PBF | LT6375IMS#TRPBF | 6375 | 16-Lead Plastic MSOP | -40°C to 85°C |
| LT6375HMS#PBF | LT6375HMS#TRPBF | 6375 | 16-Lead Plastic MSOP | -40°C to 125°C |
| LT6375AHMS#PBF | LT6375AHMS#TRPBF | 6375 | 16-Lead Plastic MSOP | -40°C to 125°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ for I-grade parts, $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$ for H-grade parts, otherwise specifications are at $T_A = 25^{\circ}\text{C}$, $V^+ = 15\text{V}$, $V^- = -15\text{V}$, $V_{CM} = V_{OUT} = V_{REF} = 0\text{V}$. V_{CMOP} is the common mode voltage of the internal op amp. For Resistor Divider Ratio = 7, $\pm\text{REFA} = \pm\text{REFC} = \text{OPEN}$, $\pm\text{REFB} = 0\text{V}$. For Resistor Divider Ratio = 20, $\pm\text{REFA} = \pm\text{REFC} = 0\text{V}$, $\pm\text{REFB} = \text{OPEN}$. For Resistor Divider Ratio = 25, $\pm\text{REFA} = \pm\text{REFB} = \pm\text{REFC} = 0\text{V}$.

| SYMBOL | PARAMETER | CONDITIONS | | LT6375A | | | LT6375 | | | UNITS |
|----------------------|--------------------------------------|--|---|---------------------------|------|------|--------------------------|-------|-----|------------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| G | Gain | V _{OUT} = ±10V | | 1 | | | 1 | | | V/V |
| ΔG | Gain Error | V _{OUT} = ±10V | ● | ±0.0007 ±0.0035 ±0.005 | | | ±0.001 ±0.006 ±0.0075 | | | % % |
| ΔG/ΔT | Gain Drift vs Temperature (Note 6) | V _{OUT} = ±10V | ● | ±0.2 ±1 | | | ±0.2 ±1 | | | ppm/°C |
| GNL | Gain Nonlinearity | V _{OUT} = ±10V | ● | ±1 ±2 ±3 | | | ±1 ±2 ±3 | | | ppm ppm |
| V _{OS} | Output Offset Voltage | V ⁻ < V _{CMOP} < V ⁺ -1.75V | | | | | | | | |
| | | Resistor Divider Ratio = 7 | ● | 100 | 300 | 120 | 450 | μV | | |
| | | Resistor Divider Ratio = 7 | ● | | 750 | | 1500 | μV | | |
| | | Resistor Divider Ratio = 20 | ● | 250 | 700 | 300 | 1200 | μV | | |
| | | Resistor Divider Ratio = 20 | ● | | 2000 | | 4000 | μV | | |
| | | Resistor Divider Ratio = 25 | ● | 300 | 900 | 400 | 1500 | μV | | |
| | | Resistor Divider Ratio = 25 | ● | | 2500 | | 5000 | μV | | |
| ΔV _{OS} /ΔT | Output Offset Voltage Drift (Note 6) | V ⁻ < V _{CMOP} < V ⁺ -1.75V | ● | | | | | | | |
| | | Resistor Divider Ratio = 7 | ● | 3 | 9 | 4 | 12 | μV/°C | | |
| | | Resistor Divider Ratio = 20 | | 8 | 23 | 10 | 30 | μV/°C | | |
| R _{IN} | Input Impedance (Note 8) | Common Mode | | | | | | | | |
| | | Resistor Divider Ratio = 7 | ● | 93 | 111 | 129 | 93 | 111 | 129 | kΩ |
| | | Resistor Divider Ratio = 20 | ● | 84 | 100 | 116 | 84 | 100 | 116 | kΩ |
| | | Resistor Divider Ratio = 25 | ● | 83 | 99 | 115 | 83 | 99 | 115 | kΩ |
| | | Differential | ● | 320 | 380 | 440 | 320 | 380 | 440 | kΩ |
| CMRR | Common Mode Rejection Ratio | MS16 Package | | | | | | | | |
| | | Resistor Divider Ratio = 7, V _{CM} = ±28V | ● | 96 | 106 | | 89 | 100 | | dB |
| | | Resistor Divider Ratio = 7, V _{CM} = ±28V | ● | 94 | | | 83 | | | dB |
| | | Resistor Divider Ratio = 20, V _{CM} = ±28V | ● | 96 | 106 | | 89 | 100 | | dB |
| | | Resistor Divider Ratio = 20, V _{CM} = ±28V | ● | 94 | | | 83 | | | dB |
| | | Resistor Divider Ratio = 25, V _{CM} = ±28V | ● | 96 | 106 | | 89 | 100 | | dB |
| | | Resistor Divider Ratio = 25, V _{CM} = ±28V | ● | 94 | | | 83 | | | dB |
| | | Resistor Divider Ratio = 25, V _{CM} = ±270V | ● | 97 | 107 | | 90 | 100 | | dB |
| | | Resistor Divider Ratio = 25, V _{CM} = ±270V | ● | 94 | | | 83 | | | dB |
| | | DF14 Package | | | | | | | | |
| | | Resistor Divider Ratio = 7, V _{CM} = ±28V | ● | 94 | 104 | | 89 | 100 | | dB |
| | | Resistor Divider Ratio = 7, V _{CM} = ±28V | ● | 92 | | | 83 | | | dB |
| | | Resistor Divider Ratio = 20, V _{CM} = ±28V | ● | 94 | 104 | | 89 | 100 | | dB |
| | | Resistor Divider Ratio = 20, V _{CM} = ±28V | ● | 92 | | | 83 | | | dB |
| | | Resistor Divider Ratio = 25, V _{CM} = ±28V | ● | 94 | 104 | | 89 | 100 | | dB |
| | | Resistor Divider Ratio = 25, V _{CM} = ±28V | ● | 92 | | | 83 | | | dB |
| | | Resistor Divider Ratio = 25, V _{CM} = ±270V | ● | 95 | 105 | | 90 | 100 | | dB |
| | | Resistor Divider Ratio = 25, V _{CM} = ±270V | ● | 92 | | | 83 | | | dB |
| V _{CM} | Input Voltage Range (Note 7) | | ● | -270 | 270 | -270 | 270 | V | | |
| PSRR | Power Supply Rejection Ratio | V _S = ±1.65V to ±25V, V _{CM} = V _{OUT} = Mid-Supply | | | | | | | | |
| | | Resistor Divider Ratio = 7 | ● | 101 | 115 | 98 | 110 | dB | | |
| | | Resistor Divider Ratio = 20 | ● | 93 | 104 | 90 | 100 | dB | | |
| | | Resistor Divider Ratio = 25 | ● | 91 | 101 | 88 | 100 | dB | | |

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ for I-grade parts, $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$ for H-grade parts, otherwise specifications are at $T_A = 25^{\circ}\text{C}$, $V^+ = 15\text{V}$, $V^- = -15\text{V}$, $V_{CM} = V_{OUT} = V_{REF} = 0\text{V}$. V_{CMOP} is the common mode voltage of the internal op amp. For Resistor Divider Ratio = 7, $\pm\text{REFA} = \pm\text{REFC} = \text{OPEN}$, $\pm\text{REFB} = 0\text{V}$. For Resistor Divider Ratio = 20, $\pm\text{REFA} = \pm\text{REFC} = 0\text{V}$, $\pm\text{REFB} = \text{OPEN}$. For Resistor Divider Ratio = 25, $\pm\text{REFA} = \pm\text{REFB} = \pm\text{REFC} = 0\text{V}$.

| SYMBOL | PARAMETER | CONDITIONS | LT6375A | | | LT6375 | | | UNITS |
|------------------------------|--|---|---------|------|------|--------|------|------|------------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| e_{no} | Output Referred Noise Voltage Density | $f = 1\text{kHz}$ | | | | | | | $\text{nV}/\sqrt{\text{Hz}}$ |
| | | Resistor Divider Ratio = 7 | | 250 | | | 250 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| | | Resistor Divider Ratio = 20 | | 508 | | | 508 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| | | Resistor Divider Ratio = 25 | | 599 | | | 599 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| | Output Referred Noise Voltage | $f = 0.1\text{Hz to } 10\text{Hz}$ | | | | | | | |
| | | Resistor Divider Ratio = 7 | | 10 | | | 10 | | μV_{P-P} |
| | | Resistor Divider Ratio = 20 | | 20 | | | 20 | | μV_{P-P} |
| | | Resistor Divider Ratio = 25 | | 25 | | | 25 | | μV_{P-P} |
| V_{OL} | Output Voltage Swing Low (Referred to V^-) | No Load $I_{SINK} = 5\text{mA}$ | ● | 5 | 50 | | 5 | 50 | mV |
| | | | ● | 280 | 500 | | 280 | 500 | mV |
| V_{OH} | Output Voltage Swing High (Referred to V^+) | No Load $I_{SOURCE} = 5\text{mA}$ | ● | 5 | 20 | | 5 | 20 | mV |
| | | | ● | 400 | 750 | | 400 | 750 | mV |
| I_{SC} | Short-Circuit Output Current | 50Ω to V^+ 50Ω to V^- | ● | 10 | 28 | | 10 | 28 | mA |
| | | | ● | 10 | 30 | | 10 | 30 | mA |
| SR | Slew Rate | $\Delta V_{OUT} = \pm 5\text{V}$ | ● | 1.6 | 2.4 | | 1.6 | 2.4 | V/ μs |
| BW | Small Signal -3dB Bandwidth | Resistor Divider Ratio = 7 | | 575 | | | 575 | | kHz |
| | | Resistor Divider Ratio = 20 | | 375 | | | 375 | | kHz |
| | | Resistor Divider Ratio = 25 | | 310 | | | 310 | | kHz |
| t_S | Settling Time | Resistor Divider Ratio = 7 | | | | | | | |
| | | 0.01%, $\Delta V_{OUT} = 10\text{V}$ | | 41 | | | 41 | | μs |
| | | 0.1%, $\Delta V_{OUT} = 10\text{V}$ | | 14 | | | 14 | | μs |
| | | 0.01%, $\Delta V_{CM} = 10\text{V}$, $\Delta V_{DIFF} = 0\text{V}$ | | 100 | | | 100 | | μs |
| | | Resistor Divider Ratio = 20 | | | | | | | |
| | | 0.01%, $\Delta V_{OUT} = 10\text{V}$ | | 31 | | | 31 | | μs |
| | | 0.1%, $\Delta V_{OUT} = 10\text{V}$ | | 11 | | | 11 | | μs |
| | | 0.01%, $\Delta V_{CM} = 10\text{V}$, $\Delta V_{DIFF} = 0\text{V}$ | | 100 | | | 100 | | μs |
| | | Resistor Divider Ratio = 25 | | | | | | | |
| V_S | Supply Voltage | | ● | 3 | 50 | | 3 | 50 | V |
| | | | | 3.3 | 50 | | 3.3 | 50 | V |
| | | | | | | | | | |
| t_{ON} | Turn-On Time | | | 16 | | | 16 | | μs |
| V_{IL} | $\overline{\text{SHDN}}$ Input Logic Low (Referred to V^+) | | ● | | -2.5 | | | -2.5 | V |
| V_{IH} | $\overline{\text{SHDN}}$ Input Logic High (Referred to V^+) | | ● | -1.2 | | | -1.2 | | V |
| $I_{\overline{\text{SHDN}}}$ | $\overline{\text{SHDN}}$ Pin Current | | ● | -10 | -15 | | -10 | -15 | μA |
| I_S | Supply Current | Active, $V_{\overline{\text{SHDN}}} \geq V^+ - 1.2\text{V}$ | | 350 | 400 | | 350 | 400 | μA |
| | | Active, $V_{\overline{\text{SHDN}}} \geq V^+ - 1.2\text{V}$ | ● | | 600 | | | 600 | μA |
| | | Shutdown, $V_{\overline{\text{SHDN}}} \leq V^+ - 2.5\text{V}$ | | 20 | 25 | | 20 | 25 | μA |
| | | Shutdown, $V_{\overline{\text{SHDN}}} \leq V^+ - 2.5\text{V}$ | ● | | 70 | | | 70 | μA |

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ for I-grade parts, $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$ for H-grade parts, otherwise specifications are at $T_A = 25^{\circ}\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = V_{\text{REF}} = \text{Mid-Supply}$. V_{CMOP} is the common mode voltage of the internal op amp. For Resistor Divider Ratio = 7, $\pm\text{REFA} = \pm\text{REFC} = \text{OPEN}$, $\pm\text{REFB} = \text{Mid-Supply}$. For Resistor Divider Ratio = 20, $\pm\text{REFA} = \pm\text{REFC} = \text{Mid-Supply}$, $\pm\text{REFB} = \text{OPEN}$. For Resistor Divider Ratio = 25, $\pm\text{REFA} = \pm\text{REFB} = \pm\text{REFC} = \text{Mid-Supply}$.

| SYMBOL | PARAMETER | CONDITIONS | LT6375A | | | LT6375 | | | UNITS |
|---------------------------------|---------------------------------------|--|-----------------------|----------------------------------|--|----------------------------------|---|--------------------------|--|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| G | Gain | $V_{\text{OUT}} = 1\text{V to } 4\text{V}$ | | 1 | | | 1 | | V/V |
| ΔG | Gain Error | $V_{\text{OUT}} = 1\text{V to } 4\text{V}$ | ● | ± 0.0007 | ± 0.0035 ± 0.005 | ± 0.001 | ± 0.006 ± 0.0075 | | % % |
| $\Delta G/\Delta T$ | Gain Drift vs Temperature (Note 6) | $V_{\text{OUT}} = 1\text{V to } 4\text{V}$ | ● | ± 0.2 | ± 1 | ± 0.2 | ± 1 | | ppm/ $^{\circ}\text{C}$ |
| GNL | Gain Nonlinearity | $V_{\text{OUT}} = 1\text{V to } 4\text{V}$ | | ± 1 | | ± 1 | | | ppm |
| V_{OS} | Output Offset Voltage | $0 < V_{\text{CMOP}} < V^+ - 1.75\text{V}$ Resistor Divider Ratio = 7 Resistor Divider Ratio = 7 Resistor Divider Ratio = 20 Resistor Divider Ratio = 20 Resistor Divider Ratio = 25 Resistor Divider Ratio = 25 | ● | 100 250 300 | 300 750 700 2000 900 2500 | 120 300 400 | 500 1500 1200 4000 1500 5000 | | μV μV μV μV μV μV |
| $\Delta V_{\text{OS}}/\Delta T$ | Output Offset Voltage Drift (Note 6) | $0 < V_{\text{CMOP}} < V^+ - 1.75\text{V}$ Resistor Divider Ratio = 7 Resistor Divider Ratio = 20 | ● ● | 3 8 | 9 23 | 4 10 | 12 30 | | $\mu\text{V}/^{\circ}\text{C}$ $\mu\text{V}/^{\circ}\text{C}$ |
| R_{IN} | Input Impedance (Note 8) | Common Mode Resistor Divider Ratio = 7 Resistor Divider Ratio = 20 Resistor Divider Ratio = 25 Differential | ● ● ● ● | 93 84 83 320 | 111 100 99 380 | 129 116 115 440 | 93 111 129 320 | 111 116 115 440 | $\text{k}\Omega$ $\text{k}\Omega$ $\text{k}\Omega$ $\text{k}\Omega$ |
| CMRR | Common Mode Rejection Ratio | MS16 Package Resistor Divider Ratio = 7 $V_{\text{CM}} = -15\text{V to } +7.75\text{V}$ $V_{\text{CM}} = -15\text{V to } +7.75\text{V}$ Resistor Divider Ratio = 20 $V_{\text{CM}} = -25.5\text{V to } +17.5\text{V}$ $V_{\text{CM}} = -25.5\text{V to } +17.5\text{V}$ Resistor Divider Ratio = 25 $V_{\text{CM}} = -25.5\text{V to } +21.25\text{V}$ $V_{\text{CM}} = -25.5\text{V to } +21.25\text{V}$ | ● ● ● ● ● | 94 92 94 92 94 92 | 105 105 105 105 | 85 83 85 83 85 83 | 95 95 95 95 | | dB dB dB dB dB dB |
| | | DF14 Package Resistor Divider Ratio = 7 $V_{\text{CM}} = -15\text{V to } +7.75\text{V}$ $V_{\text{CM}} = -15\text{V to } +7.75\text{V}$ Resistor Divider Ratio = 20 $V_{\text{CM}} = -25.5\text{V to } +17.5\text{V}$ $V_{\text{CM}} = -25.5\text{V to } +17.5\text{V}$ Resistor Divider Ratio = 25 $V_{\text{CM}} = -25.5\text{V to } +21.25\text{V}$ $V_{\text{CM}} = -25.5\text{V to } +21.25\text{V}$ | ● ● ● ● ● | 92 90 92 90 92 90 | 103 103 103 103 | 85 83 85 83 85 83 | 95 95 95 95 | | dB dB dB dB dB dB |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 1.65\text{V to } \pm 25\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = \text{Mid-Supply}$ Resistor Divider Ratio = 7 Resistor Divider Ratio = 20 Resistor Divider Ratio = 25 | ● ● ● | 101 93 91 | 115 104 101 | 98 90 88 | 110 100 100 | | dB dB dB |
| e_{no} | Output Referred Noise Voltage Density | $f = 1\text{kHz}$ Resistor Divider Ratio = 7 Resistor Divider Ratio = 20 Resistor Divider Ratio = 25 | | 250 508 599 | | 250 508 599 | | | $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ |

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ for I-grade parts, $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$ for H-grade parts, otherwise specifications are at $T_A = 25^{\circ}\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_{OUT} = V_{REF} = \text{Mid-Supply}$. V_{CMOP} is the common mode voltage of the internal op amp. For Resistor Divider Ratio = 7, $\pm\text{REFA} = \pm\text{REFC} = \text{OPEN}$, $\pm\text{REFB} = \text{Mid-Supply}$. For Resistor Divider Ratio = 20, $\pm\text{REFA} = \pm\text{REFC} = \text{Mid-Supply}$, $\pm\text{REFB} = \text{OPEN}$. For Resistor Divider Ratio = 25, $\pm\text{REFA} = \pm\text{REFB} = \pm\text{REFC} = \text{Mid-Supply}$.

| SYMBOL | PARAMETER | CONDITIONS | LT6375A | | | LT6375 | | | UNITS |
|------------------------------|--|--|---------|----------------|------|--------|----------------|------|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| | Output Referred Noise Voltage | $f = 0.1\text{Hz to } 10\text{Hz}$ Resistor Divider Ratio = 7 Resistor Divider Ratio = 20 Resistor Divider Ratio = 25 | | 10 20 25 | | | 10 20 25 | | μV_{P-P} μV_{P-P} μV_{P-P} |
| V_{OL} | Output Voltage Swing Low (Referred to V^-) | No Load $I_{SINK} = 5\text{mA}$ | ● | 5 | 50 | | 5 | 50 | mV |
| | | | ● | 280 | 500 | | 280 | 500 | mV |
| V_{OH} | Output Voltage Swing High (Referred to V^+) | No Load $I_{SOURCE} = 5\text{mA}$ | ● | 5 | 20 | | 5 | 20 | mV |
| | | | ● | 400 | 750 | | 400 | 750 | mV |
| I_{SC} | Short-Circuit Output Current | 50Ω to V^+ 50Ω to V^- | ● | 10 | 27 | | 10 | 27 | mA |
| | | | ● | 10 | 25 | | 10 | 25 | mA |
| SR | Slew Rate | $\Delta V_{OUT} = 3\text{V}$ | ● | 1.3 | 2 | | 1.3 | 2 | V/ μs |
| BW | Small Signal –3dB Bandwidth | Resistor Divider Ratio = 7 | | 565 | | | 565 | | kHz |
| | | Resistor Divider Ratio = 20 | | 380 | | | 380 | | kHz |
| | | Resistor Divider Ratio = 25 | | 325 | | | 325 | | kHz |
| t_S | Settling Time | Resistor Divider Ratio = 7 0.01%, $\Delta V_{OUT} = 2\text{V}$ | | 18 | | | 18 | | μs |
| | | 0.1%, $\Delta V_{OUT} = 2\text{V}$ | | 10 | | | 10 | | μs |
| | | 0.01%, $\Delta V_{CM} = 2\text{V}$, $\Delta V_{DIFF} = 0\text{V}$ | | 64 | | | 64 | | μs |
| | | Resistor Divider Ratio = 20 0.01%, $\Delta V_{OUT} = 2\text{V}$ | | 24 | | | 24 | | μs |
| | | 0.1%, $\Delta V_{OUT} = 2\text{V}$ | | 7 | | | 7 | | μs |
| | | 0.01%, $\Delta V_{CM} = 2\text{V}$, $\Delta V_{DIFF} = 0\text{V}$ | | 48 | | | 48 | | μs |
| | | Resistor Divider Ratio = 25 0.01%, $\Delta V_{OUT} = 2\text{V}$ | | 27 | | | 27 | | μs |
| | | 0.1%, $\Delta V_{OUT} = 2\text{V}$ | | 9 | | | 9 | | μs |
| | | 0.01%, $\Delta V_{CM} = 2\text{V}$, $\Delta V_{DIFF} = 0\text{V}$ | | 20 | | | 20 | | μs |
| V_S | Supply Voltage | | ● | 3 | 50 | | 3 | 50 | V |
| | | | | 3.3 | 50 | | 3.3 | 50 | V |
| t_{ON} | Turn-On Time | | | 22 | | | 22 | | μs |
| V_{IL} | $\overline{\text{SHDN}}$ Input Logic Low (Referred to V^+) | | ● | | –2.5 | | | –2.5 | V |
| V_{IH} | $\overline{\text{SHDN}}$ Input Logic High (Referred to V^+) | | ● | –1.2 | | | –1.2 | | V |
| $I_{\overline{\text{SHDN}}}$ | $\overline{\text{SHDN}}$ Pin Current | | ● | –10 | –15 | | –10 | –15 | μA |
| I_S | Supply Current | Active, $V_{\overline{\text{SHDN}}} \geq V^+ - 1.2\text{V}$ | | 330 | 370 | | 330 | 370 | μA |
| | | Active, $V_{\overline{\text{SHDN}}} \geq V^+ - 1.2\text{V}$ | ● | | 525 | | | 525 | μA |
| | | Shutdown, $V_{\overline{\text{SHDN}}} \leq V^+ - 2.5\text{V}$ | | 15 | 20 | | 15 | 20 | μA |
| | | Shutdown, $V_{\overline{\text{SHDN}}} \leq V^+ - 2.5\text{V}$ | ● | | 40 | | | 40 | μA |

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: See Common Mode Voltage Range in the Applications Information section of this data sheet for other considerations when taking $+IN/-IN$ pins to $\pm 270V$. All other pins should not be taken more than 0.3V beyond the supply rails.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum. This depends on the power supply, input voltages and the output current.

Note 4: The LT6375I is guaranteed functional over the operating temperature range of $-40^{\circ}C$ to $85^{\circ}C$. The LT6375H is guaranteed functional over the operating temperature range of $-40^{\circ}C$ to $125^{\circ}C$.

Note 5: The LT6375I is guaranteed to meet specified performance from $-40^{\circ}C$ to $85^{\circ}C$. The LT6375H is guaranteed to meet specified performance from $-40^{\circ}C$ to $125^{\circ}C$.

Note 6: This parameter is not 100% tested.

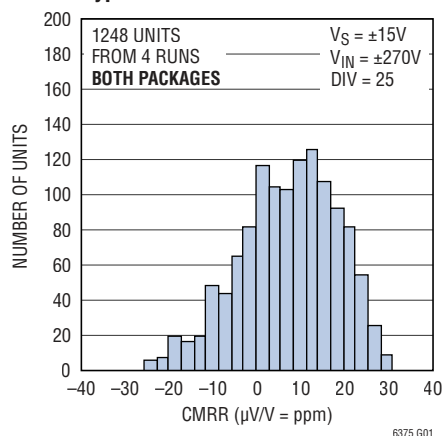
Note 7: Input voltage range is guaranteed by the CMRR test at $V_S = \pm 15V$ and all REF pins at ground (Resistor Divider Ratio = 25). For the other voltages, this parameter is guaranteed by design and through correlation with the $\pm 15V$ test. See Common Mode Voltage Range in the Applications Information section to determine the valid input voltage range under various operating conditions.

Note 8: Input impedance is tested by a combination of direct measurement and correlation to the CMRR and gain error tests.

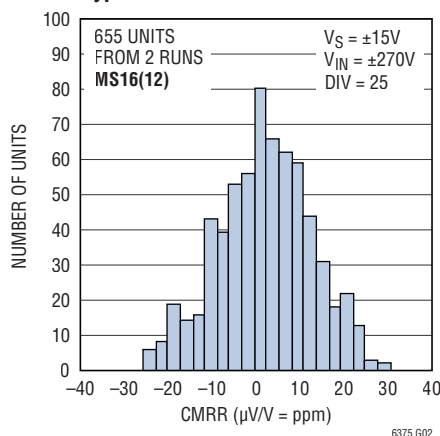
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^{\circ}C$, $V_S = \pm 15V$, unless otherwise noted.

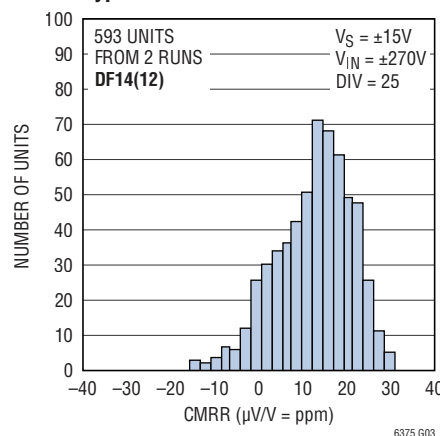
Typical Distribution of CMRR



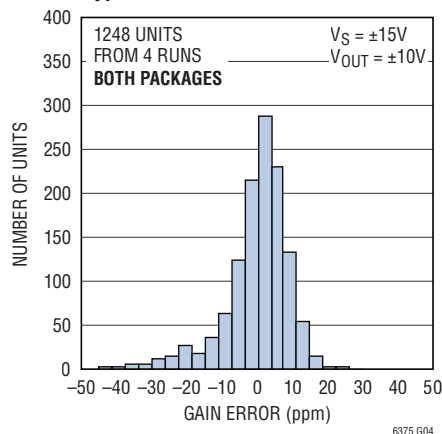
Typical Distribution of CMRR



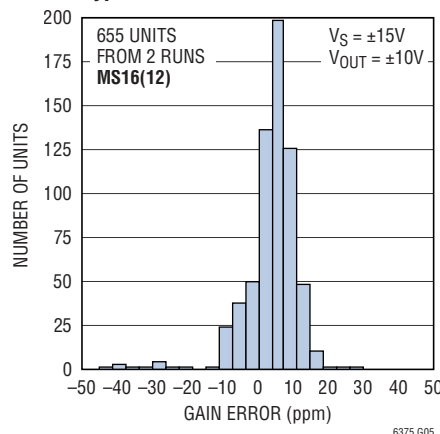
Typical Distribution of CMRR



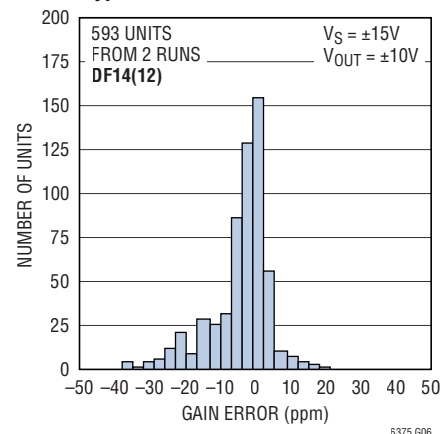
Typical Distribution of Gain Error



Typical Distribution of Gain Error

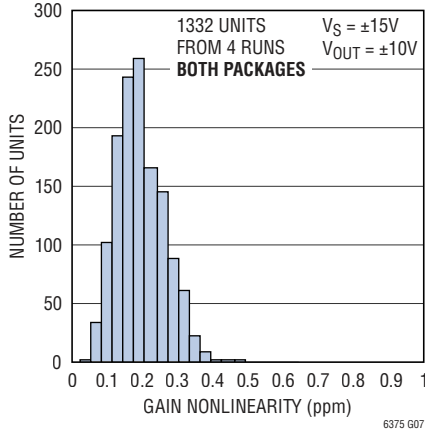


Typical Distribution of Gain Error

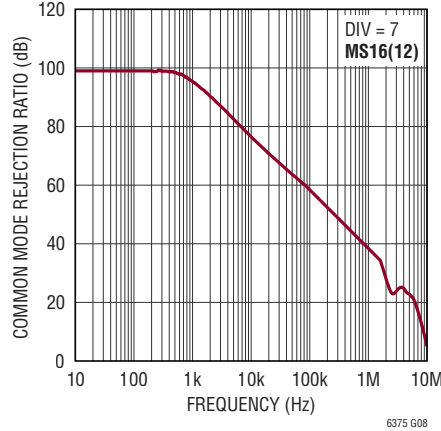


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

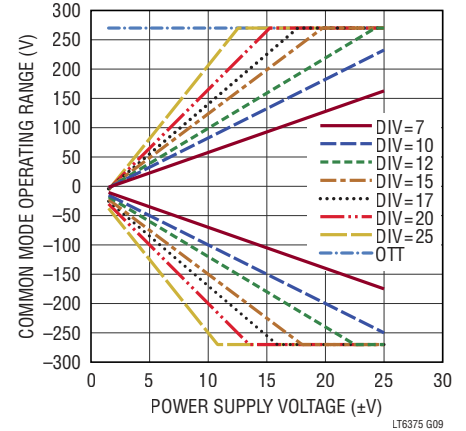
Typical Distribution of Gain Nonlinearity



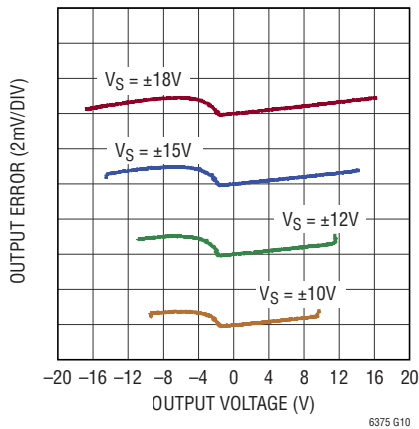
CMRR vs Frequency



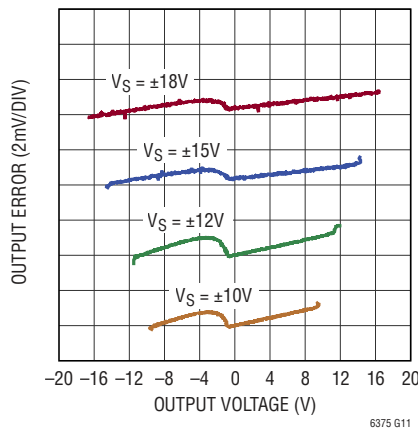
Common Mode Voltage Range vs Power Supply Voltage



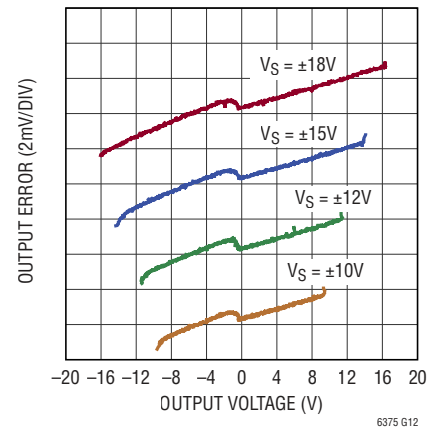
Typical Gain Error for $R_L = 10\text{k}\Omega$ (Curves Offset for Clarity)



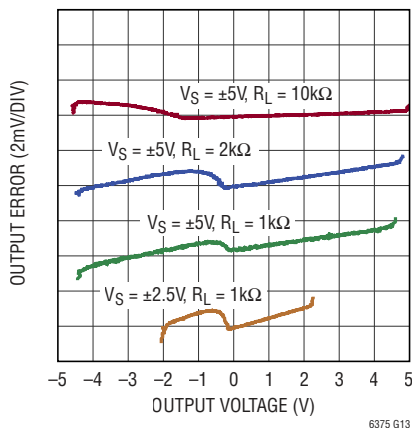
Typical Gain Error for $R_L = 5\text{k}\Omega$ (Curves Offset for Clarity)



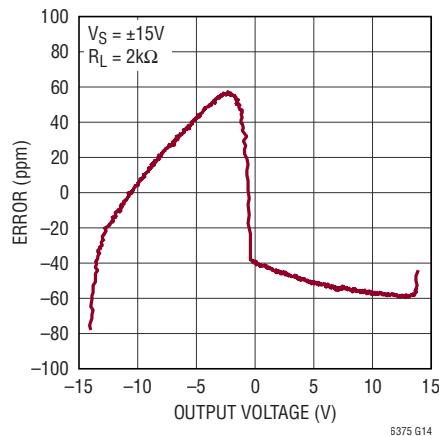
Typical Gain Error for $R_L = 2\text{k}\Omega$ (Curves Offset for Clarity)



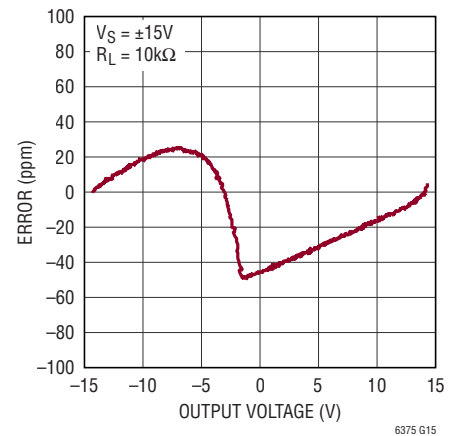
Typical Gain Error for Low Supply Voltages (Curves Offset for Clarity)



Gain Nonlinearity

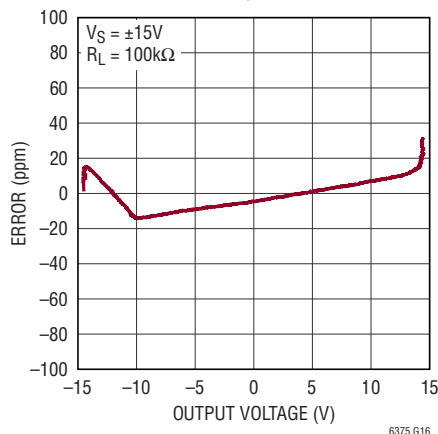


Gain Nonlinearity

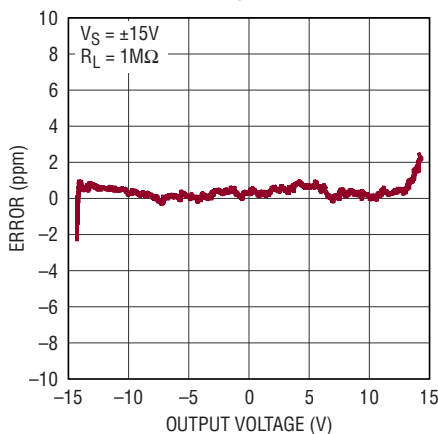


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

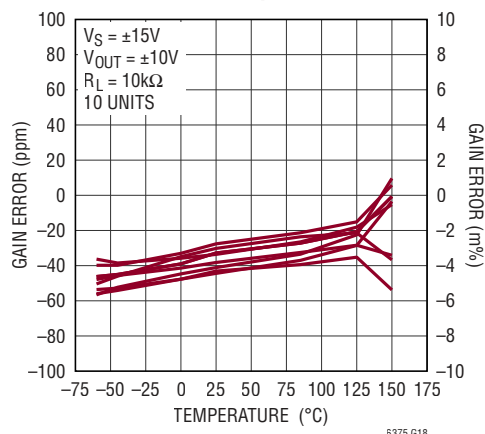
Gain Nonlinearity



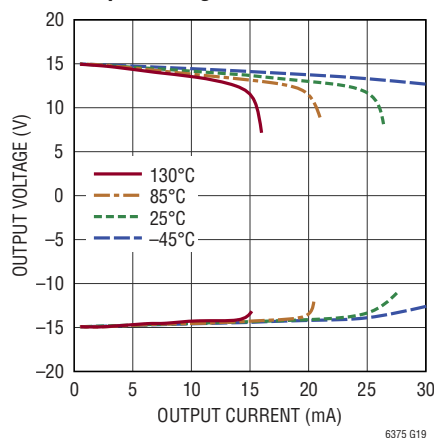
Gain Nonlinearity



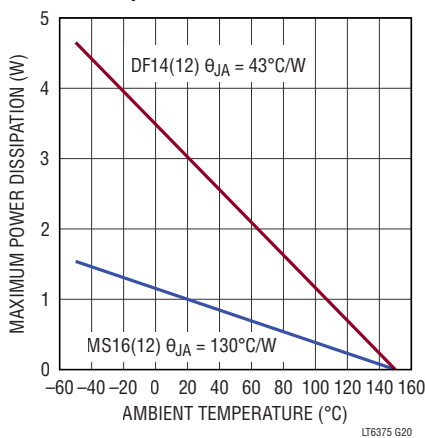
Gain Error vs Temperature



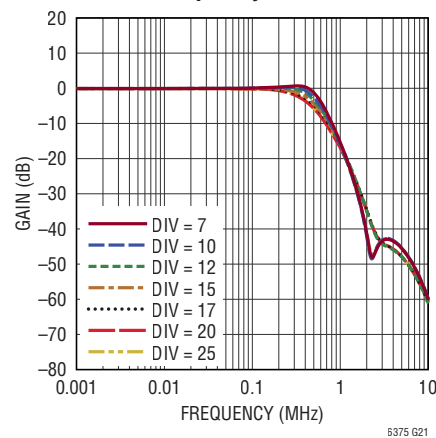
Output Voltage vs Load Current



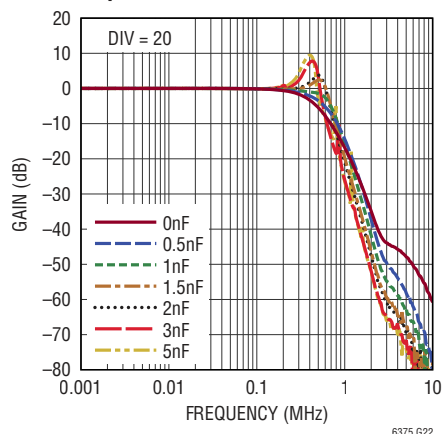
Maximum Power Dissipation vs Temperature



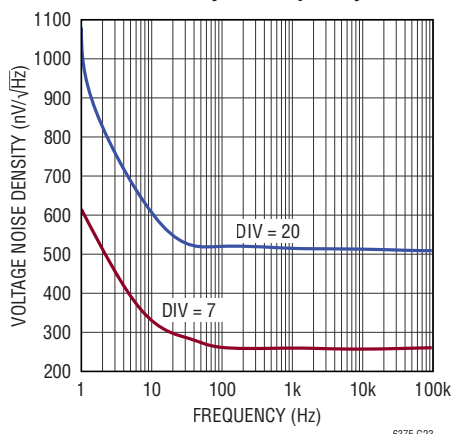
Gain vs Frequency



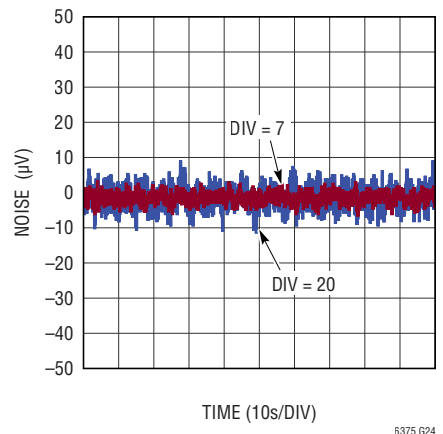
Frequency Response vs Capacitive Load



Noise Density vs Frequency

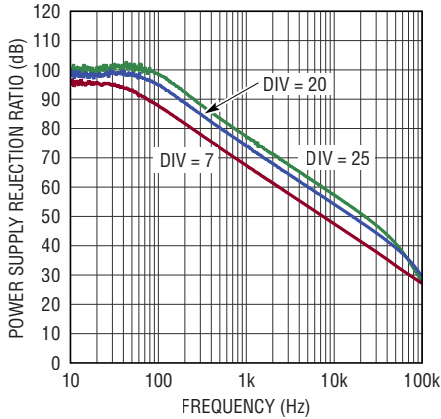


0.1Hz to 10Hz Noise

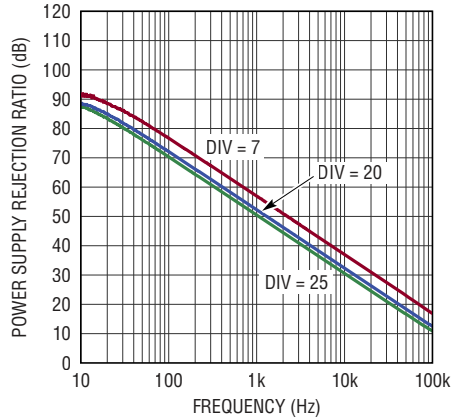


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

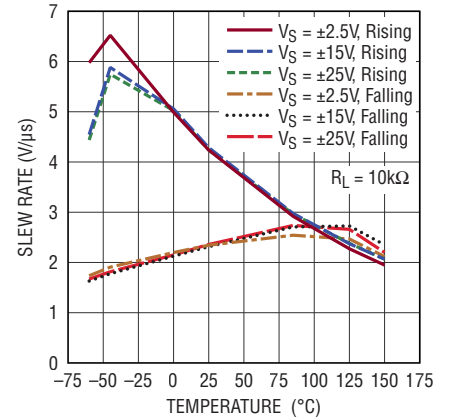
Positive PSRR vs Frequency



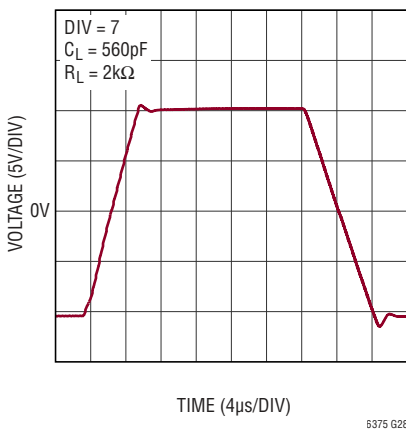
Negative PSRR vs Frequency



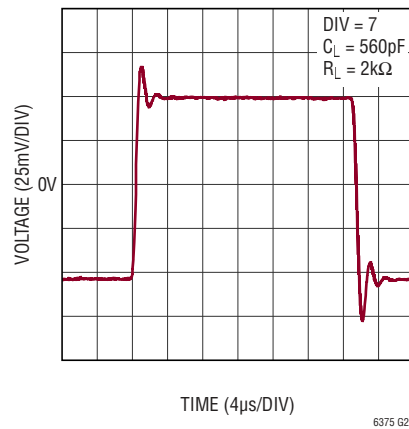
Slew Rate vs Temperature



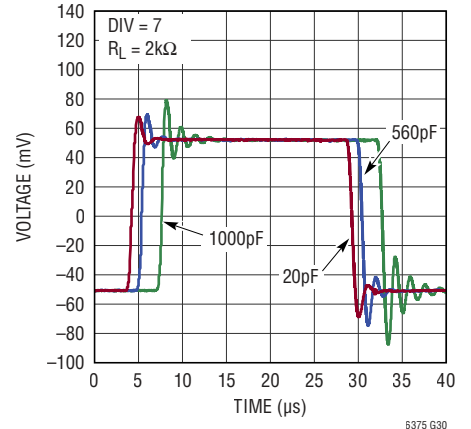
Large-Signal Step Response



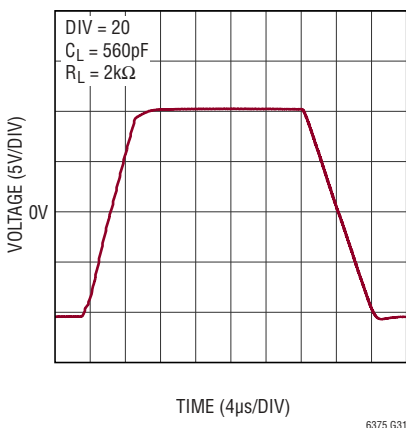
Small-Signal Step Response



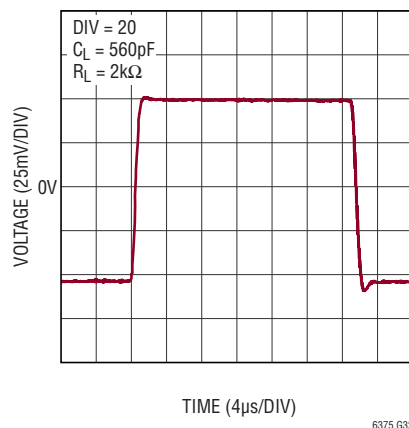
Small-Signal Step Response vs Capacitive Load



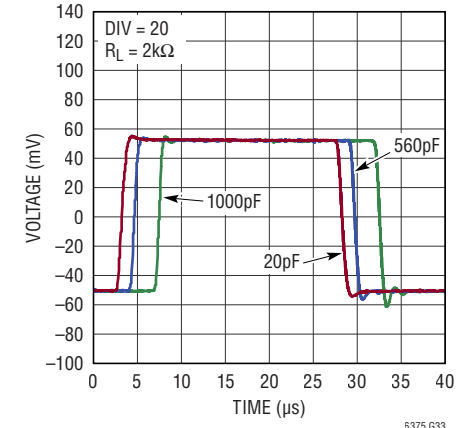
Large-Signal Step Response



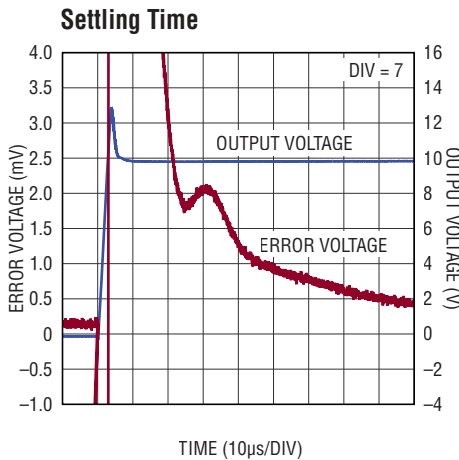
Small-Signal Step Response



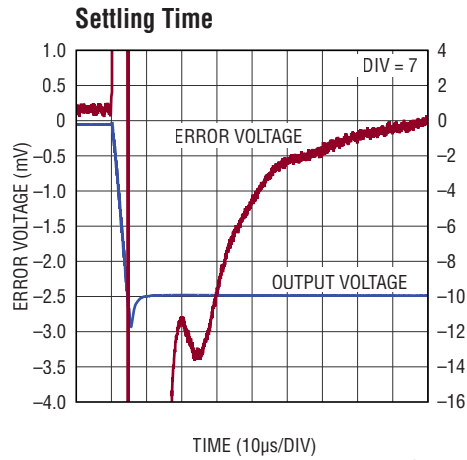
Small-Signal Step Response vs Capacitive Load



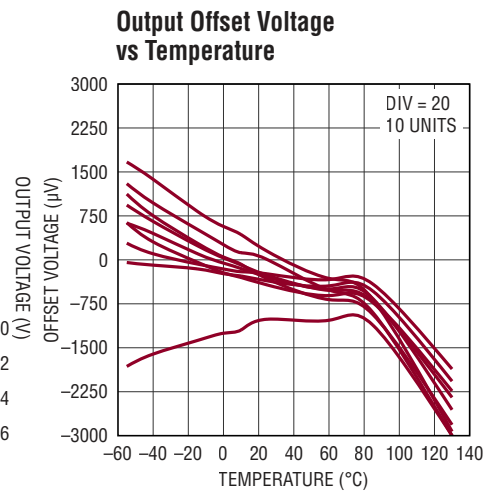
TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



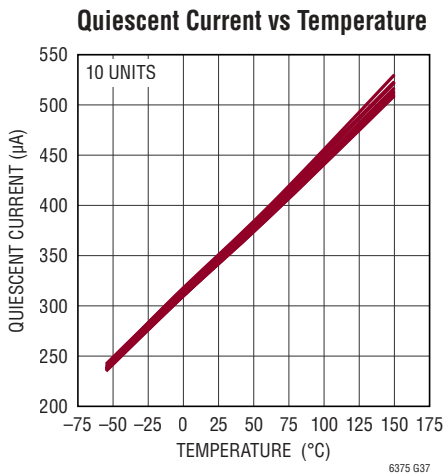
6375 G34



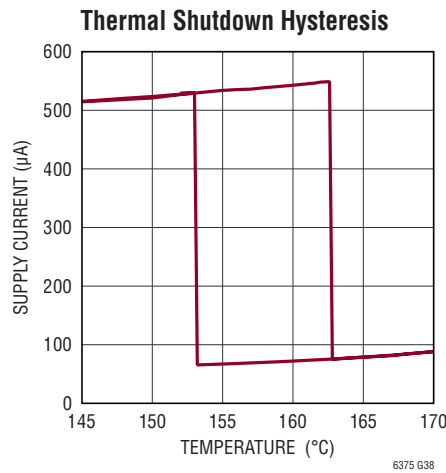
6375 G35



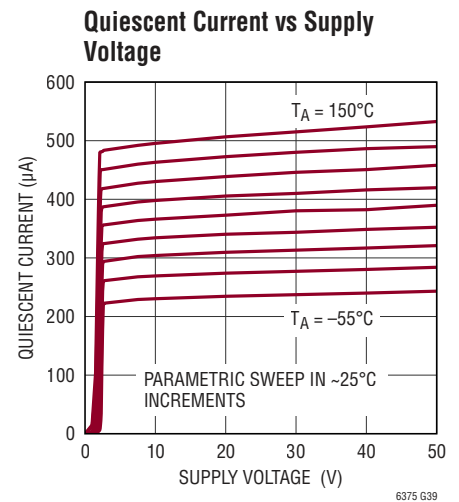
6375 G36



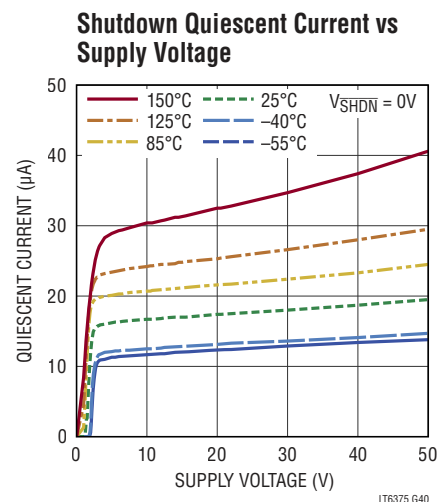
6375 G37



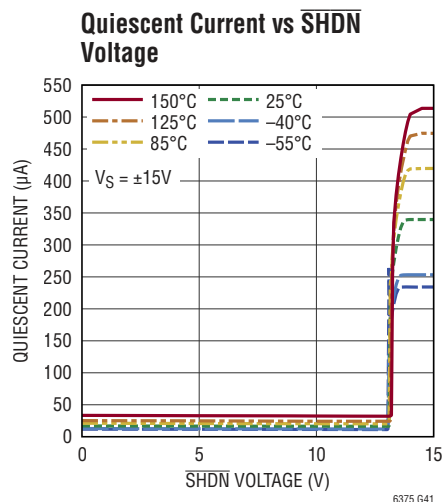
6375 G38



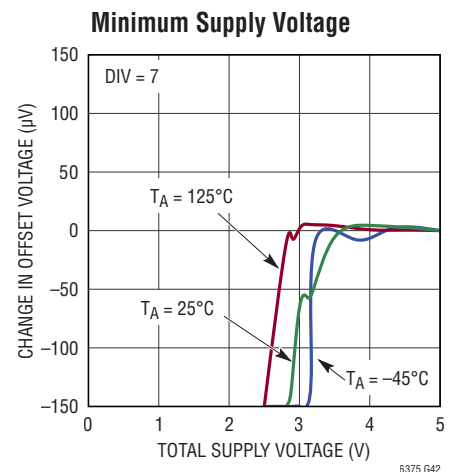
6375 G39



LT6375 G40



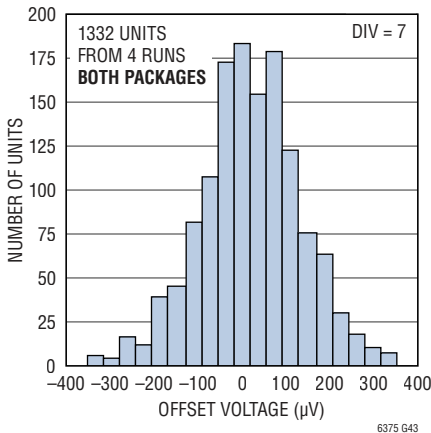
6375 G41



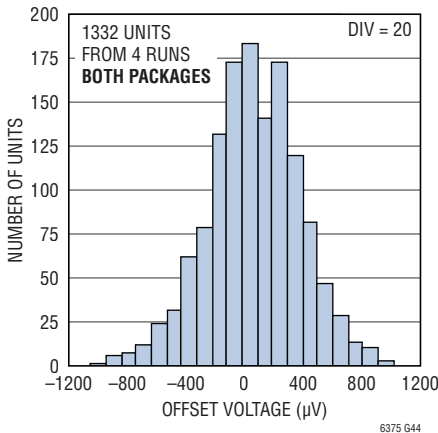
6375 G42

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^{\circ}\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

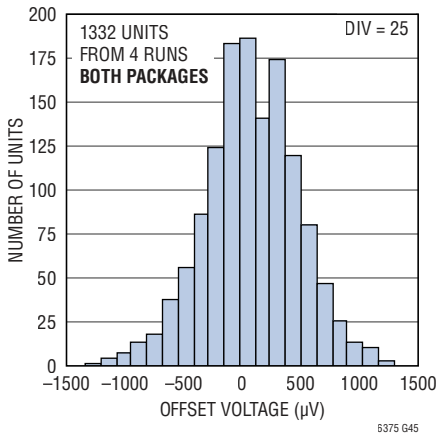
Typical Distribution of Output Offset Voltage



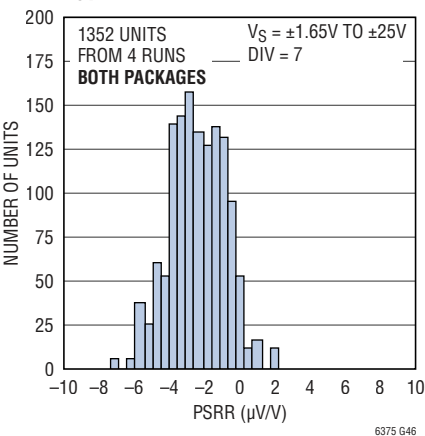
Typical Distribution of Output Offset Voltage



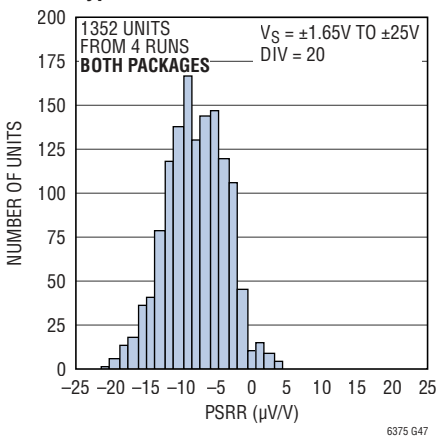
Typical Distribution of Output Offset Voltage



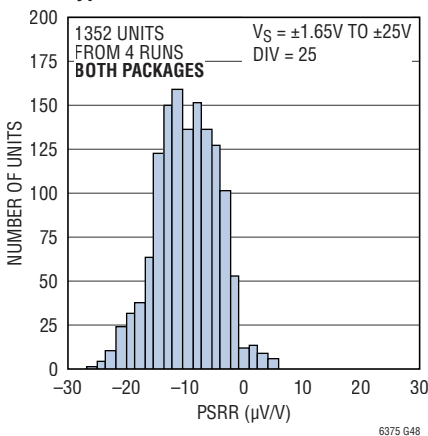
Typical Distribution of PSRR



Typical Distribution of PSRR



Typical Distribution of PSRR



PIN FUNCTIONS (DFN/MSOP)

V⁺ (Pin 9/Pin 10): Positive Supply Pin.

V⁻ (Exposed Pad Pin 15/Pin 8): Negative Supply Pin.

OUT (Pin 8/Pin 9): Output Pin.

+IN (Pin 1/Pin 1): Noninverting Input Pin. Accepts input voltages from 270V to -270V.

+REFA (Pin 3/Pin 3): Reference Pin A. Sets the input common mode range and the output noise and offset.

+REFB (Pin 4/Pin 5): Reference Pin B. Sets the input common mode range and the output noise and offset.

+REFC (Pin 5/Pin 6): Reference Pin C. Sets the input common mode range and the output noise and offset.

-IN (Pin 14/Pin 16): Inverting Input Pin. Accepts input voltages from 270V to -270V.

-REFA (Pin 12/Pin 14): Reference Pin A. Sets the input common mode range and the output noise and offset.

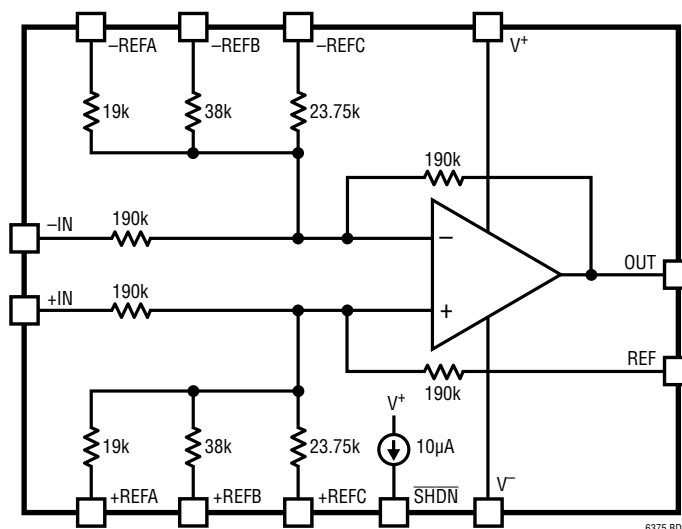
-REFB (Pin 11/Pin 12): Reference Pin B. Sets the input common mode range and the output noise and offset.

-REFC (Pin 10/Pin 11): Reference Pin C. Sets the input common mode range and the output noise and offset.

REF (Pin 6/Pin 7): Reference Input. Sets the output level when the difference between the inputs is zero.

SHDN (Pin 7) DFN Only: Shutdown Pin. Amplifier is active when this pin is tied to V⁺ or left floating. Pulling the pin >2.5V below V⁺ causes the amplifier to enter a low power state.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

TRANSFER FUNCTION

The LT6375 is a unity-gain difference amplifier with the transfer function:

$$V_{OUT} = (V_{+IN} - V_{-IN}) + V_{REF}$$

The voltage on the REF pin sets the output voltage when the differential input voltage ($V_{DIFF} = V_{+IN} - V_{-IN}$) is zero. This reference is used to shift the output voltage to the desired input level of the next stage of the signal chain.

BENEFITS OF SELECTABLE RESISTOR DIVIDER RATIOS

The LT6375 offers smaller package size, better gain accuracy and better noise performance than existing high common mode voltage range difference amplifiers. Additionally, the LT6375 allows the user to maximize system performance by selecting the resistor divider ratio (DIV) appropriate to their input common mode voltage range. A higher resistor divider ratio (DIV) enables higher common mode voltage range at the input pins, but also increases output noise, output offset/drift and decreases the -3dB bandwidth. Therefore, a trade-off exists between input range and DC, AC, and drift performance of the part. It

is recommended that the user choose the lowest resistor divider ratio that achieves the required input common mode voltage range in their application to maximize the system SNR, precision and speed.

Table 1 shows the noise, offset/drift, and -3dB bandwidth of the LT6375 for all different reference pins configurations.

COMMON MODE VOLTAGE RANGE

The wide common mode voltage range of the LT6375 is enabled by both a resistor divider at the input of the op amp and by an internal op amp that can withstand high input voltages.

The internal resistor network of the LT6375 divides down the input common mode voltage. The resulting voltage at the op amp inputs determines the op amp's operating region. In the configuration shown in Figure 1, a resistor divider is created at both op amp inputs by the 190k input resistor and the resistance from each input to ground, which is ~31.66k. The resistance to ground is formed by the 38k (REFB resistors) in parallel with the 190k (feedback/REF resistor). The result is a divide by 7 of the input voltage. As shown in Tables 1 to 5, different connections to reference pins (i.e. pins +REFA, -REFA, +REFB, -REFB,

APPLICATIONS INFORMATION

Table 1. LT6375 Performance at Different Resistor Divider Ratios

| RESISTOR DIVIDER OPTIONS | | | | RESISTOR DIVIDER RATIO (DIV) | DIFFERENTIAL GAIN | OUTPUT NOISE AT 1kHz (nV/√Hz) | MAXIMUM OFFSET (μV) | | MAXIMUM OFFSET DRIFT (μV/°C) | | –3dB BANDWIDTH (kHz) |
|--------------------------|--------------------|--------------------|------|------------------------------------|----------------------|-------------------------------------|------------------------|--------|---------------------------------|--------|----------------------------|
| +REFA AND –REFA | +REFB AND –REFB | +REFC AND –REFC | REF | | | | LT6375A | LT6375 | LT6375A | LT6375 | |
| 19k | 38k | 23.75k | 190k | | | | | | | | |
| OPEN | GND | OPEN | REF | 7 | 1 | 250 | 300 | 450 | 9 | 12 | 575 |
| OPEN | OPEN | GND | REF | 10 | 1 | 307 | 380 | 600 | 12 | 16 | 530 |
| GND | OPEN | OPEN | REF | 12 | 1 | 346 | 450 | 720 | 14 | 19 | 485 |
| OPEN | GND | GND | REF | 15 | 1 | 410 | 540 | 900 | 16 | 22 | 445 |
| GND | GND | OPEN | REF | 17 | 1 | 445 | 600 | 1000 | 19 | 25 | 405 |
| GND | OPEN | GND | REF | 20 | 1 | 508 | 700 | 1200 | 23 | 30 | 375 |
| GND | GND | GND | REF | 25 | 1 | 599 | 900 | 1500 | 28 | 37 | 310 |

+REFC, –REFC) result in different resistor divider ratios (DIV) and different attenuation of the LT6375's input common mode voltage.

The internal op amp of LT6375 has two operating regions: a) If the common mode voltage at the inputs of the internal op amp (V_{CMOP}) is between V^- and $V^+ - 1.75V$, the op amp operates in its normal region; b) If V_{CMOP} is between $V^+ - 1.75V$ and $V^- + 76V$, the op amp continues to operate, but in its Over-The-Top region with degraded performance (see Over-The-Top operation section of this data sheet for more detail).

Table 2 lists the valid input common mode voltage range for an LT6375 with different configurations of the reference pins when used with dual power supplies. Using the voltage ranges in this table ensures that the internal op amp is operating in its normal (and best) region. The figure entitled Common Mode Voltage Range vs Power Supply Voltage, in the Typical Performance Characteristics section of this data sheet, illustrates the information in Table 2 graphically.

Table 3 lists the valid input common mode voltage range for an LT6375 that results in the internal op amp operating in its Over-The-Top region.

The reference pins can be connected to ground (as in Tables 2 and 3) or to any reference voltage. In order to achieve the specified gain accuracy and CMRR performance of the LT6375, this reference must have a very low impedance. The valid input common mode range changes depending on the voltages chosen for reference pins. One positive and one negative reference should always be connected to a low impedance voltage to ensure the stability of the amplifier. Table 4 lists the valid input common mode voltage range for an LT6375 when the part is used with a single power supply, and REF and the other reference pins are connected to mid-supply. If, as shown in Table 5, the REF pin remains connected to mid-supply, while the other reference pins are connected to ground, the result is a higher positive input range at the expense of a more restricted negative input range.

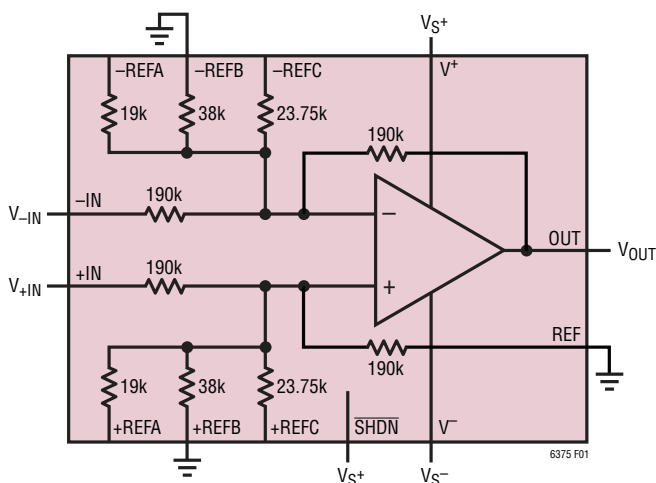


Figure 1. Basic Connections for Dual-Supply Operation (Resistor Divider Ratio = 7)

APPLICATIONS INFORMATION

Table 2. Common Mode Voltage Operating Range with Dual Power Supplies (Normal Region)

| INPUT RANGE (REF = GND) | | | | | | | | | | |
|-------------------------|-----------------------|-----------------------|-----|------------------|-------|-----------------|------|-----------------|------|--|
| +REFA AND -REFA | +REFB AND -REFB | +REFC AND -REFC | DIV | $V_S = \pm 2.5V$ | | $V_S = \pm 15V$ | | $V_S = \pm 25V$ | | |
| | | | | HIGH | LOW | HIGH | LOW | HIGH | LOW | |
| OPEN | GND | OPEN | 7 | 5.25 | -17.5 | 92.75 | -105 | 162.75 | -175 | |
| OPEN | OPEN | GND | 10 | 7.5 | -25 | 132.5 | -150 | 232.5 | -250 | |
| GND | OPEN | OPEN | 12 | 9 | -30 | 159 | -180 | 270 | -270 | |
| OPEN | GND | GND | 15 | 11.25 | -37.5 | 198.75 | -225 | 270 | -270 | |
| GND | GND | OPEN | 17 | 12.75 | -42.5 | 225.25 | -255 | 270 | -270 | |
| GND | OPEN | GND | 20 | 15 | -50 | 265 | -270 | 270 | -270 | |
| GND | GND | GND | 25 | 18.75 | -62.5 | 270 | -270 | 270 | -270 | |

Table 3. Common Mode Voltage Operating Range with Dual Power Supplies (Over-The-Top Region)

| INPUT RANGE (REF = GND) | | | | | | | | | | |
|-------------------------|-----------------------|-----------------------|-----|------------------|-------|-----------------|------|-----------------|------|--|
| +REFA AND -REFA | +REFB AND -REFB | +REFC AND -REFC | DIV | $V_S = \pm 2.5V$ | | $V_S = \pm 15V$ | | $V_S = \pm 25V$ | | |
| | | | | HIGH | LOW | HIGH | LOW | HIGH | LOW | |
| OPEN | GND | OPEN | 7 | 270 | -17.5 | 270 | -105 | 270 | -175 | |
| OPEN | OPEN | GND | 10 | 270 | -25 | 270 | -150 | 270 | -250 | |
| GND | OPEN | OPEN | 12 | 270 | -30 | 270 | -180 | 270 | -270 | |
| OPEN | GND | GND | 15 | 270 | -37.5 | 270 | -225 | 270 | -270 | |
| GND | GND | OPEN | 17 | 270 | -42.5 | 270 | -255 | 270 | -270 | |
| GND | OPEN | GND | 20 | 270 | -50 | 270 | -270 | 270 | -270 | |
| GND | GND | GND | 25 | 270 | -62.5 | 270 | -270 | 270 | -270 | |

Table 4. Common Mode Voltage Operating Range with a Single Power Supply, References to Mid-Supply (Normal Region)

| INPUT RANGE (REF = $V_S/2$) | | | | | | | | | | |
|------------------------------|-----------------------|-----------------------|-----|------------|-------|-------------|------|-------------|------|--|
| +REFA AND -REFA | +REFB AND -REFB | +REFC AND -REFC | DIV | $V_S = 5V$ | | $V_S = 30V$ | | $V_S = 50V$ | | |
| | | | | HIGH | LOW | HIGH | LOW | HIGH | LOW | |
| OPEN | $V_S/2$ | OPEN | 7 | 7.75 | -15 | 107.75 | -90 | 187.75 | -150 | |
| OPEN | OPEN | $V_S/2$ | 10 | 10 | -22.5 | 147.5 | -135 | 257.5 | -225 | |
| $V_S/2$ | OPEN | OPEN | 12 | 11.5 | -27.5 | 174 | -165 | 270 | -270 | |
| OPEN | $V_S/2$ | $V_S/2$ | 15 | 13.75 | -35 | 213.75 | -210 | 270 | -270 | |
| $V_S/2$ | $V_S/2$ | OPEN | 17 | 15.25 | -40 | 240.25 | -240 | 270 | -270 | |
| $V_S/2$ | OPEN | $V_S/2$ | 20 | 17.5 | -47.5 | 270 | -270 | 270 | -270 | |
| $V_S/2$ | $V_S/2$ | $V_S/2$ | 25 | 21.25 | -60 | 270 | -270 | 270 | -270 | |

Table 5. Common Mode Voltage Operating Range with a Single Power Supply, References to GND (Normal Region)

| INPUT RANGE (REF = $V_S/2$) | | | | | | | | | | |
|------------------------------|-----------------------|-----------------------|-----|------------|------|-------------|-----|-------------|-----|--|
| +REFA AND -REFA | +REFB AND -REFB | +REFC AND -REFC | DIV | $V_S = 5V$ | | $V_S = 30V$ | | $V_S = 50V$ | | |
| | | | | HIGH | LOW | HIGH | LOW | HIGH | LOW | |
| OPEN | GND | OPEN | 7 | 20.25 | -2.5 | 182.75 | -15 | 270 | -25 | |
| OPEN | OPEN | GND | 10 | 30 | -2.5 | 267.5 | -15 | 270 | -25 | |
| GND | OPEN | OPEN | 12 | 36.5 | -2.5 | 270 | -15 | 270 | -25 | |
| OPEN | GND | GND | 15 | 46.25 | -2.5 | 270 | -15 | 270 | -25 | |
| GND | GND | OPEN | 17 | 52.75 | -2.5 | 270 | -15 | 270 | -25 | |
| GND | OPEN | GND | 20 | 62.5 | -2.5 | 270 | -15 | 270 | -25 | |
| GND | GND | GND | 25 | 78.75 | -2.5 | 270 | -15 | 270 | -25 | |

The LT6375 will not operate correctly if the common mode voltage at its input pins goes below the range specified in above tables, but the part will not be damaged as long as the lowest common mode voltage at the inputs of the internal op amp (V_{CMOP}) remains between $V^- - 25V$ and V^- . Also, the voltage at LT6375 input pins should never be higher than 270V or lower than -270V under any circumstances.

SHUTDOWN

The LT6375 in the DFN14 package has a shutdown pin (SHDN). Under normal operation this pin should be tied to V^+ or allowed to float. Tying this pin to 2.5V below V^+ will cause the part to enter a low power state. The supply current is reduced to less than 25 μA and the op amp output becomes high impedance.

SUPPLY VOLTAGE

The positive supply pin of the LT6375 should be bypassed with a small capacitor (typically 0.1 μF) as close to the supply pin as possible. When driving heavy loads an additional 4.7 μF electrolytic capacitor should be added. When using split supplies, the same is true for the V^- supply pin.

APPLICATIONS INFORMATION

ACCURATE CURRENT MEASUREMENTS

The LT6375 can be used in high side, low side and bi-directional wide common mode range current sensing. Figure 2 shows the LT6375 sensing current by measuring the voltage across R_{SENSE} . The added sense resistors create a CMRR error and a gain error. For R_{SENSE} greater than 2Ω the source resistance mismatch degrades the CMRR. Adding a resistor equal in value to R_{SENSE} in series with the +IN terminal (R_C) eliminates this mismatch.

Using an R_{SENSE} greater than 10Ω will cause the gain error to exceed the 0.006% specification of LT6375. This is due to the loading effects of the LT6375.

$$V_{OUT} = I_{LOAD} \cdot R_{SENSE} \cdot 190k / (190k + R_{SENSE})$$

Increasing R_{SENSE} and R_C slightly to R_{SENSE}' removes the gain error.

$$R_{SENSE}' = R_{SENSE} \cdot 190k / (190k - R_{SENSE}).$$

NOISE AND FILTERING

The noise performance of the LT6375 can be optimized both by appropriate choice of its internal attenuation setting and by the addition of a filter to the amplifier output (Figure 3). For applications that do not require the full bandwidth of the LT6375, the addition of an output filter will lower system noise. Table 6 shows the output noise for different internal resistor divider ratios and output filter bandwidths.

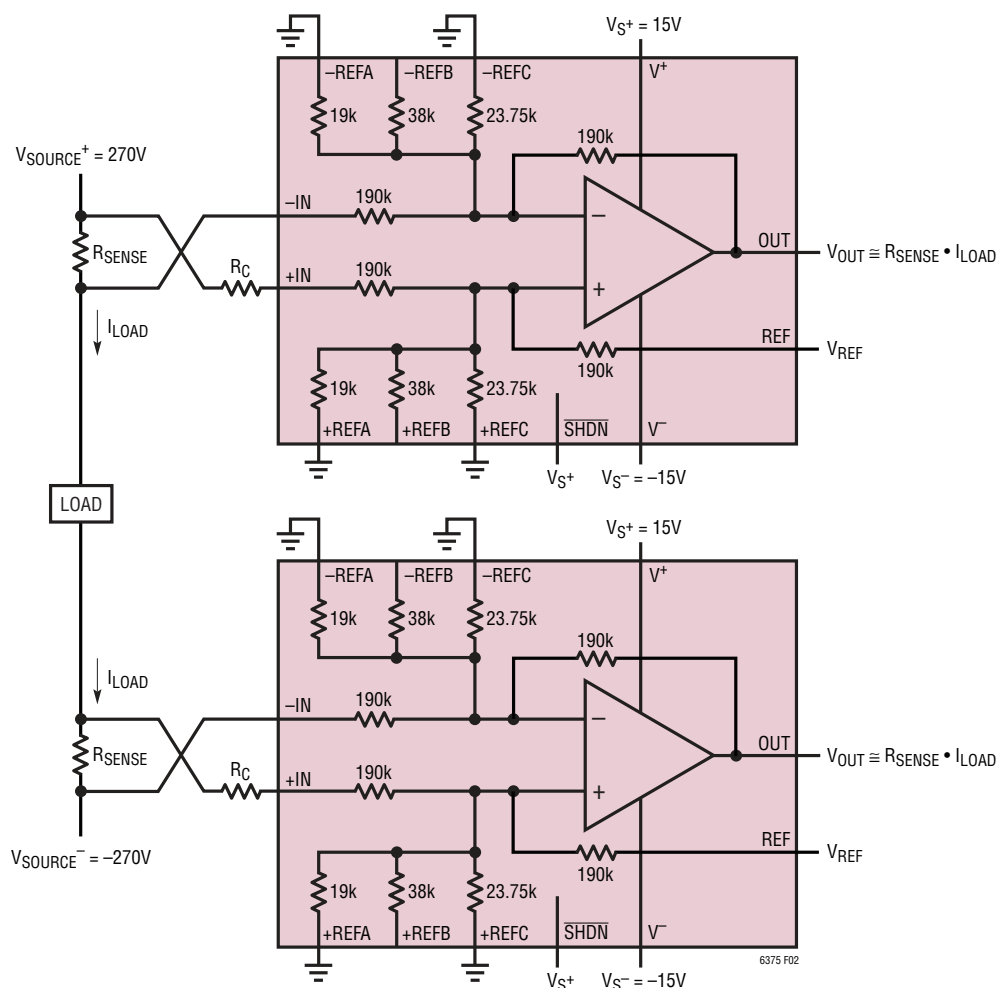


Figure 2. Wide Voltage Range Current Sensing



| Corner Frequency | 7 | 10 | 12 | 15 | 17 | 20 | 25 |
|------------------|--------|--------|--------|--------|--------|--------|--------|
| No Filter | 1705μV | 1831μV | 1901μV | 2008μV | 2073μV | 2177μV | 2330μV |
| 100kHz | 537μV | 662μV | 740μV | 853μV | 925μV | 1030μV | 1197μV |
| 10kHz | 169μV | 210μV | 236μV | 274μV | 298μV | 334μV | 393μV |
| 1kHz | 54μV | 67μV | 75μV | 87μV | 95μV | 107μV | 126μV |
| 100Hz | 18μV | 22μV | 25μV | 29μV | 32μV | 36μV | 43μV |

| Corner Frequency | R1 | R2 | C1 | C2 |
|------------------|--------------|----------------|-------------|-------------|
| 100kHz | 11k Ω | 11.3k Ω | 100pF | 200pF |
| 10kHz | 11k Ω | 11.3k Ω | 1nF | 2nF |
| 1kHz | 11k Ω | 11.3k Ω | 10nF | 20nF |
| 100Hz | 11k Ω | 11.3k Ω | 0.1 μ F | 0.2 μ F |



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ERROR BUDGET ANALYSIS

Figure 4 shows the LT6375 in a current measurement application. The error budget for this application is shown in Table 8. The resistor divider ratio is set to 15 to divide the 195V input common mode voltage down to 13V at the op amp inputs. The 1A current and 10 Ω sense resistor produce an output full-scale voltage of 10V. Table 8 shows the error sources in parts per million (ppm) of the full-scale voltage across the temperature range of 25°C to 85°C.

Different sources of error contribute to the maximum accuracy that can be achieved in an application. Gain error, offset voltage and common mode rejection error combine to set the initial error. Additionally, the gain error and offset voltage drift across the temperature range. The excellent gain accuracy, low offset voltage, high CMRR, low offset voltage drift and low gain error drift of the LT6375 all combine to enable extremely accurate measurements.

Over-The-Top OPERATION

When the input common mode voltage of the internal op amp (V_{CMOP}) in the LT6375 is biased near or above the V^+ supply, the op amp is operating in the Over-The-Top region. The op amp continues to operate with an input common mode voltage of up to 76V above V^- (regardless of the positive power supply voltage V^+), but its performance is

degraded. The op amp's input bias currents change from under ± 2 nA to 14 μ A. The op amp's input offset current rises to ± 50 nA which adds ± 9.5 mV to the output offset voltage.

In addition, when operating in the Over-The-Top region, the differential input impedance decreases from 1M Ω in normal operation to approximately 3.7k Ω in Over-The-Top operation. This resistance appears across the summing nodes of the internal op amp and boosts noise and offset while decreasing speed. Noise and offset will increase by between 66% and 83% depending on the resistor divider ratio setting. The bandwidth will be reduced by 40% to 45%. For more detail on Over-The-Top operation, consult the LT6015 data sheet.

OUTPUT

The output of the LT6375 can typically swing to within 5mV of either rail with no load and is capable of sourcing and sinking approximately 25mA. The LT6375 is internally compensated to drive at least 1nF of capacitance under any output loading conditions. For larger capacitive loads, a 0.22 μ F capacitor in series with a 150 Ω resistor between the output and ground will compensate the amplifier to drive capacitive loads greater than 1nF. Additionally, the LT6375 has more gain and phase margin as the resistor divider ratio is increased.

Table 8. Error Budget Analysis

| ERROR SOURCE | LT6375A | LT6375 | COMPETITOR 1 | COMPETITOR 2 | ERROR, ppm of FS | | | |
|---------------------------------|--------------------|--------------------|--------------------|--------------------|------------------|--------|--------------|--------------|
| | | | | | LT6375A | LT6375 | COMPETITOR 1 | COMPETITOR 2 |
| Accuracy, T _A = 25°C | | | | | | | | |
| Initial Gain Error | 0.0035% FS | 0.006% FS | 0.02% FS | 0.03% FS | 35 | 60 | 200 | 300 |
| Offset Voltage | 540μV | 900μV | 1100μV | 500μV | 54 | 90 | 110 | 50 |
| Common Mode | 195V/96dB = 3090μV | 195V/89dB = 6920μV | 195V/90dB = 6166μV | 195V/86dB = 9770μV | 309 | 692 | 617 | 977 |
| Total Accuracy Error | | | | | 398 | 842 | 927 | 1327 |
| Temperature Drift | | | | | | | | |
| Gain | 1ppm/°C ×60°C | 1ppm/°C ×60°C | 10ppm/°C ×60°C | 10ppm/°C ×60°C | 60 | 60 | 600 | 600 |
| Offset Voltage | 16μV/°C ×60°C | 22μV/°C ×60°C | 15μV/°C ×60°C | 10μV/°C ×60°C | 96 | 132 | 90 | 60 |
| Total Drift Error | | | | | 156 | 192 | 690 | 660 |
| Total Error | | | | | 554 | 1034 | 1617 | 1987 |

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DISTORTION

The LT6375 features excellent distortion performance when the internal op amp is operating within the supply rails. Operating the LT6375 with input common mode voltages that go from normal to Over-The-Top operation will significantly degrade the LT6375's linearity as the op amp must transition between two different input stages.

POWER DISSIPATION CONSIDERATIONS

Because of the ability of the LT6375 to operate on power supplies up to $\pm 25\text{V}$, to withstand very high input voltages and to drive heavy loads, there is a need to ensure the die junction temperature does not exceed 150°C . The LT6375 is housed in DF14 ($\theta_{JA} = 43^\circ\text{C/W}$, $\theta_{JC} = 4^\circ\text{C/W}$) and MS16 ($\theta_{JA} = 130^\circ\text{C/W}$) packages.

In general, the die junction temperature (T_J) can be estimated from the ambient temperature (T_A), and the device power dissipation (P_D):

$$T_J = T_A + P_D \cdot \theta_{JA}$$

Power is dissipated by the amplifier's quiescent current, by the output current driving a resistive load and by the input current driving the LT6375's internal resistor network.

$$P_D = ((V_S^+ - V_S^-) \cdot I_S) + P_{OD} + P_{RESD}$$

For a given supply voltage, the worst-case output power dissipation $P_{OD(MAX)}$ occurs with the output voltage at half of either supply voltage. $P_{OD(MAX)}$ is given by:

$$P_{OD(MAX)} = (V_S/2)^2/R_{LOAD}$$

The power dissipated in the internal resistors (P_{RESD}) depends on the input voltage, the resistor divider ratio (DIV), the output voltage and the voltage on REF and the other reference pins. The following equations and Figure 5 show different components of P_{RESD} corresponding to different groups of LT6375's internal resistors (assuming that LT6375 is used with a dual supply configuration with REF and all reference pins at ground).

$$P_{RESDA} = (V_{+IN})^2/(190k + 190k/(DIV - 1))$$

$$P_{RESDB} = (V_{-IN} - V_{+IN}/DIV)^2/(190k)$$

$$P_{RESDC} = (V_{+IN}/DIV)^2/(190k/(DIV - 2))$$

$$P_{RESDD} = (V_{+IN}/DIV - V_{OUT})^2/(190k)$$

$$P_{RESD} = P_{RESDA} + P_{RESDB} + P_{RESDC} + P_{RESDD}$$

P_{RESD} simplifies to:

$$P_{RESD} = 2(V_{+IN}^2((DIV - 1)/DIV - V_{OUT}/V_{+IN}) + V_{OUT}^2)/190k$$

In general, P_{RESD} increases with higher input voltage, higher resistor divider ratio (DIV), and lower output, REF and reference pin voltages.

Example: An LT6375 in a DFN package mounted on a PC board has a thermal resistance of 43°C/W . Operating on $\pm 25\text{V}$ supplies and driving a $2.5\text{k}\Omega$ load to 12.5V with $V_{+IN} = 270\text{V}$ and $DIV = 25$, the total power dissipation is given by:

$$\begin{aligned} P_D &= (50 \cdot 0.6\text{mA}) + 12.5^2/2.5k + 270^2/197.92k \\ &\quad + (257.5 - 270/25)^2/190k \\ &\quad + (270/25)^2/8.26k + (270/25 \\ &\quad - 12.5)^2/190k = 0.795\text{W} \end{aligned}$$

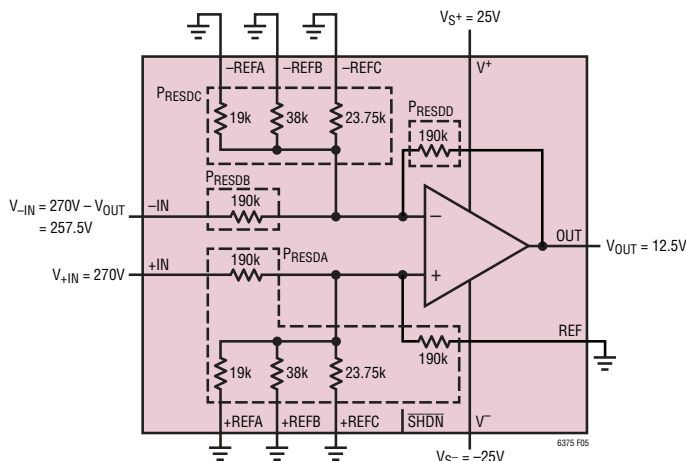


Figure 5. Power Dissipation Example

APPLICATIONS INFORMATION

Assuming a thermal resistance of 43°C/W, the die temperature will experience a 34°C rise above ambient. This implies that the maximum ambient temperature the LT6375 should operate under the above conditions is:

$$T_A = 150^\circ\text{C} - 34^\circ\text{C} = 116^\circ\text{C}$$

Keep in mind that the DFN package has an exposed pad which can be used to lower the θ_{JA} of the package. The more PCB metal connected to the exposed pad, the lower the thermal resistance.

The MSOP package has no exposed pad and a higher thermal resistance ($\theta_{JA} = 130^\circ\text{C/W}$). It should not be used in applications which have a high ambient temperature, require driving a heavy load, or require an extreme input voltage.

THERMAL SHUTDOWN

For safety, the LT6375 will enter shutdown mode when the die temperature rises to approximately 163°C. This thermal shutdown has approximately 9°C of hysteresis requiring the die temperature to cool 9°C before enabling the amplifier again.

USE AT OTHER PRECISION DC GAINS

The array of resistors within the LT6375 provides numerous configurable connections that provide precision gains other than the unity differential gain options described previously. Note that only the +IN and –IN pins can operate outside of the supply window. Since most of these alternate configurations involve driving the REFx pins, as well as the +IN and –IN pins, the input signals must be less than the supply voltages. Fully differential gains are available as shown in Table 9, and may be output-shifted with a REF offset signal. These configurations allow the LT6375 to be used as a versatile precision gain block with essentially no external components besides the supply decoupling. In most cases, only a single positive supply will be required. In Table 9, connections are identified as NC (no connect), INPUT (refers to both inputs driven, +signal to +pins, –signal to –pins), CROSS (refers to inputs cross-coupled, +signal to –pins, –signal to +pins), OUT (refers to the output fed back to –pins), or REF (refers to

connecting the REF pin to +pins). The same configurations provide inverting gains by grounding any pins intended for the +signal source. The differential input resistance is also tabulated as well as the amplification factor of the internal gain section involved (noise-gain, which helps to estimate the error-budget of the configuration).

Single-ended noninverting gains are also available as shown in Table 10, including many that operate as buffers (loaded only by the op amp input bias). A rich option set exists by using the REF pin as an additional variable. Two attenuation options exist that can accept signals outside the power supply range since they only drive the +IN pin. In Table 10, connections are identified as NC (no connect), INPUT (driven by the input), OUT (fed back from the output), or GROUND (grounded). Table 10 also includes tabulations of the internal resistor divider (DIV), noise gain (re-amplification), and the input loading presented by the circuit.

USE AS PRECISION AC GAIN BLOCK

In AC-coupled applications operating from a single power supply, it is useful to set the output voltage at mid-supply to maximize dynamic range. The LT6375 readily supports this with no additional biasing components by connecting specific pins to the V^+ and V^- potentials and AC-coupling the signal paths. Table 11 shows the available inverting gains and also tabulates the load resistances presented at the input. In Table 11, connections are identified as NC (no connect), AC IN (AC-coupled to the input) OUT (fed back from the output), tied to V^+ , tied to V^- , or AC GND (AC-grounded). All pins that require an AC ground can share a single bypass capacitor. Likewise, all pins driven from the source signal may share a coupling capacitor as well. The output should also connect to the load circuitry using a coupling capacitor to block the mid-supply DC voltage.

The LT6375 may also be used for single-supply noninverting AC gains by employing a combination of input attenuation and re-amplification. With numerous choices of attenuation and re-amplification, several hundred overall gain combinations are possible, ranging from 0.167 to 23. The combinations are more plentiful than the DC configurations because there is no constraint on matching internal source resistances to minimize offset.

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The input attenuator section dedicates some pins to establishing a mid-supply bias point and with the remaining pins, provides several choices of input signal division factors as shown in Table 12. The high attenuations that only use +IN for the signal path can accept waveform peaks that significantly exceed the supply range. Table 12 also includes tabulations of the resulting AC load resistance presented to the signal source. Here again, all pins that require an AC-ground connection may share a single bypass capacitor, and all AC signal connections may share

a coupling capacitor. Note that configurations with +IN to V+ will bias at 50% of supply, while the others shown will bias at 38% of supply.

The single-supply AC-coupled noninverting circuit is completed by configuring the post-attenuator amplification factor. Table 13 shows the available re-amplification factors. Once again, all pins that require an AC-ground connection may share a single bypass capacitor, and the output should use a coupling capacitor to its load destination as well.

Table 9. Configurations for Precision Differential Gains Other Than Unity

LT6375 DIFFERENTIAL AND INVERTING PRECISION DC GAINS

| GAIN | ±IN | ±REFA | ±REFB | ±REFC | REF | DIFF R _{IN} (k) | NOISE GAIN |
|-------|---------|-------|---------|-------|-----|--------------------------|------------|
| 0.167 | CROSS | INPUT | OUT/REF | CROSS | REF | 20 | 4.2 |
| 0.333 | NC | INPUT | OUT/REF | CROSS | REF | 21 | 4.0 |
| 0.5 | INPUT | INPUT | OUT/REF | CROSS | REF | 20 | 4.2 |
| 1.5 | OUT/REF | NC | CROSS | INPUT | REF | 29 | 7.5 |
| 2 | CROSS | NC | CROSS | INPUT | REF | 27 | 15.0 |
| 2.5 | OUT/REF | INPUT | CROSS | NC | REF | 25 | 8.5 |
| 2.833 | CROSS | INPUT | OUT/REF | INPUT | REF | 20 | 4.2 |
| 3 | NC | INPUT | OUT/REF | INPUT | REF | 21 | 4.0 |
| 3.167 | INPUT | INPUT | OUT/REF | INPUT | REF | 20 | 4.2 |
| 3.5 | OUT/REF | INPUT | INPUT | CROSS | REF | 17 | 12.5 |
| 4 | CROSS | NC | INPUT | NC | REF | 63 | 7.0 |
| 5 | NC | NC | INPUT | NC | REF | 76 | 6.0 |
| 6 | INPUT | NC | INPUT | NC | REF | 63 | 7.0 |
| 7 | CROSS | NC | NC | INPUT | REF | 42 | 10.0 |
| 8 | NC | NC | NC | INPUT | REF | 48 | 9.0 |
| 9 | INPUT | NC | NC | INPUT | REF | 42 | 10.0 |
| 10 | NC | INPUT | NC | NC | REF | 38 | 11.0 |
| 11 | INPUT | INPUT | NC | NC | REF | 35 | 12.0 |
| 12 | CROSS | NC | INPUT | INPUT | REF | 27 | 15.0 |
| 13 | NC | NC | INPUT | INPUT | REF | 29 | 14.0 |
| 14 | INPUT | NC | INPUT | INPUT | REF | 27 | 15.0 |
| 15 | NC | INPUT | INPUT | NC | REF | 25 | 16.0 |
| 16 | INPUT | INPUT | INPUT | NC | REF | 24 | 17.0 |
| 17 | CROSS | INPUT | NC | INPUT | REF | 20 | 20.0 |
| 18 | NC | INPUT | NC | INPUT | REF | 21 | 19.0 |
| 19 | INPUT | INPUT | NC | INPUT | REF | 20 | 20.0 |
| 22 | CROSS | INPUT | INPUT | INPUT | REF | 16 | 25.0 |
| 23 | NC | INPUT | INPUT | INPUT | REF | 17 | 24.0 |
| 24 | INPUT | INPUT | INPUT | INPUT | REF | 16 | 25.0 |

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Table 10. Configurations for Precision Noninverting Gains

LT6375 NONINVERTING PRECISION DC GAINS

| GAIN | FEATURE | +IN | +REFA | +REFB | +REFC | REF | –IN | –REFA | –REFB | –REFC | NOISE GAIN | DIV | R _{IN} (k) |
|-------|------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|------------|-------|---------------------|
| 0.167 | Wide Input | INPUT | GROUND | GROUND | GROUND | GROUND | GROUND | GROUND | OUT | GROUND | 4.167 | 25 | 198 |
| 0.333 | | INPUT | GROUND | GROUND | GROUND | INPUT | GROUND | GROUND | OUT | GROUND | 4.167 | 12.5 | 103 |
| 0.5 | Wide Input | INPUT | NC | NC | GROUND | GROUND | OUT | NC | NC | GROUND | 5 | 10 | 302 |
| 0.833 | | NC | GROUND | INPUT | GROUND | GROUND | NC | GROUND | OUT | GROUND | 4 | 4.8 | 48 |
| 1 | | INPUT | NC | NC | GROUND | INPUT | OUT | NC | NC | GROUND | 5 | 5 | 170 |
| 1.167 | | INPUT | GROUND | INPUT | GROUND | INPUT | GROUND | GROUND | OUT | GROUND | 4.167 | 3.571 | 38 |
| 1.333 | | GROUND | GROUND | GROUND | INPUT | NC | NC | GROUND | OUT | GROUND | 4 | 3 | 36 |
| 1.5 | | NC | GROUND | GROUND | INPUT | INPUT | NC | GROUND | OUT | GROUND | 4 | 2.667 | 34 |
| 1.667 | | NC | INPUT | GROUND | GROUND | GROUND | NC | GROUND | OUT | GROUND | 4 | 2.400 | 33 |
| 1.833 | | INPUT | INPUT | GROUND | GROUND | NC | NC | GROUND | OUT | GROUND | 4 | 2.182 | 32 |
| 2 | | INPUT | NC | GROUND | NC | INPUT | GROUND | NC | GROUND | NC | 7 | 3.500 | 37 |
| 2.167 | | GROUND | GROUND | INPUT | INPUT | NC | NC | GROUND | OUT | GROUND | 4 | 1.846 | 32 |
| 2.333 | | INPUT | GROUND | INPUT | INPUT | NC | NC | GROUND | OUT | GROUND | 4 | 1.714 | 33 |
| 2.5 | | NC | GROUND | INPUT | NC | NC | OUT | NC | GROUND | GROUND | 7.5 | 3 | 57 |
| 2.667 | | INPUT | INPUT | INPUT | GROUND | NC | NC | GROUND | OUT | GROUND | 4 | 1.500 | 36 |
| 2.833 | | INPUT | INPUT | INPUT | GROUND | INPUT | GROUND | GROUND | OUT | GROUND | 4.167 | 1.471 | 35 |
| 3 | | INPUT | NC | INPUT | GROUND | GROUND | OUT | NC | GROUND | GROUND | 7.5 | 2.500 | 53 |
| 3.167 | | INPUT | INPUT | GROUND | INPUT | NC | NC | GROUND | OUT | GROUND | 4 | 1.263 | 48 |
| 3.333 | | INPUT | INPUT | GROUND | INPUT | INPUT | GROUND | GROUND | OUT | GROUND | 4.167 | 1.250 | 47 |
| 3.5 | | INPUT | NC | INPUT | GROUND | INPUT | OUT | NC | GROUND | GROUND | 7.5 | 2.143 | 51 |
| 3.833 | | GROUND | INPUT | INPUT | INPUT | GROUND | GROUND | GROUND | OUT | GROUND | 4.167 | 1.087 | 103 |
| 4 | Buffer | INPUT | INPUT | INPUT | INPUT | NC | NC | GROUND | OUT | GROUND | 4 | 1 | Hi-Z |
| 4.167 | Buffer | INPUT | INPUT | INPUT | INPUT | INPUT | GROUND | GROUND | OUT | GROUND | 4.167 | 1 | Hi-Z |
| 4.5 | | INPUT | NC | NC | INPUT | GROUND | OUT | NC | NC | GROUND | 5 | 1.111 | 302 |
| 5 | Buffer | NC | INPUT | NC | NC | NC | OUT | NC | NC | GROUND | 5 | 1 | Hi-Z |
| 5.5 | | INPUT | INPUT | NC | NC | GROUND | OUT | GROUND | NC | NC | 6 | 1.091 | 226 |
| 6 | Buffer | INPUT | NC | INPUT | NC | NC | NC | NC | GROUND | NC | 6 | 1 | Hi-Z |
| 6.5 | | GROUND | NC | INPUT | INPUT | GROUND | OUT | NC | GROUND | GROUND | 7.5 | 1.154 | 110 |
| 7 | Buffer | INPUT | NC | INPUT | NC | INPUT | GROUND | NC | GROUND | NC | 7 | 1 | Hi-Z |
| 7.5 | Buffer | NC | INPUT | INPUT | NC | NC | OUT | NC | GROUND | GROUND | 7.5 | 1 | Hi-Z |
| 8 | | NC | NC | NC | INPUT | GROUND | NC | NC | NC | GROUND | 9 | 1.125 | 321 |
| 8.5 | Buffer | NC | NC | NC | INPUT | GROUND | OUT | GROUND | GROUND | NC | 8.5 | 1 | Hi-Z |
| 9 | Buffer | INPUT | NC | NC | INPUT | NC | NC | NC | NC | GROUND | 9 | 1 | Hi-Z |
| 9.5 | | INPUT | INPUT | NC | INPUT | GROUND | OUT | GROUND | NC | GROUND | 10 | 1.053 | 200 |
| 10 | Buffer | NC | INPUT | NC | NC | NC | GROUND | NC | NC | GROUND | 10 | 1 | Hi-Z |
| 11 | Buffer | INPUT | INPUT | NC | NC | NC | NC | GROUND | NC | NC | 11 | 1 | Hi-Z |
| 11.5 | | GROUND | INPUT | INPUT | INPUT | GROUND | OUT | GROUND | GROUND | GROUND | 12.5 | 1.087 | 103 |

APPLICATIONS INFORMATION

Table 10. Configurations for Precision Noninverting Gains

| GAIN | FEATURE | +IN | +REFA | +REFB | +REFC | REF | –IN | –REFA | –REFB | –REFC | NOISE GAIN | DIV | R _{IN} (k) |
|------|---------|-------|-------|-------|-------|--------|--------|--------|--------|--------|------------|-------|---------------------|
| 12 | Buffer | INPUT | INPUT | NC | NC | INPUT | GROUND | GROUND | NC | NC | 12 | 1 | Hi-Z |
| 12.5 | Buffer | INPUT | INPUT | INPUT | INPUT | INPUT | OUT | GROUND | GROUND | GROUND | 12.5 | 1 | Hi-Z |
| 13 | | NC | NC | INPUT | INPUT | GROUND | NC | NC | GROUND | GROUND | 14 | 1.077 | 205 |
| 14 | Buffer | INPUT | NC | INPUT | INPUT | NC | NC | NC | GROUND | GROUND | 14 | 1 | Hi-Z |
| 15 | Buffer | NC | INPUT | INPUT | NC | NC | GROUND | NC | GROUND | GROUND | 15 | 1 | Hi-Z |
| 16 | Buffer | INPUT | INPUT | INPUT | NC | NC | NC | GROUND | GROUND | NC | 16 | 1 | Hi-Z |
| 17 | Buffer | NC | NC | NC | INPUT | GROUND | GROUND | GROUND | GROUND | NC | 17 | 1 | Hi-Z |
| 18 | | NC | INPUT | NC | INPUT | GROUND | NC | GROUND | NC | GROUND | 19 | 1.056 | 201 |
| 19 | Buffer | INPUT | INPUT | NC | INPUT | NC | NC | GROUND | NC | GROUND | 19 | 1 | Hi-Z |
| 20 | Buffer | INPUT | INPUT | NC | INPUT | INPUT | GROUND | GROUND | NC | GROUND | 20 | 1 | Hi-Z |
| 23 | | NC | INPUT | INPUT | INPUT | GROUND | NC | GROUND | GROUND | GROUND | 24 | 1.043 | 198 |
| 24 | Buffer | INPUT | INPUT | INPUT | INPUT | NC | NC | GROUND | GROUND | GROUND | 24 | 1 | Hi-Z |
| 25 | Buffer | INPUT | INPUT | INPUT | INPUT | INPUT | GROUND | GROUND | GROUND | GROUND | 25 | 1 | Hi-Z |

Table 11. Configurations for Single-Supply AC-Coupled Inverting Gains

LT6375 SINGLE-SUPPLY INVERTING AC GAINS

| GAIN | –IN | –REFA | –REFB | –REFC | +IN | +REFA | +REFB | +REFC | REF | AC R _{IN} (k) |
|--------|-------|-------|-------|-------|----------------|--------|--------|--------|----------------|------------------------|
| –3 | NC | AC IN | OUT | AC IN | V ⁺ | AC GND | AC GND | AC GND | V [–] | 11 |
| –3.167 | AC IN | AC IN | OUT | AC IN | V ⁺ | AC GND | AC GND | AC GND | V [–] | 10 |
| –5 | NC | NC | AC IN | NC | V ⁺ | AC GND | AC GND | AC GND | V [–] | 38 |
| –6 | AC IN | NC | AC IN | NC | V ⁺ | AC GND | AC GND | AC GND | V [–] | 32 |
| –8 | NC | NC | NC | AC IN | V ⁺ | AC GND | AC GND | AC GND | V [–] | 24 |
| –9 | AC IN | NC | NC | AC IN | V ⁺ | AC GND | AC GND | AC GND | V [–] | 21 |
| –10 | NC | AC IN | NC | NC | V ⁺ | AC GND | AC GND | AC GND | V [–] | 19 |
| –11 | AC IN | AC IN | NC | NC | V ⁺ | AC GND | AC GND | AC GND | V [–] | 17 |
| –13 | NC | NC | AC IN | AC IN | V ⁺ | AC GND | AC GND | AC GND | V [–] | 15 |
| –14 | AC IN | NC | AC IN | AC IN | V ⁺ | AC GND | AC GND | AC GND | V [–] | 14 |
| –15 | NC | AC IN | AC IN | NC | V ⁺ | AC GND | AC GND | AC GND | V [–] | 13 |
| –16 | AC IN | AC IN | AC IN | NC | V ⁺ | AC GND | AC GND | AC GND | V [–] | 12 |
| –18 | NC | AC IN | NC | AC IN | V ⁺ | AC GND | AC GND | AC GND | V [–] | 11 |
| –19 | AC IN | AC IN | NC | AC IN | V ⁺ | AC GND | AC GND | AC GND | V [–] | 10 |
| –23 | NC | AC IN | AC IN | AC IN | V ⁺ | AC GND | AC GND | AC GND | V [–] | 8 |
| –24 | AC IN | AC IN | AC IN | AC IN | V ⁺ | AC GND | AC GND | AC GND | V [–] | 8 |

APPLICATIONS INFORMATION

Table 12. Configurations for Single-Supply AC-Coupled Input Attenuations

LT6375 SINGLE-SUPPLY AC ATTENUATOR CONFIGURATIONS

| DIV | +IN | +REFA | +REFB | +REFC | REF | AC R _{IN} (k) |
|-------|----------------|--------|----------------|----------------|----------------|------------------------|
| 1.087 | V ⁺ | AC IN | AC IN | AC IN | V ⁻ | 103 |
| 1.111 | V ⁺ | AC IN | NC | AC IN | V ⁻ | 106 |
| 1.133 | V ⁺ | AC IN | AC IN | NC | V ⁻ | 108 |
| 1.154 | V ⁺ | NC | AC IN | AC IN | V ⁻ | 110 |
| 1.2 | V ⁺ | AC IN | NC | NC | V ⁻ | 114 |
| 1.25 | V ⁺ | NC | NC | AC IN | V ⁻ | 119 |
| 1.389 | V ⁺ | AC IN | AC GND | AC IN | V ⁻ | 38 |
| 1.4 | V ⁺ | NC | AC IN | NC | V ⁻ | 133 |
| 1.7 | V ⁺ | AC IN | AC GND | NC | V ⁻ | 46 |
| 1.875 | V ⁺ | NC | AC GND | AC IN | V ⁻ | 51 |
| 1.923 | V ⁺ | AC GND | AC IN | AC IN | V ⁻ | 30 |
| 2.083 | AC IN | AC IN | V ⁺ | V ⁻ | AC IN | 30 |
| 2.182 | AC IN | AC IN | V ⁺ | V ⁻ | NC | 32 |
| 2.273 | AC IN | AC IN | V ⁺ | V ⁻ | AC GND | 31 |
| 2.3 | NC | AC IN | V ⁺ | V ⁻ | NC | 34 |
| 2.4 | NC | AC IN | V ⁺ | V ⁻ | AC GND | 33 |
| 2.5 | V ⁺ | AC IN | AC GND | AC GND | V ⁻ | 32 |
| 3.125 | V ⁺ | AC GND | AC GND | AC IN | V ⁻ | 35 |
| 3.4 | V ⁺ | AC GND | AC IN | NC | V ⁻ | 54 |
| 5 | V ⁺ | AC GND | AC IN | AC GND | V ⁻ | 47 |
| 7.5 | AC IN | NC | V ⁺ | V ⁻ | AC IN | 110 |
| 12 | AC IN | AC GND | V ⁺ | V ⁻ | AC IN | 103 |
| 14 | AC IN | NC | V ⁺ | V ⁻ | NC | 205 |
| 15 | AC IN | NC | V ⁺ | V ⁻ | AC GND | 204 |
| 24 | AC IN | AC GND | V ⁺ | V ⁻ | NC | 198 |
| 25 | AC IN | AC GND | V ⁺ | V ⁻ | AC GND | 198 |

APPLICATIONS INFORMATION

Table 13. Configurations for Single-Supply AC-Coupled Re-Amplifications

LT6375 NONINVERTING AC RE-AMPLIFICATIONS

| GAIN | –IN | –REFA | –REFB | –REFC |
|-------|--------|--------|--------|--------|
| 4 | NC | AC GND | OUT | AC GND |
| 4.167 | AC GND | AC GND | OUT | AC GND |
| 5 | OUT | NC | NC | AC GND |
| 6 | NC | NC | AC GND | NC |
| 7 | AC GND | NC | AC GND | NC |
| 7.5 | OUT | NC | AC GND | AC GND |
| 8.5 | OUT | AC GND | AC GND | NC |
| 9 | NC | NC | NC | AC GND |
| 10 | AC GND | NC | NC | AC GND |
| 11 | NC | AC GND | NC | NC |
| 12 | AC GND | AC GND | NC | NC |
| 12.5 | OUT | AC GND | AC GND | AC GND |
| 14 | NC | NC | AC GND | AC GND |
| 15 | AC GND | NC | AC GND | AC GND |
| 16 | NC | AC GND | AC GND | NC |
| 17 | AC GND | AC GND | AC GND | NC |
| 19 | NC | AC GND | NC | AC GND |
| 20 | AC GND | AC GND | NC | AC GND |
| 24 | NC | AC GND | AC GND | AC GND |
| 25 | AC GND | AC GND | AC GND | AC GND |

The circuit diagram shows the 6375 TA03 precision centesimal divider. It features a 3.3V supply (V_S) and a 50V supply. The input voltage V_{IN} is connected to the $-IN$ pin through a $2.2\mu F$ capacitor. The output voltage V_{OUT} is connected to the OUT pin through a $2.2\mu F$ capacitor. The circuit includes several resistors: $19k\Omega$, $38k\Omega$, $23.75k\Omega$, $190k\Omega$, and $19k\Omega$. The output voltage is given by the equation $\frac{V_{OUT}}{V_{IN}} = -24$. The circuit is labeled 6375 TA03.

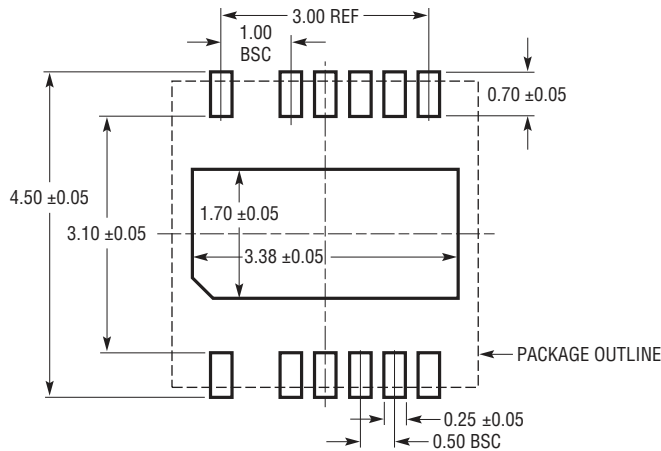
The diagram shows the AD637 3-terminal multiplier/divider circuit. The device is represented by a pink rectangular block with various pins and internal resistors. The supply voltages are V_{S+} and V_{S-} . The input voltages are V_{IN+} and V_{IN-} . The output voltage is V_{OUT} . The reference voltage is V_{REF} . The shutdown pin is $SHDN$. The internal resistors are labeled: $-REFA$ (19k), $-REFB$ (38k), $-REFC$ (23.75k), $-IN$ (190k), $+IN$ (190k), $+REFA$ (19k), $+REFB$ (38k), $+REFC$ (23.75k), and a 190k resistor between the inverting input and the output. The non-inverting input is connected to V_{S-} through a 190k resistor. The output is connected to a load through a resistor R_S (32.4Ω). The reference pin (REF) is connected to the output through R_S . The input voltages are V_{IN+} and V_{IN-} . The shutdown pin (SHDN) is connected to V_{S-} . The reference pin (REF) is connected to the output through R_S . The output current is I_{OUT} .

$$I_{OUT} = \frac{V_{CTL}}{6 \cdot R_S} - \frac{V_{OUT}}{41.6k}$$

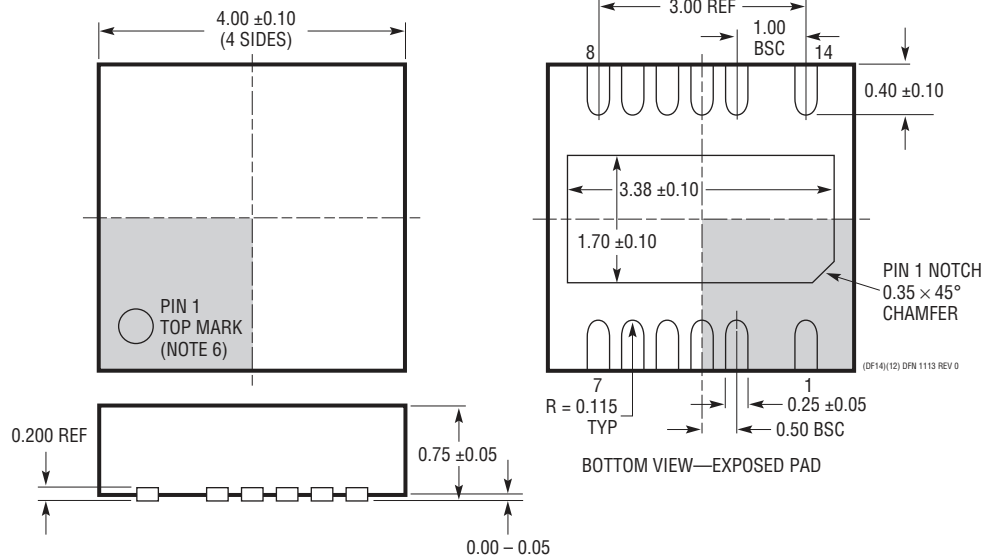
PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LT6375#packaging> for the most recent package drawings.

DF Package
14(12)-Lead Plastic DFN (4mm × 4mm)
 (Reference LTC DWG # 05-08-1963 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



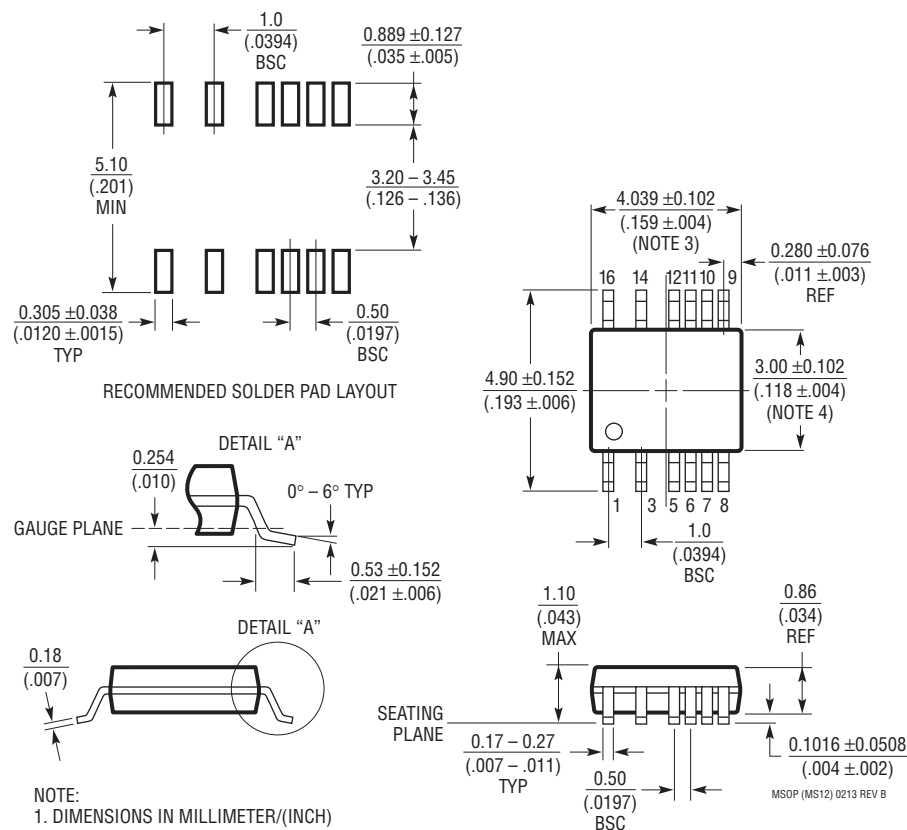
NOTE:

1. PACKAGE OUTLINE DOES NOT CONFORM TO JEDEC MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LT6375#packaging> for the most recent package drawings.

MS Package 16 (12)-Lead Plastic MSOP with 4 Pins Removed (Reference LTC DWG # 05-08-1847 Rev B)



NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm ($.006$) PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm ($.006$) PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm ($.004$) MAX

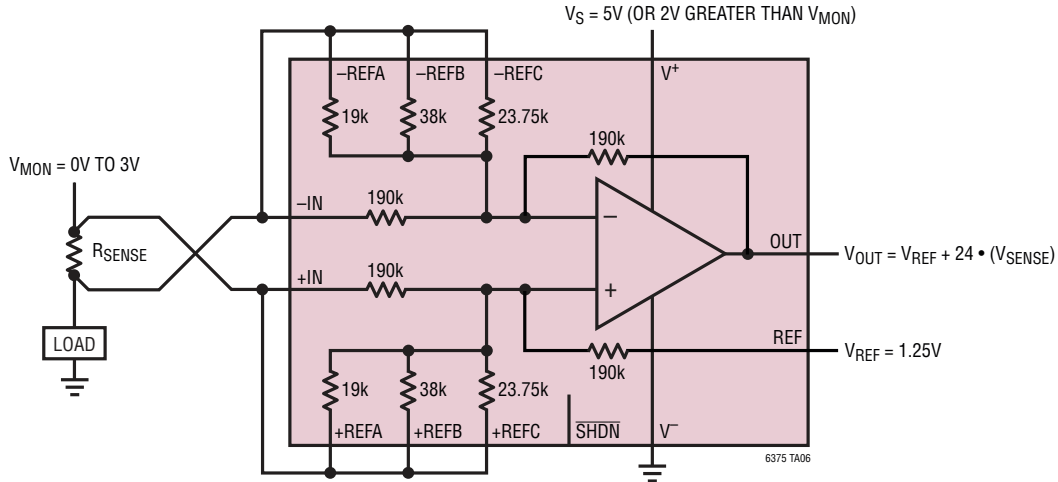
MSOP (MS12) 0213 REV B

REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|-----|-------|----------------|-------------|
| A | 12/15 | Added A-grade. | 1-7, 15, 19 |

TYPICAL APPLICATION

Bidirectional Full Range Current Monitor



RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|----------------------|---|--|
| LT1990 | ±250V Input Range Difference Amplifier | 2.7V to 36V Operation, CMRR > 70dB, Input Voltage = ±250V |
| LT1991 | Precision, 100µA Gain Selectable Amplifier | 2.7V to 36V Operation, 50µV Offset, CMRR > 75B, Input Voltage = ±60V |
| LT1996 | Precision, 100µA Gain Selectable Amplifier | Micropower, Pin Selectable Up to Gain = 118 |
| LT1999 | High Voltage, Bidirectional Current Sense Amplifier | –5V to 80V, 750 µV, CMRR 80dB 100kHz Gain: 10V/V, 20V/V, 50V/V |
| LT6015/LT6016/LT6017 | Single, Dual, and Quad, Over-The-Top Precision Op Amp | 3.2MHz, 0.8V/µs, 50µV V _{OS} , 3V to 50V V _S , 0.335mA I _S , RRIO |
| LTC6090 | 140V Operational Amplifier | 50pA I _B , 1.6mV V _{OS} , 9.5V to 140V V _S , 4.5mA I _S , RR Output |
| LT6108 | High Side Current Sense Amplifier with Reference and Comparator with Shutdown | 2.7V to 60V, 125µV, Resistor Set Gain, ±1.25% Threshold Error |
| LT1787/LT1787HV | Precision, Bidirectional High Side Current Sense Amplifier | 2.7V to 60V Operation, 75µV Offset, 60µA Current Draw |
| LTC6101/LTC6101HV | High Voltage High Side Current Sense Amplifier | 4V to 60V/5V to 100V Operation, External Resistor Set Gain, SOT23 |
| LTC6102/LTC6102HV | Zero Drift High Side Current Sense Amplifier | 4V to 60V/5V to 100V Operation, ±10µV Offset, 1µs Step Response, MSOP8/DFN Packages |
| LTC6104 | Bidirectional, High Side Current Sense | 4V to 60V, Gain Configurable, 8-Pin MSOP Package |