



MX575ABA100M000

Ultra-low Jitter 100MHz LVPECL XO

ClockWorks™ FUSION

General Description

The MX575ABA100M000 is an ultra-low phase jitter XO with LVPECL output optimized for high line rate applications.

Applications

- PCI-Express
- Storage

Absolute Maximum Ratings

Supply Voltage (VIN).....	+3.6V
Lead Temperature (soldering, 10s).....	260°C
Storage Temperature (T _s).....	125°C
ESD Rating (HBM).....	2kV

Electrical Characteristics

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 50 Ohms to VDD - 2.¹

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				120	mA
F0	Center Frequency			100		MHz
	Frequency Stability	Note 2			±50	ppm
∅j	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		220 100		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		300			ps
	Duty Cycle		45		55	%
VOH	Output High Voltage	LVPECL output levels	VDD - 1.35	VDD - 1.01	VDD - 0.8	V
VOL	Output Low Voltage	LVPECL output levels	VDD - 2.0	VDD - 1.78	VDD - 1.6	V
Vswing	Peak to Peak Output Voltage Swing		0.65	0.77	0.95	V

Notes:

1. Guaranteed after thermal equilibrium.
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration from -40°C to +85°C.

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Revision 1.0
tcghelp@micrel.com or (408) 955-1690

Features

- 100MHz LVPECL
- Typical phase noise:
-100fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 7mm x 5mm LGA package

Operating Ratings

Supply Voltage (VIN).....	+2.375V to +3.63V
Ambient Temperature (TA).....	-40°C to +85°C

Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX575ABA100M000	MX575AB	A100M000	Tube	6-Pin 7mm x 5mm LGA
MX575ABA100M000 TR	MX575AB	A100M000	Tape and Reel	6-Pin 7mm x 5mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

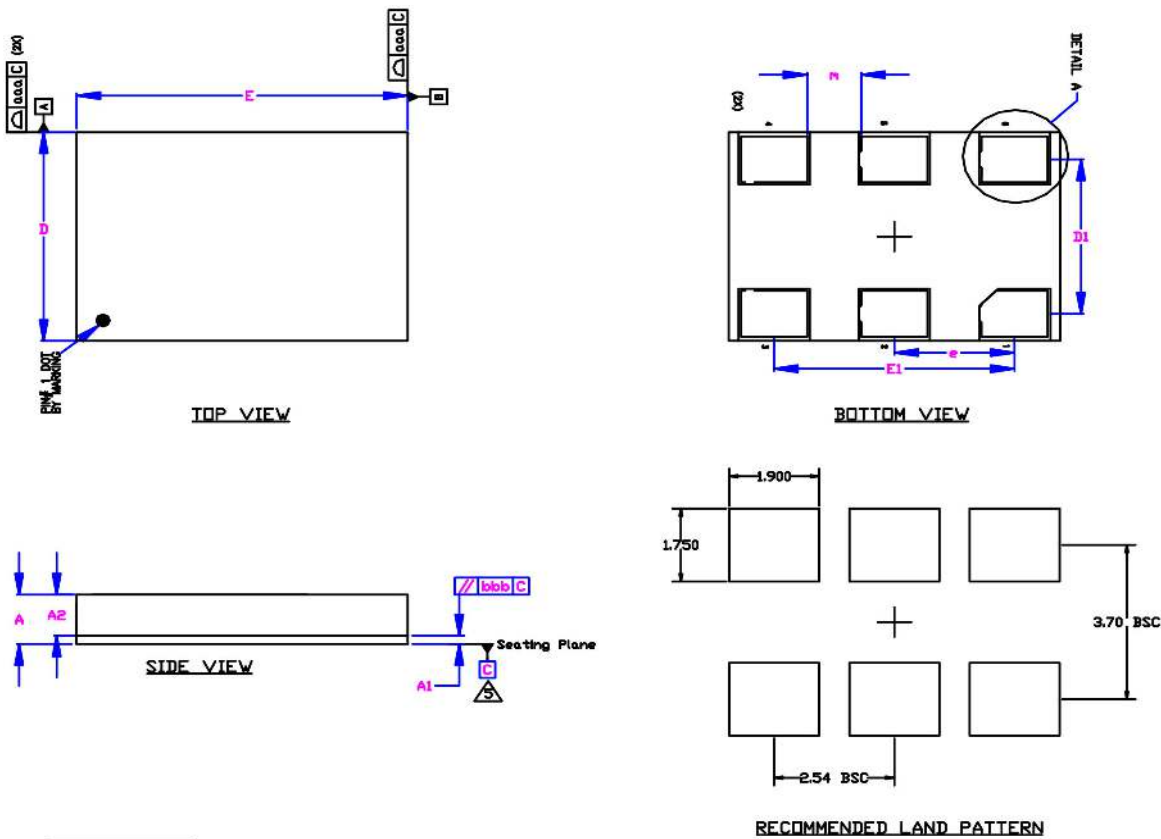
Pin Configuration



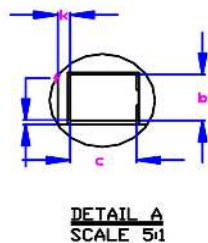
Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	LVPECL	Clock Output Frequency = 100MHz
6	VDD	PWR		Power Supply

Package Information and Recommended Land Pattern for 6-Pin LGA³



Dimensional Tol.			
aaa			0.10
bbb			0.17
Dimensional Ref.			
REF.	Min.	Nom	Max.
A	1.26	1.33	1.40
A1	0.19	0.23	0.27
A2	1.070	1.100	1.130
D	4.9	5.0	5.1
D1	3.7 BSC		
E	6.9	7.0	7.1
E1	5.0 BSC		
b	1.05	1.10	1.15
c	1.35	1.40	1.45
e	2.54 BSC		
f	0.15	0.18	0.21
k	0.21	0.26	0.31
m	1.19	1.14	1.19
n	36		



- Notes
1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
 2. Dimensions are in millimeters.
 3. 'e' represents the basic LGA pitch
 4. 'n' is the maximum no. of Land for a specified Package.
 5. Package warp shall be 0.051 max.
 6. Substrate base is BT Resin
 7. The Pin#1 corner must be identified on top side only.
 8. Reference Jeduc Spec M1-221
 9. Land pattern tolerance is 0.15mm unless otherwise specified

6-Pin LGA (7x5mm)

Note:

3. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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