



Automotive Dual P-Channel 30 V (D-S) 175 °C MOSFET

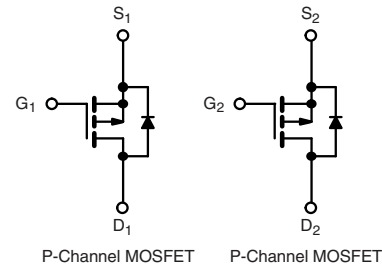
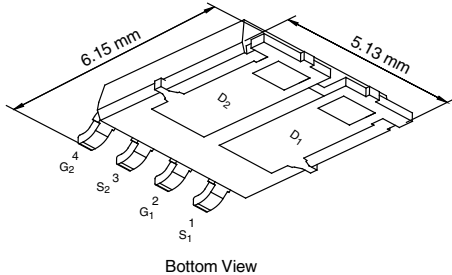
PRODUCT SUMMARY	
V _{DS} (V)	- 30
R _{DS(on)} (Ω) at V _{GS} = - 10 V	0.024
R _{DS(on)} (Ω) at V _{GS} = - 4.5 V	0.039
I _D (A) per leg	- 8
Configuration	Dual

FEATURES

- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- AEC-Q101 Qualified^d
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



PowerPAK® SO-8L Dual



ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ941EP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V _{DS}	- 30	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current ^a	T _C = 25 °C	- 8	A	
	T _C = 125 °C	- 8		
Continuous Source Current (Diode Conduction) ^a	I _S	- 8		
Pulsed Drain Current ^b	I _{DM}	- 32		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	- 24	
Single Pulse Avalanche Energy		E _{AS}	28.8	mJ
Maximum Power Dissipation ^b	T _C = 25 °C	P _D	55	W
	T _C = 125 °C		18.5	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature) ^{e, f}		260		

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount ^c	R _{thJA}	85
Junction-to-Case (Drain)		R _{thJC}	2.7

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = - 250 μA	- 30	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1.5	- 2.0	- 2.5	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = - 30 V	-	-	- 1	μA
		V _{GS} = 0 V, V _{DS} = - 30 V, T _J = 125 °C	-	-	- 50	
		V _{GS} = 0 V, V _{DS} = - 30 V, T _J = 175 °C	-	-	- 150	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = - 10 V, V _{DS} = - 5 V	- 24	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 9 A	-	0.020	0.024	Ω
		V _{GS} = - 10 V, I _D = - 9 A, T _J = 125 °C	-	0.028	0.034	
		V _{GS} = - 10 V, I _D = - 9 A, T _J = 175 °C	-	0.032	0.039	
		V _{GS} = - 4.5 V, I _D = - 5 A	-	0.032	0.039	
Forward Transconductance ^b	g _{fs}	V _{DS} = - 15 V, I _D = - 2.5 A	-	10	-	S
Dynamic^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 10 V, f = 1 MHz	-	1500	1800	pF
Output Capacitance	C _{oss}		-	370	445	
Reverse Transfer Capacitance	C _{rss}		-	260	315	
Total Gate Charge ^c	Q _g	V _{GS} = - 10 V, V _{DS} = - 15 V, I _D = - 9 A	-	35	55	nC
Gate-Source Charge ^c	Q _{gs}		-	4.6	-	
Gate-Drain Charge ^c	Q _{gd}		-	8.1	-	
Gate Resistance	R _g	f = 1 MHz	2.8	5.95	9.5	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = - 15 V, R _L = 1.66 Ω I _D ≅ - 9 A, V _{GEN} = - 10 V, R _g = 6 Ω	-	49	60	ns
Rise Time ^c	t _r		-	35	50	
Turn-Off Delay Time ^c	t _{d(off)}		-	47	60	
Fall Time ^c	t _f		-	26	33	
Source-Drain Diode Ratings and Characteristics^b						
Pulsed Current ^a	I _{SM}		-	-	- 32	A
Forward Voltage	V _{SD}	I _F = - 2.5 A, V _{GS} = 0	-	- 0.8	- 1.2	V

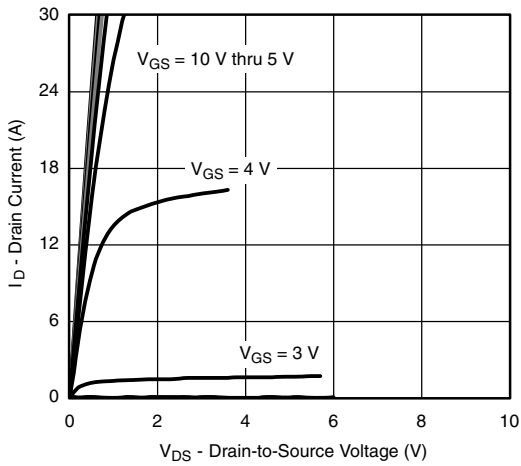
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
 b. Guaranteed by design, not subject to production testing.
 c. Independent of operating temperature.

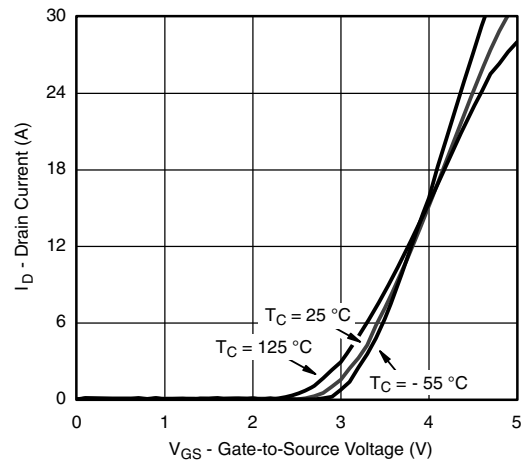
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



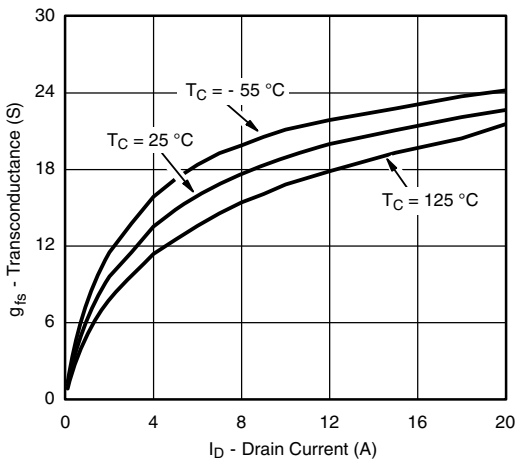
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



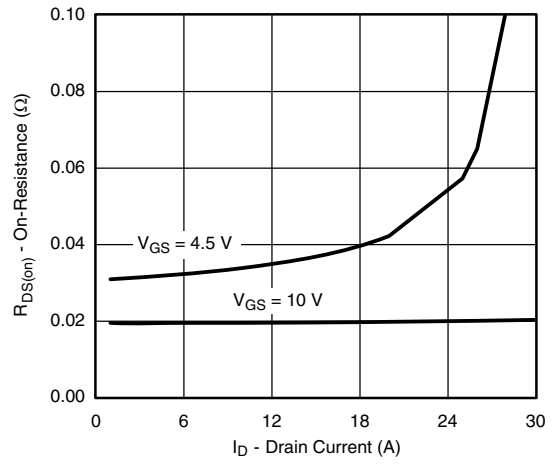
Output Characteristics



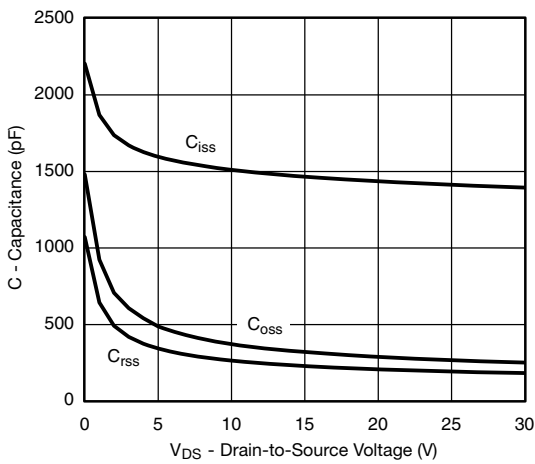
Transfer Characteristics



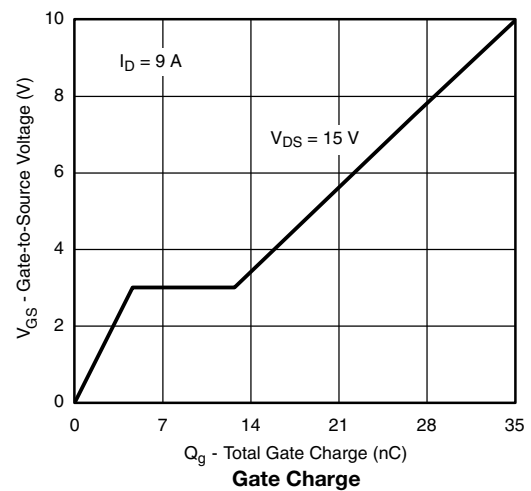
Transconductance



On-Resistance vs. Drain Current



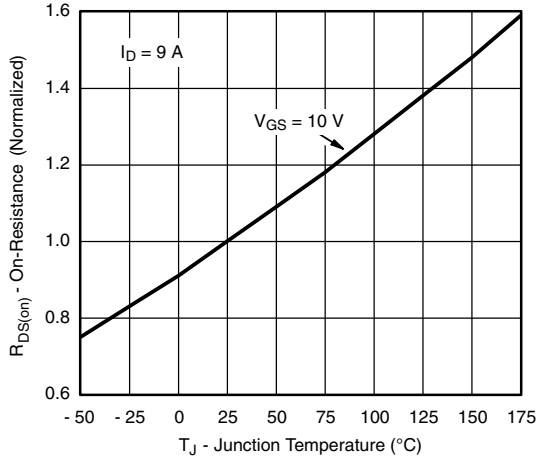
Capacitance



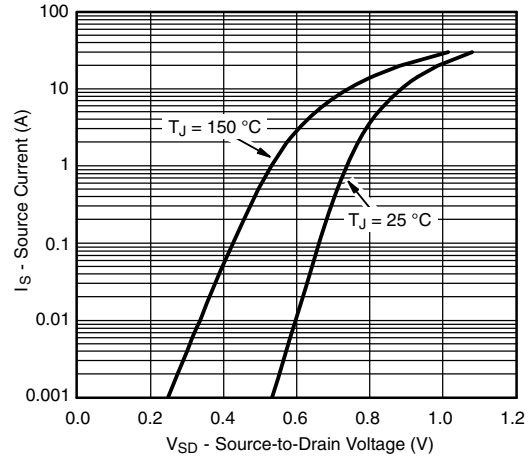
Gate Charge



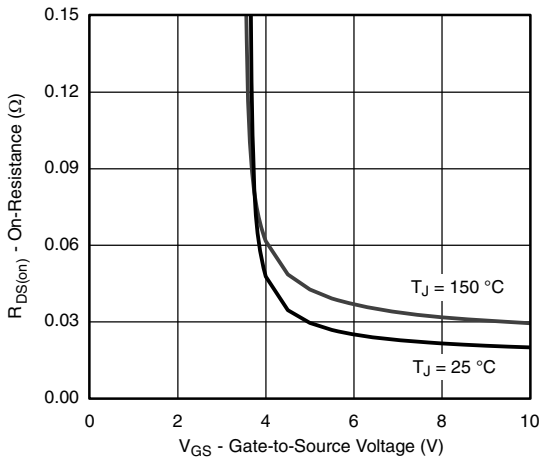
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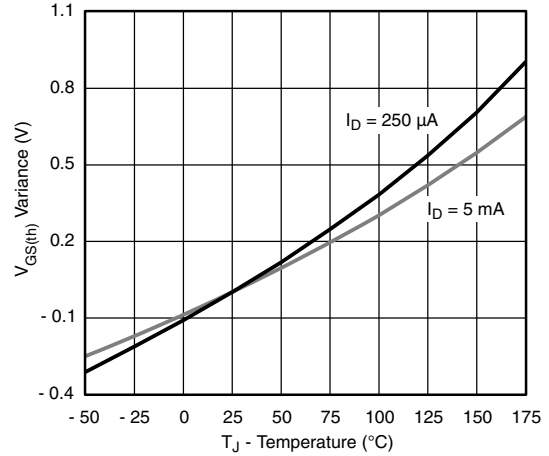
On-Resistance vs. Junction Temperature



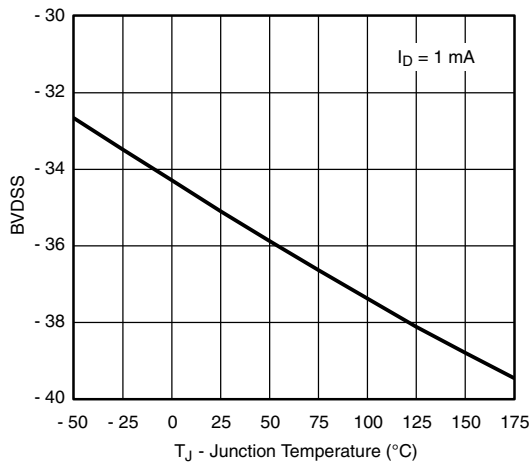
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



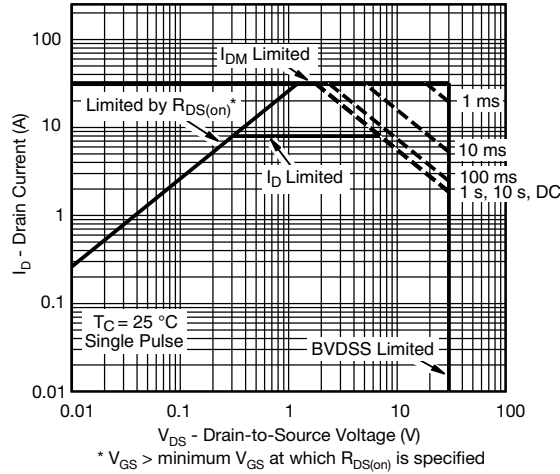
Threshold Voltage



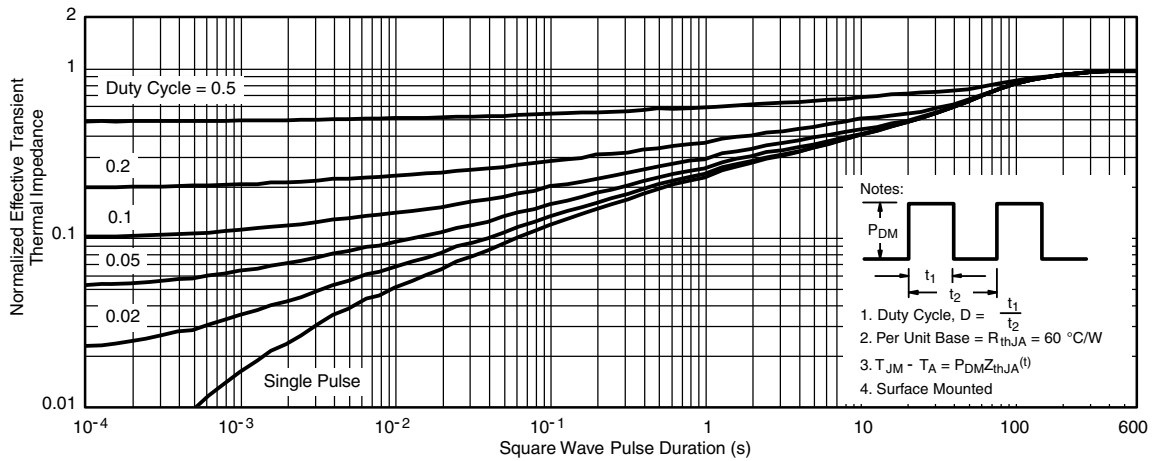
BVDSS vs. Junction Temperature



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



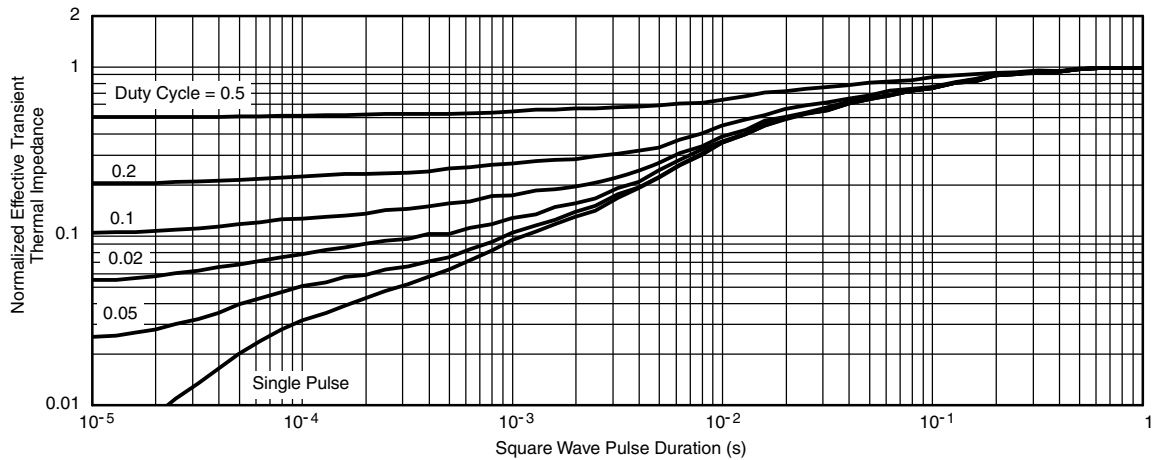
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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