LX1675

Multiple Output LoadSHARE™ PWM

PRODUCTION DATA SHEET

DESCRIPTION

The LX1675 is a highly integrated power supply controller IC featuring three voltage mode PWM switching regulator stages with an additional onboard linear regulator driver.

Two of the constant frequency PWM phases can be easily configured for a single Bi-Phase high current output or operated as two independently regulated outputs. All outputs (PWM phases and LDO) have separate, programmable soft-start sequencing. This versatility yields either three or four independently regulated outputs with full power sequencing capability giving system designers the ultimate flexibility in power supply design.

Current limit for each PWM regulator is provided by monitoring the voltage drop across the lower MOSFET power stage during conduction, utilizing the Rds(on) impedance. This eliminates the need for expensive current sense resistors. Once current limit has been reached and persist for 4 clock cycles, the output is shut off and Soft Start is initialized to force a hiccup mode for protection.

High current MOSFETs can be directly driven to provide an LDO output of 5A and 15A for each PWM controller. This is useful for I/O, memory, termination, and other supplies surrounding today's micro-processor based designs.

The LX1675 accepts a wide range of supply voltage ranging from 4.5V to 24V. Each PWM regulator output voltage is programmed via a simple voltage-divider network. The LX1675 design gives engineers maximum flexibility with respect to the MOSFET supply. Each phase can utilize different supply voltages for efficient use of available supply rails.

Additionally, when two phases are configured in Bi-Phase output, the LoadSHARE™ topology can be programmed via inductor ESR selection. The split phase operation reduces power loss, noise due to the ESR of the input capacitors and allows for reduction in capacitance values while maximizing regulator response time. The internal reference voltage is buffered and brought out on a separate pin to be used as an external reference voltage.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: http://www.microsemi.com

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Protected by U.S. Patents 6,285,571 and 6,292,378

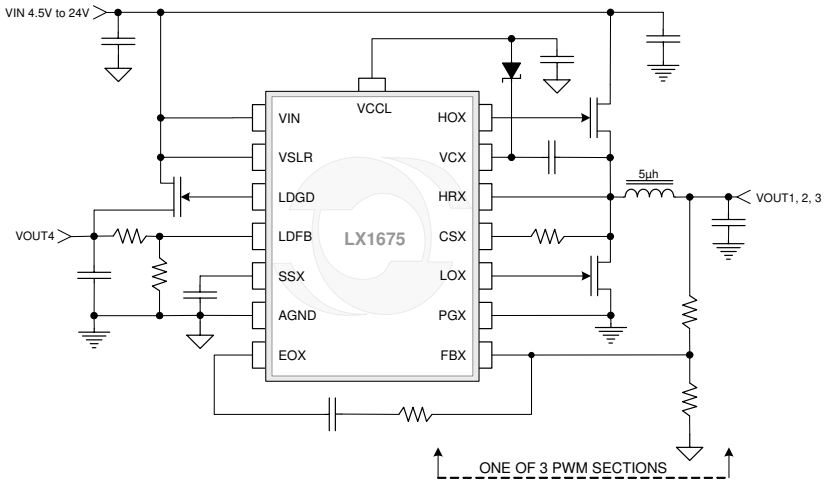
KEY FEATURES

- Four Independently Regulated Outputs
- Single Input Supply with Wide Voltage Range: 4.5-24V
- Outputs As Low As 0.8V Generated From a Precision Internal Reference
- Selectable PWM Frequency of 300KHz or 600KHz
- Buffered Reference Voltage Output
- Multiphase Output Reduces Need for Large Input Capacitance at High Currents
- Integrated High Current MOSFET Drivers
- Independent Soft-Start and Power Sequencing
- Adjustable Linear Regulator Driver Output
- No Current-Sense Resistors
- DDR Termination Compliant
- RoHS Compliant for Pb Free

APPLICATIONS

- Multi-Output Power Supplies
- Video Card Power Supplies
- PC Peripherals
- Portable PC Processor and I/O Supply

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_A (°C)	LQ Plastic MLPQ 38-Pin RoHS Compliant / Pb-free
0 to 85	LX1675CLQ
-40 to 85	LX1675ILQ

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1675CLQ-TR)

Rev. 1.2a, 2006-02-16

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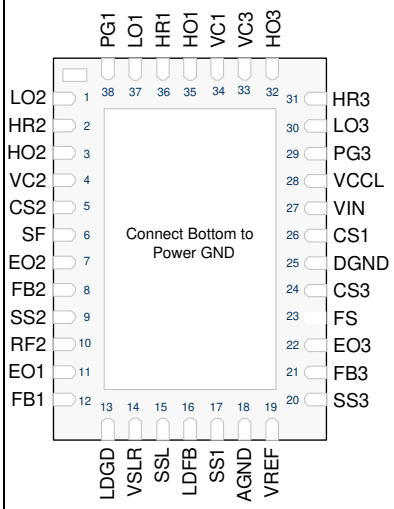
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VIN, VSLR, HRX) ..... -0.3V to 24V
Supply Voltage (VCCL) ..... -0.3V to 6.0V
Driver Supply Voltage (VCX) ..... -0.3V to 30V
Current Sense Inputs (CSX) ..... -0.3V to 30V
Error Amplifier Inputs (FB_X, RF2, LDFB) ..... -0.3V to 5.5V
Internal regulator Current (I_{VCCL}) 50mA
Output Drive Peak Current Source (HO_X, LO_X) 1A (200ns)
Output Drive Peak Current Sink (HO_X, LO_X) 1.5A (200ns)
Differential Voltage: $V_{HOX} - V_{HRX}$ (High Side Return) ..... -0.3V to 6V
Soft Start Input (SSX, SSL) ..... -0.3V to V_{REF}
Logic Inputs (SF, FS) ..... -0.3V to V_{CCL} + 0.5V
LDO Gate Drive (LDGD) Output Drive can source 10mA
LDO Feedback (LDFB) Input 6.0V
Operating Junction Temperature ..... 150°C
Operating Temperature Range ..... -40°C to 85°C
Storage Temperature Range ..... -65°C to 150°C
Peak Package Solder Reflow Temp. (40 seconds maximum exposure) ..... 260°C (+0 -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.
Limitations affecting transient pulse duration is thermally related to the clamping zener diodes connected to the supply pins, application of maximum voltage will increase current into that pin and increase power dissipation.
x denotes respective pin designator 1, 2, or 3.

PACKAGE PIN OUT



LQ PACKAGE
(Top View)

RoHS / Pb-free 100% Matte Tin Lead Finish

THERMAL DATA

LQ **Plastic MLPQ 38-Pin**

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	30 to 55°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are dependent on heat spreading and layout considerations for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

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FUNCTIONAL PIN DESCRIPTION

Name	Description
FB1	Bi-Phase Operation: Phase 1 and 2 Voltage Feedback Single Phase Operation: Phase 1 Voltage Feedback, connect to the output through a resistor network to set desired output voltage of Phase 1.
FB2	Bi-Phase Operation: Load Sharing Voltage Sense Feedback – Connect filtered phase 2 switching output (pre-inductor) to FB2 to ensure proper current sharing between phase 1 and phase 2. Single Phase Operation: Phase 2 Voltage Feedback, connect to the output through a resistor network to set desired output voltage of Phase 2.
FB3	Phase 3 Voltage Feedback , connect to the output through a resistor network to set desired output voltage of Phase 3.
RF2	Bi-Phase Operation: Load Sharing Voltage Sense Feedback Reference – Sets reference for current sharing control loop. Connecting filtered phase 1 switching output (pre-inductor) to RF2 forces the average current in phase 2 to be equal to phase 1. Single Phase Operation: Phase 2 Voltage Reference – connected to SS2 pin as the reference.
EOX	Error Amplifier Output – Sets external compensation for the corresponding phase denoted by “X”.
VIN	Controller supply voltage.
VCCL	For 4.5V < VIN < 6V, this pin becomes the input voltage supply for the controller’s internal logic and gate drivers. For VIN > 6V this pin is an output of the internal 5V regulator that supplies internal logic, Low Side Gate drivers and High Side charge pump capacitor charging, if used. User must provide low ESR decoupling capacitor for pulse load currents
AGND	Analog ground reference.
DGND	Digital/Switching ground reference for current paths of the PWM driver circuits.
VSLR	Supply pin for LDO regulator section.
LDFB	Low Dropout Regulator Voltage Feedback – Sets the output voltage of external MOSFET via resistor network.
LDGD	Low Dropout Regulator Gate Drive – Connects to gate of external N-MOSFET for linear regulator supply.
SSL	LDO Enable and Soft-start/Hiccup Capacitor Pin - During start-up, the voltage on this pin ramps from 0V to VREF controlling the output voltage of the regulator. An internal 20kΩ resistor connected to VREF and the external capacitor set the time constant for soft-start function. The Soft-start function does not initialize until the supply voltage exceeds the UVLO threshold.
SF	Shared Fault - If SF input = Logic 1(VCCL) and current limit threshold is reached during 4 clock cycles all outputs are shutdown by discharging SS caps to zero and the start-up sequence begins again, this becomes hiccup mode protection with the duty cycle set by the size of the SS capacitor. When operated in Bi-phase mode, SF must be set High. If SF = logic 0, the other outputs continue to function normally and the faulted output enters the hiccup mode for current limit.
FS	Frequency Select Logic Input - Connect to ground for 300KHz and VCCL for 600KHz operation. Input has 100KΩ Pull down resistor.
VREF	Buffered version of the internal 0.8 voltage reference.
CSX	Over-Current Limit Set – Connecting a resistor between CSX pin and the drain of the low-side MOSFET sets the current-limit threshold for the corresponding phase denoted by “X”. A minimum of 500Ω must be in series with this input. Whenever the current limit threshold is reached for 4 consecutive clock cycles the soft start capacitor is discharged through an internal resistor initiating Soft Start and Hiccup mode.
SSX	Enable & Soft-start/Hiccup Capacitor Pin – During start-up, the voltage on this pin controls the output voltage of its respective regulator. An internal 20kΩ resistor and the external capacitor set the time constant for soft-start function. The Soft-start function does not initialize until the supply voltage exceeds the UVLO threshold. When an over-current condition occurs, this capacitor is used for the timing of hiccup mode protection. Pulling the SS pin below 0.1V disables the corresponding phase denoted by “X”.
VCX	PWM High-Side MOSFET Gate Driver Supply – Connect to separate supply or to boot strap supply to ensure proper high-side gate driver supply voltage. “X” denotes corresponding phase. If the phase is not used connect to VCC.
HOX	High Side MOSFET Gate Driver – “X” denotes corresponding phase.
LOX	Low Side MOSFET Gate Driver – “X” denotes corresponding phase.
PGX	Low-side Driver Power Ground. Connects to the source of the bottom N-channel MOSFETS of each phase, where X denotes corresponding phase. PG1 is the shared ground of PWM 1 and PWM 2 Low-side drivers.
HRX	High Side driver return, connect this pin to High Side MOSFET source. “X” denotes corresponding phase.

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ELECTRICAL CHARACTERISTICS

For the LX1675ILQ the following specifications apply over the ambient temperature -40°C ≤ TA ≤ 85°C and for the LX1675CLQ 0°C ≤ T_A ≤ 85°C except where otherwise noted and the following test conditions: V_{IN} & VSLR = 12V, V_{CX} = 17V, HOX and LOX =3000pF Load, FS = 0 (f = 300KHz).

Parameter	Symbol	Test Conditions	LX1675 Min	LX1675 Typ	LX1675 Max	Units
SWITCHING REGULATORS						
Input Voltage	VIN	Regulator Functional	4.5		24	V
	VCX				30	
	VCCL				6	
Operation Current	I_{VIN}	Static		6		mA
Feedback Voltage Internal Reference	V_{FB}	4.5V < VIN < 12V	0.784		0.816	V
Line Regulation			-1		1	%
Load Regulation		System Level measurement, Closed Loop	-1		1	%
High Side Minimum Pulse Width		Load = 3000pF		50		nS
Maximum Duty Cycle	PWM_{DC}	600kHz	74			%
			85			%
Lox Minimum On Time	VLOx	@ 25°C from 3V going high to 1V going low	180	225	320	nS
Buffered Reference Voltage	V_{REF}	Max Load Current 0.5mA	0.778		0.822	V
ERROR AMPLIFIER						
Input Offset Voltage	V_{OS}	Common Mode Input Voltage = 1V	-7.0		7.0	mV
DC Open Loop Gain				70		dB
Unity gain bandwidth	AV_{UGBW}			10		MHz
High Output Voltage	V_{OH}	I Source = 2mA	3.75	5.0		V
Low Output Voltage	V_{OL}	I Sink = 100µA			100	mV
Input Common Mode Range		Input Offset Voltage ≤ 20mV	0.1		3.5	V
Input Bias Current	I_{IN}	0V and 3.5V Common Mode Voltage		100		nA
CURRENT SENSE						
CS Bias Current (Source)	I_{SET}	V_{CSX} = -0.2V, V_{PGX} = 0V @ 25°C	48	55	62	µA
CS Trip Threshold	V_{TRIP}	Referenced to V_{CSX}, V_{PGX} = 0V		±3		mV
CS Delay (Blanking)	T_{CSD}			150		nS
Shared Fault Mode	V_{IH}	Any PWM Output Activating Current Limit for More than 4 Clock Cycles, Soft Starts all PWM Outputs			2	V
	V_{IL}	Current Limit Event of One PWM Does Not Effect the Continued Function of the Two Other PWM Regulators	0.8			
OUTPUT DRIVERS – N Channel MOSFETS						
Low Side Driver Operating Current	I_{VCCL}	Static		2.5		mA
High Side Driver Operating Current	I_{VCX}	Static		3		mA
Drive Rise and Fall Time	$T_{R/F}$	C_L = 3000pF		50		nS
Dead Time – High Side to Low Side or Low Side to High Side	T_{DEAD}	Drive Load = 3000pF, V_{DRIVE} < 1V		50		nS
High Side Driver Voltage						
Drive High	V_{HOx}	I_{HOx} = 20mA, VCx – HRx = 5.0V	4.8	4.9		V
Drive Low		I_{HOx} = -20mA, VCx – HRx = 5.0V		0.1	0.2	
Low Side Driver Voltage						
Drive High	V_{LOx}	I_{LOx} = 20mA, VCCL – PGx = 5.0V	4.8	4.9		V
Drive Low		I_{LOx} = -20mA, VCCL – PGx = 5.0V		0.1	0.2	
High Side Driver Current	I_{HOx}	VCx – HRx = 5.0V, Capacitive Load, PW < 200ns		±1		A_{PEAK}
Low Side Driver Current	I_{LOx}	VCCL – PGx = 5.0V, Capacitive Load, PW < 200ns		±1.5		A_{PEAK}
Maximum Load	Qg_{MAX}			50		nC
OSCILLATOR						
PWM Switching Frequency	F_{SW}	V_{FS} <0.8V @ 25°C	255	300	345	KHz
		V_{FS} >2V @ 25°C	510	600	690	KHz
Ramp Amplitude	VRAMP			1.6		VPP

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ELECTRICAL CHARACTERISTICS (CONTINUED)

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Parameter	Symbol	Test Conditions	LX1675			Units
			Min	Typ	Max	
INTERNAL 5V REGULATOR						
Regulated Output	VCCL	Internal + External Load: 0mA < I_{VCCL} < 50mA	4.5		5.5	V
UVLO AND SOFT-START (SS)						
Start-Up Threshold (VCX, VCCL, VIN)		Rising	3.75		4.38	V
Hysteresis				0.30		V
SS Input Resistance	R_{SS}			20		KΩ
SS Shutdown Threshold	V_{SHDN}			100		mV
Hiccup Mode Duty Cycle		C_{SS} = 0.1µF		6		%
LINEAR REGULATOR CONTROLLER						
Voltage Reference Tolerance		V_{LDFB} = 0.8V, C_{OUT} = 330µF		3		%
LDO Supply	IVSLR	VSLR = 12V		4		mA
LDO Gate Drive		VOH, Output Source Current = 0.5mA			9.0	V
		VOH, Output Source Current = 10mA	7.35			
Source Current	I_{LDGD}	V_{LDGD} = 7.5V			10	mA
Sink Current	I_{LDGD}	V_{LDGD} = 0.4V		0.25		mA
LDO Output Voltage Range	V_{OUT4}		0.8		5.25	V
Regulator Disable Threshold	V_{SSL}			100		mV
Line Regulation		Note 2, 1V < V_{LDO} – V_{OUT4} < 10V, I_{VOUT4} = 50mA	-1		1	%
Load Regulation		Note 2	-1		1	%
LOGIC INPUTS						
FS,SF		Threshold Logic High			2	V
		Threshold Logic Low	0.8			V
		Pulldown Resistance		100		KΩ
THERMAL SHUTDOWN	TSD	Hiccup Mode Operation at Limit		160		°C
Die Temperature						

Note 1: X = Phase 1, 2, 3
Note 2: System Level Measurement; Closed Loop

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SIMPLIFIED BLOCK DIAGRAM

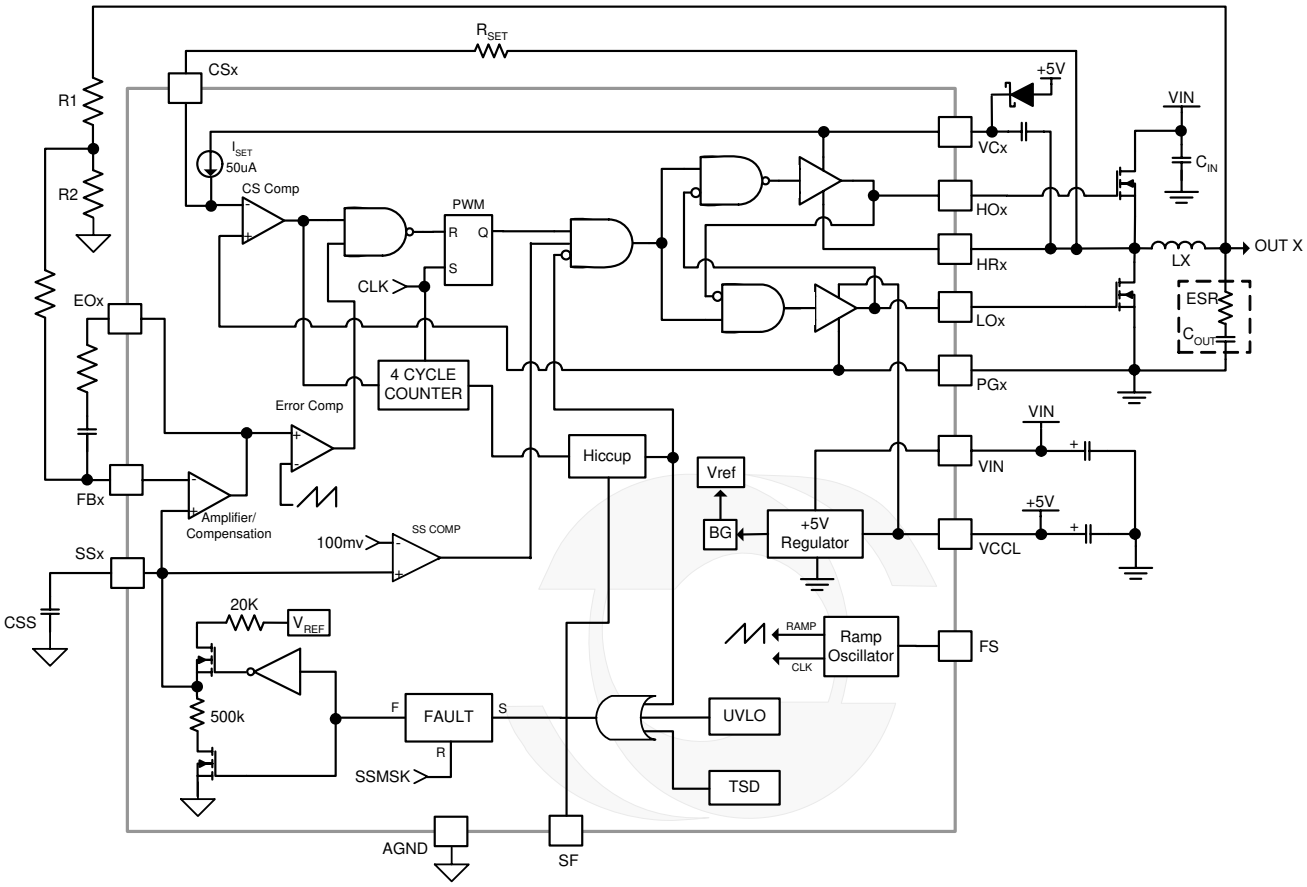

Figure 1 – Typical Block Diagram for Phases 1, and 3

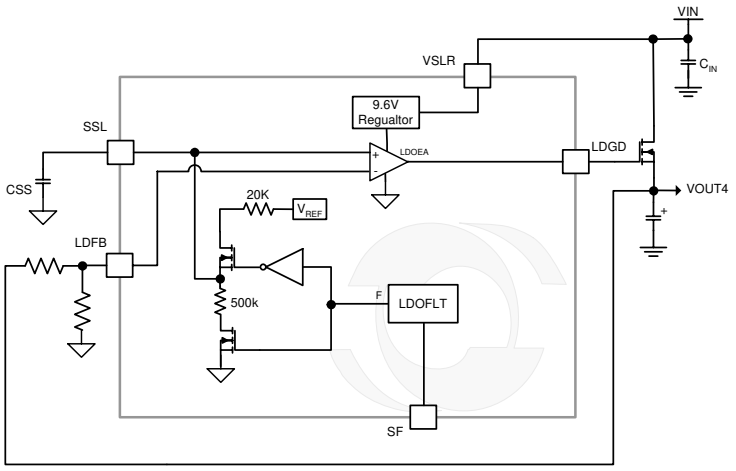

Figure 2 – LDO Controller Block Diagram

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SIMPLIFIED BLOCK DIAGRAM

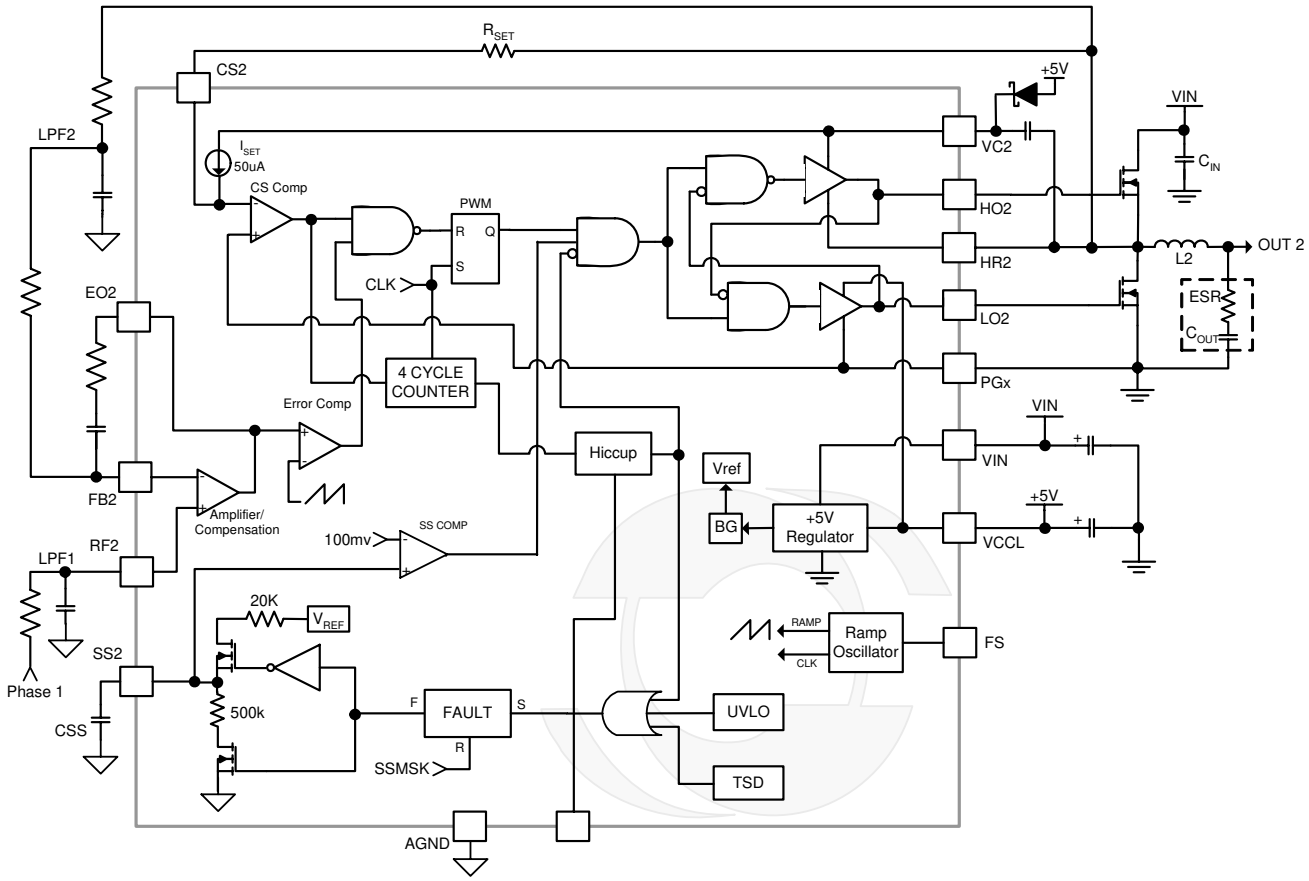

Figure 3 – Block Diagram of Phase 2 Connected in LoadSHARE Mode

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APPLICATION CIRUIT

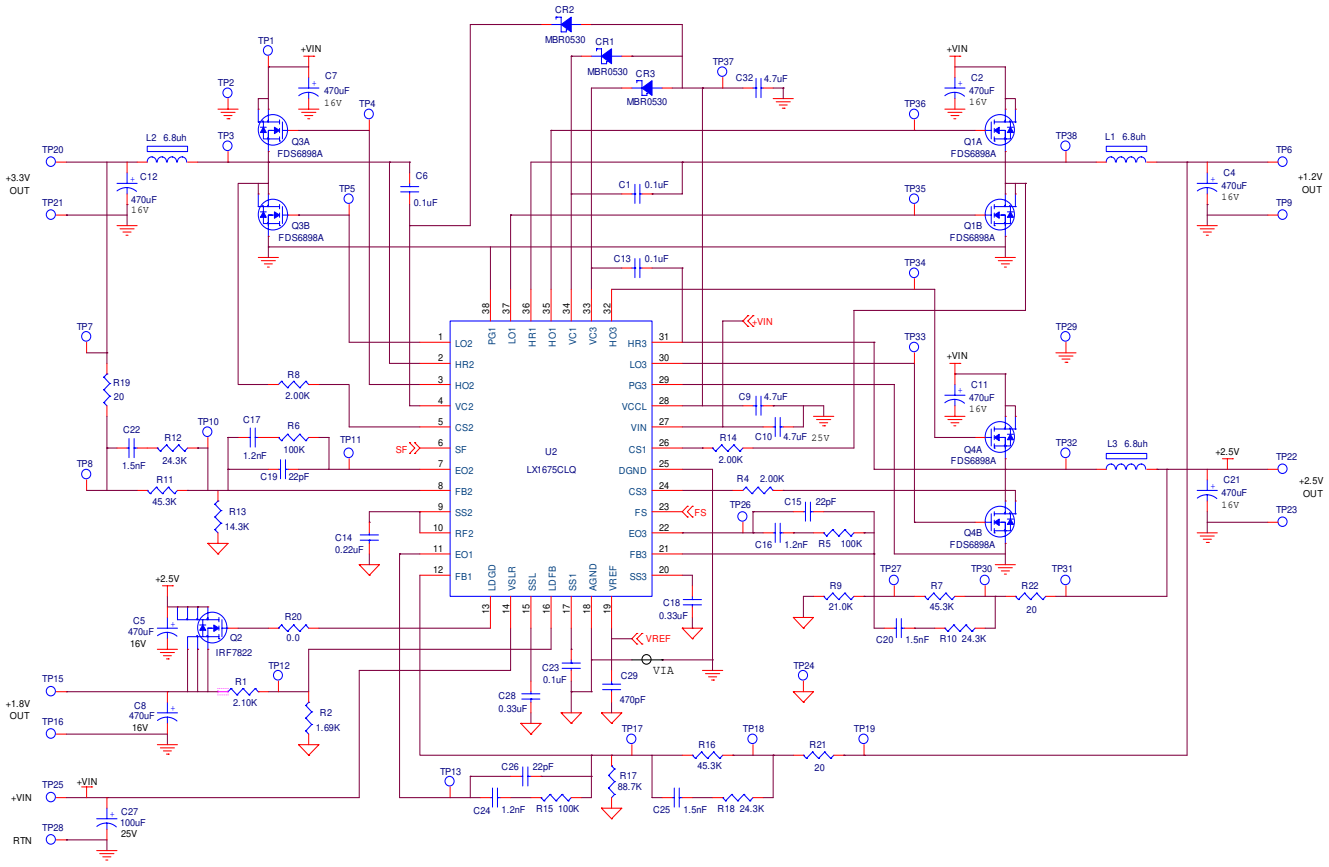

Figure 4 – Four Separate Voltage Outputs with Sequential Power Up Sequence. All High-side MOSFET Drivers Bootstrapped to V_{IN}.

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THEORY OF OPERATION

GENERAL DESCRIPTION

The LX1675 is a voltage-mode pulse-width modulation controller integrated circuit. The internal ramp generator frequency is set to 300kHz or 600kHz by the FS logic input. The device has external compensation, for more flexibility of output current magnitude.

UNDER VOLTAGE LOCKOUT (UVLO)

At power up, the LX1675 monitors the supply voltage at the VCCL pin. The VIN supply voltage has to be sufficient to produce a voltage greater that 4.4 volts at the VCCL pin before the controller will come out of the under-voltage lock-out state. The soft-start (SS) pin is held low to prevent soft-start from beginning and the oscillator is disabled and all MOSFETs are held off.

SOFT-START

Once the VCCL output is above the UVLO threshold, the soft-start capacitor begins to be charged by the reference through a 20kΩ internal resistor. The capacitor voltage at the SS pin rises as a simple RC circuit. The SS pin is connected to the error amplifier's non-inverting input that controls the output voltage. The output voltage will follow the SS pin voltage if sufficient charging current is provided to the output capacitor.

The simple RC soft-start allows the output to rise faster at the beginning and slower at the end of the soft-start interval. Thus, the required charging current into the output capacitor is less at the end of the soft-start interval. A comparator monitors the SS pin voltage and indicates the end of soft-start when SS pin voltage reaches 95% of V_{REF}.

OVER-CURRENT PROTECTION (OCP) AND HICCUP

The LX1675 uses the $R_{DS(ON)}$ of the lower MOSFET, together with a resistor (R_{SET}) to set the actual current limit point. The current sense comparator senses the MOSFET current 50nS after the lower MOSFET is switched on in order to reduce inaccuracies due to ringing. A current source supplies a current (I_{SET}), whose magnitude is 50µA. The set resistor R_{SET} is selected to set the current limit for the application. R_{SET} should be connected directly at the lower MOSFET drain and the source needs a low impedance return to get an accurate measurement across the low resistance $R_{DS(ON)}$.

When the sensed voltage across $RDS_{(ON)}$ plus the set resistor voltage drop exceeds the 0.0Volt, V_{TRIP} threshold, the OCP comparator outputs a signal to reset the PWM latch on a cycle by cycle basis until the current limit counter has reached a count of 4. After a count of 4 the hiccup mode is started. The soft-start capacitor (C_{SS}) is discharged slowly (14 times slower than when being charged up by R_{SS}). When the voltage on the SS pin reaches a 0.1V threshold, hiccup finishes and the circuit soft-starts again. During hiccup both MOSFETs for that phase are held off. The Shared Fault, SF logic input, allows all phases to be totally independent if the SF pin is grounded. If the SF pin is tied to VCCL then when one phase has a fault and goes into the hiccup mode, all phases, including the LDO output will go into the hiccup mode together.

Hiccup is disabled during the soft-start interval, allowing start up with maximum current. If the rate of rise of the output voltage is too fast, the required charging current to the output capacitor may be higher than the current limit setting. In this case, the peak MOSFET current is regulated to the limit-current by the current-sense comparator. If the MOSFET current still reaches its limit after the soft-start finishes, the hiccup is triggered again. When the output has a short circuit the hiccup circuit ensures that the average heat generation in both MOSFETs and the average current is much less than in normal operation.

Over-current protection can also be implemented using a sense resistor, instead of using the $R_{DS(ON)}$ of the lower MOSFET, for greater set-point accuracy.

OSCILLATOR FREQUENCY

An internal oscillator has a selectable switching frequency of 300kHz or 600kHz set by the FS logic input pin. Connect FS to ground for 300kHz and to VCCL for 600kHz operation.

THEORY OF OPERATION FOR A BI-PHASE, LOADSHARE CONFIGURATION

The basic principle used in LoadSHARE, in a multiple phase buck converter topology, is that if multiple, identical, inductors have the same identical voltage impressed across their leads, they must then have the same identical current passing through them. The current that we would like to balance between inductors is mainly the DC component along with as much as possible the transient current. All inductors in a multiphase buck converter topology have their output side tied together at the output filter capacitors. Therefore this side of all the inductors have the same identical voltage.

If the input side of the inductors can be forced to have the same equivalent DC potential on this lead, then they will have the same DC current flowing. To achieve this requirement, phase 1 will be the control phase that sets the output operating voltage, under normal PWM operation. To force the current of phase 2 to be equal to the current of phase 1, a second feedback loop is used. Phase 2 has a low pass filter connected from the input side of each inductor. This side of the inductors has a square wave signal that is proportional to its duty cycle. The output of each LPF is a DC (+ some AC) signal that is proportional to the magnitude and duty cycle of its respective inductor signal. The second feedback loop will use the output of the phase 1 LPF as a reference signal for an error amplifier that will compare this reference to the output of the phase 2 LPF. This error signal will be amplified and used to control the PWM circuit of phase 2. Therefore, the duty cycle of phase 2 will be set so that the equivalent voltage potential will be forced across the phase 2 inductor as compared to the phase 1 inductor. This will force the current in the phase 2 inductor to follow and be equal to the current in the phase 1 inductor.

There are four methods that can be used to implement the LoadSHARE feature of the LX1675 in the Bi-Phase mode of operation.

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THEORY OF OPERATION (CONTINUED)

BI-PHASE, LOADSHARE (ESR METHOD)

The first method is to change the ratio of the inductors equivalent series resistance, (ESR). As can be seen in the previous example, if the offset error is zero and the ESR of the two inductors are identical, then the two inductor currents will be identical. To change the ratio of current between the two inductors, the value of the inductor's ESR can be changed to allow more current to flow through one inductor than the other. The inductor with the lower ESR value will have the larger current. The inductor currents are directly proportional to the ratio of the inductor's ESR value.

The following circuit description shows how to select the inductor ESR for each phase where a different amount of power is taken from two different input power supplies. A typical setup will have a +5V power supply connected to the phase 1 half bridge driver and a +3.3V power supply connected to the phase 2 half bridge driver. The combined power output for this core voltage is 18W (+1.5V @ 12A). For this example the +5V power supply will supply 7W and the +3.3V power supply will supply the other 11W. 7W @ 1.5V is a 4.67A current through the phase 1 inductor. 11W @ 1.5V is a 7.33A current through the phase 2 inductor. The ratio of inductor ESR is inversely proportional to the power level split.

$$\frac{ESR1}{ESR2} = \frac{I2}{I1}$$

The higher current inductor will have the lower ESR value. If the ESR of the phase 1 inductor is selected as 10mΩ, then the ESR value of the phase 2 inductor is calculated as:

$$\left(\frac{4.67A}{7.33A}\right) \times 10m\Omega = 6.4m\Omega$$

Depending on the required accuracy of this power sharing; inductors can be chosen from standard vendor tables with an ESR ratio close to the required values. Inductors can also be designed for a given application so that there is the least amount of compromise in the inductor's performance.

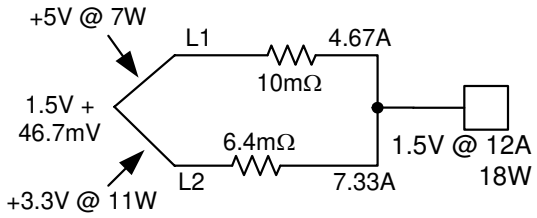

Figure 7 –LoadSHARE Using Inductor ESR

BI-PHASE, LOADSHARE (FEEDBACK DIVIDER METHOD)

Sometimes it is desirable to use the same inductor in both phases while having a much larger current in one phase versus the other. A simple resistor divider can be used on the input side of the Low Pass Filter that is taken off of the switching side of the inductors. If the Phase 2 current is to be larger than the current in Phase 1; the resistor divider is placed in the feedback path before the Low Pass Filter that is connected to the Phase 2 inductor. If the Phase 2 current needs to be less than the current in Phase 1; the resistor divider is then placed in the feedback path before the Low Pass Filter that is connected to the Phase 1 inductor.

As in Figure 7, the millivolts of DC offset created by the resistor divider network in the feedback path, appears as a voltage generator between the ESR of the two inductors.

A divider in the feedback path from Phase 2 will cause the voltage generator to be positive at Phase 2. With a divider in the feedback path of Phase 1 the voltage generator becomes positive at Phase 1. The Phase with the positive side of the voltage generator will have the larger current. Systems that operate continuously above a 30% power level can use this method.

A down side is that the current difference between the two inductors still flows during a no load condition. This produces a low efficiency condition during a no load or light load–state, this method should not be used if a wide range of output power is required.

The following description and Figure 8 show how to determine the value of the resistor divider network required to generate the offset voltage necessary to produce the different current ratio in the two output inductors. The power sharing ratio is the same as that of Figure 7. The Offset Voltage Generator is symbolic for the DC voltage offset between Phase 1 & 2. This voltage is generated by small changes in the duty cycle of Phase 2. The output of the LPF is a DC voltage proportional to the duty cycle on its input. A small amount of attenuation by a resistor divider before the LPF of Phase 2 will cause the duty cycle of Phase 2 to increase to produce the added offset at V2. The high DC gain of the error amplifier will force LPF2 to always be equal to LPF1. The following calculations determine the value of the resistor divider necessary to satisfy this example.

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THEORY OF OPERATION (CONTINUED)

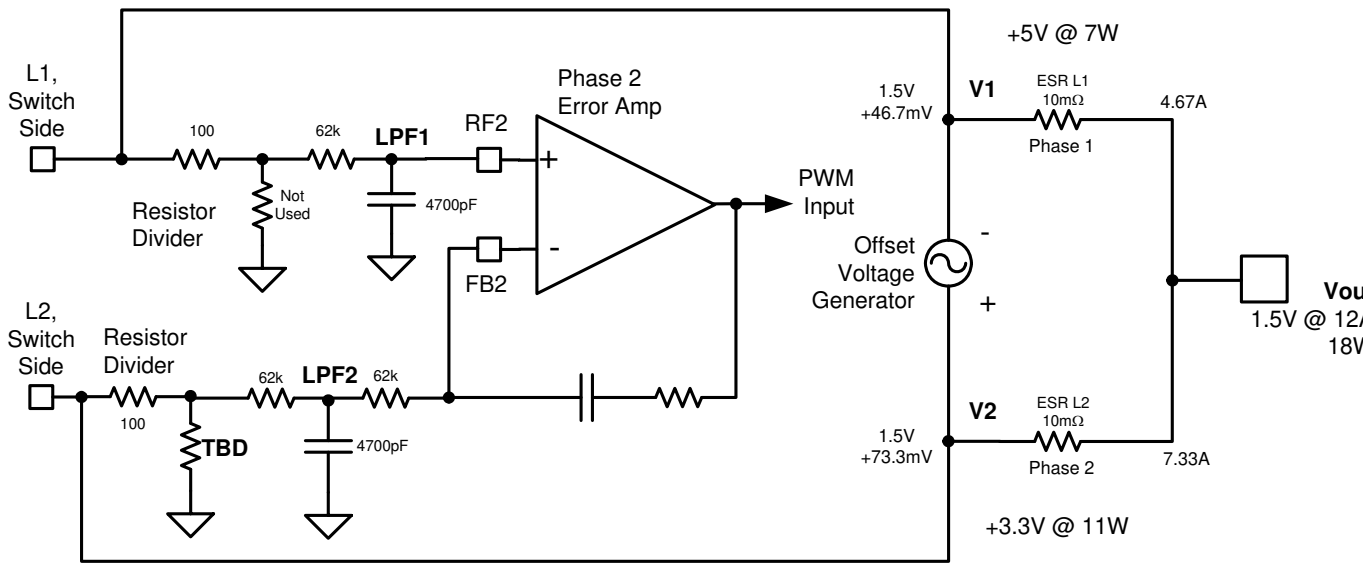

Figure 8 – LoadSHARE Using Feedback Divider Offset

Where V1 = 1.5467 ; V2 = 1.5733 and $K = \frac{V1}{V2}$ then $TBD = \frac{K \times 100}{1 - K} = 5.814\,K$

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THEORY OF OPERATION (CONTINUED)

BI-PHASE, LOADSHARE (PROPORTIONAL METHOD)

The best topology for generating a current ratio at full load and proportional between full load and no load is shown in figure 9. The DC voltage difference between LPF1 and VOUT is a voltage that is proportional to the current flowing in the Phase 1 inductor. This voltage can be amplified and used to offset the voltage at LPF2 through a large impedance that will not significantly alter the characteristics of the low pass filter. At no load there will be no offset voltage and no offset current between the two phases. This will give the highest efficiency at no load.

Also a speed up capacitor can be used between the offset amplifier output and the negative input of the Phase 2 error amplifier. This will improve the transient response of the Phase 2 output current, so that it will share more equally with phase 1 current during a transient condition.

The use of a MOSFET input amplifier is required for the buffer to prevent loading the low pass filter. The gain of the offset amplifier, and the value of Ra and Rb, will determine the ratio of currents between the phases at full load. Two external amplifiers are required or this method.

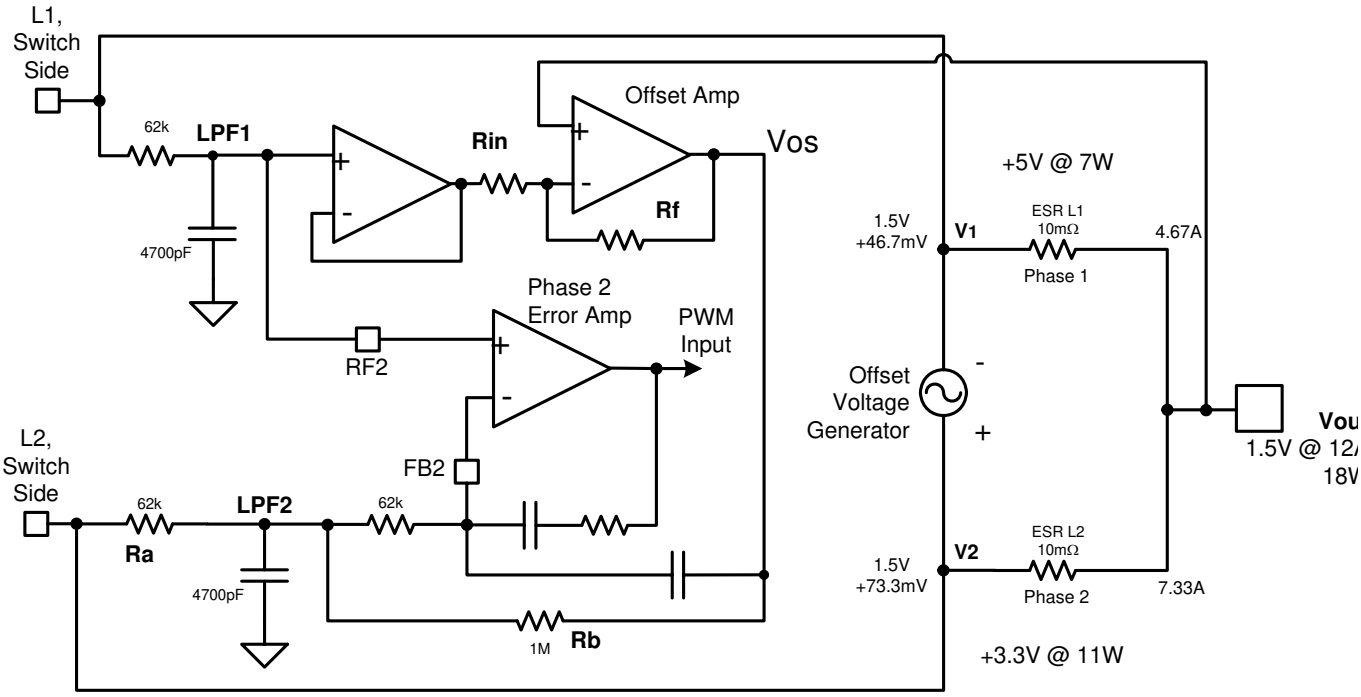

Figure 9 – LoadSHARE Using Proportional Control

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THEORY OF OPERATION (CONTINUED)

The circuit in Figure 9 sums a current through a 1MΩ resistor (Rb) offsetting the phase 2 error amplifier to create an imbalance in the L1 and L2 currents. Although there are many ways to calculate component values the approach taken here is to pick Ra, Rb, Rin, Vout, and inductor ESR. A value for the remaining resistor Rf can then be calculated.

The first decision to be made is the current sharing ratio. Follow the previous examples to understand the basics of LoadSHARE. The most common reason to imbalance the currents in the two phases is because of limitations on the available power from the input rails for each phase. Use the available input power and total required output power to determine the inductor currents for each phase.

All references are to Figure 9

1) Calculate the voltages V1 and V2.

$$V1 = L1\,Current \times L1\,ESR + Vout$$

$$V2 = L2\,Current \times L2\,ESR + Vout$$

2) Select values for Ra and Rb (Ra is typically 62KΩ ; Rb is typically 1MΩ)

3) Calculate the offset voltage Vos at the output of the offset amplifier

$$Vos = V2 - \left(\frac{V2 - V1}{Ra}\right) \times (Ra + Rb)$$

4) Calculate the value for Rf

(select a value for Rin typically 5KΩ)

$$Rf = Rin\left(\frac{Vos - Vout}{Vout - V1}\right)$$

Due to the high impedances in this circuit layout can affect the actual current ratio by allowing some of the switching waveforms to couple into the current summing path. It may be necessary to make some adjustment in Rf after the final layout is evaluated. Also the equation for Rf requires very accurate numbers for the voltages to insure an accurate result.

BI-PHASE, LOADSHARE (SERIES RESISTOR METHOD)

A fourth but less desirable way to produce the ratio current between the two phases is to add a resistor in series with one of the inductors. This will reduce the current in the inductor that has the resistor and increase the current in the inductor of the opposite phase. The example of Figure 7 can be used to determine the current ratio by adding the value of the series resistor to the ESR value of the inductor. The added resistance will lower the overall efficiency

LoadSHARE ERROR SOURCES

With the high DC feedback gain of this second loop, all phase timing errors, $R_{DS(On)}$ mismatch, and voltage differences across the half bridge drivers are removed from the current sharing accuracy. The errors in the current sharing accuracy are derived from the tolerance on the inductor's ESR and the input offset voltage specification of the error amplifier. The equivalent circuit is shown next for an absolute worst case difference of phase currents between the two inductors.

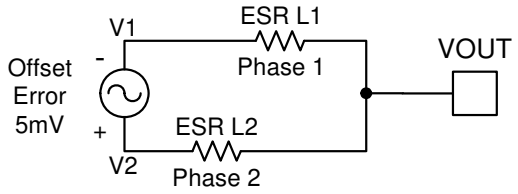

Figure 10 – Error Amplitude

Nominal ESR of 6mΩ. ESR ±5%

Max offset Error = 6mV

+5% ESR L1 = 6.3 mΩ

-5% ESR L2 = 5.7 mΩ

$$\text{If phase 1 current} = 12\,A = \frac{V1 - V_{OUT}}{ESR\,L1}$$

$$V1 - V_{OUT} = 12 \times 6.3 \times 10^{-3} = 75.6\,mV$$

$$V2 = V1 + 6\,mV = 81.6\,mV$$

$$\text{Phase 2 current} = \frac{V2 - V_{OUT}}{ESR\,L2} = \frac{81.6 \times 10^{-3}}{5.7 \times 10^{-3}} = 14.32\,A$$

Phase 2 current is 2.32A greater than Phase 1.

Input bias current also contributes to imbalance.

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APPLICATION NOTE

OUTPUT INDUCTOR

The output inductor should be selected to meet the requirements of the output voltage ripple in steady-state operation and the inductor current slew-rate during transient. The peak-to-peak output voltage ripple is:

$$V_{RIPPLE} = ESR \times I_{RIPPLE}$$

where

$$\Delta I = \frac{V_{IN} - V_{OUT}}{L} \times \frac{D}{f\,s}$$

ΔI is the inductor ripple current, L is the output inductor value and ESR is the Effective Series Resistance of the output capacitor.

ΔI should typically be in the range of 20% to 40% of the maximum output current. Higher inductance results in lower output voltage ripple, allowing slightly higher ESR to satisfy the transient specification. Higher inductance also slows the inductor current slew rate in response to the load-current step change, ΔI, resulting in more output-capacitor voltage droop. When using electrolytic capacitors, the capacitor voltage droop is usually negligible, due to the large capacitance

The inductor-current rise and fall times are:

$$T_{RISE} = L \times \frac{\Delta I}{(V_{IN} - V_{OUT})}$$

and

$$T_{FALL} = L \times \frac{\Delta I}{V_{OUT}}$$

.The inductance value can be calculated by

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \times \frac{D}{f\,s}$$

OUTPUT CAPACITOR

The output capacitor is sized to meet ripple and transient performance specifications. Effective Series Resistance (ESR) is a critical parameter. When a step load current occurs, the output voltage will have a step that equals the product of the ESR and the current step, ΔI. In an advanced microprocessor power supply, the output capacitor is usually selected for ESR instead of capacitance or RMS current capability. A capacitor that satisfies the ESR requirements usually has a larger capacitance and current capability than strictly needed. The allowed ESR can be found by:

$$ESR \times (I_{RIPPLE} + \Delta I) < V_{EX}$$

Where I_{RIPPLE} is the inductor ripple current, ΔI is the maximum load current step change, and V_{EX} is the allowed output voltage excursion in the transient.

Electrolytic capacitors can be used for the output capacitor, but are less stable with age than tantalum capacitors. As they age, their ESR degrades, reducing the system performance and increasing the risk of failure. It is recommended that multiple parallel capacitors be used, so that, as ESR increase with age, overall performance will still meet the processor's requirements.

There is frequently strong pressure to use the least expensive components possible; however, this could lead to degraded long-term reliability, especially in the case of filter capacitors. Microsemi's demonstration boards use the CDE Polymer AL-EL (ESRE) filter capacitors, which are aluminum electrolytic, and have demonstrated reliability. The OS-CON series from Sanyo generally provides the very best performance in terms of long term ESR stability and general reliability, but at a substantial cost penalty. The CDE Polymer AL-EL (ESRE) filter series provides excellent ESR performance at a reasonable cost. Beware of off-brand, very low-cost filter capacitors, which have been shown to degrade in both ESR and general electrolytic characteristics over time.

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APPLICATION NOTE (CONTINUED)

INPUT CAPACITOR

The input capacitor and the input inductor, if used, are to filter the pulsating current generated by the buck converter to reduce interference to other circuits connected to the same 5V rail. In addition, the input capacitor provides local de-coupling for the buck converter. The capacitor should be rated to handle the RMS current requirements. The RMS current is:

$$I_{RMS} = I_L \sqrt{d(1-d)}$$

Where I_L is the inductor current and d is the duty cycle. The maximum value occurs when d = 50% then $I_{RMS} = 0.5I_L$. For 5V input and output in the range of 2 to 3V, the required RMS current is very close to $0.5I_L$.

SOFT-START CAPACITOR

The value of the soft-start capacitor determines how fast the output voltage rises and how large the inductor current is required to charge the output capacitor. The output voltage will follow the voltage at the SS pin if the required inductor current does not exceed the maximum allowable current for the inductor. The SS pin voltage can be expressed as:

$$V_{SS} = V\,ref\left(1 - e^{-t/R_{SS}C_{SS}}\right)$$

Where R_{SS} and C_{SS} are the soft-start resistor and capacitor.

The current required to charge the output capacitor during the soft start interval is.

$$Iout = Cout\frac{dVss}{dt}$$

Taking the derivative with respect to time results in

$$Iout = \frac{VrefCout}{RssCss}e^{-t/R_{SS}C_{SS}}$$

and at t = 0

$$Imax = \frac{VrefCout}{RssCss}$$

The required inductor current for the output capacitor to follow the soft start voltage equals the required capacitor current plus the load current. The soft-start capacitor should be selected to provide the desired power on sequencing and insure that the overall inductor current does not exceed its maximum allowable rating.

Values of C_{SS} equal to 0.1µF or greater are unlikely to result in saturation of the output inductor unless very large output capacitors are used.

OVER-CURRENT PROTECTION

Current limiting occurs at current level I_{CL} when the voltage detected by the current sense comparator is greater than the current sense comparator threshold, V_{TRIP} (0.0 Volts).

$$I_{SET} \bullet R_{SET} - I_{CL} \bullet R_{DS(ON)} = V_{TRIP}$$

So,

$$R_{SET} = \frac{I_{CL} \times R_{DS(ON)}}{I_{SET}} = \frac{I_{CL} \times R_{DS(ON)}}{50\mu A}$$

Example:

For 10A current limit, using FDS6670A MOSFET (10mΩ $R_{DS(ON)}$):

$$R_{SET} = \frac{10 \times 0.010}{50 \times 10^{-6}} = 2.00K\Omega \;\; 1\%$$

Note: If R_{SET} is 0.0Ω or the CSx pin has become shorted to ground the device will be continuously in the current limit mode. If the CSx pin is left open then the current limit will never be enabled. A resistor should be selected for the maximum desired current limit and this should also provide enough current to charge up the output filter capacitance during the soft-start time.

The current limit comparator is followed by a counter that does not allow the hiccup mode until the current limit condition has existed for 4 PWM cycles. If the current limit condition goes away after a count of 2 the counter will be reset. This mode will prevent a single cycle current or noise glitch from starting the hiccup mode current limit.

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APPLICATION NOTE (CONTINUED)

OUTPUT ENABLE

The LX1675 MOSFET driver outputs are shut off by pulling the soft-start pin below 0.1V.

The LDO voltage regulator has its own soft-start pin: SSL, that is the same as any of the other switching phases for control of its output voltage shut down.

PROGRAMMING THE OUTPUT VOLTAGE

The output voltage is sensed by the feedback pin (FB_X) which is compared to a 0.8V reference. The output voltage can be set to any voltage above 0.8V (and lower than the input voltage) by means of a resistor divider R1-R2 (see Figure 1).

$$V_{OUT} = V_{REF}(1 + R_1/R_2)$$

Note: This equation is simplified and does not account for error amplifier input current. Keep R_1 and R_2 close to 1kΩ (order of magnitude).

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For more information see Microsemi Application Note 1307: *LX1671 Product design Guide*. The LX1675 and LX1671 have the same functionality and this information will be applicable.

DDR V_{TT} TERMINATION VOLTAGE

Double Data Rate (DDR) SDRAM requires a termination voltage (V_{TT}) in addition to the line driver supply voltage (VDDQ) and receiver supply voltage (VDD). Although it is not a requirement VDD is generally equal to VDDQ so that only V_{TT} and VDDQ are required.

The LX1675 can supply both voltages by using two of the three PWM phases. Since the currents for V_{TT} and (VDD plus VDDQ) are quite often several amps, (2A to 6A is common) a switching regulator is a logical choice

V_{TT} for DDR memory can be generated with the LX1675 by using the positive input of the phase 2 error amplifier RF2 as a reference input from an external reference voltage V_{REF} which is defined as one half of VDDQ. Using V_{REF} as the reference input will insure that all voltages are correct and track each other as specified in the JEDEC (EIA/JESD8-9A) specification. The phase 2 output will then be equal to V_{REF} and track the VDDQ supply as required.

When an external reference is used the Soft Start will not be functional for that phase

See Microsemi Application Note 1306: *DDR SDRAM Memory Termination* for more details.

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APPLICATION NOTE CONSIDERATIONS

1. The power N-MOSFET transistor's total gate charge spec, (Qg) should not exceed 50nC. This condition will guarantee operation over the specified ambient temperature range with 600kHz operating frequency. The Qg value of the N-MOSFET is directly related to the amount of power dissipation inside the IC package, from the three sets of MOSFET drivers. The equation relating Qg to the power dissipation of a MOSFET driver is: Pd = f * Qg * Vd . f = 300KHs and Vd is the supply voltage for the MOSFET driver. The three bottom MOSFET drivers are powered by the VCCL pin that is connected to +5V. The upper MOSFET drivers are connected to a bootstrap supply generated by its output bridge. The bootstrap supply will ride on top of the VIN rail. Depending on the thermal environment of the application circuit, the Qg value of the N-MOSFETs will have to be less than the 50nC value. A typical configuration of the input voltage rails to generate the output voltages required by having the VIN supply on all phases. At the max Qg value, the three bottom MOSFET drivers will dissipate 75mw each. The upper MOSFET drivers for all three phases will also operate off of +5volts. Their dissipation is 75mw each. The total power dissipation for all gate drives is 450mw. Icc x Vcc =15ma x 5 V= 75mW. Total package power dissipation = 525mW. Using the thermal equation of: Tj = Ta + Pd * Oja, the Junction temperature for this IC package is = 23 + .525 * 85 which = 68°C. This means that the ambient temperature rise has to be less than 82°C. At 600kHz the switching losses double so the ambient temperature rise has to be less than 44°C.

2. The Soft-Start reference input has a 100mv threshold, above which the PWM starts to operate. The internal operating reference level is set at 800mv. This means that the output voltage is 12.5% low when the PWM becomes active. This starts each phase up in the current limit mode without Hiccup operation. If more than one phase is using the 5V rail for conversion, then their soft-start capacitor values should be changed so that the two phases do not start up together. This will help reduce the amount of 5V input capacitance required. Also the VCCL pin should have sufficient decoupling capacitance to keep from drooping back below the UVLO set point during start up.

3. It should be noted here that if the VIN power supply voltage falls between 4.5V to 6.0V the VIN pin and the VCCL pin should be connected together. If the VIN power supply voltage is greater than 6V then the two pins are kept separate and VCCL becomes a 5V output supply for the bootstrap capacitors. The UVLO is looking for the voltage at the VCCL pin to be above 4.4V to start up.

4. When phases 1 and 2 are used in the Bi-phase mode to current share into the same output load, the phase 2 current is forced to follow the phase 1 current. It is important to use a larger soft-start capacitor on phase 2 than phase 1 so that the phase 1 current becomes active before phase 2 becomes active. This will minimize any start up transient. It is also important to disable phase 1 and 2 at the same time. Disabling phase 1 without disabling phase 2, in the Bi-phase mode, allows phase 2 turn on and off randomly because it has lost its reference.

5. The maximum output voltage when using LoadSHARE is limited by the input common mode voltage of the error amplifier and cannot exceed the input common mode voltage.

6. A resistor has been put in series with the gate of the LDO pass transistor to reduce the output noise level. The resistor value can be changed to optimize the output transient response versus output noise.

7. The LDO controller inside the IC uses the voltage at VSLR pin as the drive voltage. This pin should be connected to the VIN voltage to insure reliable operation of the LDO controller. An additional decoupling capacitor can be connected to this pin to eliminate any high frequency noise.

8. The LDO controller has its own soft-start pin so that its turn on delay can be set so that the voltage rail connected to its pass transistor has had time to come up first. This will allow a smooth ramp up of the LDO voltage rail. The voltage rail for the LDO pass transistor can come from any of the other PWM phases if desirable.

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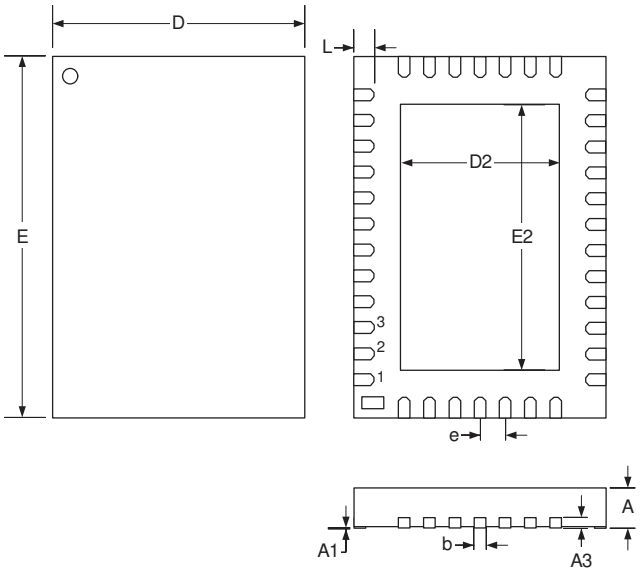
PACKAGE DIMENSIONS

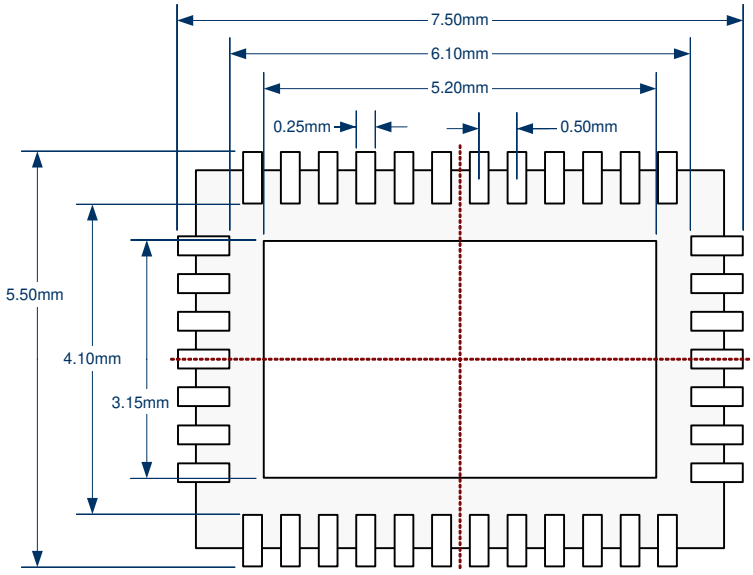
LQ 38-Pin Plastic MLPQ (5x7mm EP)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.011
D	5.00 BSC		0.196 BSC	
D2	3.00	3.25	0.118	0.127
E	7.00 BSC		0.275 BSC	
E2	5.00	5.25	0.196	0.206
e	0.50 BSC		0.019 BSC	
L	0.30	0.50	0.012	0.020

Note: Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(0.006") on any side. Lead dimension shall not include solder coverage.

Recommended Solder Pad Layout



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