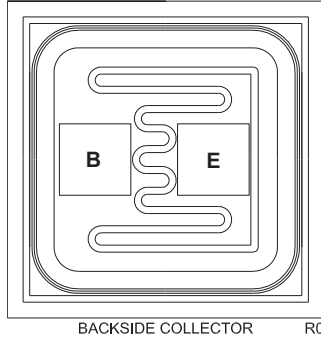


CP336V-2N5551

NPN - High Voltage Transistor Die

The CP336V-2N5551 is a silicon NPN transistor designed for high voltage, general purpose applications.



MECHANICAL SPECIFICATIONS:

| | |
|--------------------------|------------------|
| Die Size | 17.3 x 17.3 MILS |
| Die Thickness | 7.1 MILS |
| Base Bonding Pad Size | 3.9 x 3.9 MILS |
| Emitter Bonding Pad Size | 3.9 x 3.9 MILS |
| Top Side Metalization | Al-Si – 17,000Å |
| Back Side Metalization | Au – 9,000Å |
| Scribe Alley Width | 1.8 MILS |
| Wafer Diameter | 5 INCHES |
| Gross Die Per Wafer | 57,735 |

MAXIMUM RATINGS: (T_A=25°C)

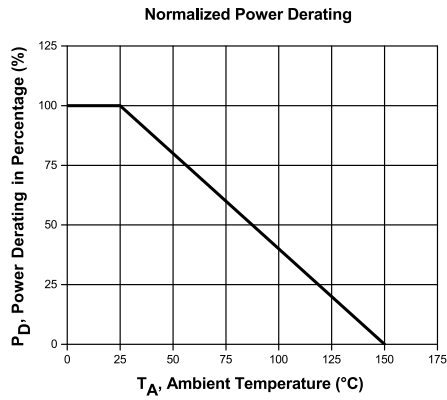
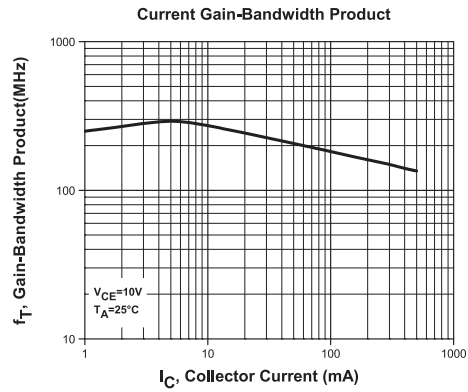
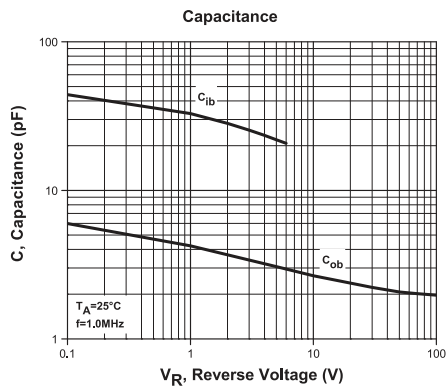
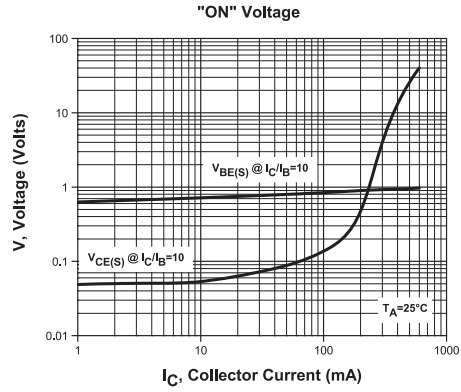
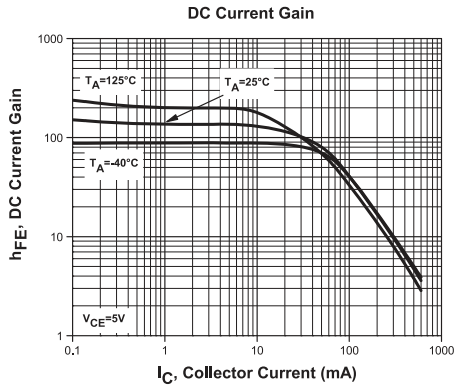
| | SYMBOL | | UNITS |
|--|-----------------------------------|-------------|-------|
| Collector-Base Voltage | V _{CB0} | 180 | V |
| Collector-Emitter Voltage | V _{CEO} | 160 | V |
| Emitter-Base Voltage | V _{EBO} | 6.0 | V |
| Continuous Collector Current | I _C | 600 | mA |
| Operating and Storage Junction Temperature | T _J , T _{stg} | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS: (T_A=25°C)

| SYMBOL | TEST CONDITIONS | MIN | MAX | UNITS |
|----------------------|--|-----|------|-------|
| I _{CBO} | V _{CB} =120V | | 50 | nA |
| I _{EBO} | V _{EB} =4.0V | | 50 | nA |
| BV _{CB0} | I _C =100µA | 180 | | V |
| BV _{CEO} | I _C =1.0mA | 160 | | V |
| BV _{EBO} | I _E =10µA | 6.0 | | V |
| V _{CE(SAT)} | I _C =10mA, I _B =1.0mA | | 0.15 | V |
| V _{CE(SAT)} | I _C =50mA, I _B =5.0mA | | 0.20 | V |
| V _{BE(SAT)} | I _C =50mA, I _B =5.0mA | | 1.0 | V |
| h _{FE} | V _{CE} =5.0V, I _C =1.0mA | 80 | | |
| h _{FE} | V _{CE} =5.0V, I _C =10mA | 80 | 250 | |
| h _{FE} | V _{CE} =5.0V, I _C =50mA | 30 | | |
| f _T | V _{CE} =10V, I _C =10mA, f=100MHz | 100 | 300 | MHz |
| C _{ob} | V _{CB} =10V, I _E =0, f=1.0MHz | | 6.0 | pF |

CP336V-2N5551

Typical Electrical Characteristics



BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

CONTACT US

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