MC74VHCT257A

Quad 2-Channel Multiplexer with 3-State Outputs

The MC74VHCT257A is an advanced high speed CMOS quad 2−channel multiplexer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

It consists of four 2−input digital multiplexers with common select (S) and enable ($\overline{OE}$) inputs. When ($\overline{OE}$) is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the A or B inputs get routed to the corresponding Y outputs.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V because it has full 5.0 V CMOS level output swings.

The VHCT257A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when V_{CC} = 0 V. These input and output structures help prevent device destruction caused by supply voltage−input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffered output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

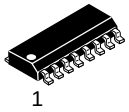
- High Speed: t_{PD} = 4.1 ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 4.0 μA (Max) at T_A = 25°C
- TTL−Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  Human Body Model > 2000 V;
  Machine Model > 200 V
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

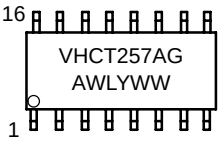
ON Semiconductor®

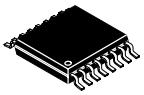
http://onsemi.com

MARKING DIAGRAMS

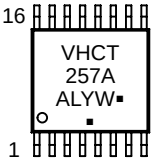


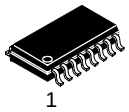
SOIC−16
D SUFFIX
CASE 751B



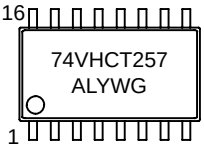


TSSOP−16
DT SUFFIX
CASE 948F





SOEIAJ−16
M SUFFIX
CASE 966



A	=	Assembly Location
WL, L	=	Wafer Lot
Y	=	Year
WW, W	=	Work Week
G or ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs		Outputs
$\overline{OE}$	S	Y0 − Y3
H	X	Z
L	L	A0−A3
L	H	B0−B3

A0 − A3, B0 − B3 = the levels of the respective Data−Word Inputs.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

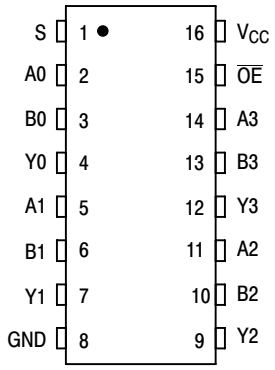


Figure 1. Pin Assignment

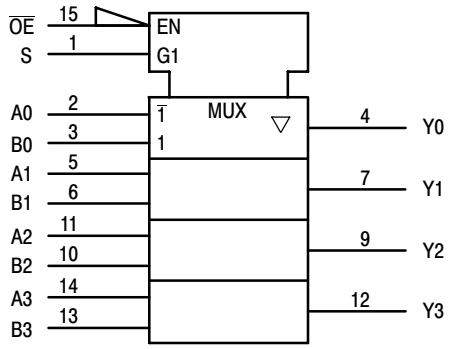


Figure 2. IEC Logic Symbol

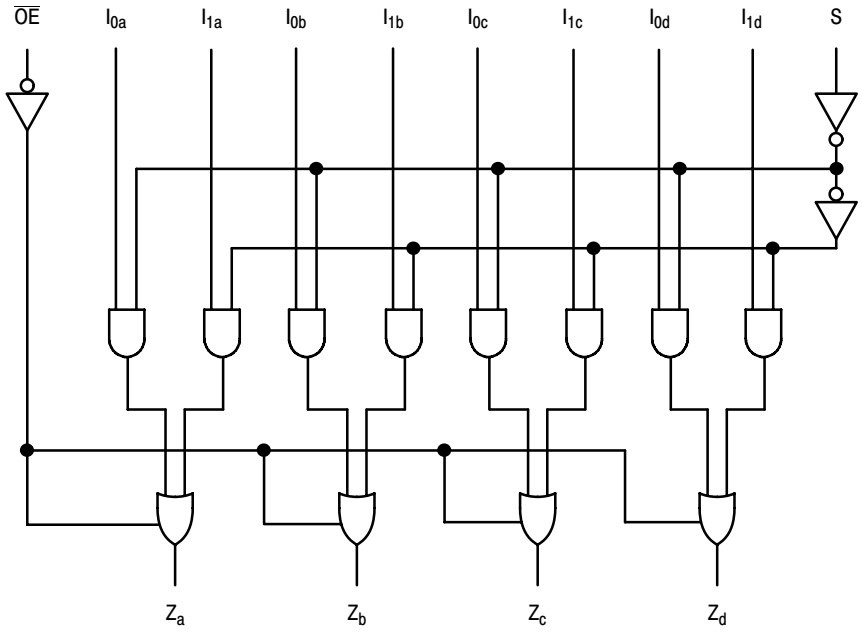


Figure 3. Expanded Logic Diagram

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq$ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	Digital Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage	Output in 3−State High or Low State	−0.5 to +7.0 −0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current		−20	mA
I_{OK}	Output Diode Current		± 20	mA
I_{OUT}	DC Output Current, per Pin		± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 75	mA
P_D	Power Dissipation in Still Air	SOIC Package TSSOP	200 180	mW
T_{STG}	Storage Temperature Range		−65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >200 >2000	V
$I_{LATCHUP}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 4)	± 300	mA
θ_{JA}	Thermal Resistance, Junction−to−Ambient	SOIC Package TSSOP	143 164	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22−A114−A
2. Tested to EIA/JESD22−A115−A
3. Tested to JESD22−C101−A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		4.5	5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage		0	5.5	V
T_A	Operating Temperature Range, all Package Types		−55	125	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 5.0 V ± 0.5 V	0	20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

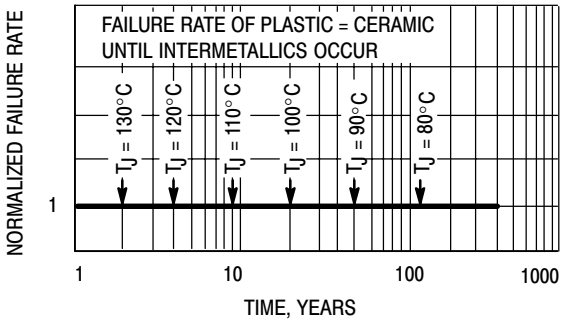


Figure 4. Failure Rate vs. Time Junction Temperature

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			$T_A \le$ 85°C		−55°C ≤ $T_A \le$ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High−Level Input Voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Maximum Low−Level Input Voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	Maximum High−Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} I_{OH} = −50 μA	4.5	3.94			3.8		3.66		V
		$V_{IN} = V_{IH}$ or V_{IL} I_{OH} = −8 mA	4.5	3.94			3.8		3.66		
V_{OL}	Maximum Low−Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} I_{OL} = 50 μA	4.5		0	0.1		0.1		0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} I_{OH} = 8 mA	4.5			0.36		0.44		0.52	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{OZ}	Maximum 3−State Leakage Current	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5			±0.25		±2.5		±2.5	μA
I_{CCT}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			1.35		1.5		1.65	mA
I_{CC}	Additional Quiescent Supply Current (per pin)	$V_{IN} = V_{CC}$ or GND	5.5			4.0		40		40	μA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5 V	0			0.5		5		5	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = ≤ 85°C		−55°C ≤ $T_A \le$ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A or B to Y	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF C_L = 50 pF		5.8 8.3	9.3 12.8	1.0 1.0	11.0 14.5	1.0 1.0	11.0 14.5	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF C_L = 50 pF		3.6 5.1	5.9 7.9	1.0 1.0	7.0 9.0	1.0 1.0	7.0 9.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, S to Y	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF C_L = 50 pF		7.0 9.5	11.0 14.5	1.0 1.0	13.0 16.5	1.0 1.0	13.0 16.5	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF C_L = 50 pF		4.0 5.5	6.8 8.8	1.0 1.0	8.0 10.0	1.0 1.0	8.0 10.0	
t_{PZL}, t_{PZH}	Maximum Output Enable, Time, $\overline{OE}$ to Y	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF R_L = 1 kΩ C_L = 50 pF		6.7 9.2	10.5 14.0	1.0 1.0	12.5 16.0	1.0 1.0	12.5 16.0	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF R_L = 1 kΩ C_L = 50 pF		3.6 5.1	6.8 11.0	1.0 12.0	8.0 10.0	1.0 1.0	8.0 12.0	
t_{PLZ}, t_{PHZ}	Maximum Output Disable, Time, $\overline{OE}$ to Y	V_{CC} = 3.3 ± 0.3 V C_L = 50 pF R_L = 1 kΩ		10.5	14.0	1.0	15.0	1.0	15.0	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 50 pF R_L = 1 kΩ		9.5	12.0	1.0	13.0	1.0	13.0	
C_{IN}	Maximum Input Capacitance			4	10		10		10	pF

Symbol		Typical @ 25°C, V_{CC} = 5.0 V	Unit
C_{PD}	Power Dissipation Capacitance (Note 5)	20	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0 ns, C_L = 50 pF, V_{CC} = 5.0 V)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	− 0.3	− 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

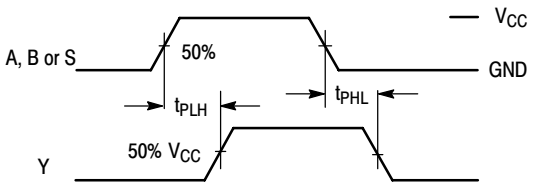


Figure 5. Switching Waveform

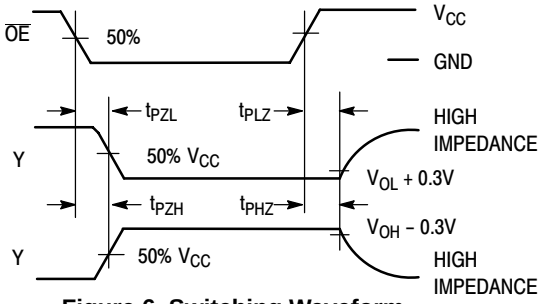
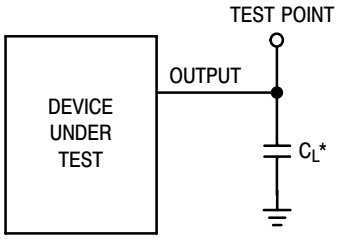
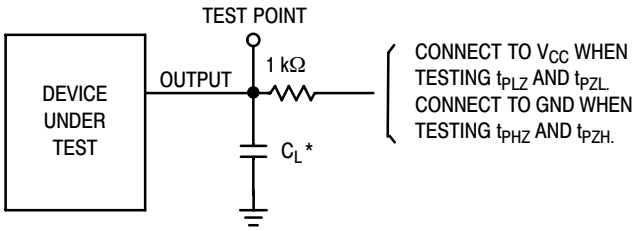


Figure 6. Switching Waveform



*Includes all probe and jig capacitance

Figure 7. Test Circuit



*Includes all probe and jig capacitance

Figure 8. Test Circuit

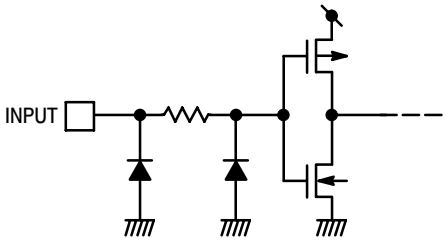


Figure 9. Input Equivalent Circuit

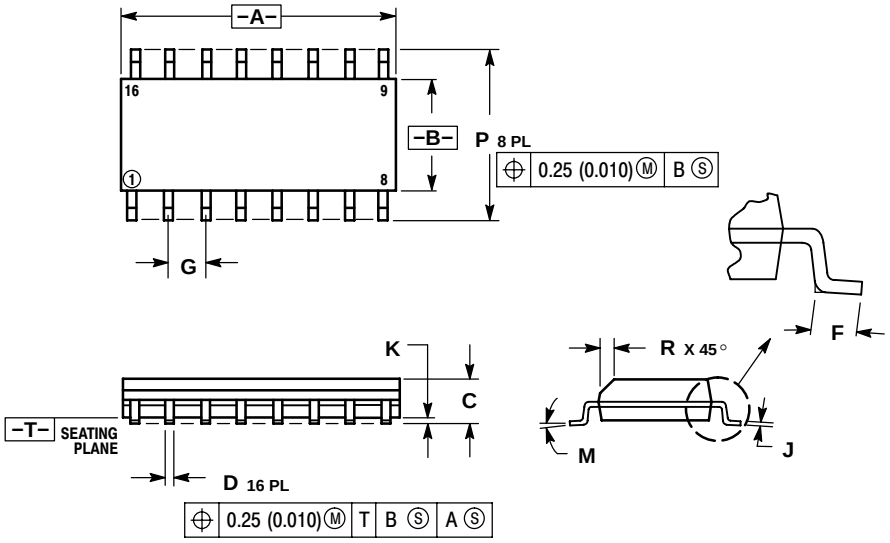
ORDERING INFORMATION

Device	Package	Shipping†
MC74VHCT257AD	SOIC−16	48 Units / Rail
MC74VHCT257ADG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74VHCT257ADR2	SOIC−16	2500 Tape & Reel
MC74VHCT257ADR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74VHCT257ADT	TSSOP−16*	96 Units / Rail
MC74VHCT257ADTG	TSSOP−16*	96 Units / Rail
MC74VHCT257ADTR2	TSSOP−16*	2500 Tape & Reel
MC74VHCT257ADTRG	TSSOP−16*	2500 Tape & Reel
MC74VHCT257AM	SOEIAJ−16	50 Units / Rail
MC74VHCT257AMG	SOEIAJ−16 (Pb−Free)	50 Units / Rail
MC74VHCT257AMEL	SOEIAJ−16	2000 Tape & Reel
MC74VHCT257AMELG	SOEIAJ−16 (Pb−Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

PACKAGE DIMENSIONS

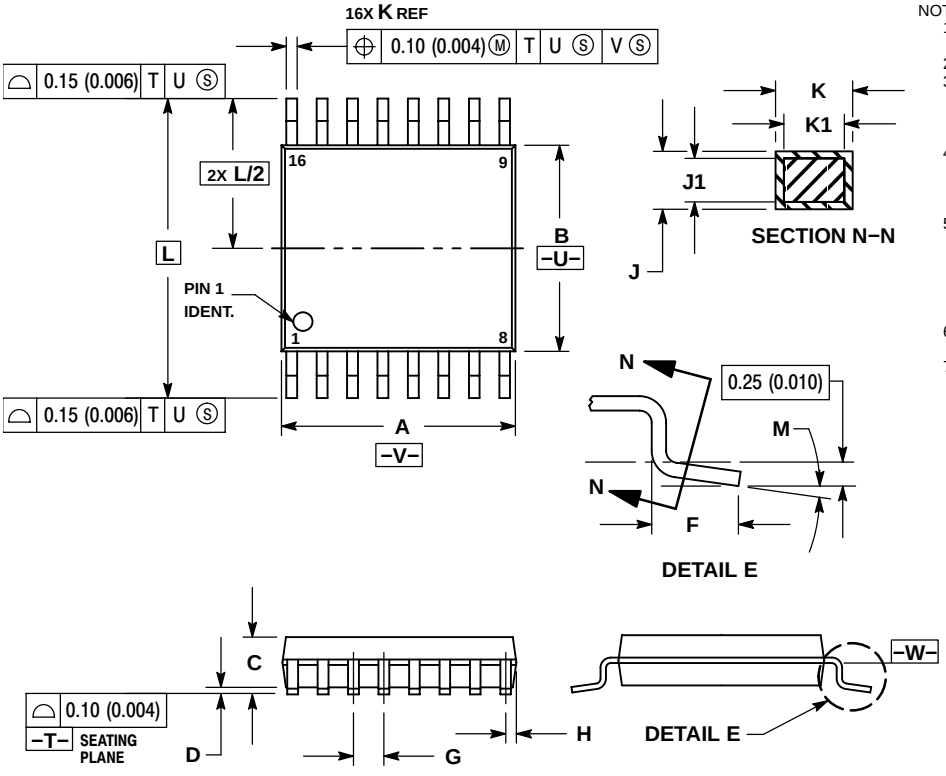
SOIC−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TSSOP−16
DT SUFFIX
CASE 948F−01
ISSUE A

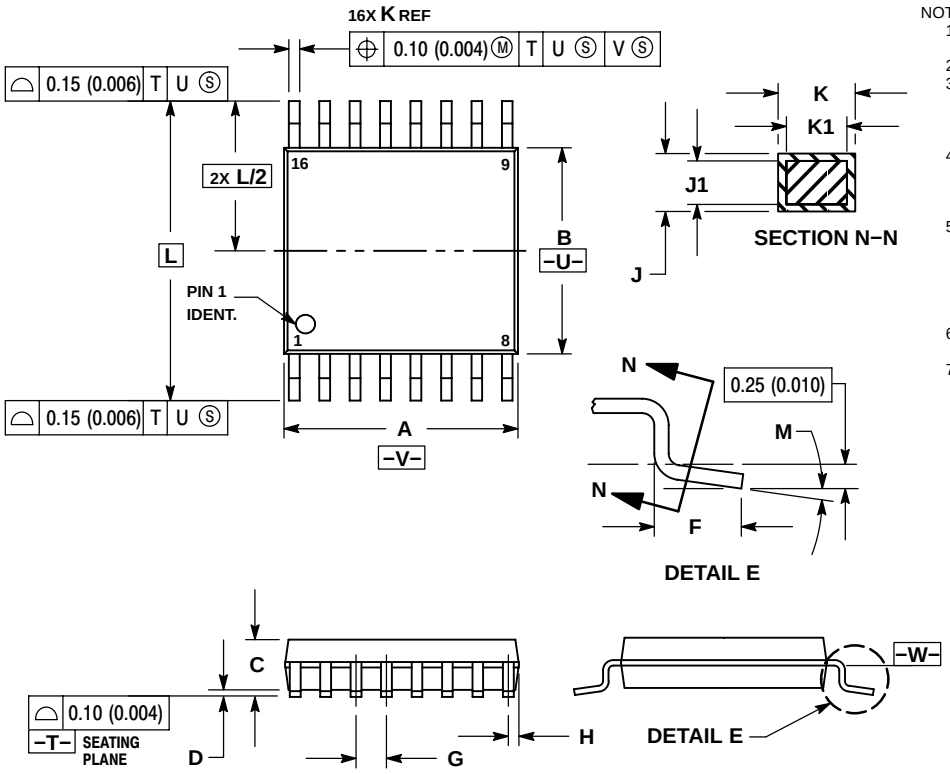


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

SOEIAJ−16
M SUFFIX
CASE 966−01
ISSUE A



NOTES:
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4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.