

HMC715LP3 / 715LP3E

v01.0808



GaAs PHEMT MMIC LOW NOISE AMPLIFIER, 2.1 - 2.9 GHz

Typical Applications

The HMC715LP3(E) is ideal for:

- Cellular/3G and LTE/WiMAX/4G
- BTS & Infrastructure
- Repeaters and Femtocells
- Public Safety Radio
- Access Points

Features

Noise Figure: 0.9 dB

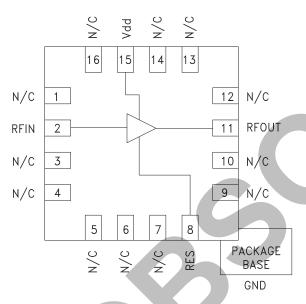
Gain: 19 dB

Output IP3: +33 dBm

Single Supply: +3V to +5V

16 Lead 3x3mm QFN Package: 9 mm²

Functional Diagram



General Description

The HMC715LP3(E) is a GaAs PHEMT MMIC Low Noise Amplifier that is ideal for Cellular/3G and LTE/WiMAX/4G basestation front-end receivers operating between 2.1 and 2.9 GHz. The amplifier has been optimized to provide 0.9 dB noise figure, 19 dB gain and +33 dBm output IP3 from a single supply of +5V. Input and output return losses are excellent and the LNA requires minimal external matching and bias decoupling components. The HMC715LP3(E) can be biased with +3V to +5V and features an externally adjustable supply current which allows the designer to tailor the linearity performance of the LNA for each application.

Electrical Specifications

 $T_A = +25^{\circ}$ C, Rbias = 2k Ohms for Vdd = +5V, Rbias = 47k Ohms for Vdd = +3V [1]

Powerston			Vdd =	= +3V			Vdd = +5V				11-2-		
Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
Frequency Range		2.1 - 2.9			2.3 - 2.7			2.1 - 2.9			2.3 - 2.7	•	MHz
Gain	14.5	18		15	18		15.5	19		16.5	19		dB
Gain Variation Over Temperature		0.01			0.01			0.01			0.01		dB/ °C
Noise Figure		0.9	1.2		0.9	1.2		0.9	1.2		0.9	1.2	dB
Input Return Loss		11.5			11			11.5			11		dB
Output Return Loss		14			13.5			12.5			12		dB
Output Power for 1 dB Compression (P1dB)	10.5	14.5		12.5	15		15	19		16.5	19.5		dBm
Saturated Output Power (Psat)		16			16.5			20			20.5		dBm
Output Third Order Intercept (IP3)		28			28.5			33			33.5		dBm
Supply Current (Idd)		47	65		47	65		95	126		95	126	mA

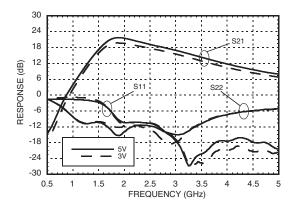
^[1] Rbias resistor sets current, see application circuit herein



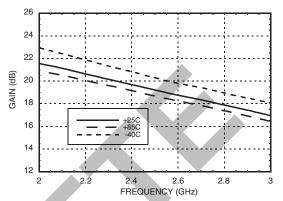


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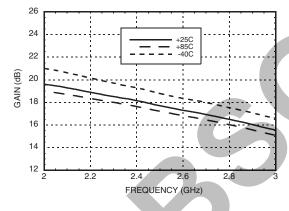
Broadband Gain & Return Loss [1] [2]



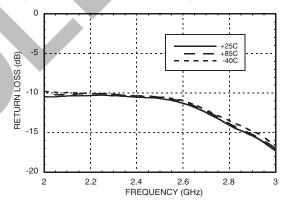
Gain vs. Temperature [1]



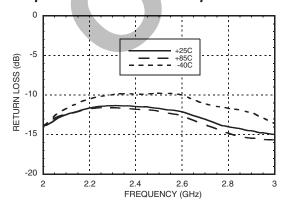
Gain vs. Temperature [2]



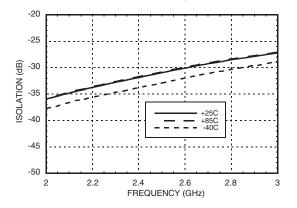
Input Return Loss vs. Temperature [1]



Output Return Loss vs. Temperature [1]



Reverse Isolation vs. Temperature [1]



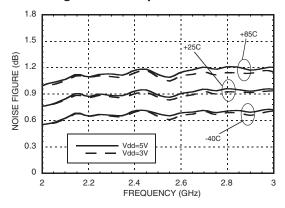
[1] Vdd = 5V, $Rbias = 2k\Omega$ [2] Vdd = 3V, $Rbias = 47k\Omega$



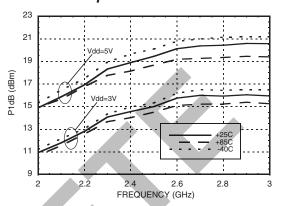


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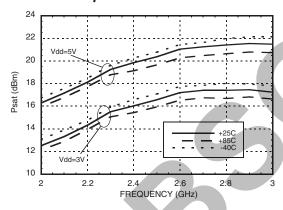
Noise Figure vs. Temperature [1] [2] [4]



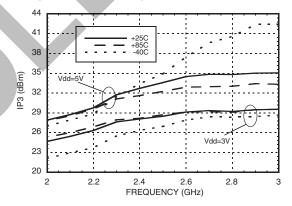
P1dB vs. Temperature [1] [2]



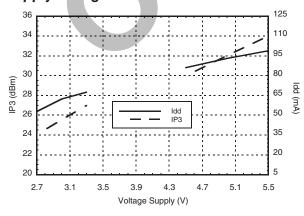
Psat vs. Temperature [1] [2]



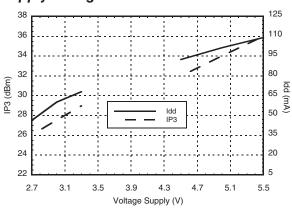
Output IP3 vs. Temperature [1] [2]



Output IP3 and Supply Current vs. Supply Voltage @ 2300 MHz [3]



Output IP3 and Supply Current vs. Supply Voltage @ 2700 MHz [3]



[1] Vdd = 5V, $Rbias = 2k \Omega$ [2] Vdd = 3V, $Rbias = 47k\Omega$

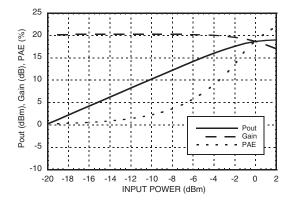
[3] Rbias = $2k\Omega$ for Vdd = 5V, Rbias = $47k\Omega$ for Vdd = 3V [4] Measurement reference plane shown on evaluation PCB drawing.



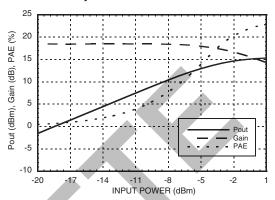


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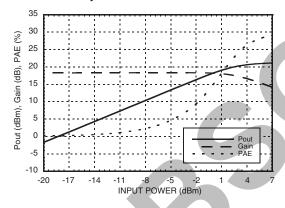
Power Compression @ 2300 MHz [1]



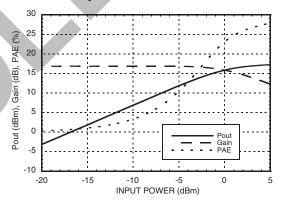
Power Compression @ 2300 MHz [2]



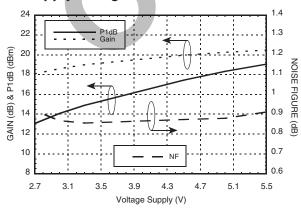
Power Compression @ 2700 MHz [1]



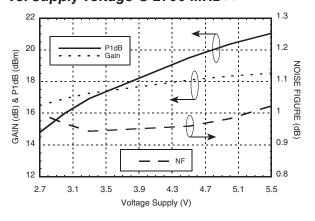
Power Compression @ 2700 MHz [2]



Gain, Power & Noise Figure vs. Supply Voltage @ 2300 MHz [3]



Gain, Power & Noise Figure vs. Supply Voltage @ 2700 MHz [3]



[1] Vdd = 5V, $Rbias = 2k\Omega$ [2] Vdd = 3V, $Rbias = 47k\Omega$ [3] $Rbias = 2k\Omega$ for Vdd = 5V, $Rbias = 47k\Omega$ for Vdd = 3V



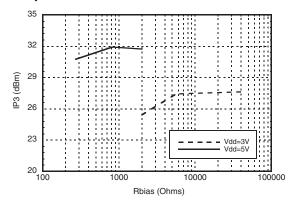
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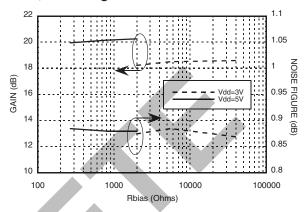


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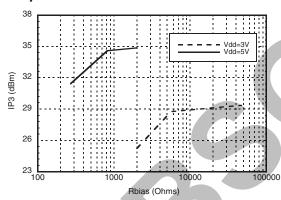
Output IP3 vs. Rbias @ 2300 MHz



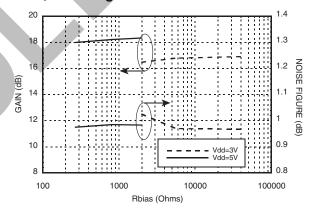
Gain, Noise Figure & Rbias @ 2300 MHz



Output IP3 vs. Rbias @ 2700 MHz



Gain, Noise Figure & Rbias @ 2700 MHz







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Absolute Bias Resistor Range & Recommended Bias Resistor Values

\/dd (\/\)		Idd (m A)		
Vdd (V)	Min	Max Recommend		ldd (mA)
			2K	28
3V	1.8k ^[1]	Open Circuit 5.6K 47K	40	
			47K	47
			270	61
5V	0	Open Circuit	820	81
			2K	95

^[1] With Vdd= 3V and Rbias < 1.8k Ohms may result in the part becoming conditionally stable which is not recommended.

Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+5.5V
RF Input Power (RFIN) (Vdd = +5 Vdc)	+10 dBm
Channel Temperature	150 °C
Continuous Pdiss (T= 85 °C) (derate 11.1 mW/°C above 85 °C)	0.72 W
Thermal Resistance (channel to ground paddle)	90 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A



Typical Supply Current vs. Supply Voltage

(Rbias = 2k for Vdd = 5V, Rbias = 47k for Vdd = 3V)

Vdd (V)	ldd (mA)
2.7	35
3.0	47
3.3	57
4.5	80
5.0	95
5.5	110

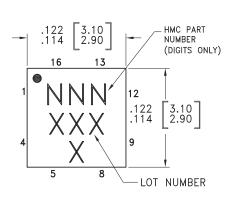
Note: Amplifier will operate over full voltage ranges shown above.

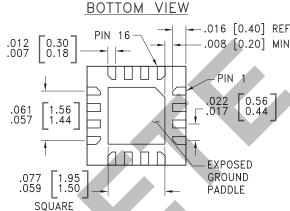


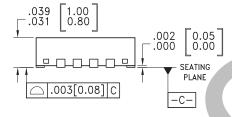


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Outline Drawing







NOTES:

- 1. LEADFRAME MATERIAL: COPPER ALLOY
- 2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
- 3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
- PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.
 PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
- 5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
- 6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
- 7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC715LP3	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	715 XXXX
HMC715LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	7 <u>15</u> XXXX

- [1] Max peak reflow temperature of 235 $^{\circ}\text{C}$
- [2] Max peak reflow temperature of 260 $^{\circ}\text{C}$
- [3] 4-Digit lot number XXXX

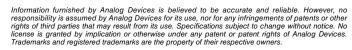




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Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3 - 7, 9, 10, 12 - 14, 16	N/C	No connection required. These pins may be connected to RF/DC ground without affecting performance.	
2	RFIN	This pin is DC coupled. See application circuit for off chip component.	RFIN O ESD
11	RFOUT	This pin is DC coupled. See application circuit for off chip component.	RFOUT ESD =
8	RES	This pin is used to set the DC current of the amplifier by selection of external bias resistor. See application circuit.	RES ESD =
15	Vdd	Power supply voltage. Bypass capacitors are required. See application circuit.	Vdd ESD =
	GND	Ground paddle must be connected to RF/DC ground.	GND =

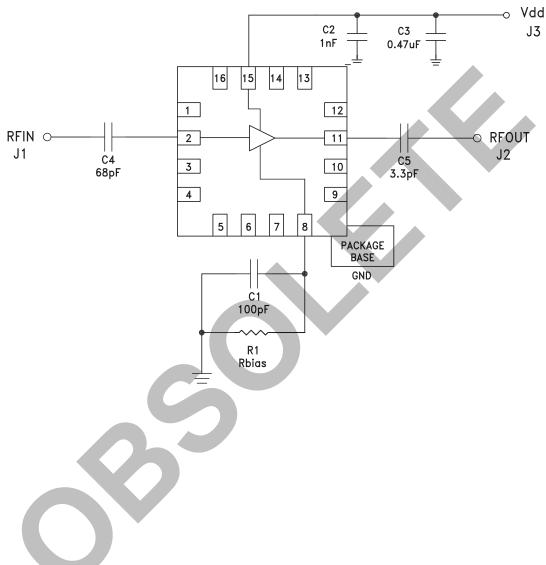






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Application Circuit

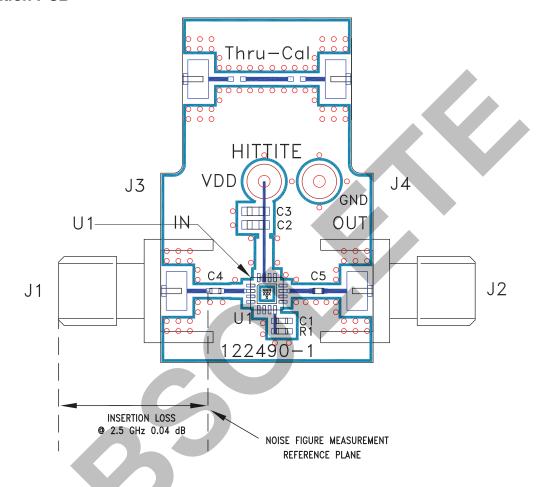






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Evaluation PCB



List of Materials for Evaluation PCB 122492 [1]

Item	Description	
J1, J2	PCB Mount SMA RF Connector	
J3, J4	DC Pin	
C1	100pF Capacitor, 0402 Pkg.	
C2	1000 pF Capacitor, 0603 Pkg.	
C3	0.47μF Capacitor, 0603 Pkg.	
C4	68pF Capacitor, 0402 Pkg.	
C5	3.3pF Capacitor, 0402 Pkg.	
R1	2kΩ Resistor, 0402 Pkg.	
U1	HMC715LP3(E) Amplifier	
PCB [2]	122490 Evaluation PCB	

^[1] Reference this number when ordering complete evaluation PCB $\,$

The circuit board used in this application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.

^[2] Circuit Board Material: Rogers 4350. or Arlon 25R