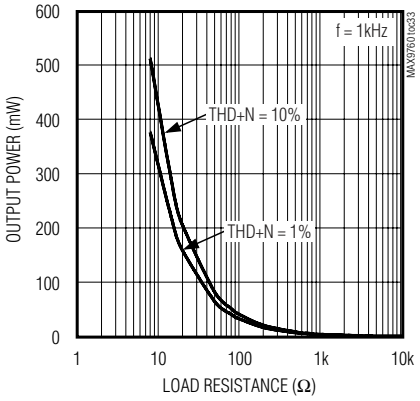
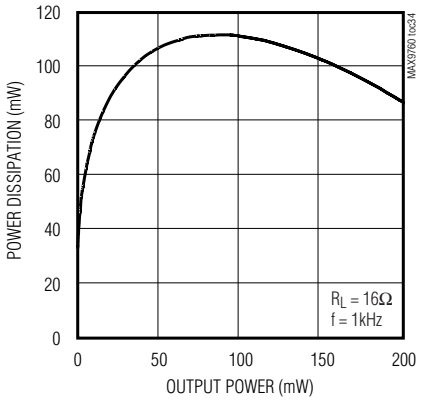
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = 5V, T_A = +25°C, unless otherwise noted.)

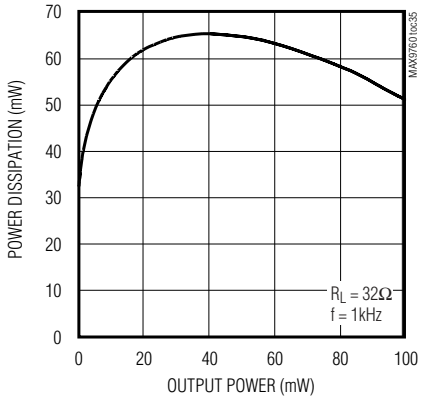
OUTPUT POWER vs. LOAD RESISTANCE (HEADPHONE MODE)



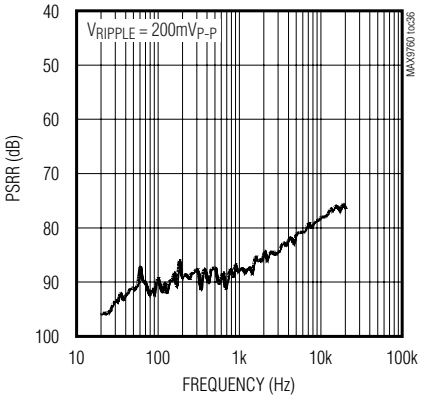
POWER DISSIPATION vs. OUTPUT POWER (HEADPHONE MODE)



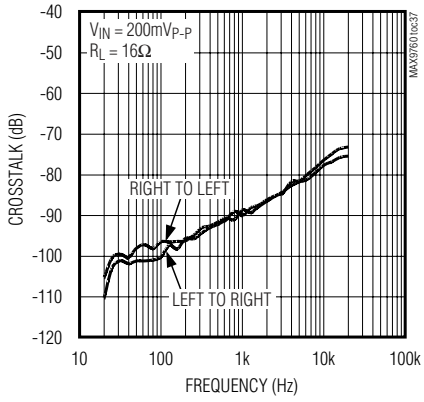
POWER DISSIPATION vs. OUTPUT POWER (HEADPHONE MODE)



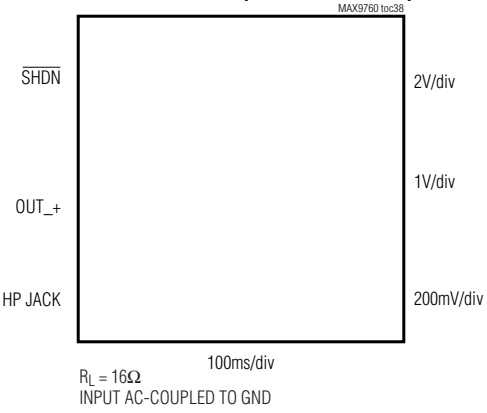
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (HEADPHONE MODE)



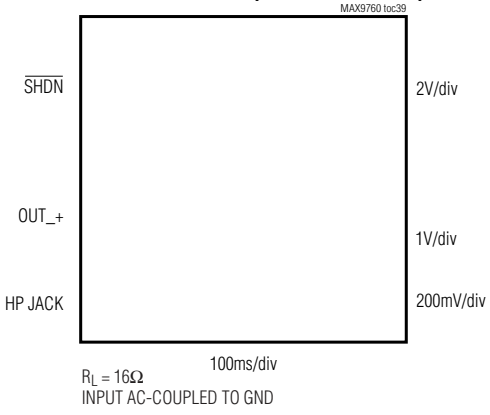
CROSSTALK vs. FREQUENCY (HEADPHONE MODE)



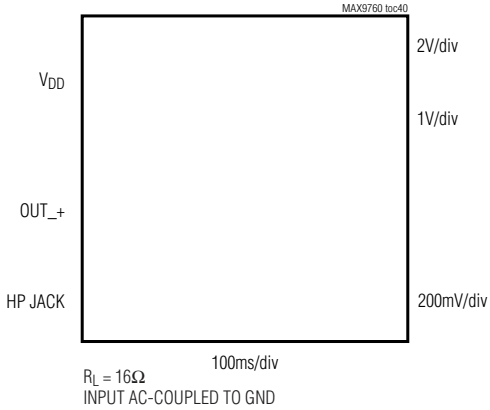
EXITING SHUTDOWN (HEADPHONE MODE)



ENTERING SHUTDOWN (HEADPHONE MODE)



EXITING POWER-DOWN (HEADPHONE MODE)

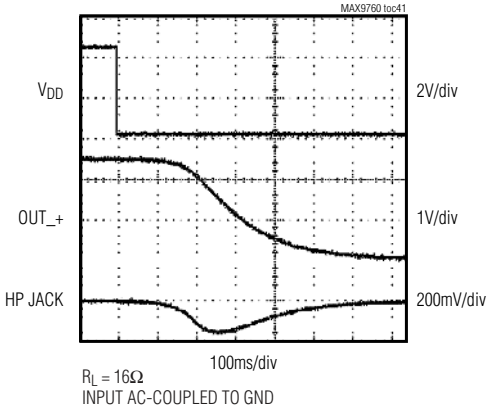


Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

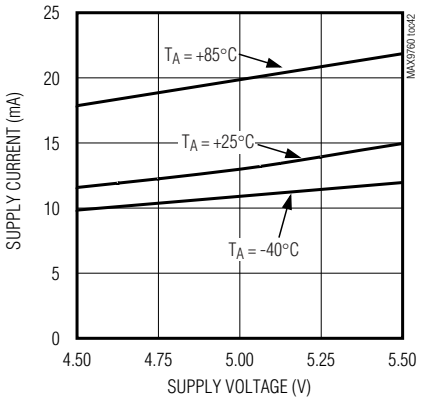
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = 5V, T_A = +25°C, unless otherwise noted.)

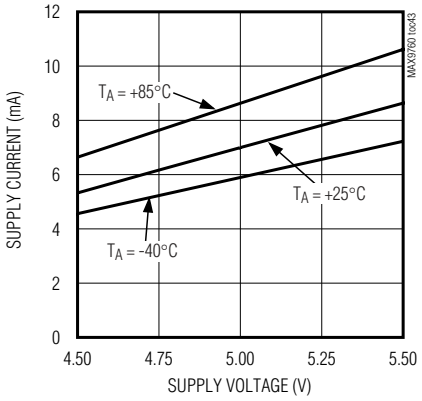
ENTERING POWER-DOWN (HEADPHONE MODE)



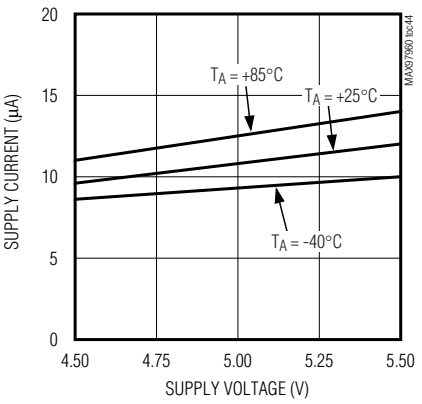
SUPPLY CURRENT vs. SUPPLY VOLTAGE (SPEAKER MODE)



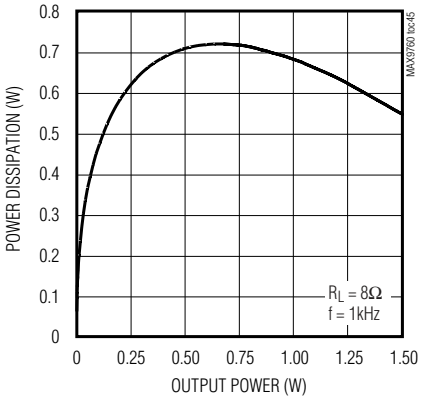
SUPPLY CURRENT vs. SUPPLY VOLTAGE (HEADPHONE MODE)



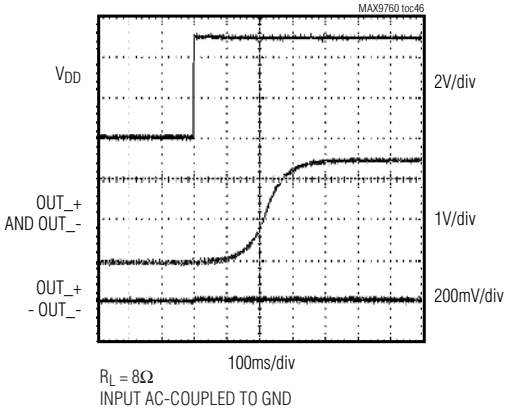
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



POWER DISSIPATION vs. OUTPUT POWER (SPEAKER MODE)



EXITING POWER-DOWN (SPEAKER MODE)



Pin Description

PIN								NAME	FUNCTION
MAX9760		MAX9761		MAX9762		MAX9763			
QFN	TSSOP	QFN	TSSOP	QFN	TSSOP	QFN	TSSOP		
1	26	—	—	1	26	—	—	SDA	Bidirectional Serial Data I/O
2	27	—	—	2	27	—	—	$\overline{INT}$	µC Interrupt Output
3	28	3	28	3	28	3	28	V_{DD}	Power Supply
4	1	4	1	4	1	4	1	SV_{DD}	Standby Power Supply. Connect to a standby power supply that is always on, or connect to V_{DD} through a Schottky diode and bypass with 220µF capacitor to GND. Short to V_{DD} if clickless operation is not essential.
5	2	5	2	5	2	5	2	INL1	Left-Channel Input 1
6	3	6	3	6	3	6	3	INL2	Left-Channel Input 2
7	4	7	4	7	4	7	4	GAINLA	Left-Channel Gain Set A
8	5	8	5	8	5	8	5	GAINLB	Left-Channel Gain Set B
9, 13, 23, 27	6, 10, 20, 24	9, 13, 23, 27	6, 10, 20, 24	9, 23, 27	6, 20, 24	9, 23, 27	6, 20, 24	PGND	Power Ground
10	7	10	7	10	7	10	7	OUTL+	Left-Channel Bridged Amplifier Positive Output. OUTL+ also serves as the left-channel headphone amplifier output.
11, 25	8, 22	11, 25	8, 22	11, 25	8, 22	11, 25	8, 22	PV_{DD}	Output Amplifier Power Supply
12	9	12	9	—	—	—	—	OUTL-	Left-Channel Bridged Amplifier Negative Output
14	11	14	11	14	11	14	11	$\overline{SHDN}$	Active-Low Shutdown. Connect $\overline{SHDN}$ to V_{DD} for normal operation.
15	12	—	—	15	12	—	—	ADD	Address Select. A logic high sets the address LSB to 1, a logic low sets the address LSB to zero.
16	13	16	13	16	13	16	13	HPS	Headphone Sense Input. A logic high configures the device as a single-ended headphone amp. A logic low configures the device as a BTL speaker amp.
17	14	17	14	17	14	17	14	BIAS	DC Bias Bypass. See *BIAS Capacitor Selection* section for capacitor selection. Connect C_{BIAS} from BIAS to GND.
18	15	18	15	13	10	13	10	GND	Ground

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Pin Description (continued)

PIN								NAME	FUNCTION
MAX9760		MAX9761		MAX9762		MAX9763			
QFN	TSSOP	QFN	TSSOP	QFN	TSSOP	QFN	TSSOP		
19	16	19	16	19	16	19	16	INR1	Right-Channel Input 1
20	17	20	17	20	17	20	17	INR2	Right-Channel Input 2
21	18	21	18	21	18	21	18	GAINRA	Right-Channel Gain Set A
22	19	22	19	22	19	22	19	GAINRB	Right-Channel Gain Set B
24	21	24	21	24	21	24	21	OUTR+	Right-Channel Bridged Amplifier Positive Output. OUTR+ also serves as the right-channel headphone amplifier output.
26	23	26	23	26	23	26	23	OUTR-	Right-Channel Bridged Amplifier Negative Output
28	25	—	—	28	25	—	—	SCL	Serial Clock Line
—	—	—	—	12	9	12	9	N.C.	No Connection. Not internally connected.
—	—	—	—	18	15	18	15	GAINM	Mono Gain Set
—	—	1	26	—	—	1	26	MUTE	Active-High Mute Input
—	—	2	27	—	—	2	27	HPS_EN	Headphone Enable. A logic high enables HPS. A logic low disables HPS and the device is always configured as a BTL speaker amp.
—	—	15	12	—	—	15	12	GAIN$\overline{A}$/B	Gain Select. A logic low selects the gain set by GAIN_A. A logic high selects the gain set by GAIN_B.
—	—	28	25	—	—	28	25	IN$\overline{1}$/2	Input Select. A logic low selects amplifier input 1. A logic high selects amplifier input 2.

Detailed Description

The MAX9760–MAX9763 feature 3W BTL speaker amplifiers, 200mW headphone amplifiers, input multiplexers, headphone sensing, and comprehensive click-and-pop suppression. The MAX9760/ MAX9761 are stereo BTL/headphone amplifiers. The MAX9762/ MAX9763 are mono BTL/stereo headphone amplifiers. The MAX9760/MAX9762 are controlled through an I²C-compatible, 2-wire serial interface. The MAX9761/ MAX9763 are controlled through five logic inputs: MUTE, $\overline{SHDN}$, HPS_EN, GAIN$\overline{A}$/B, and IN$\overline{1}$/2 (see *Selector Guide*). The MAX9760–MAX9763 feature exceptional PSRR (100dB at 1kHz), allowing these devices to operate from noisy digital supplies without the need for a linear regulator.

The speaker amplifiers use a BTL configuration. The signal path is composed of an input amplifier and an output amplifier. Resistor R_{IN} sets the input amplifier's gain, and resistor R_F sets the output amplifier's gain. The output of these two amplifiers serves as the input to a slave amplifier configured as an inverting unity-gain follower. This results in two outputs, identical in magnitude, but 180° out of phase. The overall gain of the speaker amplifiers is twice the product of the two amplifier gains (see *Gain-Setting Resistor* section). A feature of this architecture is that there is no phase inversion from input to output.

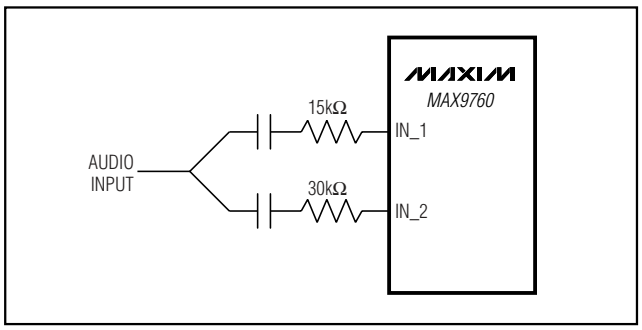


Figure 1. Using the Input Multiplexer for Gain Setting

When configured as a headphone (single-ended) amplifier, the slave amplifier is disabled, muting the speaker and the main amplifier drives the headphone. The MAX9760–MAX9763 can deliver 3W of continuous average power into a 3Ω load with less than 1% THD+N in speaker mode, and 200mW of continuous average power into a 16Ω load with less than 1% THD+N in headphone mode. These devices also feature thermal overload protection.

Mono Mode

The MAX9762/MAX9763 are 3W mono speaker amplifiers, 200mW stereo headphone amplifiers, and a mixer/attenuator (see the MAX9762/MAX9763 *Functional Diagram*). In speaker (mono) mode, the mixer/attenuator combines the two stereo inputs (INL_ and INR_) and attenuates the resultant signal by a factor of 2. This allows for full reproduction of a stereo signal through a single speaker, while maintaining optimum headroom. The resistor connected between GAINM and OUTR+, sets the gain of the devices in speaker mode (see the MAX9762 *Functional Diagram*). This allows the speaker amplifier to have a different gain and feedback network from the headphone amplifier.

BIAS

These devices operate from a single 5V supply, and feature an internally generated, power-supply independent, common-mode bias voltage of 2.5V referenced to GND. BIAS provides both click-and-pop suppression and sets the DC bias level for the audio outputs. BIAS is internally connected to the noninverting input of each speaker amplifier (see *Typical Application Circuit/ Functional Diagram*). Choose the value of the bypass capacitor as described in the *BIAS Capacitor* section. No external load should be applied to BIAS. Any load lowers the BIAS voltage, affecting the overall performance of the device.

Input Multiplexer

Each amplifier features a 2:1 input multiplexer, allowing input selection between two stereo sources. Both multiplexers are controlled by bit 1 in the control register (MAX9760/MAX9762) or by the $\overline{IN1}$/2 pin (MAX9761/ MAX9763). A logic low selects input IN_1 and a logic high selects input IN_2.

The input multiplexer can also be used to further expand the number of gain options available from the MAX9760–MAX9763 family. Connecting the audio source to the device through two different input resistors (Figure 1) increases the number of gain options from two to four (MAX9760/MAX9761) and from three to six (MAX9762/MAX9763). Additionally, the input multiplexer allows a speaker equalization network to be switched into the speaker signal path. This is typically useful in optimizing acoustic response from speakers with small physical dimensions.

Headphone Sense Enable

The HPS pin is enabled by HPS_EN (MAX9762/ MAX9763) or the HPSD bit (MAX9760/MAX9761). HPSD or HPS_EN determines whether the device is in automatic detection mode or fixed mode operation (see Tables 1a and 1b).

Headphone Sense Input (HPS)

A voltage on HPS less than 0.7 × V_{DD} sets the device to speaker mode. A voltage greater than 0.9 × V_{DD} disables the inverting bridge amplifier (OUT_-), which mutes the speaker amplifier and sets the device into headphone mode.

For automatic headphone detection, connect HPS to the control pin of a 3-wire headphone jack as shown in Figure 2. With no headphone present, the resistive voltage-divider created by R1 and R2 sets the voltage on HPS to be less than 0.7 × V_{DD}, setting the device to speaker mode and the gain setting defaults to GAINA (MAX9760/MAX9762). When a headphone plug is inserted into the jack, the control pin is disconnected from the tip contact, and HPS is pulled to V_{DD} through R1, setting the device into headphone mode and the gain-setting defaults to GAINB (MAX9760/MAX9762) (see *Gain Select* section). Place a resistor in series with the control pin and HPS (R3) to prevent any audio signal from coupling into HPS when the device is in speaker mode.

Shutdown

The MAX9760–MAX9763 feature a 10µA, low-power shutdown mode that reduces quiescent current consumption and extends battery life. The drive amplifiers and bias circuitry are disabled, the amplifier outputs (OUT_) go high impedance, and BIAS is driven to

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

GND. Driving $\overline{SHDN}$ low places the devices into shutdown mode, disables the interface, and resets the I²C registers to a default state. A logic high on $\overline{SHDN}$ enables the devices.

MAX9760/MAX9762 Software Shutdown

A logic high on bit 0 of the SHDN register places the MAX9760/MAX9762 in shutdown mode. A logic low enables the device. The digital section of the MAX9760/MAX9762 remains active when the device is shut down through the interface. All devices feature a logic low on the $\overline{SHDN}$ input.

MUTE

All devices feature a mute mode. When the device is muted, the input is disconnected from the amplifiers. MUTE does not shut down the device.

MAX9760/MAX9762 MUTE

The MAX9760/MAX9762 MUTE mode is selected by writing to the MUTE register (see the *Command Byte Definitions* section). The left and right channels can be independently muted.

MAX9761/MAX9763 MUTE

The MAX9761/MAX9763 feature an active-high MUTE input that mutes both channels.

Click-and-Pop Suppression

The MAX9760–MAX9763 feature Maxim's comprehensive click-and-pop suppression. During startup and shutdown, the common-mode bias voltage of the amplifiers is slowly ramped to and from the DC bias point using an S-shaped waveform. In headphone mode, this waveform shapes the frequency spectrum, minimizing the amount of audible components present at the headphone. In speaker mode, the BTL amplifiers start up in the same fashion as in headphone mode. When entering shutdown, both amplifier outputs ramp to GND quickly and simultaneously. The MAX9760–MAX9763 can also be connected to a standby power source that ensures that the device undergoes its full shutdown cycle even after power has been removed.

Standby Power Supply (SV_{DD})

The MAX9760–MAX9763 feature a system that provides clickless power-down when power is inadvertently removed from the device. SV_{DD} is an **optional** secondary supply that powers the device through its shutdown cycle when V_{DD} is removed. During this cycle, the amplifier output DC level slowly ramps to GND, ensuring clickless power-down. If clickless power-down is required, connect SV_{DD} to either a secondary power supply that is always on, or connect a reservoir capacitor from SV_{DD} to GND. SV_{DD} does not need to be connected to either a secondary power supply or reservoir capacitor for normal device operation. If click-and-pop suppression during power-down is not required, connect SV_{DD} to V_{DD} directly.

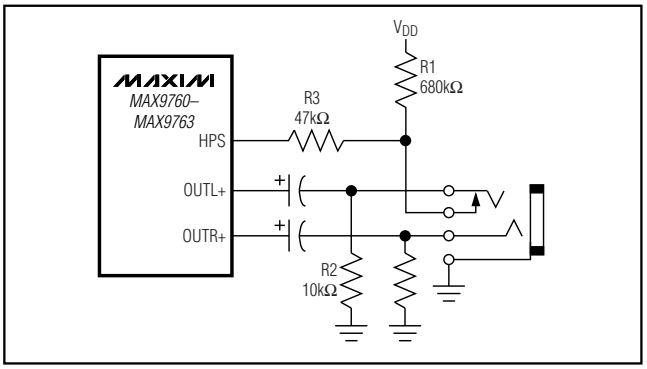


Figure 2. HPS Configuration Circuit

Table 1a. HPS Setting (MAX9760/MAX9761)

INPUTS			MODE	MAX9760 GAIN PATH*	MAX9762 GAIN PATH*
HPSD	HPS	SPKR/HP			
0	0	X	BTL	A	M
0	1	X	SE	B	B
1	X	0	BTL	A or B	M
1	X	1	SE	A or B	A or B

***Note:**

A – GAINA path selected

B – GAINB path selected

M – GAINM path selected

A or B – Gain path selected by GAINAB control bit in register 02h

Table 1b. HPS Setting (MAX9762/MAX9763)

INPUTS		MODE	MAX9761 GAIN PATH*	MAX9763 GAIN PATH*
HPSEN	HPS			
0	X	BTL	A or B	M
1	0	BTL	A or B	M
1	1	SE	A or B	A or B

***Note:**

A or B – Gain path selected by external GAINAB

M – GAINM path selected

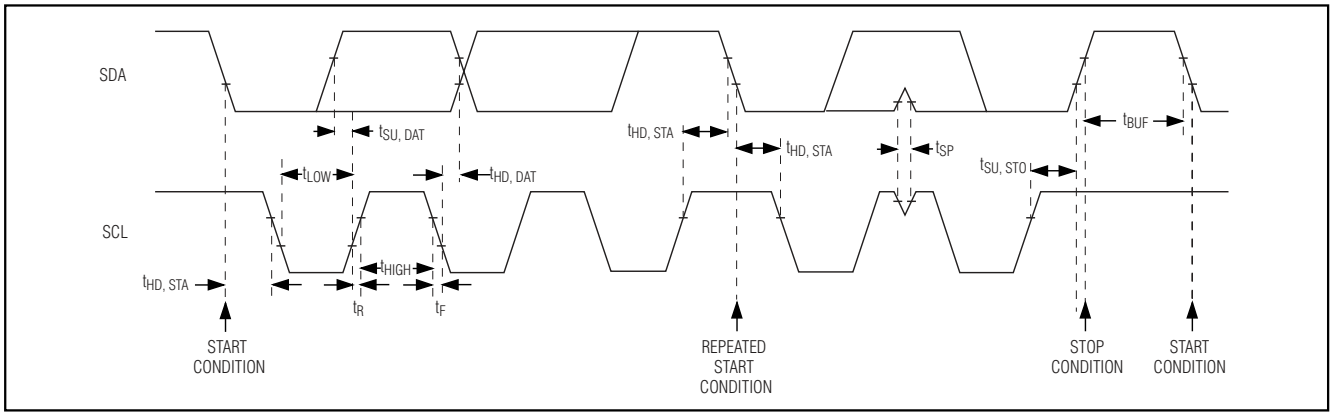


Figure 3. 2-Wire Serial Interface Timing Diagram

The clickless power-down cycle only occurs when the device is in headphone mode. The speaker mode is inherently clickless, the differential architecture cancels the DC shift across the speaker. The MAX9760–MAX9763 BTL outputs are pulled to GND quickly and simultaneously, resulting in no audible components. If the MAX9760–MAX9763 are only used as speaker amplifiers, then reservoir capacitors or secondary supplies are not necessary.

When using a reservoir capacitor, a 220µF capacitor provides optimum charge storage for the shutdown cycle for all conditions. If a smaller reservoir capacitor is desired, decrease the size of C_{BIAS}. A smaller C_{BIAS} causes the output DC level to decay at a faster rate, increasing the audible content at the speaker, but reducing the duration of the shutdown cycle.

Digital Interface

The MAX9760/MAX9762 feature an I²C/SMBus-compatible 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX9760/MAX9762 and the master at clock rates up to 400kHz. Figure 3 shows the 2-wire interface timing diagram. The MAX9760/MAX9762 are transmit/receive slave-only devices, relying upon a master to generate a clock signal. The master (typically a microcontroller) initiates data transfer on the bus and generates SCL to permit that transfer.

A master device communicates to the MAX9760/MAX9762 by transmitting the proper address followed by a command and/or data words. Each transmit sequence is framed by a START (S) or REPEATED START (S_r) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

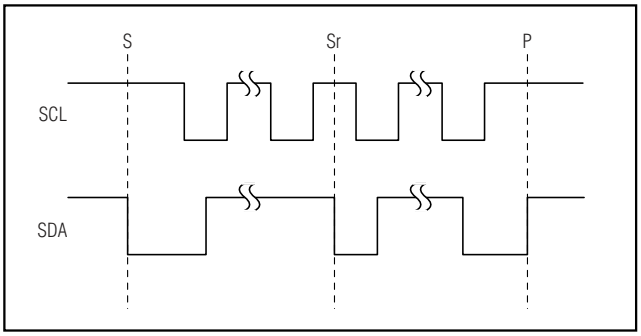


Figure 4. START/STOP Conditions

The MAX9760/MAX9762 SDA and SCL amplifiers are open-drain outputs requiring a pullup resistor (500Ω or greater) to generate a logic high voltage. Series resistors in line with SDA and SCL are optional. These series resistors protect the input stages of the devices from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals (see *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 4). A START condition from the master signals the beginning of a transmission to the MAX9760/

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

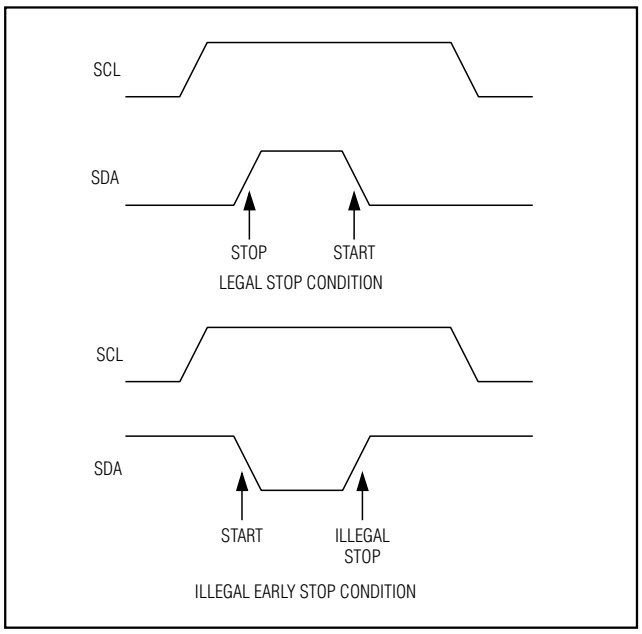


Figure 5. Early STOP Condition

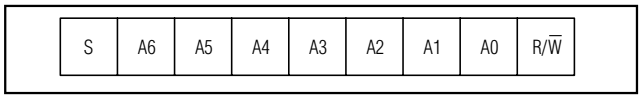


Figure 6. Slave Address Byte Definition

MAX9762. The master terminates transmission by issuing the STOP condition, this frees the bus. If a REPEATED START condition is generated instead of a STOP condition, the bus remains active.

Early STOP Conditions

The MAX9760/MAX9762 recognize a STOP condition at any point during the transmission except if a STOP condition occurs in the same high pulse as a START condition (Figure 5). This condition is not a legal I²C format, at least one clock pulse must separate any START and STOP conditions.

REPEATED START Conditions

A REPEATED START (S_r) condition may indicate a change of data direction on the bus. Such a change occurs when a command word is required to initiate a read operation. S_r may also be used when the bus master is writing to several I²C devices and does not want to relinquish control of the bus. The MAX9760/MAX9762 serial interface supports continuous write operations with or without an S_r condition separating them. Continuous read operations require S_r conditions because of the change in direction of data flow.

Acknowledge Bit (ACK)

The acknowledge bit (ACK) is the ninth bit attached to any 8-bit data word. The receiving device always generates ACK. The MAX9760/MAX9762 generate an ACK when receiving an address or data by pulling SDA low during the night clock period. When transmitting data, the MAX9760/MAX9762 wait for the receiving device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

The bus master initiates communication with a slave device by issuing a START condition followed by a 7-bit slave address (Figure 6). When idle, the MAX9760/MAX9762 wait for a START condition followed by its slave address. The LSB of the address word is the Read/$\overline{\text{Write}}$ (R/$\overline{W}$) bit. R/$\overline{W}$ indicates whether the master is writing to or reading from the MAX9760/MAX9762 (R/$\overline{W}$ = 0 selects the write condition, R/$\overline{W}$ = 1 selects the read condition). After receiving the proper address, the MAX9760/MAX9762 issue an ACK by pulling SDA low for one clock cycle.

The MAX9760/MAX9762 have a factory-/user-programmed address. Address bits A6–A2 are preset, while A0 and A1 is set by ADD. Connect ADD to either V_{DD}, GND, SCL, or SDA to change the last 2 bits of the slave address (Table 2).

Write Data Format

There are three registers that configure the MAX9760/MAX9762: the MUTE register, SHDN register, and control register. In write data mode (R/$\overline{W}$ = 0), the register address and data byte follow the device address (Figure 7).

MUTE Register

The MUTE register (01hex) is a read/write register that sets the MUTE status of the device. Bit 3 (MUTEL) of the MUTE register controls the left channel, bit 4 (MUTER) controls the right channel. A logic high mutes the respective channel, a logic low brings the channel out of mute.

SHDN Register

The SHDN register (02hex) is a read/write register that controls the power-up state of the device. A logic high in bit 0 of the SHDN register shuts down the device; a logic low turns on the device. A logic high is required in bits 2 to 7 to reset all registers to their default settings.

S	ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	P
	7 BITS			8 BITS		8 BITS		1
	I²C SLAVE ADDRESS. SELECTS DEVICE.			REGISTER ADDRESS. SELECTS REGISTER TO BE WRITTEN TO.		REGISTER DATA		

S	ADDRESS	WR	ACK	COMMAND	ACK	S	ADDRESS	WR	ACK	DATA	P
	7 BITS			8 BITS			7 BITS			8 BITS	1
	I²C SLAVE ADDRESS. SELECTS DEVICE.			REGISTER ADDRESS. SELECTS REGISTER TO BE READ.			I²C SLAVE ADDRESS. SELECTS DEVICE.			DATA FROM SELECTED REGISTER	

Figure 7. Write/Read Data Format Example

Table 2. I²C Slave Addresses

ADD CONNECTION	I²C ADDRESS
GND	100 1000
V_{DD}	100 1001
SDA	100 1010
SCL	100 1011

Table 3. MUTE Register Format

REGISTER ADDRESS		0000 0001	
BIT	**NAME**	**VALUE**	**DESCRIPTION**
7	X	Don't Care	—
6	X	Don't Care	—
5	X	Don't Care	—
4	MUTER	0*	Unmute right channel
		1	Mute right channel
3	MUTEL	0*	Unmute left channel
		1	Mute left channel
2	X	Don't Care	—
1	X	Don't Care	—
0	X	Don't Care	—

**Default state.*

Control Register

The control register (03hex) is a read/write register that determines the device configuration. Bit 1 (IN1/IN2) controls the input multiplexer, a logic high selects input 1, a logic low selects input 2. Bit 2 (HPS_D) controls the headphone sensing. A logic low configures the device in automatic headphone detection mode. A logic high disables the HPS input. Bit 3 (GAINA/B) controls the gain-select multiplexer. A logic low selects GAINA. A logic high selects GAINB. GAINA/B is ignored when HPS_D = 0. Bit 4 (SPKR/HP) selects the amplifier operating mode when HPS_D = 1. A logic high selects speaker mode and a logic low selects headphone mode.

Table 4. SHDN Register Format

REGISTER ADDRESS		0000 0010	
BIT	**NAME**	**VALUE**	**DESCRIPTION**
7	RESET	0*	—
		1	Reset device
6	RESET	0*	—
		1	Reset device
5	RESET	0*	—
		1	Reset device
4	RESET	0*	—
		1	Reset device
3	RESET	0*	—
		1	Reset device
2	RESET	0*	—
		1	Reset device
1	X	Don't Care	—
0	SHDN	0*	Normal operation
		1	Shutdown

**Default state.*

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Table 5. Control Register Format

REGISTER ADDRESS		0000 0011	
BIT	**NAME**	**VALUE**	**DESCRIPTION**
7	X	Don't Care	—
6	X	Don't Care	—
5	X	Don't Care	—
4	SPKR/HP	0*	Speaker mode selected
		1	Headphone mode selected
3	GAINA/B	0*	Gain-setting A selected
		1	Gain-setting B selected
2	HPS_D	0*	Automatic headphone detection enabled
		1	Automatic headphone detection disabled (HPS ignored).
1	IN1/IN2	0*	Input 1 selected
		1	Input 2 selected
0	X	Don't Care	—

Read Data Format

In read mode (R/$\overline{W}$ = 1), the MAX9760/MAX9762 write the contents of the selected register to the bus. The direction of the data flow reverses following the address acknowledge by the MAX9760/MAX9761. The master device reads the contents of all registers, including the read-only status register. Table 6 shows the status register format.

Interrupt Output ($\overline{INT}$)

The MAX9760/MAX9762 include an interrupt output ($\overline{INT}$) that can indicate to a master device that an event has occurred. $\overline{INT}$ is triggered when the state of HPS changes. During normal operation, $\overline{INT}$ idles high. If a headphone is inserted/removed from the jack and that action is detected by HPS, $\overline{INT}$ pulls the line low. $\overline{INT}$ remains low until a read data operation is executed.

I²C Compatibility

The MAX9760/MAX9762 are compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain that pulls the data line low during the ninth clock pulse. The communication protocol supports the standard I²C 8-bit communications. The general call address is ignored. The MAX9760/MAX9762 addresses are compatible with the 7-bit I²C addressing protocol only. No 10-bit formats are supported.

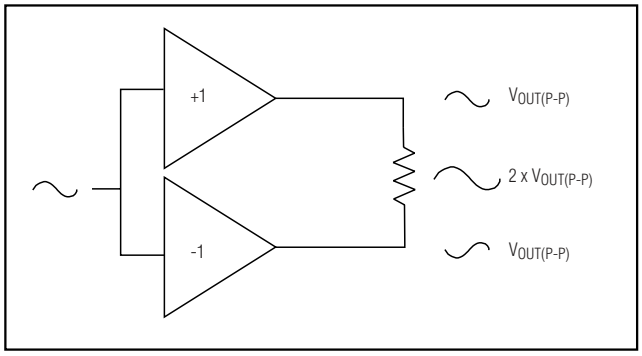


Figure 8. Bridge-Tied Load Configuration

Applications Information

BTL Speaker Amplifiers

The MAX9760–MAX9763 feature speaker amplifiers designed to drive a load differentially, a configuration referred to as bridge-tied load (BTL). The BTL configuration (Figure 8) offers advantages over the single-ended configuration, where one side of the load is connected to ground. Driving the load differentially doubles the output voltage compared to a single-ended amplifier under similar conditions. Thus, the devices' differential gain is twice the closed-loop gain of the input amplifier. The effective gain is given by:

$$A_{VD} = 2 \times \frac{R_F}{R_{IN}}$$

Substituting 2 x $V_{OUT(P-P)}$ for $V_{OUT(P-P)}$ into the following equations yields four times the output power due to doubling of the output voltage:

$$V_{RMS} = \frac{V_{OUT(P-P)}}{2\sqrt{2}}$$

$$P_{OUT} = \frac{V_{RMS}^2}{R_L}$$

Since the differential outputs are biased at midsupply, there is no net DC voltage across the load. This eliminates the need for DC-blocking capacitors required for single-ended amplifiers. These capacitors can be large, expensive, consume board space, and degrade low-frequency performance.

Table 6. Status Register Format

REGISTER ADDRESS		0000 0000	
BIT	**NAME**	**VALUE**	**DESCRIPTION**
7	THRM	0	Device temperature below thermal limit
		1	Device temperature exceeding thermal limit
6	AMPR-	0	OUTR- current below current limit
		1	OUTR- current exceeding current limit
5	AMPR+	0	OUTR+ current below current limit
		1	OUTR+ current exceeding current limit
4	AMPL-	0	OUTL- current below current limit
		1	OUTL- current exceeding current limit
3	AMPL+	0	OUTL+ current below current limit
		1	OUTL+ current exceeding current limit
2	HPSTS	0	Device in speaker mode
		1	Device in headphone mode
1	X	Don't Care	—
0	X	Don't Care	—

When the MAX9760/MAX9762 are configured to automatically detect the presence of a headphone jack, the device defaults to gain setting A when the device is in speaker mode. When the MAX9762/MAX9763 are configured as speaker amplifiers, the gain setting defaults to the mono setting (GAINM).

Single-Ended Headphone Amplifier

The MAX9760–MAX9763 can be configured as single-ended headphone amplifiers through software or by sensing the presence of a headphone plug (HPS). In headphone mode, the inverting output of the BTL amplifier is disabled, muting the speaker. The gain is 1/2 that of the device in speaker mode, and the output power is reduced by a factor of 4.

In headphone mode, the load must be capacitively coupled to the device, blocking the DC bias voltage from the load (see *Typical Application Circuit).*

Power Dissipation and Heat Sinking

Under normal operating conditions, the MAX9760–MAX9763 can dissipate a significant amount of power. The maximum power dissipation for each package is given in the *Absolute Maximum Ratings* section under Continuous Power Dissipation or can be calculated by the following equation:

$$P_{DISSPKG(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is +150°C, T_A is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in °C/W as specified in the *Absolute Maximum Ratings* section. For example, θ_{JA} of the QFN package is +42°C/W.

The increase in power delivered by the BTL configuration directly results in an increase in internal power dissipation over the single-ended configuration. The maximum power dissipation for a given V_{DD} and load is given by the following equation:

$$P_{DISS(MAX)} = \frac{2V_{DD}^2}{\pi^2 R_L}$$

If the power dissipation for a given application exceeds the maximum allowed for a given package, either reduce V_{DD}, increase load impedance, decrease the ambient temperature, or add heat sinking to the device. Large output, supply, and ground PC board traces improve the maximum power dissipation in the package.

Thermal overload protection limits total power dissipation in these devices. When the junction temperature exceeds +160°C, the thermal protection circuitry disables the amplifier output stage. The amplifiers are enabled once the junction temperature cools by 15°C. This results in a pulsing output under continuous thermal-overload conditions as the device heats and cools.

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Component Selection

Gain-Setting Resistors

External feedback components set the gain of the MAX9760–MAX9763. Resistor R_{IN} sets the gain of the input amplifier (A_{VIN}) and resistor R_F sets the gain of the second stage amplifier (A_{VOUT}):

$$A_{VIN} = -\left(\frac{10k\Omega}{R_{IN}}\right),\ A_{VOUT} = -\left(\frac{R_F}{10k\Omega}\right)$$

Combining A_{VIN} and A_{VOUT}, R_{IN} and R_F set the single-ended gain of the device as follows:

$$A_V = A_{VIN} \times A_{VOUT} = -\left(\frac{10k\Omega}{R_{IN}}\right) \times -\left(\frac{R_F}{10k\Omega}\right) = +\left(\frac{R_F}{R_{IN}}\right)$$

As shown, the two-stage amplifier architecture results in a noninverting gain configuration, preserving absolute phase through the MAX9760–MAX9763. The gain of the device in BTL mode is twice that of the single-ended mode. Choose R_{IN} between 10kΩ and 15kΩ and R_F between 15kΩ and 100kΩ.

Input Filter

The input capacitor (C_{IN}), in conjunction with R_{IN}, forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose R_{IN} according to the *Gain-Setting Resistors* section. Choose the C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the amplifier's low-frequency response. Use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in an increased distortion at low frequencies.

Other considerations when designing the input filter include the constraints of the overall system, the actual frequency band of interest, and click-and-pop suppression.

Output-Coupling Capacitor

The MAX9760/MAX9763 require output-coupling capacitors to operate in single-ended (headphone) mode. The output-coupling capacitor blocks the DC component of the amplifier output, preventing DC current from flowing to the load. The output capacitor and the load impedance form a highpass filter with a -3dB point determined by:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}}$$

As with the input capacitor, choose C_{OUT} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the amplifier's low-frequency response.

Load impedance is a concern when choosing C_{OUT}. Load impedance can vary, changing the -3dB point of the output filter. A lower impedance increases the corner frequency, degrading low-frequency response. Select C_{OUT} such that the worst-case load/C_{OUT} combination yields an adequate response. Select capacitors with low ESR to minimize resistive losses and optimize power transfer to the load.

BIAS Capacitor

BIAS is the output of the internally generated 2.5VDC bias voltage. The BIAS bypass capacitor, C_{BIAS}, improves PSRR and THD+N by reducing power supply and other noise sources at the common-mode bias node, and also generates the clickless/popless, start-up/shutdown DC bias waveforms for the speaker amplifiers. Bypass BIAS with a 1µF capacitor to GND.

Supply Bypassing

Proper power-supply bypassing ensures low-noise, low-distortion performance. Place a 0.1µF ceramic capacitor from V_{DD} to GND. Add additional bulk capacitance as required by the application, typically 100µF. Bypass PV_{DD} with a 100µF capacitor to GND. Locate bypass capacitors as close to the device as possible.

Gain Select

The MAX9760–MAX9763 feature multiple gain settings on each channel, making available different gain and feedback configurations. The gain-setting resistor (R_F) is connected between the amplifier output (OUT_+) and the gain setpoint (GAIN_). An internal multiplexer switches between the different feedback resistors

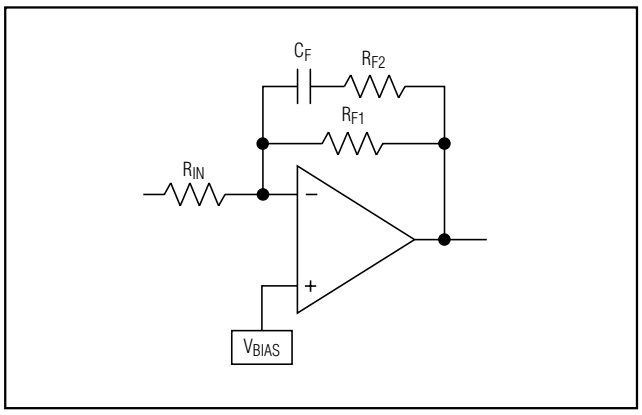


Figure 9. Bass Boost Circuit

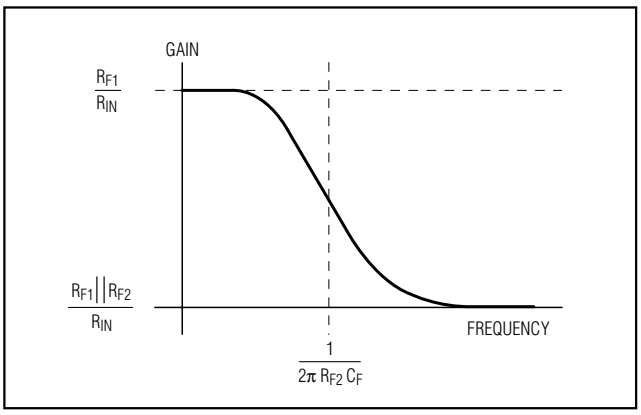


Figure 10. Bass Boost Response

depending on the status of the gain control input. The stereo MAX9760/MAX9761 feature two gain options per channel. The mono MAX9762/MAX9763 feature two gain options per single-ended channel, and a single gain option for the mono speaker amplifier (see Tables 1a and 1b for the gain-setting options).

The MAX9762 defaults to GAINM in speaker mode and can switch between GAINA and GAINB in headphone mode.

Bass Boost Circuit

Headphones typically have a poor low-frequency response due to speaker and enclosure size limitations. A bass boost circuit compensates the poor low-frequency response (Figure 9). At low frequencies, the capacitor C_F is an open circuit, and the effective impedance in the feedback loop ($R_{F(EFF)}$) is $R_{F(EFF)} = R_{F1}$.

At the frequency:

$$\frac{1}{2\pi R_{F2} C_F}$$

where the impedance, C_F, begins to decrease, and at high frequencies, the C_F is a short circuit. Here the impedance of the feedback loop is:

$$R_{F(EFF)} = \frac{R_{F1} \times R_{F2}}{R_{F1} + R_{F2}}$$

Assuming $R_{F1} = R_{F2}$, then $R_{F(EFF)}$ at low frequencies is twice that of $R_{F(EFF)}$ at high frequencies (Figure 10). Thus, the amplifier has more gain at lower frequencies, boosting the system's bass response. Set the gain roll-off frequency based upon the response of the speaker and enclosure.

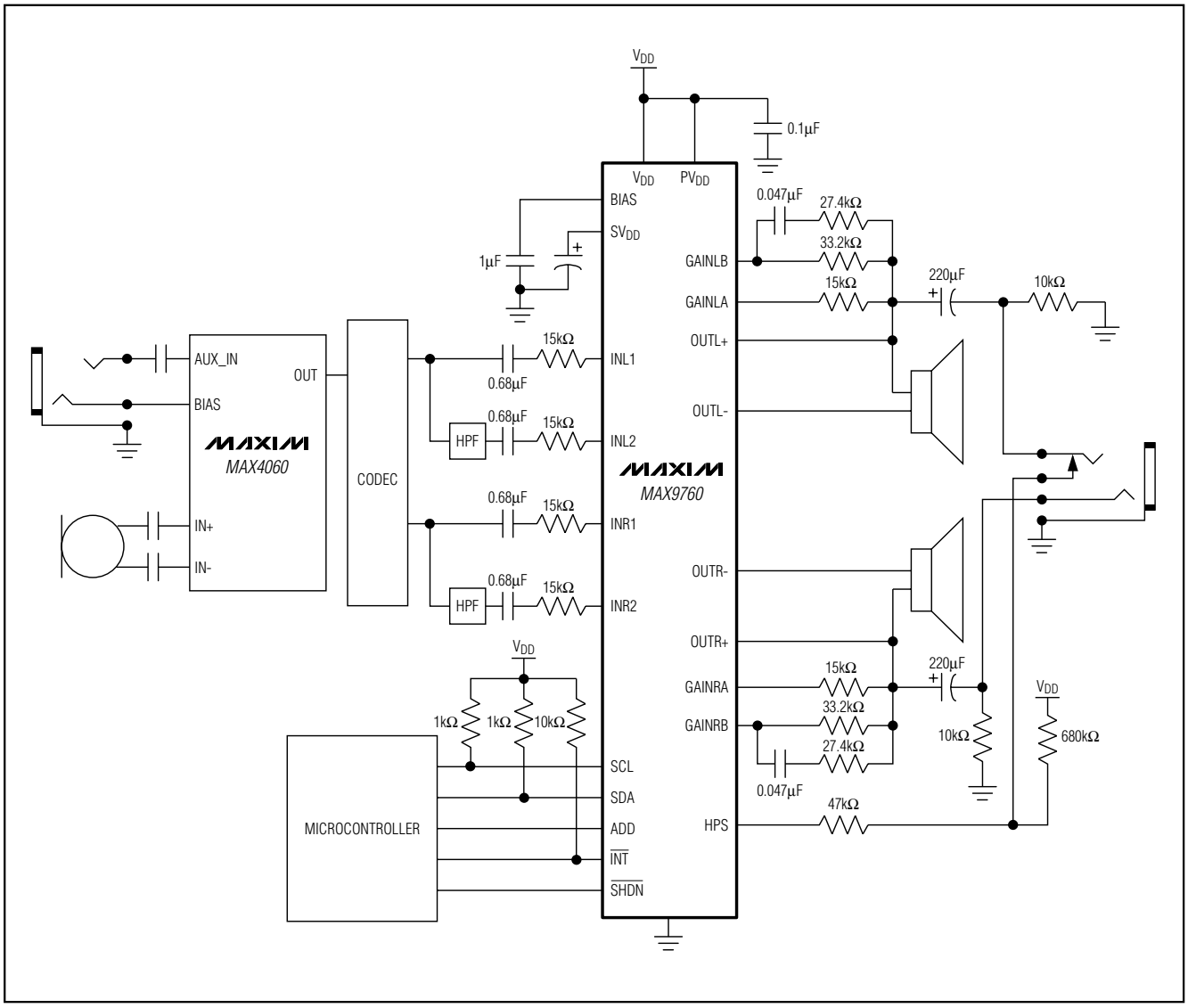
Layout and Grounding

Good PC board layout is essential for optimizing performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance, as well as route heat away from the device. Good grounding improves audio performance, minimizes crosstalk between channels, and prevents any digital switching noise from coupling into the audio signal. If digital signal lines must cross over or under audio signal lines, ensure that they cross perpendicular to each other.

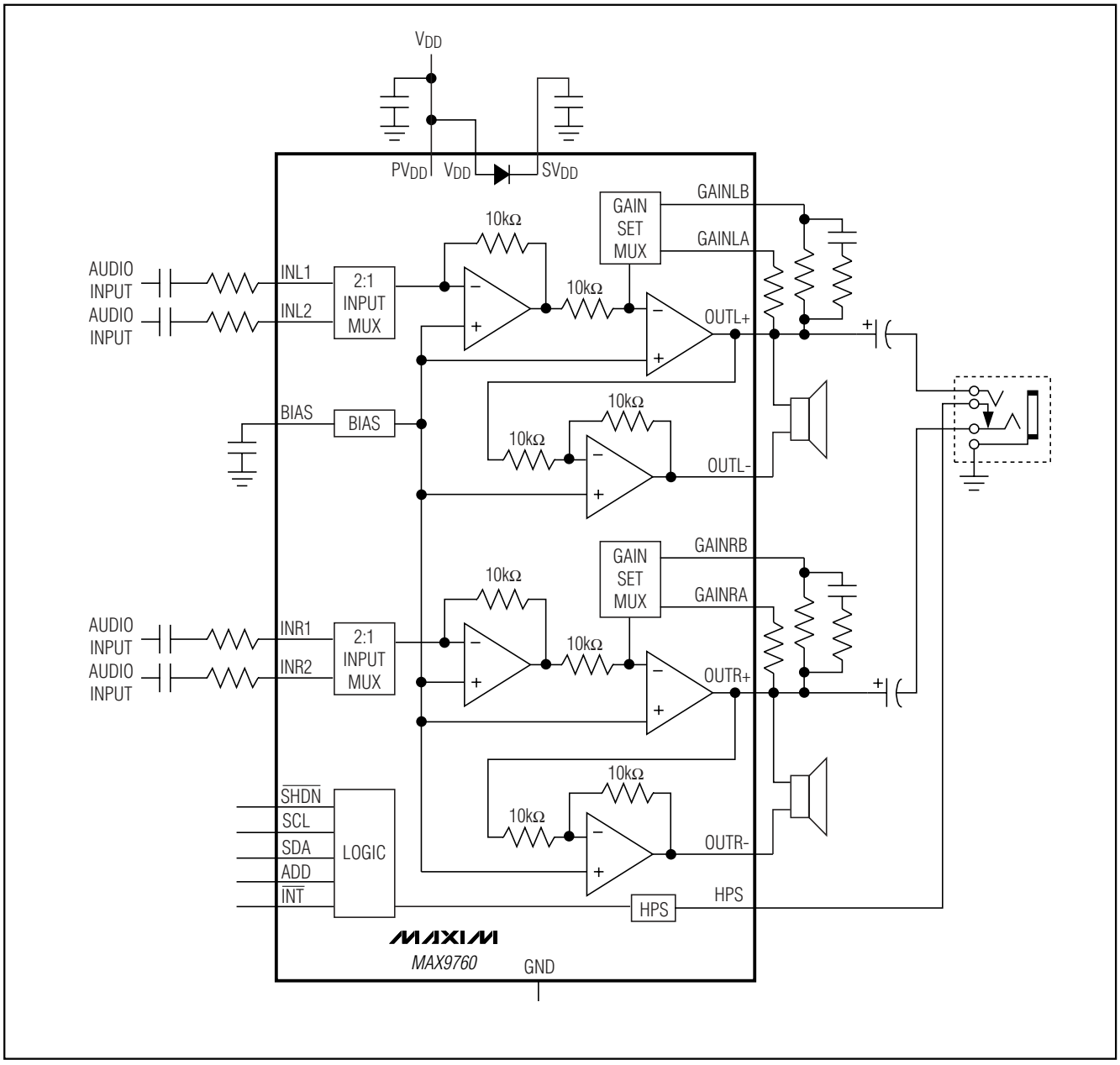
The MAX9760–MAX9763 QFN and TSSOP-EP packages feature exposed thermal pads on their undersides. This pad lowers the package's thermal resistance by providing a direct heat conduction path from the die to the printed circuit board. Connect the pad to signal ground by using a large pad, or multiple vias to the ground plane.

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Typical Application Circuit

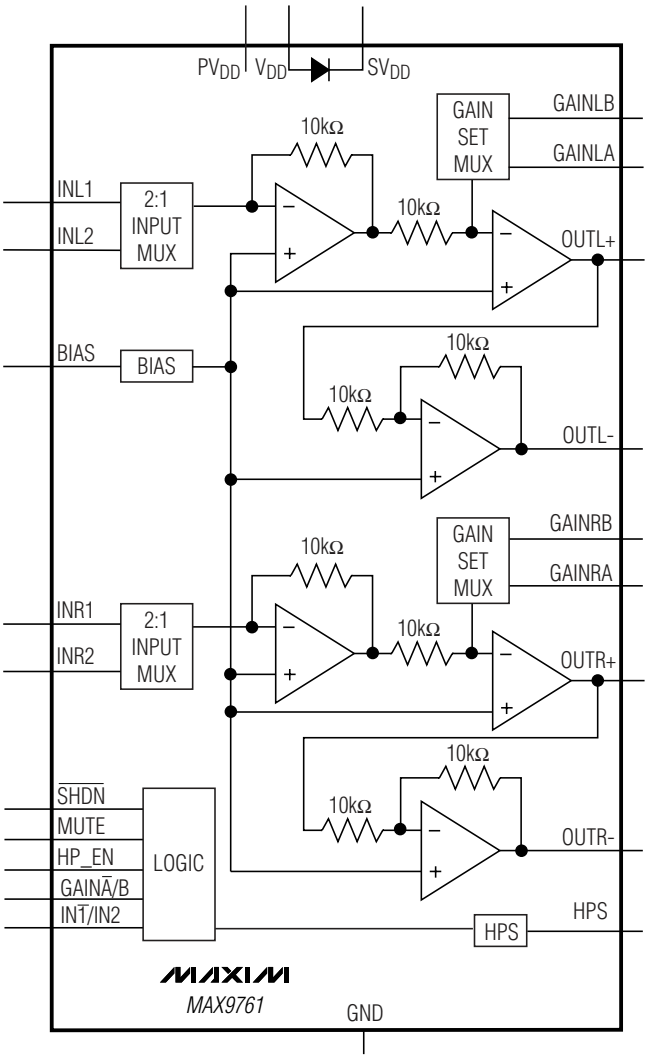


Functional Diagrams

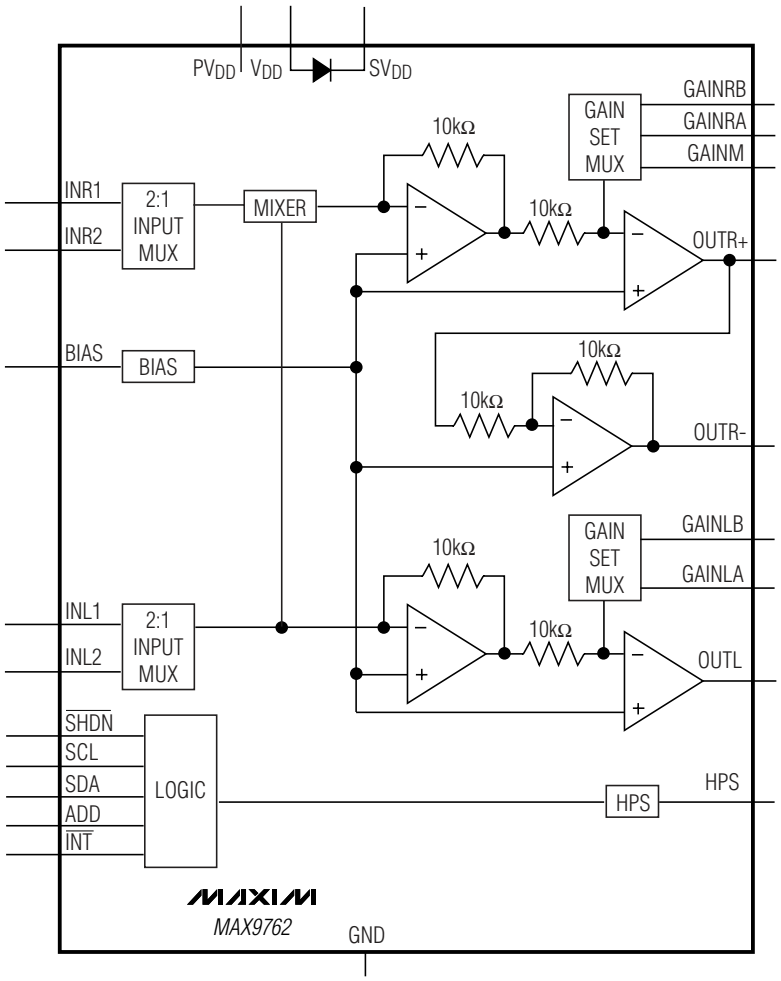


Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Functional Diagrams (continued)

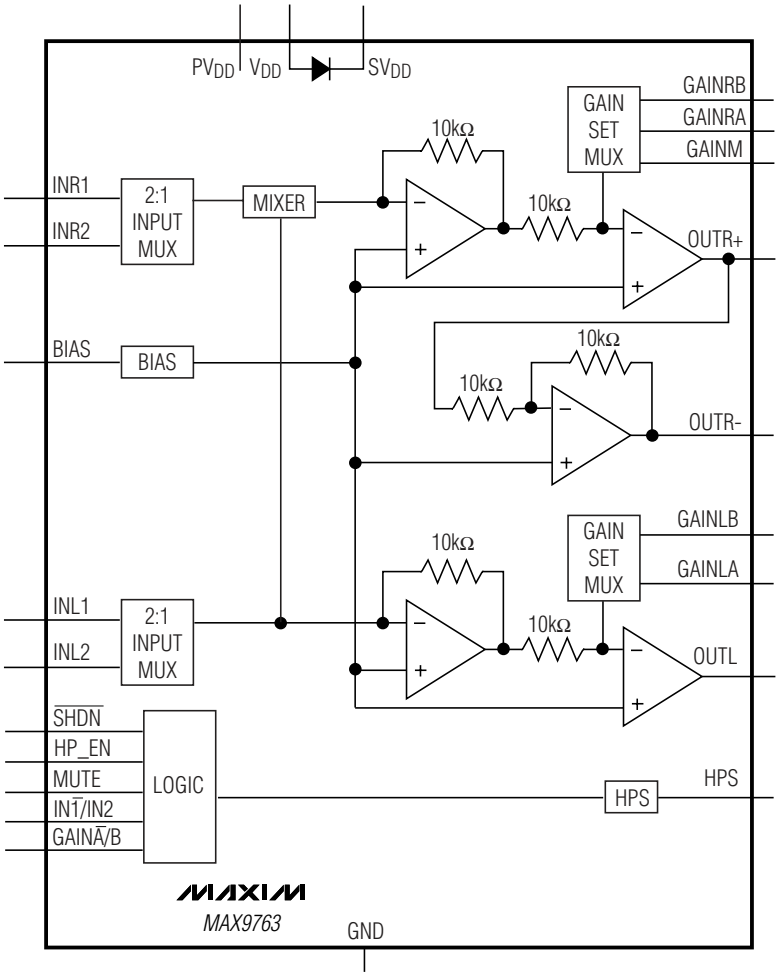


Functional Diagrams (continued)

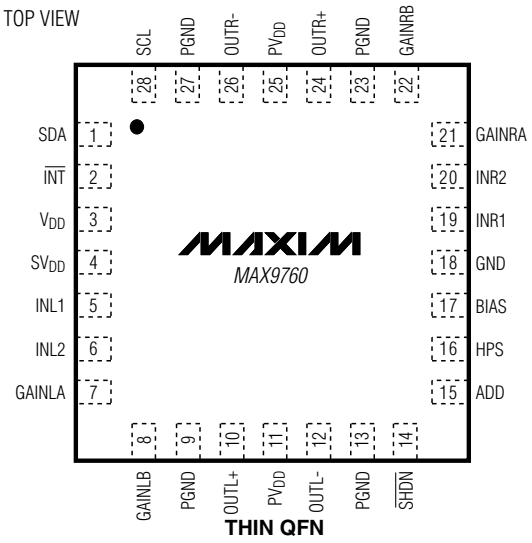


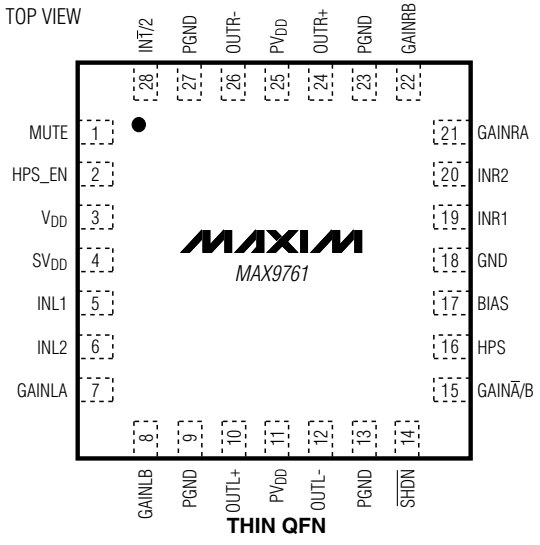
Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

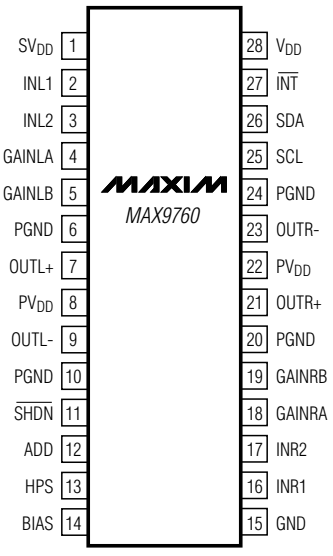
Functional Diagrams (continued)

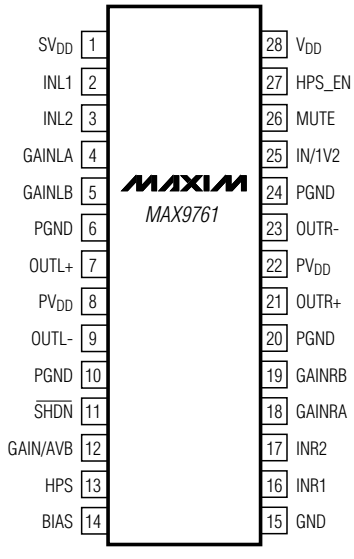


Pin Configurations



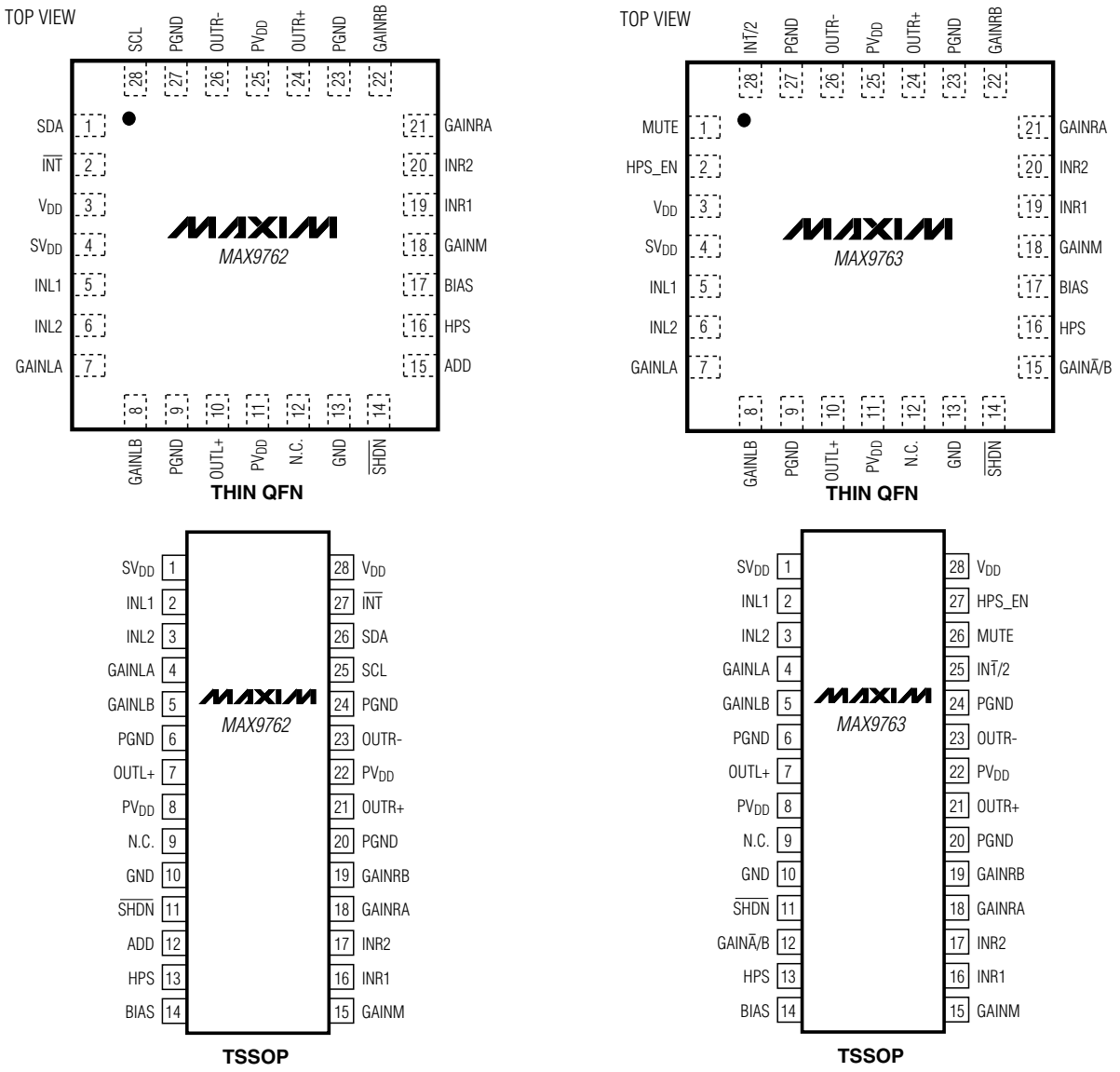






Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Pin Configurations (continued)



Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX9761ETI	-40°C to +85°C	28 Thin QFN-EP*
MAX9761EUI	-40°C to +85°C	28 TSSOP-EP*
MAX9762ETI	-40°C to +85°C	28 Thin QFN-EP*
MAX9762EUI	-40°C to +85°C	28 TSSOP-EP*
MAX9763ETI	-40°C to +85°C	28 Thin QFN-EP*
MAX9763EUI	-40°C to +85°C	28 TSSOP-EP*

**EP = Exposed paddle.*

Chip Information

MAX9760 TRANSISTOR COUNT: 5256
MAX9761 TRANSISTOR COUNT: 2715
MAX9762 TRANSISTOR COUNT: 5046
MAX9763 TRANSISTOR COUNT: 2505
PROCESS: BiCMOS

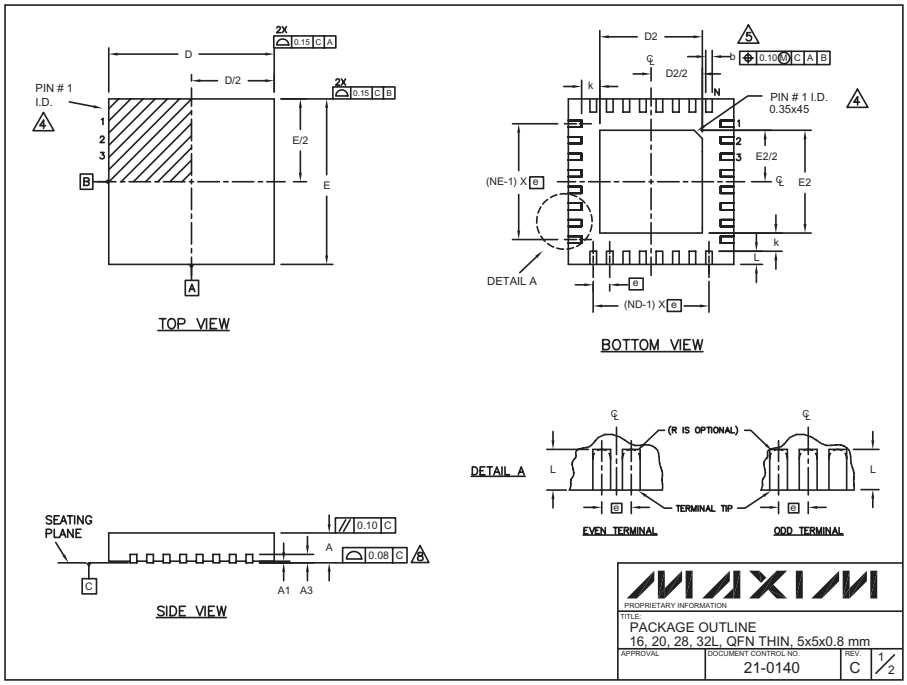
Selector Guide

PART	CONTROL INTERFACE	SPEAKER AMPLIFIER	HEADPHONE AMPLIFIER	INPUT MUX
MAX9760	I^2C Compatible	Stereo	Stereo	Yes
MAX9761	Parallel	Stereo	Stereo	Yes
MAX9762	I^2C Compatible	Mono	Stereo	Yes
MAX9763	Parallel	Mono	Stereo	Yes

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS												
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

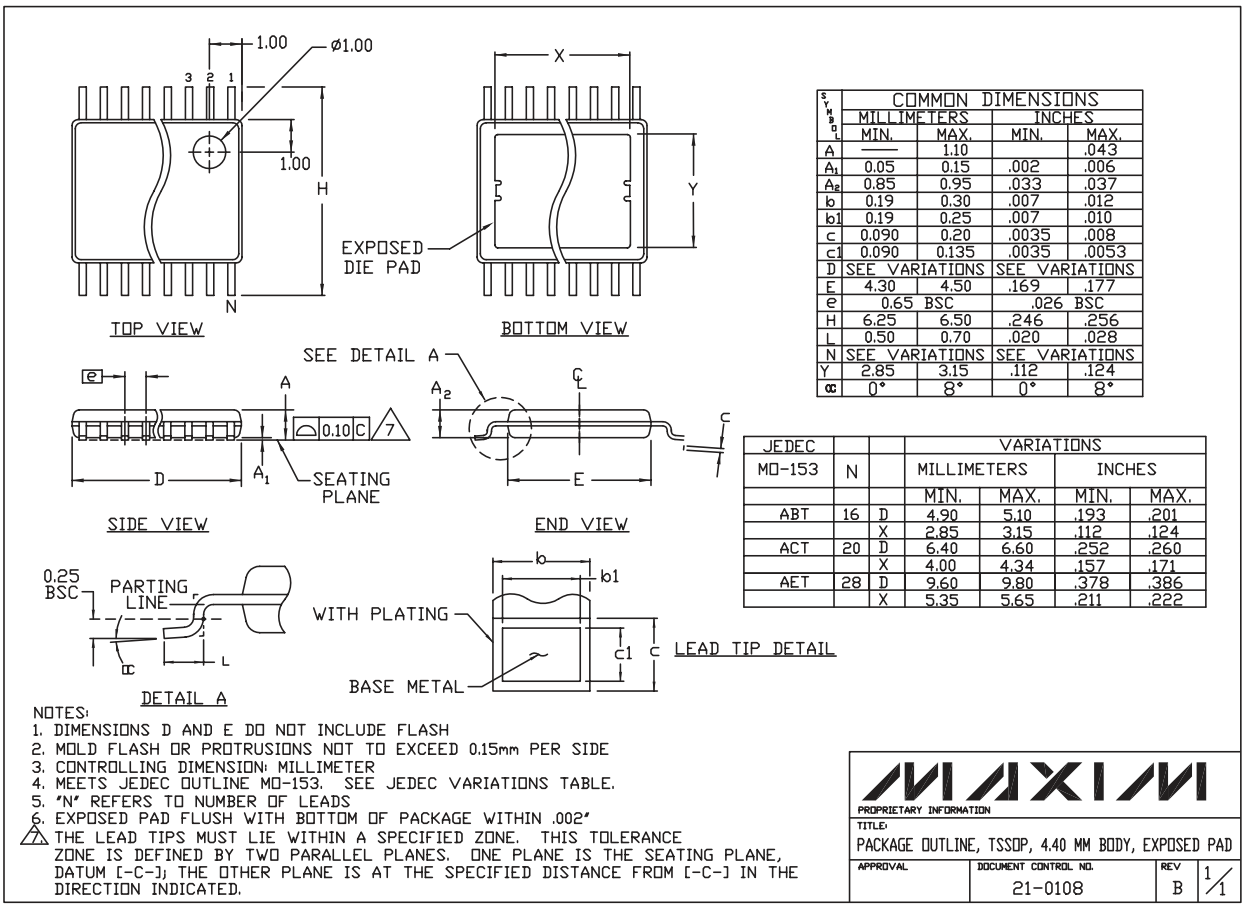
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE
16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm
APPROVAL
DOCUMENT CONTROL NO.
21-0140
REV.
C
2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP, 4.0,EXP PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
ACT	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AET	28	D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002"
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-], THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0108	B	1/1