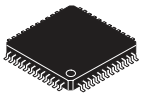


SLUS565F − JULY 2003 − REVISED DECEMBER 2004

OCTAL POWER SOURCING EQUIPMENT POWER MANAGER

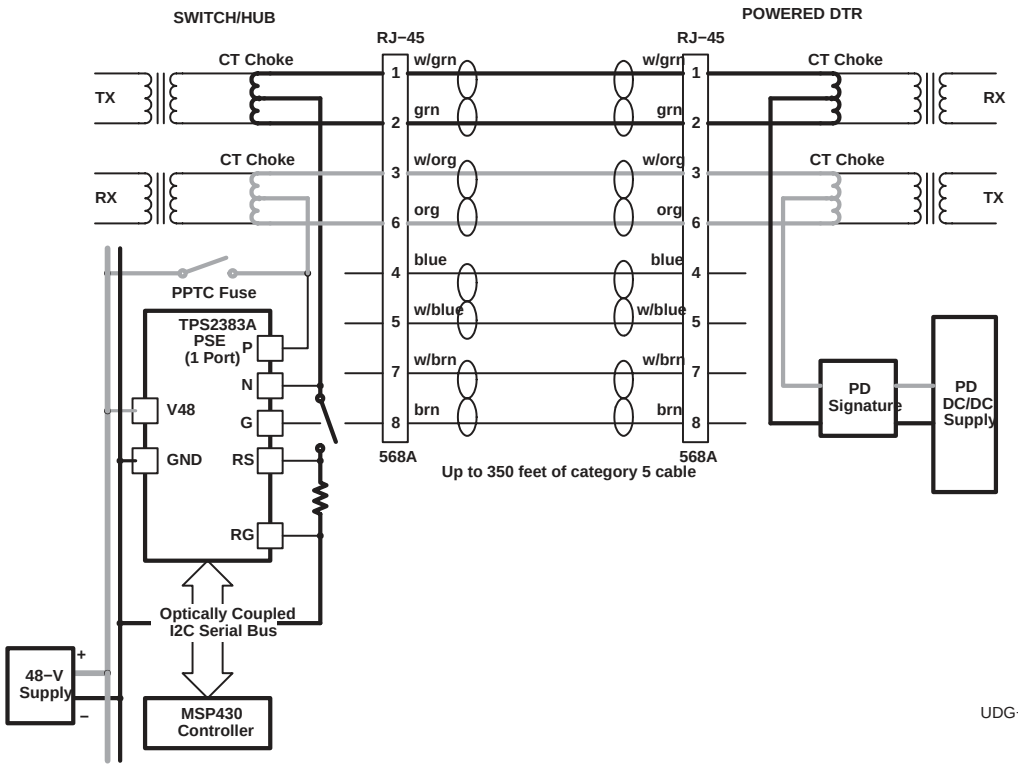
FEATURES

- Compliant to Power Over Ethernet IEEE 802.3af Standard
- Two-Point 25-kΩ Resistor Discovery
- Capacitive Detection for Non-Compliant Legacy Loads
- Power Classification
- Controlled di/dt Ramp Power-Up and Power-Down for EMI Reduction
- Current Management for Charging Powered Device Bulk Capacitance
- Electronic Circuit Breaker
- Fault detection
- Input Undervoltage Lockout (UVLO)
- Load Overcurrent and Undercurrent Detection
- 12-Bit Port Current and Voltage Acquisition
- Standard Slave I^2C Serial Interface
- 5-Bit Serial Address Selectability
- Discovery and/or Classification Bypass Modes Selectable Via Register
- Opto-Coupler Compatible SDA and SCL Lines for System Ground Isolation
- Dual Color LED Driver for Port Status
- Hardware FAULT Interrupt

APPLICATIONS

- PoE Switches
- Mid-Span Injectors

APPLICATION DIAGRAM



DESCRIPTION

The TPS2383A and TPS2383B family of products are power sourcing equipment power managers (PSEPM) that are compliant to the power-over-ethernet (PoE) IEEE 802.3af Standard. The TPS2383A and the TPS2383B are pin-for-pin functionally equivalent products. A PSEPM port can discover, classify and deliver power to a powered device (PD) capable of accepting PoE twisted pair cable. The TPS2383A/B is fully programmable by the user. This allows for the detection and powering of both fully compliant 802.3 devices as well as custom detection of legacy devices.

The TPS2383A/B PSEPM can individually manage power for up to eight ethernet ports. All operations of the TPS2383A/B are controlled through register read and write operations over a standard (slave) I^2C serial interface. The TPS2383A/B has dual SDA lines to allow easy application of opto-coupler circuitry to maintain ethernet port isolation when a ground based controller is used. Each TPS2383A/B has five selection pins making it possible to address up to 32 devices on the I^2C bus and allows individual control and monitoring of up to 256 ethernet ports from a single master I^2C controller. Per-port write registers initiate and manipulate the flow of the discovery, classification, and power-up states while the read registers contain status information of the enable process, faults, classification value, and real time port operating current and voltage. Per-port status LED drivers are provided which can be manually controlled through the serial I/O.

The TPS2383A/B is available in a full function 64-pin LQFP.

External N-channel MOSFETs switch port power. High-voltage (HV) gate drive ensures that these FETs are fully enhanced, resulting in lower power dissipation and enabling the use of lower costs FETs. The TPS2383A/B generates its HV gate supply from the 48-V port power, simplifying system power supply design. An external 3.3-V digital supply is also used. This supply can be active when 48-V power is not present which allows the user to access the part through the serial I/O in this case. A 5-V analog supply is used to power port LEDs and internal analog functions. Due to the very low quiescent current, both the 3.3-V and 5-V supply can be generated from the 48-V power bus with minimal external components. An internal power-on-reset (POR) circuit with an ORed external input pin resets all registers positions to a known safe state upon power up.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TPS2383A/B	UNIT
Input voltage range, V_{CC}	V48, 1P, 2P, 3P, 4P, 5P, 6P, 7P, 8P, 1N, 2N, 3N, 4N, 5N, 6N, 7N, 8N	−0.5 to 80	V
	1RS, 2RS, 3RS, 4RS, 5RS, 6RS, 7RS, 8RS, 1G, 2G, 3G, 4G, 5G, 6G, 7G, 8G, V10	−0.5 to 12	
	VL	−0.5 to 3.9	
	V5	−0.5 to 6	
	SCL_I, SDA_I, SDA_O, INTB, A1, A2, A3, A4, A5, EN, PORB	−0.5 to 6	
Storage temperature, T_{stg}		−55 to 150	°C
Operating temperature, T_J		−40 to 125	
Lead temperature, $T_{sol,}$ 1,6 mm (1/16 inch) from case for 10 seconds		260	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into and negative out of, the specified terminal.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, V_{V48}	44	48	57	V
Operating ambient temperature, T_a	−40		85	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MAX	UNIT
Human body model	1.5	kV
CDM	1	
Machine model	0.2	

ORDERING INFORMATION

T_A	PACKAGED DEVICES(2)
	LQFP−64 (PM)
−40°C to 85°C	TPS2383APM
	TPS2383BPM

(2) The PM package is available taped and reeled. Add R suffix to device type (e.g.TPS2383APMR) to order quantities of 2,500 devices per reel.

OPERATING TEMPERATURE RANGE

PACKAGE	θ_{jc}	θ_{ja}	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
LQFD−64	9°C/W	65°C/W	1.5 W	15.4 mW/°C	615 mW0000000000000000

ELECTRICAL CHARACTERISTICS

V_{V48}= 48 V, R_T = 120 kΩ, –40°C to 85°C, and $T_A = T_J$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES					
Quiescent current, V48	Off mode (all ports)		3	5	mA
	Powered mode (all ports)		5	10	
Quiescent current, V5	Powered mode (all ports), V_{V5} = 5 V		3	15	
Quiescent current, VL	Powered mode (all ports), V_{VL} = 3.3 V		0.28	4	
Internal analog supply, V10		9.75	10.50	11.50	V
Internal reference(1)		2.475	2.500	2.525	
Input UVLO			30	38	
Internal POR timeout (I^2C)	After all supplies are good (8 CLK periods)		8		CLKs
Internal POR timeout (state machine)	After all supplies are good (65536 CLK periods)		65536		
LED OUTPUTS					
High-level output voltage, L1 through L8	I_{SRC} = 5 mA	4			V
Low-level output voltage, L1 through L8	I_{SINK} = 5 mA			0.75	
Tri−state leakage(1)			0.1		µA
ANALOG CIRCUITS − PORT VOLTAGE CONTROL LOOP					
Input resistance, *n*P to *n*N		480	800	1280	kΩ
Classification voltage	A/B select = B	15.5	17.5	20.5	V
Discovery voltage, high		7.5	8.8	9.5	
Discovery voltage, low		3.5	4.4	5.5	
Loop power supply feedthru loop control range C(1)			1.5		mV
Discovery short-circuit current				3	mA
Port output, undervoltage		40	42	44	V
Port output, overvoltage		56.0	59.5	63.0	
Classification current limit	ClassLimit1 = 0, ClassLimit2 = 0		160		mA
	ClassLimit1 = 1, ClassLimit2 = 0		80		
	ClassLimit1 = 0, ClassLimit2 = 1		40		
	ClassLimit1 = 1, ClassLimit2 = 1		20		
N-CHANNEL MOSFET GATE CONTROL					
Gate turn-off MOSFET $R_{DS(on)}$			200		Ω
Maximum gate voltage		8	10	12	V
Gate turn-off timer from UV/OV fault	After port enabled and ramped up, (1024 CLK periods)		1024		CLKs
UV/OV spike timer, power quality warning(1)	(256 CLK periods)		256		
Gate turn-off timer from overload fault	(32768 CLK periods)		32768		

NOTE: (1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS

V_{V48}= 48 V, R_T = 120 kΩ, –40°C to 85°C, and $T_A = T_J$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW-SIDE CURRENT-SENSE					
Overload threshold voltage		175	187	200	mV
Current limit threshold voltage		200	213	225	
Maximum swing, CINT		9		11	V
Reset voltage, CINT			10	100	mV
Internal pull-up current, CINT	V_{CINT} < 1.25 V, A/D inputs = −100 mV		850		nA
Maximum swing, CR			4.5	6.0	V
Input leakage, *n*RS			10		µA
ANALOG-TO-DIGITAL CONVERTER					
A/D resistive scaling(1)	R_{RD} = 1 kΩ		72		count/kΩ
Port-to-port resistance variation	Referenced to port #1	−5%	0%	5%	
A/D classificatin scaling(1)	R_{RS} = 0.5 Ω		35		count/mA
A/D load current scaling(1)	R_{RS} = 0.5 Ω		4.72		
A/D load voltage scaling(1)			33.6		count/V
A/D load current conversion	I_{LOAD} = 50 mA, R_{RS} = 0.5 Ω		236		count
	I_{LOAD} = 300 mA, R_{RS} = 0.5 Ω		1416		
A/D port voltage conversion	V_{PORT} = 5 V		168		
	V_{PORT} = 45 V		1512		
DIGITAL I/O					
Logic input threshold voltage, SCL, SDA_I, A1 through A5, EN, PORB			1.5		V
Input hysteresis, SCL, SDA_I			250		mV
Input hysteresis, EN, PORB			150		
Input pull-down resistance, EN, PORB			50		kΩ
Pull-up current, A0, A1, A2, A3, A4, A5			10	25	µA
Logic high leakage, SDA_O	Drain = 6 V		10		
Logic low output voltage, SDA_O	I_{SINK} = 3 mA		200		mV
Logic high leakage, INTB	Drain = 6 V		10		µA
Logic low output voltage, INTB	I_{SINK} = 3 mA		200		mV
DIGITAL I/O TIMING I^2C CHARACTERISTICS					
Clock frequency, SCL		0		400	kHz
Pulse duration	SCL high	1.3			µs
	SCL low	0.6			
Rise time, SCL, SDA(1)				300	ns
Fall time, SCL, SDA(1)				300	
Setup time SDA to SCL		250			
Hold time SCL to SDA		0			
Bus free time between startup and stop		1.3			µs
Setup time SCL to start condition		0.6			
Hold time start condition to SCL		0.6			
Setup time, SCL to stop condition		0.6			

NOTE: (1) Ensured by design. Not production tested.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	PIN		
POWER AND GROUND			
AG1	26	I	Analog ground 1. Analog ground of the V5, V10 and V48 power systems. It should be externally tied to the common copper 48-V return plane. This pin should carry the low side of two de-coupling capacitors tied to V48 and V10
AG2	51	I	Analog ground 2. Analog ground, which ties to the substrate and ESD of the device. It should be externally tied to the common copper 48-V return plane. AG1 and AG2 must be tied together directly for lowest noise operation.
DG	56	I	Digital ground. It connects to the internal logic ground bus. It should be externally tied to the common copper 48V return plane. In addition a 0.1uF de−coupling capacitor should terminate as close to this node and the VL pin as possible.
RG	29	I	Reference ground. A precision sense of the external ground plane. It should also be used as the ground guard ring for the integration capacitor (CINT). It should be the closest ground to the low side of the 0.5-Ω current sense resistors, as well as RD, CINT, and RT. It should tie to common copper 48-V return plane.
V10	28	O	+10V analog supply.Connects to the internal analog power bus. This voltage is generated internally. This pin should not be tied to any external supplies. A 0.1-μF de-coupling capacitor should terminate as close to this node and the AG2 pin as possible. This pin can be used for external generation of V5.
V48	27	I	+48V input to the device. This supply can have a range of 44 V to 57 V. This pin should be de-coupled with a 0.1-μF capacitor from V48 to AG2 placed as close to the device as possible.
V5	25	I	External +5V analog supply.Connects to the internal analog power bus. This supplies the LED output drivers and internal analog circuits. A 0.1-μF de-coupling capacitor should terminate as close to this node and the AG1 pin as possible.
VL	54	I	External +3.3V logic supply. This pin connects to the internal logic power bus. This is the supply voltage for the internal device logic. A 0.1-μF de-coupling capacitor should terminate as close to this node and the DG pin as possible. This pin can be powered from V5 by using a 4.22-kΩ resistor from V5 to VL..
PORT ANALOG SIGNALS			
1P	1	I	Port positive. +48V load sense pin. Terminal voltage is monitored and controlled differentially with respect to *n*N. Optionally, if the application warrants it, this high-side path can be protected with the use of a self-resetting poly fuse.
2P	8	I	
3P	9	I	
4P	16	I	
5P	33	I	
6P	40	I	
7P	41	I	
8P	48	I	
1N	2	I	Port negative. −48V load return sense pin. The low side of the load is switched and protected with the external N-channel MOSFET.
2N	7	I	
3N	10	I	
4N	15	I	
5N	34	I	
6N	39	I	
7N	42	I	
8N	47	I	

TERMINAL FUNCTIONS (continued)

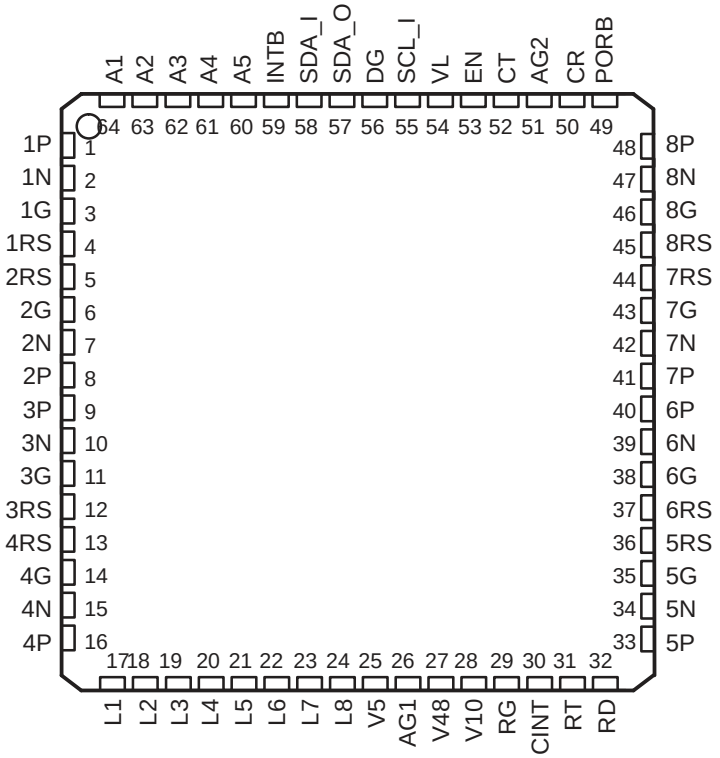
TERMINAL		I/O	DESCRIPTION
NAME	PIN		
PORT ANALOG SIGNALS (continued)			
1G	3	O	Port gate. Connect to the gate of an external N-channel MOSFET. During turn-on, this pin is controlled by a linear current amplifier (LCA) such that the load current ramps up from zero to a maximum sourcing current of 425 mA. This pin is driven to as high as 10 V. During controlled turn-off, this pin is driven such that the load current ramps down from a maximum of 425 mA to zero. The capacitor on the CR pin is utilized to generate the ramp control signal voltages. During a fault turn-off this pin is discharged quickly with a low on-resistance internal switch.
2G	6	O	
3G	11	O	
4G	14	O	
5G	35	O	
6G	38	O	
7G	43	O	
8G	46	O	
1RS	4	I	Port resistor sense. This is the kelvin sense path for the high potential end of the load current sense resistor. Parameters controlled by the load current sense resistor include: the average undercurrent/overcurrent and peak-load current thresholds, the peak PD inrush current limit during startup, and the nominal classification current levels. Use a 0.5-Ω load current sense resistor to be compliant to the 802.3 specification levels.
2RS	5	I	
3RS	12	I	
4RS	13	I	
5RS	36	I	
6RS	37	I	
7RS	44	I	
8RS	45	I	
ANALOG SIGNALS			
CR	50	I	Ramp capacitor. During load power up and down, this capacitor is used as the di/dt current slew capacitor. A 1.5-V peak triangular waveform is present on this pin during ramp up/down. Connect a 0.1-μF capacitor from this pin to AG2 and a 120-kΩ resistor at RT to meet the 802.3af specification timing levels.
CT	52	I	Timing capacitor. This capacitor and the resistor on the RT pin set the internal clock frequency of the device. This clock is used for the internal state machine, integrating A/D counters, POR time-out, and fault and delay timers of each port. Use a 100-pF to 470-pF capacitor for CT and a 120-kΩ resistor on RT to set the internal clock in a range of 100 kHz to 500 kHz. This timing can be overridden by driving the CT pin with a 0 V to 5 V square wave with a frequency from 0 kHz to 500 kHz.
CINT	30	I	This capacitor is used for the ramp A/D converter signal integration. Connect a 0.033-μF capacitor from this pin to RG. For minimal errors due to dielectric absorption, use a poly or Teflon capacitor type. Ceramic types can be used, but note the increased conversion error.
L1	17	O	LED lamp drivers. Dual or single color LEDs can be connected to each of these pins. Each pin indicates the state of the corresponding port. This is a tri-state port that is under full control of the host micro-controller. As such it can also be used as a data port, or general-purpose output driver.
L2	18	O	
L3	19	O	
L4	20	O	
L5	21	O	
L6	22	O	
L7	23	O	
L8	24	O	
RD	32	I	The discovery current-sense resistor is connected in the path from the RD pin to RG ground. The discovery current-sense resistor sets the discovery value to 25-kΩ (nominal) when a 665-Ω value is used. For best noise performance, de-couple this pin with a 0.68-μF, ceramic capacitor to RG ground.
RT	31	I	Bias set resistor. This resistor sets all precision bias currents within the device. This pin is forced to an internal 1.25-V reference voltage level. The current that flows into this resistor due to the applied 1.25-V bias is replicated and used throughout the device. This resistor also works in conjunction with the capacitors on CR, CT and CINT to set internal timing values. Use a 120-kΩ resistor to be compliant to the requirements of 802.3af.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	PIN		
DIGITAL SIGNALS			
A1	64	I	Addresses 1 through 5. This is the I2C address select input. Select the appropriate binary address on these pins by connecting this pin to device ground for a logic low and tying this pin to the VL pin for a logic high.
A2	63	I	
A3	62	I	
A4	61	I	
A5	60	I	
EN	53	I	This pin is normally to be held low. It has been reserved for future expansion of the TPS238x device family
INTB	59	O	This is an open drain output that goes low if a fault condition is produced on any of the eight ports.
PORB	49	I	This pin can be used to override the internal POR. When held low, the I2C interface, all the state machines, and registers are held in reset. When all internal and external supplies are within specification, and this pin is set to a logic high level, the POR delay begins. The I2C interface and registers becomes active within eight CLK periods of this event and communications to read or preset registers can begin. The reset delay for the remainder of the device then extinguishes within 65536 CLK periods.
SCL_I	55	I	Serial clock input pin for the I2C interface.
SDA_I	58	I	Serial data input pin for the I2C interface. When jumpered with the SDA_O pin, this connection becomes the standard bi-directional serial data line (SDA).
SDA_O	57	O	Serial data open drain output for the I2C interface. When jumpered with the SDA_I pin, this connection becomes the standard bi-directional serial data line (SDA). This is a high-voltage open drain output that can drive opto-coupler LEDs directly from the +48-V bus with an external, series current limiting resistor.

PACKAGE DESCRIPTION

PM PACKAGE
(TOP VIEW)



FUNCTIONAL DESCRIPTION

The TPS2383A/B architecture has been designed to work efficiently with simple low-cost controllers such as those in the MSP430 family of devices. Reference design and code examples for complete PSE management are available from TI for the TPS2383A/B/MSP430 chipset solution.

The PSEPM discovery method, as defined in the IEEE 802.3af Standard, uniquely identifies a powered device 25-kΩ − resistor. Use of low-level probe signals during discovery prevents damage to non-802.3 devices. The use of a point-to-point slope detection method for the PD 25-kΩ resistor measurement allows accurate detection, even if series steering diodes are present at the PD. For legacy loads, capacitive detection can be enabled. In this mode the TPS2383A/B A/D is used to measure the loads capacitive value.

After a successful discovery of the PD, the TPS2383A/B has a classification feature to identify the expected PD power level based on a current signature from the PD. The classification current level is measured at a reduced terminal voltage of 17.5 V and classified with 12 bits of resolution. The controller can then use this information to classify per the levels of the IEEE 802.3af standard or use levels custom to the application. Knowledge of the expected load power allows the power sourcing equipment to be built with a smaller and less expensive system power supply. For installations where classification is not needed, and reduced power-up time is desired, classification can be bypassed by setting the appropriate bits in the per-port write register.

In classification and powered modes, the PSEPM drives an external low side N-channel MOSFET for control of the 48-V return line. The use of an external N-channel MOSFET enables selection of very low $R_{DS(on)}$ devices to minimize board power dissipation in enclosures that may be controlling 100’s of ports. Current sensing is performed with a low value resistor, again minimizing board power dissipation. In discovery mode, due to the very low current used, an internal N-channel MOSFET is utilized in conjunction with an external, high value, current sense resistor.

The TPS2383A/B identifies all fault conditions defined in the PoE IEEE 802.3af Standard. The monitored conditions include input undervoltage lockout (UVLO), output undervoltage (UV) and overvoltage (OV), average and peak overcurrent detection, average undercurrent detection, and run current. If a fault condition is detected during power ramp or at any other time, the PSEPM circuit breaks by disconnecting the 48-V return line and then updates the fault status of the corresponding port register. When the TPS2383A/B is disabled the PSEPM ramps the current down at a controlled rate and the PSEPM changes states to a lower power sleep mode.

To maintain full compliance to Underwriters Laboratory (UL), IEC950 SELV and NEMKO safety standards an optional, low cost self-resetting PTC fuse can be added to the unswitched +48-V line to protect the system supply and wiring infrastructure from secondary building wiring faults.

When the PSEPM is enabled and a PD is discovered and optionally classified, power is ramped to the PD at a controlled current ramp rate to reduce EMI. Upon completion of the current ramp up, the port current remains limited at less than 400 mA. Upon startup the port can remain in current limit for a timed value of 50 ms which allows the bulk filter capacitance of the PD to charge. Once a PD is successfully powered and the external N-channel MOSFET is fully on, the average and peak current to the PD is continuously monitored. A disconnected load is detected if the average current falls below 10 mA. An overcurrent is detected if the average current exceeds 375 mA. If any of these conditions exist, status bits are set in the per-port read register set and the power is removed from the load.

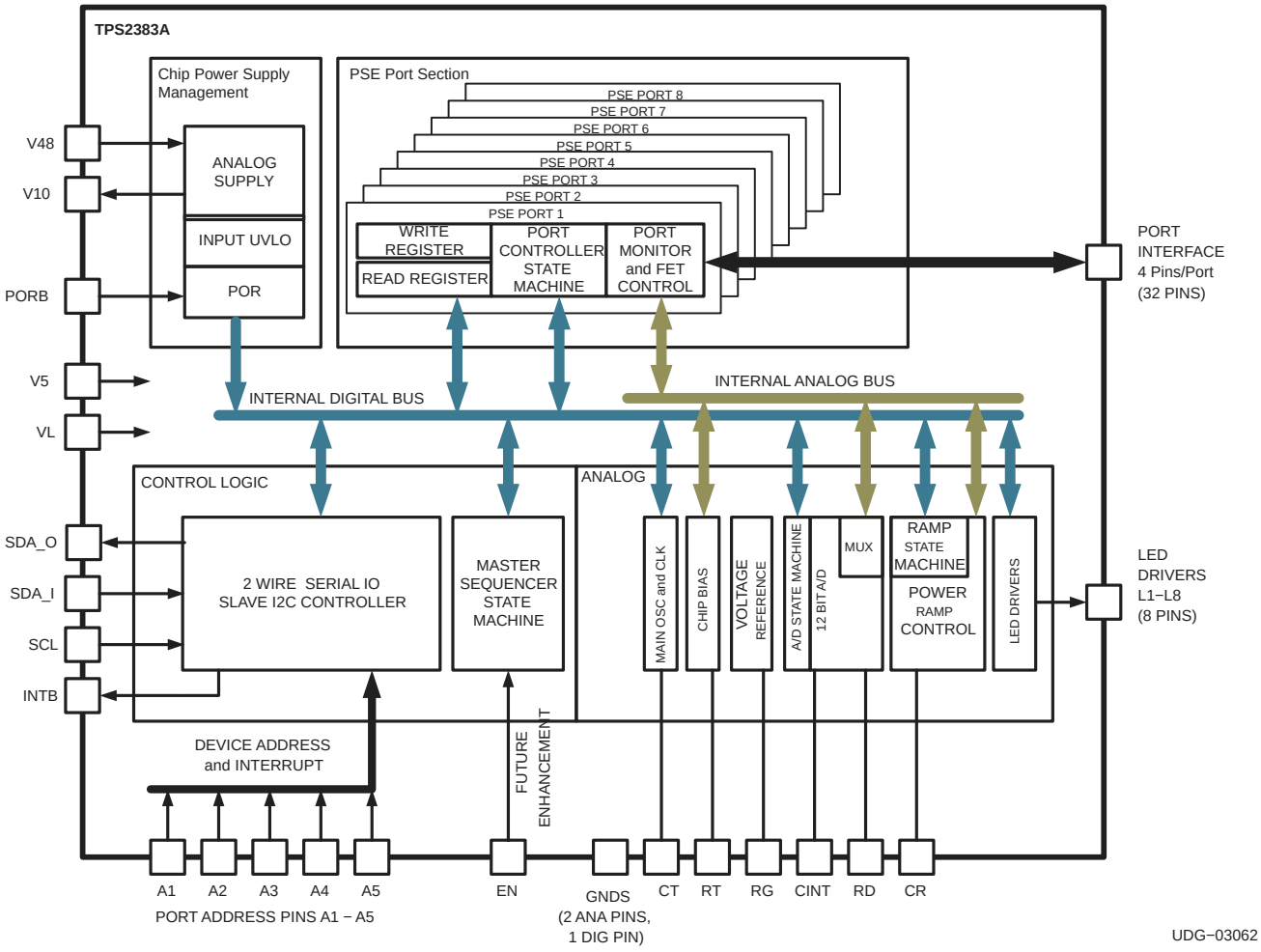
For maximum rejection of external wiring and power supply noise sources during the measurement of line current, voltage, resistance or capacitance in discovery, classification and powered modes, a proprietary low noise A/D converter is used. Converted measurements are processed and compared with digital set-points for limit compliance. The 12-bit conversion of this data-acquisition system is available through the read register enabling measurement of the discovery resistance, classification current and powered mode port running current and voltage. This is a valuable feature in ethernet switch management as it allows monitoring of real-time parameters across the system network.

The TPS2383A/B is available in a full function 64 pin LQFP package.

TPS2383A/B Evaluation Board

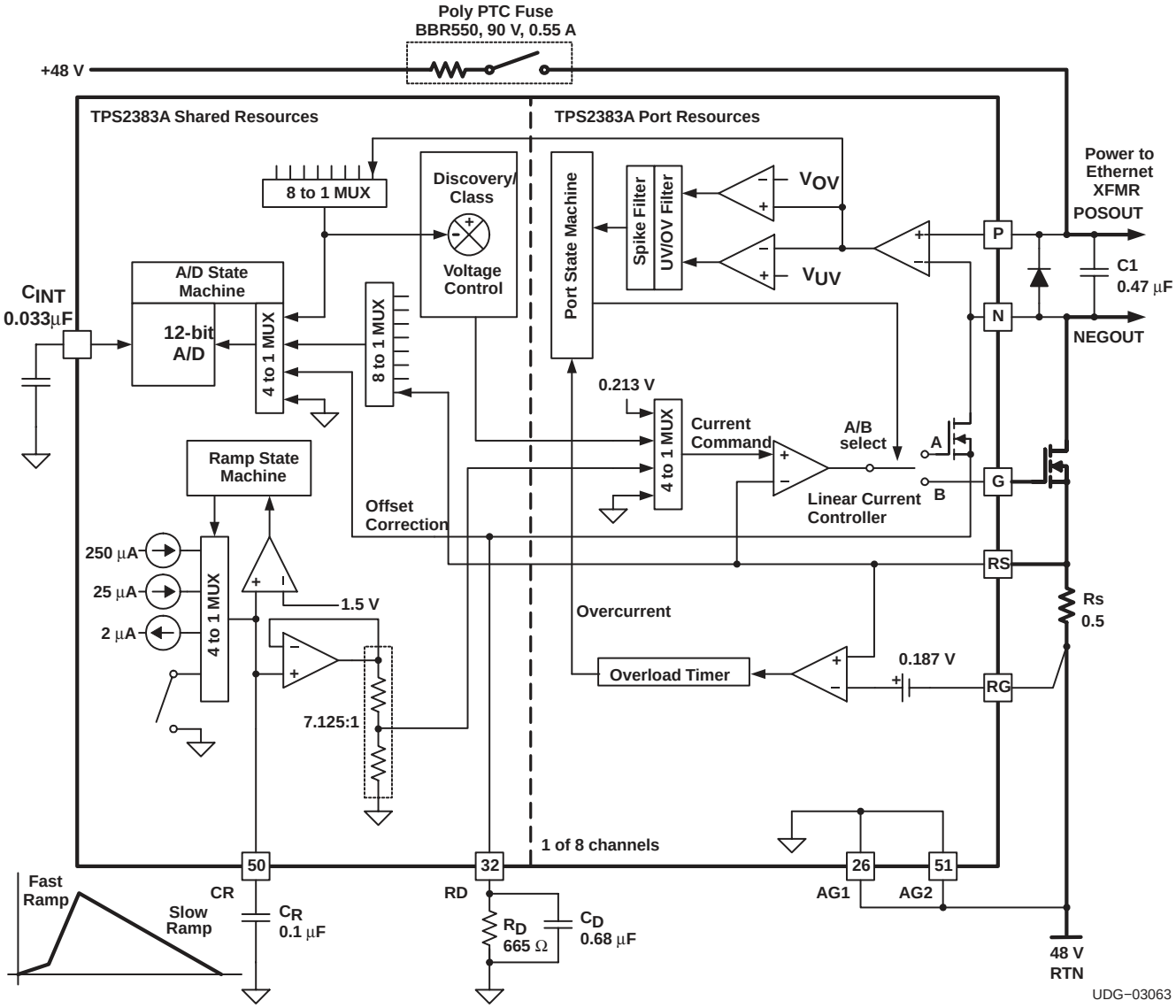
The full performance features of the TPS2383A/B/MSP430 chipset can be demonstrated with the TPS2383A/BEVM−001 evaluation board. The TPS2383A/BEVM−001 is a scaleable system that can be expanded to support 48 ports using a single microcontroller. This evaluation design can be used as a hardware/firmware template for modification to specific customer requirements. Please contact Texas Instruments or refer to the TPS2383A/BEVM−001 Users Guide (SLUU177) for complete information.

FUNCTIONAL BLOCK DIAGRAM



UDG−03062

TPS2383A/B BLOCK DIAGRAM − SHARED PORT ANALOG RESOURCES



FUNCTIONAL DESCRIPTION

SEPM STATE MACHINES

The TPS2383A/B has circuit resources that are common to each port and circuit resources that are shared by all ports. Five independent state machines are used to control the common and shared PSEPM resources. Port control, UV/OV/OC and overload protection are all features that are common to each port. Data acquisition and power ramping are shared functions for all the ports.

The master sequencer state machine is used to index the port presently being serviced and to distribute the shared resources to the currently selected port. The single master sequencer is responsible for incrementally accessing ports 1 through 8 and allowing those ports to process register data when they are accessed. Ports 1 through 8 each have a port sequencer, which controls all the power enabling and fault protection functions of the port per the register commands. The A/D has an A/D Sequencer that triggers, cycles and signals the port and master sequencer upon completion. The ramp sequencer controls the power ramping resource and is triggered by the port and master sequencer and provides a completion signal when power ramping is over.

Upon power-up the master sequencer is enabled and running after a POR delay and begins acting on register commands. A shorter POR delay releases the reset on the I^2C function and registers before the port reset is removed. This arrangement allows for register setup and polling over the I^2C bus quickly upon power up but ensures that power cannot be applied until the power supply is fully energized and stable. The default power-up state for all command registers is a null condition. The state sequence order of the TPS2383A/B is discovery, classification and power delivery if a POE compliant device is detected on the other end of the data cable.

The master sequencer powers-up in a default free-running mode. The TPS2383A/B also has a JOG mode. By setting the JOG_MODE register bit high, the master sequencer then no longer runs freely, but increments to the next sequential port each time the JOG register bit is set to a logic 1. The JOG bit is self-cleared once the port increments to the next position.

Sequencing starts with port 1 and ends with port 8 and then repeats. The port sequencer signals status information to the master sequencer and skips over disabled ports. When the master sequencer detects an enabled port, it pauses at that port until discovery, classification and power-up is complete before proceeding to the next. When the master sequencer reaches a powered port, it pauses and take a reading of the ports run-time current and/or voltage before proceeding to the next port. When a powered PD load is disconnected, the disconnect event can be detected the next time that port is selected by the master sequencer. When the disable bit of a powered port is set in the corresponding register, that operation is completed the next time the master sequencer selects that port. An overcurrent fault event shuts down the offending port independent of any sequencer state.

DUAL COLOR LED DRIVERS

The LED driver pins (L1 through L8) can be used to drive single or dual, color LEDs. These LEDs are intended to provide installation or service personnel with the necessary information to install and troubleshoot the system infrastructure. The L*n* pins have internal tri-state drivers. These LEDs can be controlled directly from the I^2C registers. The reset state of all the LEDs is tri-state. Cross-conduction logic disables both internal high- and low-side MOSFETS if an attempt is made to enable both transistors on a given port. These are high current (10-mA) drivers that can be used for other applications such as the drive of optocouplers or electromechanical devices, or can just be used as an 8-bit data port.

FUNCTIONAL DESCRIPTION

I²C INTERFACE

The serial interface used in the TPS2383A/B is a standard two-wire I²C slave architecture core. The standard bi-directional SDA lines of the I²C architecture are broken out into an independent input and output path. This feature simplifies, earth grounded, controller applications that require opto-isolators to keep the 48-V return of the ethernet power system floating. For applications where opto-isolation is not required, the bi-directional property of the SDA line can be restored by connecting SDA_I to SDA_O. The SCL line is a unidirectional input only line as the TPS2383A/B is always accesses as a slave device and it never controls the bus.

Data transfers that require a data-flow reversal on the SDA line are four-byte operations. This occurs during a TPS2383A/B port read access cycle where a slave address byte is sent, followed by a port/register address byte write. A second slave address byte is sent followed by the data byte read using the port/register setup from the second byte in the sequence.

Data write transfers to the TPS2383A/B do not require a data-flow reversal and as such only a three-byte operation is required. The sequence in this case is to send a slave address byte, followed by a write of the port/register address followed by a write of the data byte for the addressed port.

The I²C access cycle consists of the following steps 1 through 7 and is also shown in Figure 4.

1. Start sequence (S)
2. Slave address field
3. Read/write
4. Acknowledge
5. Port/register address or data field
6. Acknowledge/not acknowledge
7. Stop sequence (P)

The I²C interface and the port read write registers are held in active reset until input voltage is within specification and the internal POR timer has timed out.

Start/Stop

The high-to-low transition of SDA while SCL is high defines the start condition. The low-to-high transition of SDA while SCL is high defines the stop condition. The master device initiates all start and stop conditions.

A first serial packet enclosed within start and stop bits, consists of a seven-bit address field, read/write bit, and the acknowledge bit. The acknowledge bit is always generated by the device receiving the address or data field. Five of the seven address bits are used by the TPS2383A/B. The sixth and seventh bit is a placeholder for future expansion. During a write operation to the TPS2383A/B from the master device, the data field is eight bits. During a read operation where the TPS2383A/B is writing to the master device, the data field is also eight bits.

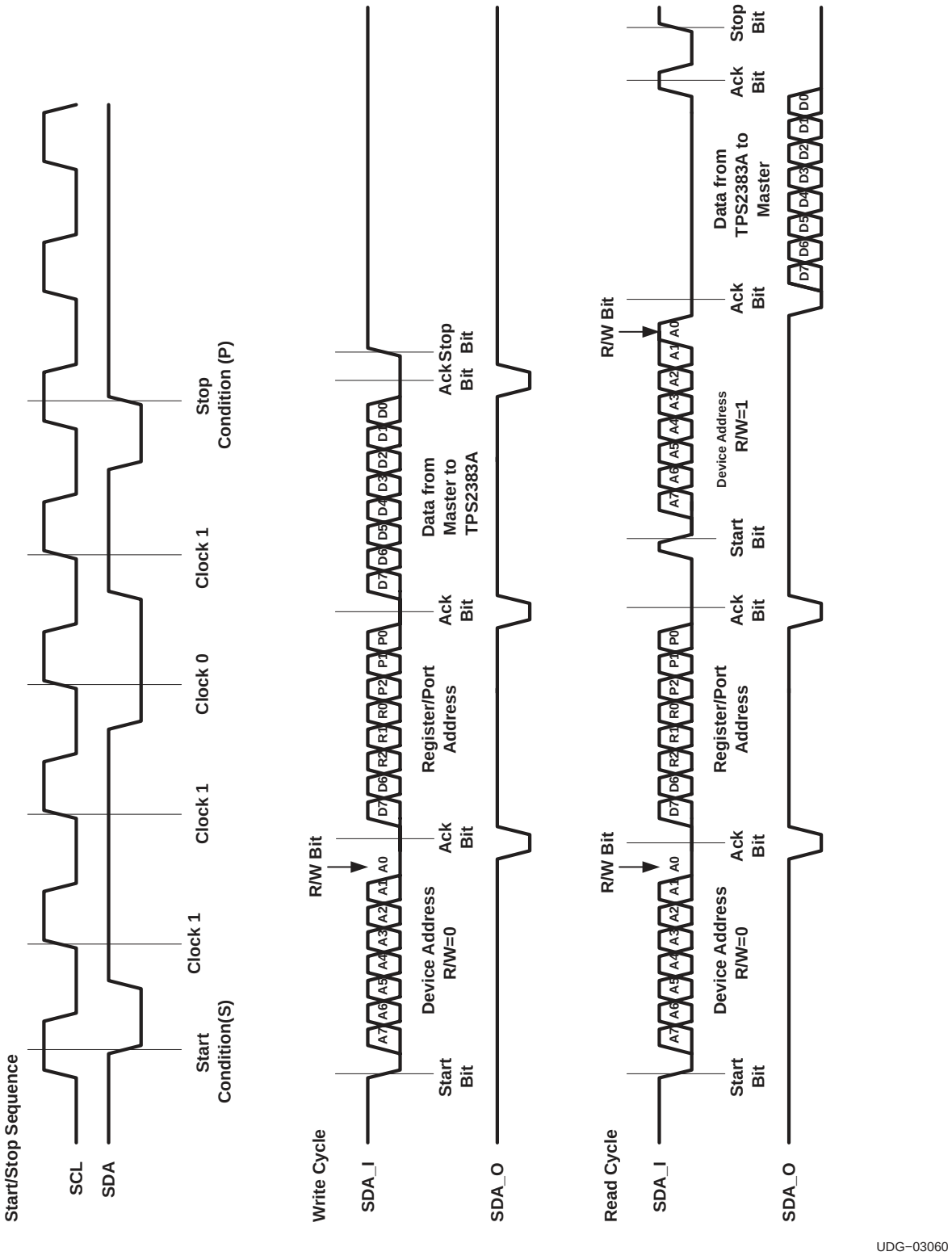


Figure 1. I²C Read/Write Cycles

FUNCTIONAL DESCRIPTION

Chip Address

The address field of the TPS2383A/B is eight bits and contains five bits of device address select, a read/write bit, and two reserved bits per Table 1. The leading two bits are reserved for future port expansion, and must be set to 0 for address acknowledge. The five device address select bits follow this. These bits are compared against the hard-wired state of the corresponding, device address select pins (A1 through A5). When the field contents are equivalent to the pin logic states, the device is addressed. These bits are followed by a least significant bit (LSB), which is used to set the read or write condition (1 for read and 0 for write). Following a start condition and an address field, the TPS2383A/B responds with an acknowledgement by pulling the SDA line low during the ninth clock cycle if the address field is equivalent to the value programmed by the pins. The SDA line remains a stable low while the ninth clock pulse is high.

Table 1. Address Selection Field

BIT	FUNCTION
A7	Future expansion set to 0
A6	Future expansion set to 0
A5	Device address. Compared with A5
A4	Device address. Compared with A4
A3	Device address. Compared with A3
A2	Device address. Compared with A2
A1	Device address. Compared with A1
A0	Read/write

Port/Register Cycle

After the chip address cycle, the TPS2383A/B accepts eight bits of port/register select data as defined in Table 2. The SCL line high-to-low transition after the eighth data bit then latches the selection of the appropriate internal register for the follow on data read or write operation. After latching the eight-bit data field, the TPS2383A/B pulls the SDA line low for one clock cycle.

Data Write Cycle

For a data write sequence, after the Port/Register address cycle, the TPS2383A/B accepts the eight bits of data. The data is latched into the previously selected Write Register, and the TPS2383A/B generates a data acknowledge pulse by pulling the SDA line low for one clock cycle. To reset the interface, the host or master subsequently generates a Stop bit by releasing the SDA line during the clock-high portion of an SCL pulse.

FUNCTIONAL DESCRIPTION

Data Read Cycle

For a data read sequence, after the register acknowledge bit, the master device generates a Stop condition. This is followed by a second Start condition, and retransmitting the device address as described in Chip Address above. For this cycle, however, the R/W bit is set to a 1 to signal the read operation. The TPS2383A/B again responds with an acknowledge pulse. The address acknowledge is then followed by sequentially presenting each of the eight data bits on the SDA line (MSB first), to be read by the host device on the rising edges of SCL. After eight bits are transmitted, the host acknowledges by pulling the SDA line high for one clock pulse. The completed data transfer is terminated with the host generating a Stop condition.

Table 2. Register/Port Addressing

BIT	FUNCTION	STATE
D7	Future expansion	
D6	Future expansion	
D5	R2, register select MSB	000 = Control (common Write register) 001 = Port Status (per port Read register) 010 = Port Control (per port Write register) 011 = A2D Register low byte (common read register) 100 = A2D Register high byte (common read register) 101 = Chip identification/revision (common read register)
D4	R1, register select	
D3	R0, register select LSB	
D2	P2, port address MSB	000 = Port 1 001 = Port 2 010 = Port 3 011 = Port 4 100 = Port 5 101 = Port 6 110 = Port 7 111 = Port 8
D1	P1, port address	
D0	P0, port address LSB	

Table 3. *Common Control*
Write Register, Register Address = 000 (Common Register)

BIT	FUNCTION	STATE	PRESET STATE
D7	Jog_mode	0 = Normal mode 1 = Jog mode	0
D6	Jog	0 = Don't jog 1 = Jog. This bit is self-clearing. It does not need to be reset to a 0 for each new jog.	0
D5	Bypass ramp	0 = Normal mode 1 = Bypass power−up ramp and powered mode for all ports	0
D4	Disconnect disable	0 = Normal mode 1 = Disable the effect of the logic signal from the Disconnect detection circuits. This is an expansion function for future parts. This bit should be set to a logic 1	0
D3	Bypass discovery	0 = Normal mode 1 = Bypass discovery mode.	0
D2	Bypass sample	0 = Normal mode 1 = Bypass current sample of all powered ports.	0
D1	Bypass classification	0 = Normal mode 1 = Bypass classification of all ports.	0
D0	Discovery fault disable	0 = Normal mode 1 = Disable the effect of the logic signal from the Discovery circuits. This is an expansion function for future parts. This bit should be set to a logic 1.	0

FUNCTIONAL DESCRIPTION

Port Status Registers

The Port Status registers (address 001) contain port specific information regarding the operational or faulted state of each of the eight Ethernet ports, as shown in Tables 4 and 5. In addition, the Port 1 Status register (Register/Port address xx00/1000) bits D6:D3 contain the current usage information of some of the common hardware resources, as they are accessed in the servicing of the port presently selected by the master sequencer.

Table 4. *Port Status Port 1*
Read Register, Register Address = 001, Port Address = 000

BIT	FUNCTION	STATE	PRESET STATE
D7	Port service	0 = Port not selected 1 = Port selected and being serviced	0
D6	Down	0 = Selected port is being ramped up 1 = Selected port is not being ramped up	1
D5	Ramp ServiceB	0 = Selected port is using the RAMP module 1 = Selected port is not using the RAMP module	1
D4	Current SampleB	0 = Selected port current is being acquired 1 = Selected port current is not being acquired	1
D3	A to D ServiceB	0 = Discovery/classification data acquisition in process 1 = A/D not performing a discovery/classification	1
D2	Fault status (MSB)	000 = Reset state 001 = UV/OV fault/spike 010 = UV/OV spike 100 = Overload fault 101 = Discovery Fail 110 = Load disconnect 111 = Reserved for future	000
D1	Fault status		
D0	Fault status (LSB)		

FUNCTIONAL DESCRIPTION

Table 5. *Port Status*
Read Register, Register Address = 001, Port Address = 001–111 (Port 2 through Port 8)

BIT	FUNCTION	STATE	PRESET STATE
D7	Port service	0 = Port not selected 1 = Port selected and being serviced	0
D6	Spare		0
D5	Spare		1
D4	Spare		1
D3	Spare		1
D2	Fault status (MSB)	000 = Reset state 001 = UV/OV fault/spike 010 = UV/OV spike 100 = Overload fault 101 = Discovery Fail 110 = Load disconnect 111 = Reserved for future	000
D1	Fault status		
D0	Fault status (LSB)		

Port Control Registers

The Port Control registers' (address 010) bit maps are shown in the following tables. These registers contain port specific control bits, accessible over the I^2C bus, for setting the port powered and port LED modes. To conserve hardware resources, some common control functions have been assigned to available bit locations within these registers. To clarify usage, these common functions are identified as such in the table RANK column.

Table 6. *Port Control*
Write Register, Register Address = 010, Port Address = 000 (Port 1 Register)

BIT	FUNCTION	RANK	STATE	PRESET STATE
D7	Port fault disable	Port	0 = Normal mode 1 = Disable the port overload timer	0
D6	POR disable	Common	0 = Normal POR timing 1 = Force POR to a non-reset state	0
D5	Software RESET	Common	0 = Normal operation 1 = Reset all circuits and start a device POR timing cycle	0
D4	LED blink enable	Port	0 = LED is continuous 1 = Blink the enabled LED at a fast-blink rate. Note fast-blink rate (in milliseconds) equivalent to 0.00013 x TPS2383A/B clock (CLK). This could be as fast as 65 ms for a 500-kHz, TPS2383A/B clock.	0
D3	LED low-side enable	Port	1 = Enable the low-side FET and drive the LED pin low	0
D2	LED high-side enable	Port	1 = Enable the high-side FET and drive the LED pin to V5	0
D1	Enable modes	Port	00 = Port OFF or disable 01 = Discovery − classification − power on sequence 10 = Sample powered-mode current 11 = Power-down an active port	0
D0				

FUNCTIONAL DESCRIPTION

Table 7. *Port Control*
Write Register, Register Address = 010, Port Address = 001 (Port 2 Register)

BIT	FUNCTION	RANK	STATE	PRESET STATE
D7	Overload fault disable	Port	0 = Normal mode 1 = Disable the port overload timer	0
D6	A/D advance	Common	0 = Normal mode 1 = Bypass offset correction ramp	0
D5	Class Limit 1	Common	Class Limit2, Class Limit1 0,0 = 160-mA classification current limit 0,1 = 80-mA classification current limit 1,0 = 40-mA classification current limit 1,1 = 20-mA classification current limit	0
D4	LED blink enable	Port	0 = LED is on continuous. 1 = Blink the enabled LED at a fast-blink rate. Note fast-blink rate (in milliseconds) equivalent to 0.00013 x TPS2383A/B clock (CLK). This could be as fast as 65 ms for a 500-kHz, TPS2383A/B clock.	0
D3	LED low-side enable	Port	1 = Enable the low-side FET and drive the LED pin low	0
D2	LED high-side enable	Port	1 = Enable the high-side FET and drive the LED pin to V5	0
D1 D0	Enable modes	Port	00 = Port OFF or disable 01 = Discovery − classification − power on sequence 10 = Sample powered-mode current 11 = Power-down an active port	0

Table 8. *Port Control*
Write Register, Register Address = 010, Port Address = 010 (Port 3 Register)

BIT	FUNCTION	RANK	STATE	PRESET STATE
D7	Overload fault disable	Port	0 = Normal mode 1 = Disable the port overload timer	0
D6	Discovery hold	Common	0 = Normal mode 1 = Hold A/D after detection	0
D5	Class Limit 2	Common	Class Limit2, Class Limit1 0,0 = 160-mA classification current limit 0,1 = 80-mA classification current limit 1,0 = 40-mA classification current limit 1,1 = 20-mA classification current limit	0
D4	LED blink enable	Port	0 = LED is on continuous. 1 = Blink the enabled LED at a fast-blink rate. Note fast-blink rate (in milliseconds) equivalent to 0.00013 x TPS2383A/B clock (CLK). This could be as fast as 65 ms for a 500-kHz TPS2383A/B clock.	0
D3	LED low-side enable	Port	1 = Enable the low-side FET and drive the LED pin low	0
D2	LED high-side enable	Port	1 = Enable the high-side FET and drive the LED pin to V5	0
D1 D0	Enable modes	Port	00 = Port OFF or disable 01 = Discovery − classification − power on sequence 10 = Sample powered-mode current 11 = Power-down an active port	0

FUNCTIONAL DESCRIPTION

Table 9. *Port Control*
Write Register, Register Address = 010, Port Address = 011 (Port 4 Register)

BIT	FUNCTION	RANK	STATE	PRESET STATE
D7	Overload fault disable	Port	0 = Normal mode 1 = Disable the port overload timer	0
D6	Overvoltage fault disable	Common	0 = Normal mode 1 = Disable all ports overvoltage timer	0
D5	A/D input select	Common	0 = Normal mode − select port currents 1 = Select port voltage	0
D4	LED blink enable	Port	0 = LED is on continuous. 1 = Blink the enabled LED at a ”fast blink” rate. Note ”fast blink” rate (in milliseconds) equivalent to 0.00013 x TPS2383A/B clock (CLK). This could be as fast as 65ms for a 500 kHz TPS2383A/B clock.	0
D3	LED low-side enable	Port	1 = Enable the low-side FET and drive the LED pin low	0
D2	LED high-side enable	Port	1 = Enable the high-side FET and drive the LED pin to V5	0
D1 D0	Enable modes	Port	00 = Port OFF or disable 01 = Discovery − classification − power on sequence 10 = Sample powered-mode current 11 = Power-down an active port	0

Table 10. *Port Control*
Write Register, Register Address = 010, Port Address = 100 (Port 5 Register)

BIT	FUNCTION	RANK	STATE	PRESET STATE
D7	Overload fault disable	Port	0 = Normal mode 1 = Disable the port overload timer	0
D6	Undervoltage fault disable	Common	0 = Normal mode 1 = Disable all ports undervoltage timers	0
D5	Spare			0
D4	LED blink enable	Port	0 = LED is on continuous. 1 = Blink the enabled LED at a ”fast blink” rate. Note ”fast blink” rate (in milliseconds) equivalent to 0.00013 x TPS2383A/B clock (CLK). This could be as fast as 65ms for a 500 kHz TPS2383A/B clock.	0
D3	LED low-side enable	Port	1 = Enable the low-side FET and drive the LED pin low	0
D2	LED high-side enable	Port	1 = Enable the high-side FET and drive the LED pin to V5	0
D1 D0	Enable modes	Port	00 = Port OFF or disable 01 = Discovery − classification − power on sequence 10 = Sample powered-mode current 11 = Power-down an active port	0

FUNCTIONAL DESCRIPTION

Table 11. *Port Control*
Write Register, Register Address = 010, **Port Address =** 101–111, (**Port 6 through Port 8 Registers)**

BIT	FUNCTION	RANK	STATE	PRESET STATE
D7	Overload fault disable	Port	0 = Normal mode 1 = Disable the port overload timer	0
D6	Spare			0
D5	Spare			0
D4	LED blink enable	Port	0 = LED is on continuous. 1 = Blink the enabled LED at a ”fast blink” rate. Note ”fast blink” rate (in milliseconds) equivalent to 0.00013 x TPS2383A/B clock (CLK). This could be as fast as 65ms for a 500 kHz TPS2383A/B clock.	0
D3	LED low-side enable	Port	1 = Enable the low-side FET and drive the LED pin low	0
D2	LED high-side enable	Port	1 = Enable the high-side FET and drive the LED pin to V5	0
D1 D0	Enable modes	Port	00 = Port OFF or disable 01 = Discovery − classification − power on sequence 10 = Sample powered-mode current 11 = Power-down an active port	0

Run Current/Voltage

During power delivery, the average value of the port running current or voltage is available from the read register. The slope type converter used produces 12 bits of input offset corrected conversion with a typical integration or averaging period of approximately one line cycle (16 ms). The actual averaging period is set by the CLK frequency and is equivalent to 8192 periods of that frequency. The lower eight bits of this conversion are available at the port register 011. The remaining upper four bits and A/D status bits are available at register 100. The converter span is 4096 bits. The A/D conversion port displays the real time counter output and holds the final static value at the completion of conversion

FUNCTIONAL DESCRIPTION

Table 12. *Common Analog to Digital Conversion Port*
Read Register, Register Address = 011

BIT	FUNCTION	STATE	PRESET STATE
D7	A2D bit 7	A/D lower bits	
D6	A2D bit 6		
D5	A2D bit 5		
D4	A2D bit 4		
D3	A2D bit 3		
D2	A2D bit 2		
D1	A2D bit 1		
D0	A2D bit 0		

Table 13. *Common Analog to Digital Conversion Port*
Read Register, Register Address = 100

BIT	FUNCTION	STATE	PRESET STATE
D7	A2D zero cross	0 = CINT is above zero threshold 1 = CINT is below zero threshold	
D6	A2D overflow	1 = A2D overflow detected	
D5	Reserved for test		
D4	Reserved for test		
D3	A2D bit 11	A/D upper bits	
D2	A2D bit 10		
D1	A2D bit 9		
D0	A2D bit 8		

Table 14. *Chip Identification/Revision*
Read Register, Register Address = 101

BIT	FUNCTION	STATE	PRESET STATE
D7	Rev ID MSB	Internally hardwired (function of revision)	0
D6	Rev ID		
D5	Rev ID LSB		
D4	Device ID MSB		
D3	Device ID		
D2	Device ID		
D1	Device ID		1
D0	Device ID LSB		0

APPLICATION INFORMATION

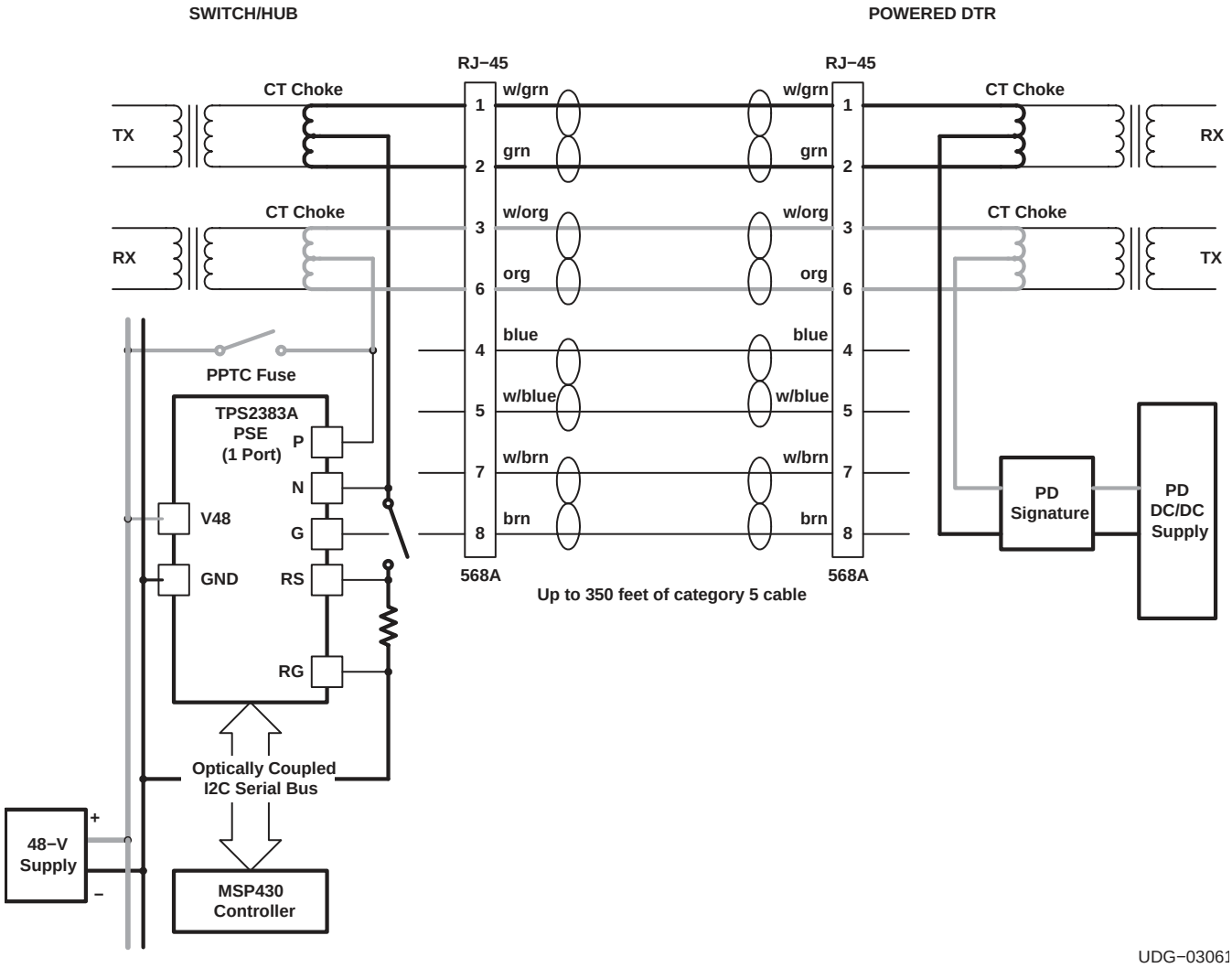


Figure 2. System Block Diagram

APPLICATION INFORMATION

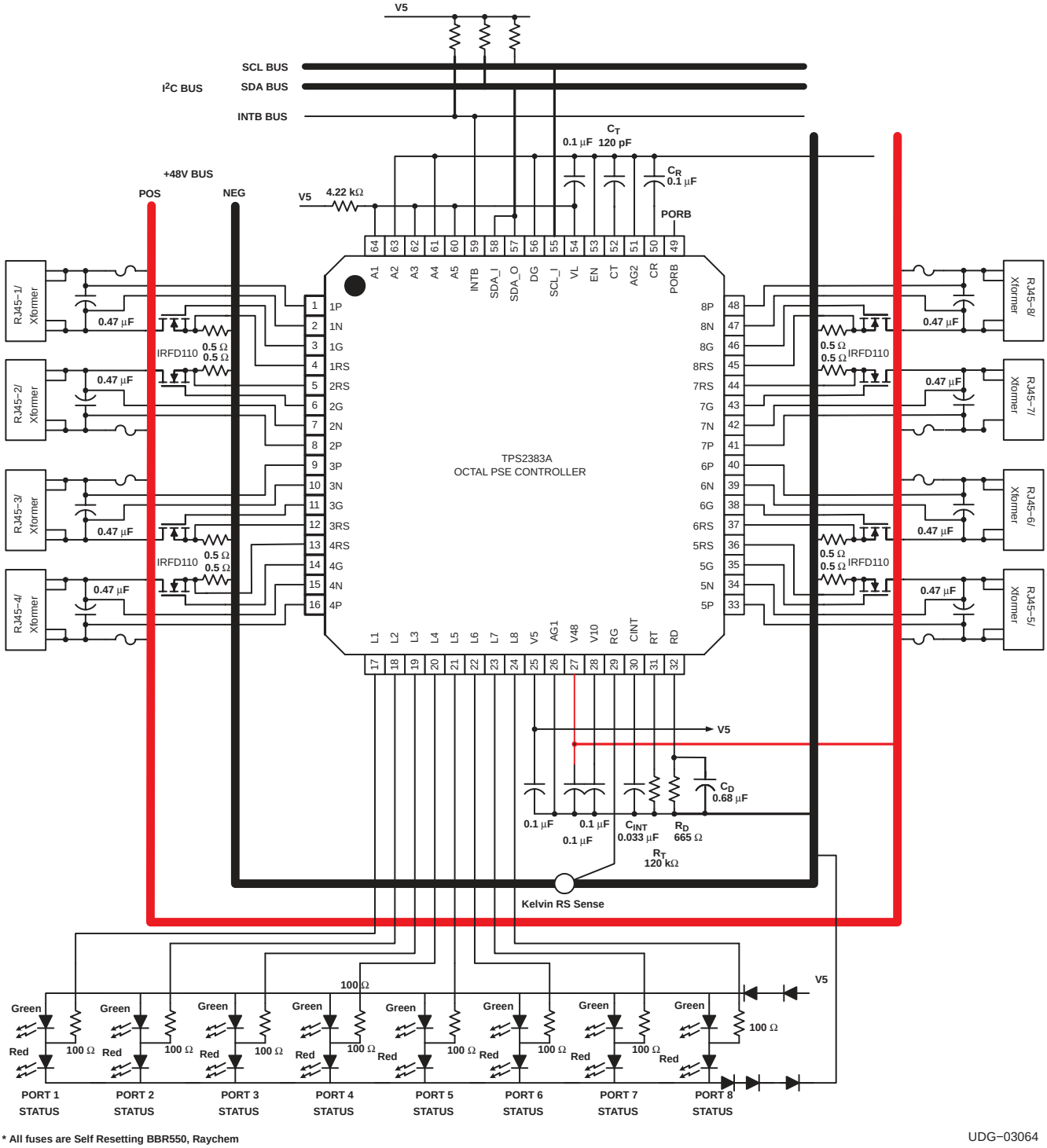


Figure 3. Typical Eight-Port Application

APPLICATION INFORMATION

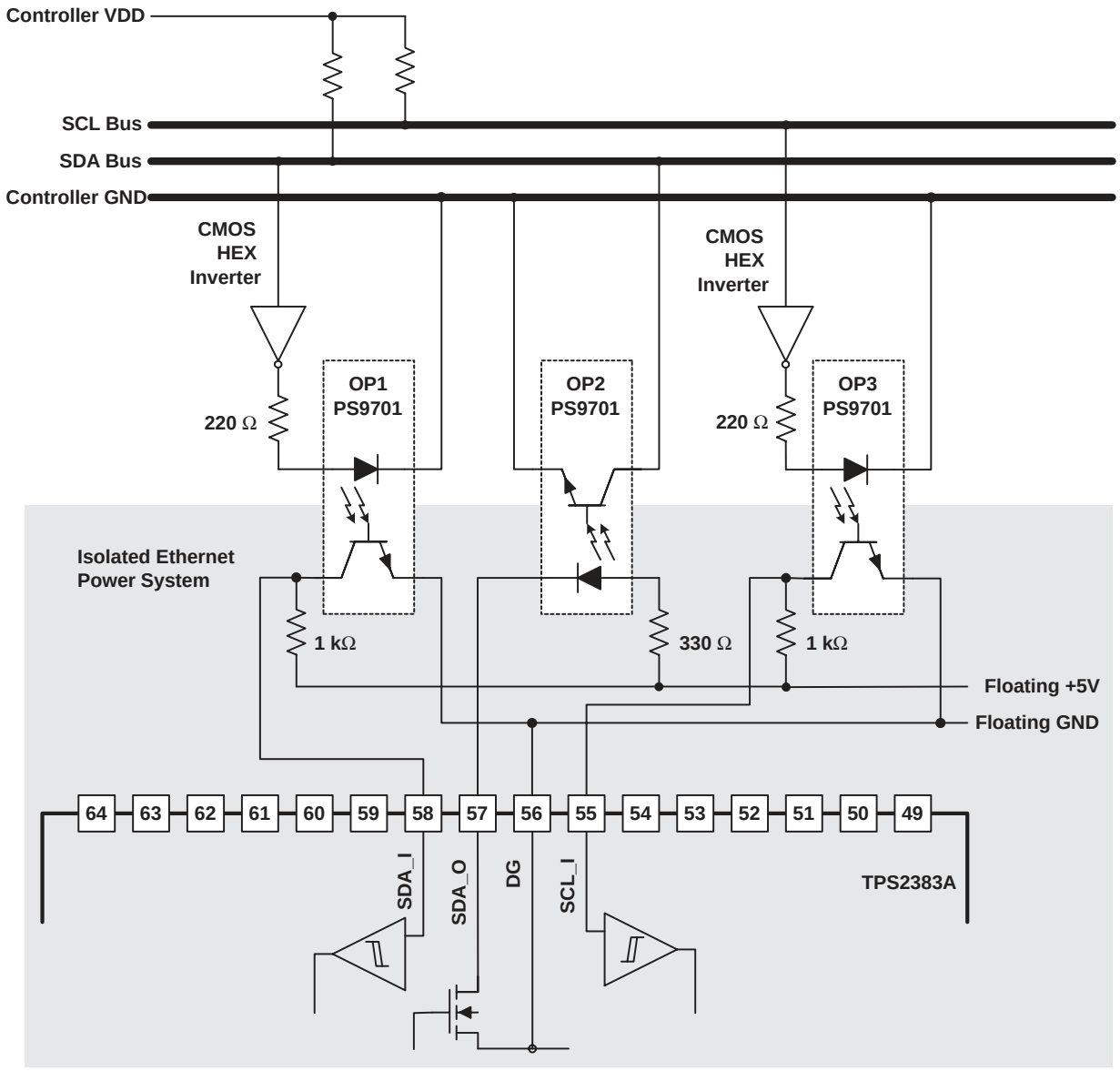


Figure 4. Using Optoisolators for I2C Bus/System Ground Isolation

APPLICATION INFORMATION

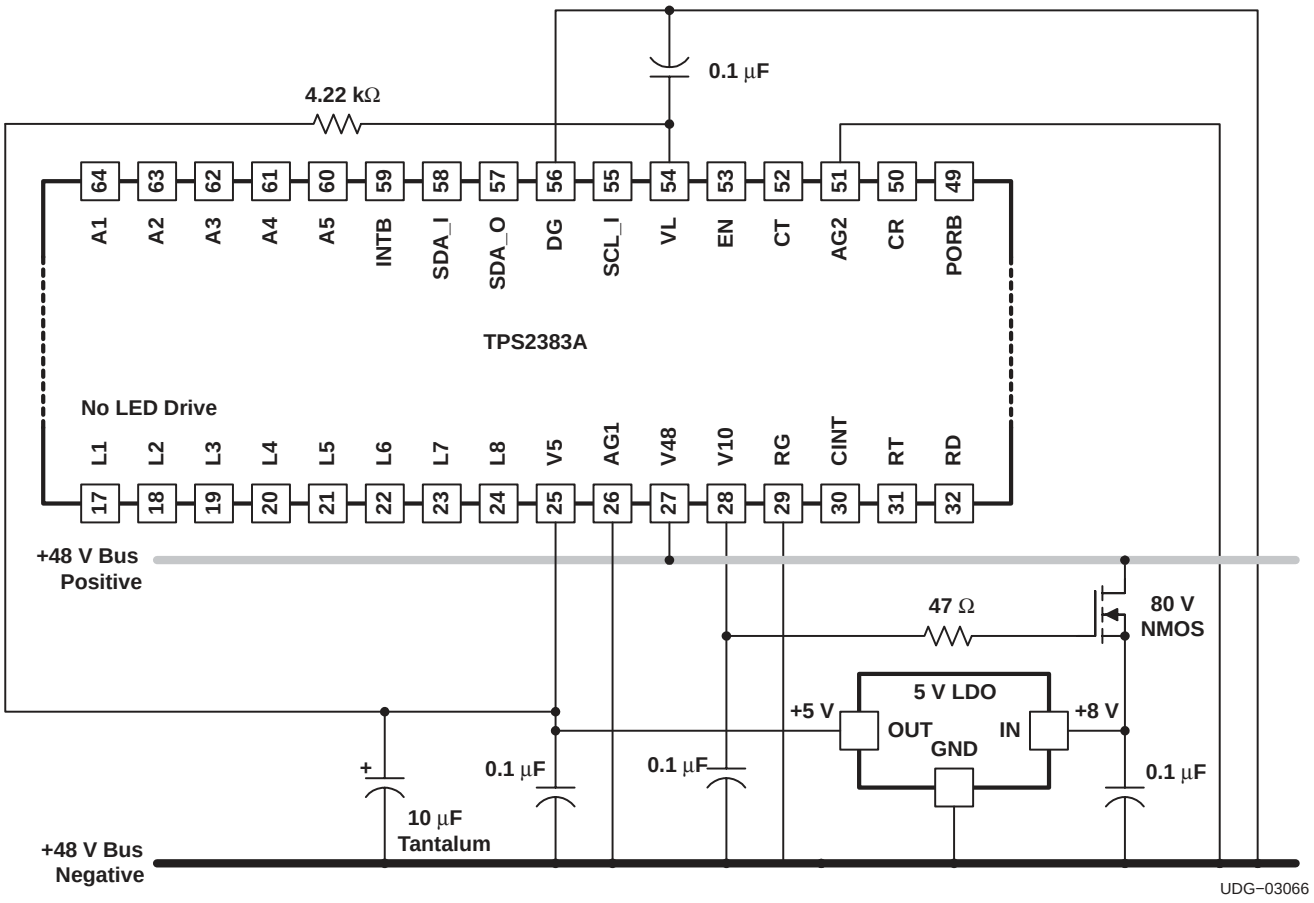
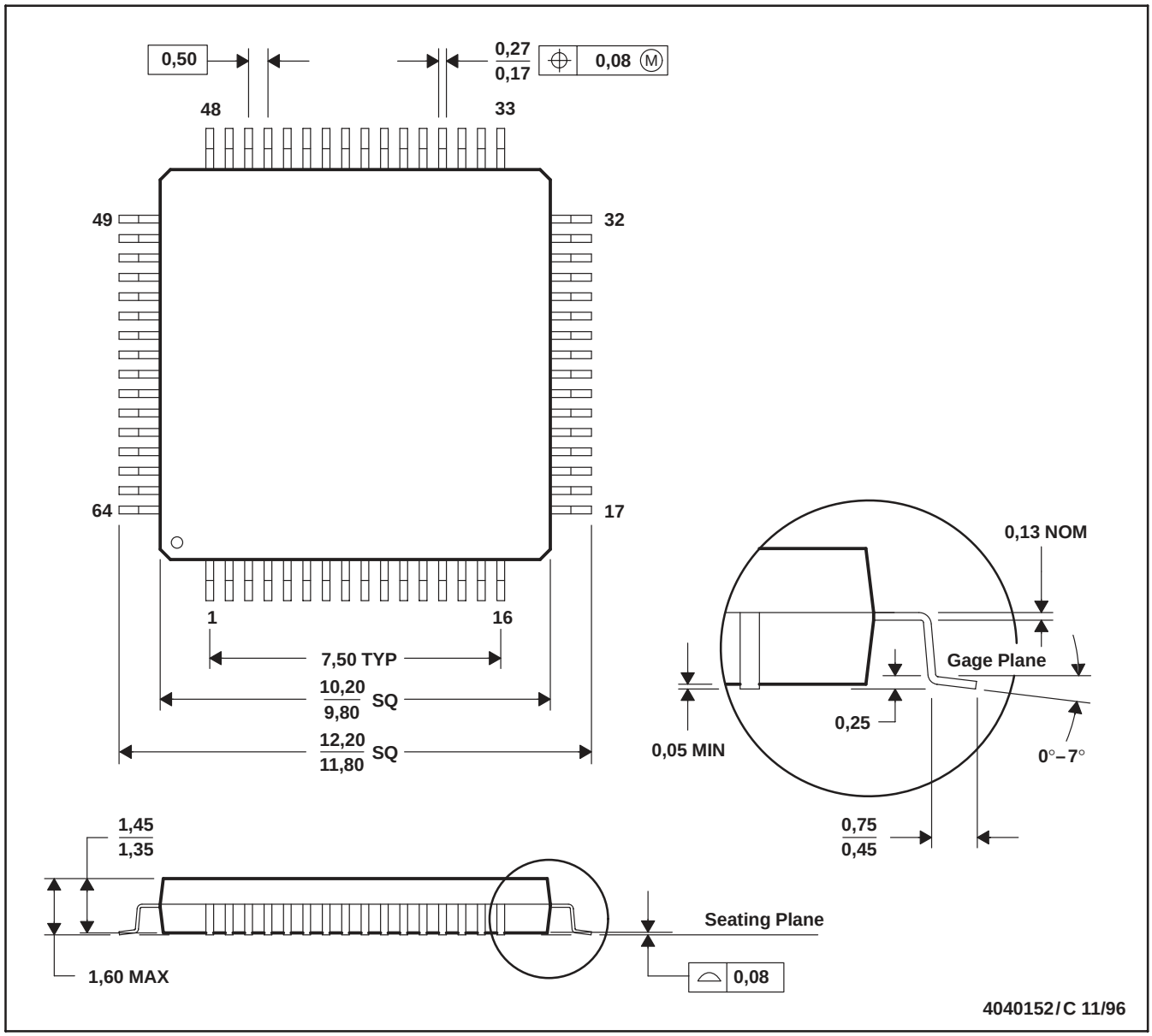


Figure 5. V5 and VL Generation from Single +48-V Supply

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265