19-2391; Rev 2; 2/07

+3.3V, 10.7Gbps Limiting Amplifier

General Description

The MAX3971A is a compact 10.7Gbps limiting amplifier. It accepts signals over a wide range of input voltage levels and provides constant-level output voltages with controlled edge speeds. It functions as a data quantizer with a 240mVP-P differential CML output signal with a 100Ω differential termination. The MAX3971A has a disable function that allows the outputs to be squelched if required by the application.

The MAX3971A is designed to work with the MAX3970 transimpedance amplifier (TIA). The limiting amplifier operates on a single +3.3V supply and functions over a 0°C to +85°C temperature range.

The MAX3971A is offered in die form and in a compact 4mm × 4mm 20-pin QFN and thin QFN package.

Applications

VSR OC-192 Receivers

10Gbps Ethernet Optical Receivers

10Gbps Fibre Channel Receivers

Pin Configurations appear at end of data sheet.

Features

- **Single +3.3V Power Supply**
- **2mVP-P Input Sensitivity**
- **1.8ps Typical Deterministic Jitter (V_{IN} = 800mVP-P)**
- **Dice and 4mm × 4mm QFN or Thin QFN Package Available**
- **Output Disable Feature**

Ordering Information

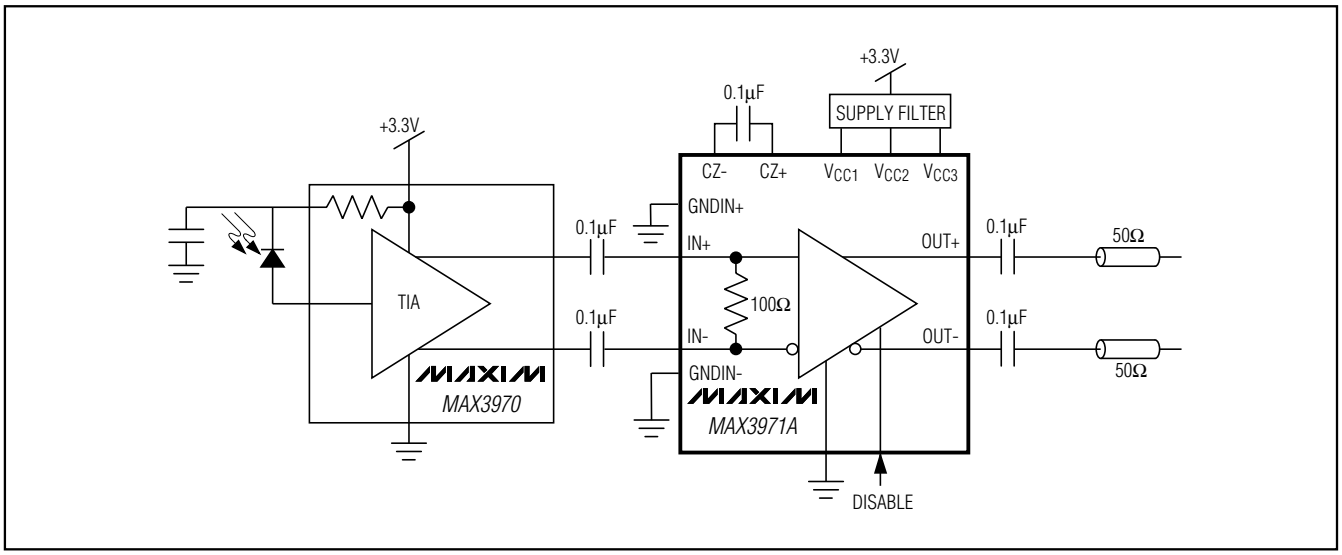
PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3971AUGP	0°C to +85°C	20 QFN-EP*	G2044-4
MAX3971AUTP	0°C to +85°C	20 Thin QFN-EP*	T2044-3
MAX3971AUTP+	0°C to +85°C	20 Thin QFN-EP*	T2044-3
MAX3971AU/D	0°C to +85°C	Dice**	—

*EP = Exposed pad.

**Dice are designed to operate over a 0°C to +110°C junction-temperature (T_J) range, but are tested and guaranteed at T_A = +25°C.

+Denotes lead-free package.

Typical Application Circuit



+3.3V, 10.7Gbps Limiting Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC1}, V_{CC2}, V_{CC3} .....-0.5V to +5.0 V
Voltage at IN+, IN-, DISABLE, CZ+, CZ-,
OUT+, OUT- .....+0.5V to (V_{CC} + 0.5V)
Differential Voltage Between CZ+ and CZ- .....±1V
Differential Voltage Between IN+ and IN- .....±2.5V
Continuous Power Dissipation (T_A = +85°C)
20-Pin QFN (derate 20mW/°C above +85°C) 1.3W
Operating Ambient Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Die Attach Temperature .....+400°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, output load = 50Ω to V_{CC}, T_A = 0°C to +85°C, unless otherwise noted. All AC parameters are measured with a 2^{23} - 1 PRBS pattern applied to the input at 10.7Gbps. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

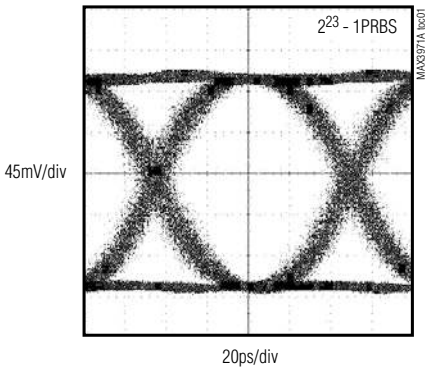
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}			50	85	mA
Small-Signal Bandwidth	BW			10		GHz
Input Sensitivity	V_{IN-min}	(Notes 1, 2)		2	5	mV_{P-P}
Input Overload	V_{IN-max}	(Note 1)	1200			mV_{P-P}
Low-Frequency Cutoff		CZ = 0.1µF (Note 1)		60	75	kHz
Deterministic Jitter		$5mV_{P-P}$ input (Notes 1, 3)		5.2	16.0	ps
		$10mV_{P-P}$ input (Notes 1, 3)		3.5	14.0	
		$800mV_{P-P}$ input (Notes 1, 3)		1.8	7.0	
		$1200mV_{P-P}$ input (Notes 1, 3)		1.9	11.0	
Random Jitter		$20mV_{P-P}$ < input < $1200mV_{P-P}$ (Notes 1, 4)		0.6	1.1	ps_{RMS}
Transition Time	t_r, t_f	20% to 80%, differential output (Note 1)		20	30	ps
Data Input Impedance		Single ended	42	50	58	Ω
Data Output-Voltage Swing		Differential signal amplitude between OUT+ and OUT-	190	240	400	mV_{P-P}
Data Output Voltage when Disabled		Differential signal amplitude between OUT+ and OUT-		0.25	50	mV_{P-P}
Data Output Common-Mode Voltage				V_{CC} - 75		mV
Data Output Impedance		Single ended	42	50	58	Ω
Data Output Offset when DISABLE is High				75	200	mV
Disable Input Current				30	60	µA
DISABLE High Voltage	V_{IH}		2			V
DISABLE Low Voltage	V_{IL}				0.8	V
Disable Response Time				20		ns

Note 1: Guaranteed by design and characterization.
Note 2: The output signal amplitude at the sensitivity is ≥ .95 × the amplitude with large input.
Note 3: Deterministic jitter is measured with K28.5 pattern (0011 1110 1011 0000 0101) at 10.7Gbps. It is the peak-to-peak deviation from the ideal time crossing, measured at the zero-level crossing of the differential output.
Note 4: For a bit-error rate of 10^{-12}, the peak-to-peak random jitter is 14.1 × the RMS random jitter.

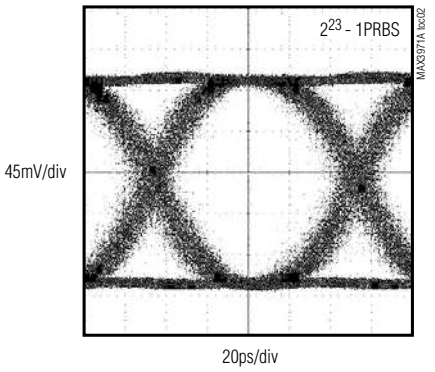
Typical Operating Characteristics

(V_{CC} = +3.3V, output load = 50Ω to V_{CC}, T_A = +25°C, unless otherwise noted.)

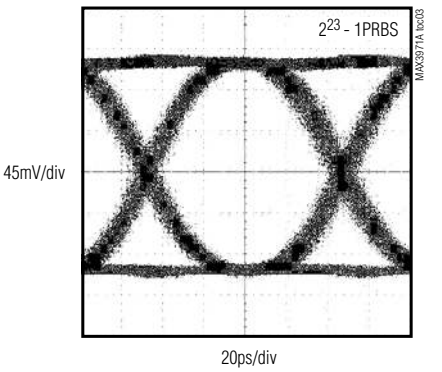
OUTPUT EYE DIAGRAM (INPUT SIGNAL = 10mV$_{P-P}$, AT 10.7Gbps)



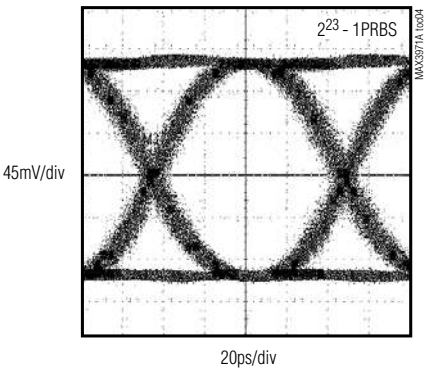
OUTPUT EYE DIAGRAM (INPUT SIGNAL = 5mV$_{P-P}$, AT 10.3Gbps)



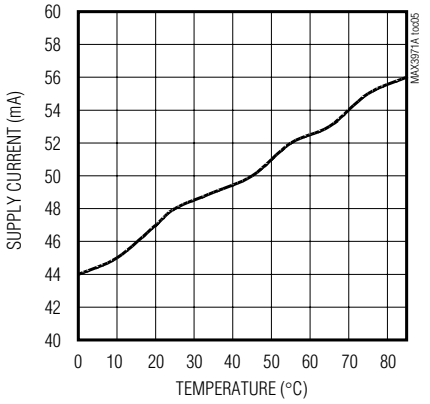
OUTPUT EYE DIAGRAM (INPUT SIGNAL = 1200mV$_{P-P}$, AT 10.3Gbps)



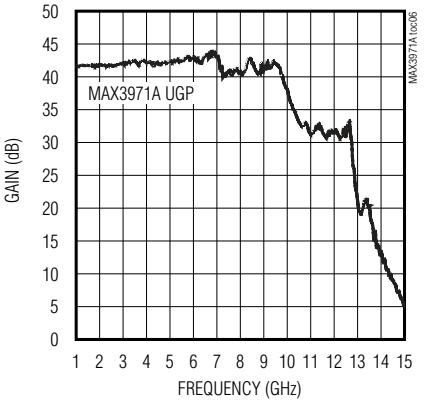
OUTPUT EYE DIAGRAM (INPUT SIGNAL = 800mV$_{P-P}$, AT 10.7Gbps)



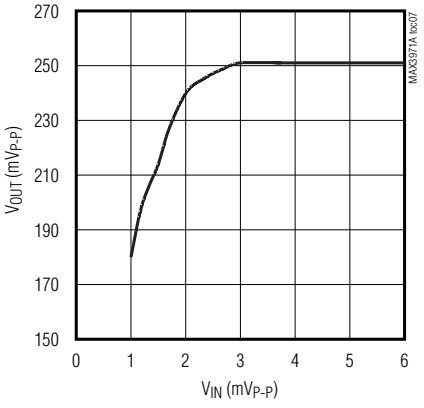
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



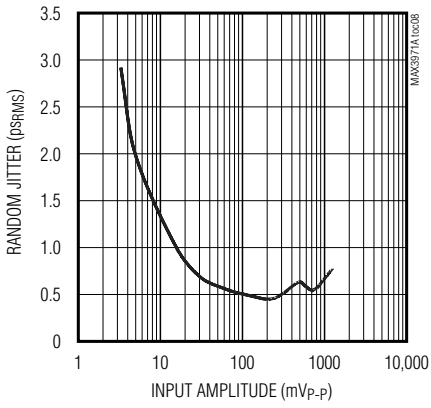
SMALL-SIGNAL GAIN



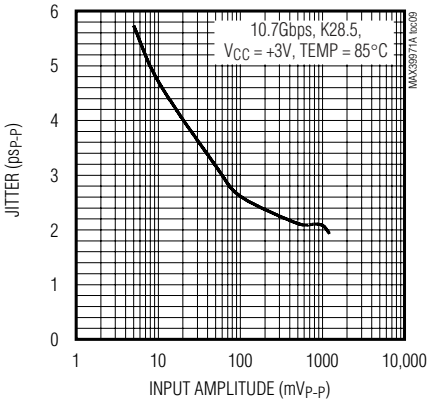
OUTPUT VOLTAGE vs. INPUT VOLTAGE



RANDOM JITTER vs. INPUT AMPLITUDE



DETERMINISTIC JITTER vs. INPUT AMPLITUDE

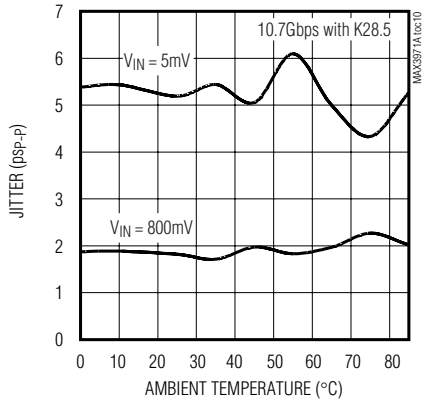


+3.3V, 10.7Gbps Limiting Amplifier

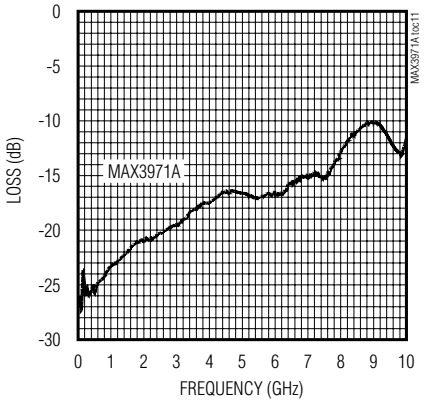
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, output load = 50Ω to V_{CC}, T_A = +25°C, unless otherwise noted.)

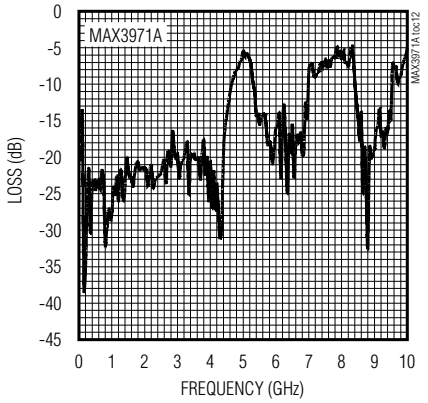
DETERMINISTIC JITTER vs. TEMPERATURE



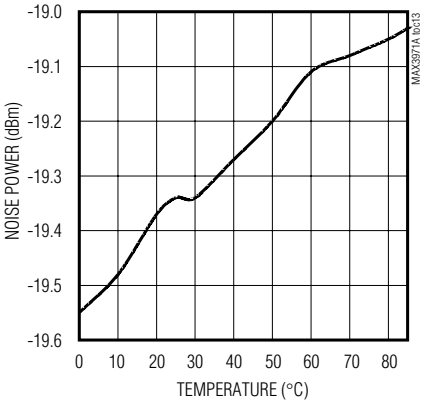
INPUT RETURN LOSS (S11) (V_{CC} = +3.3V)



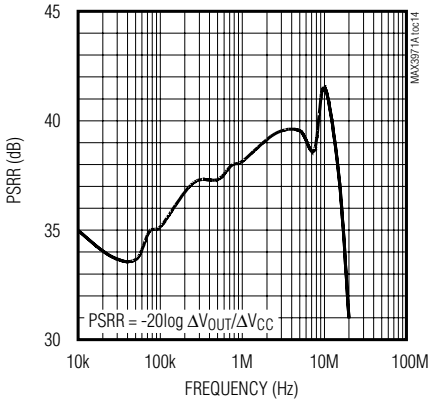
OUTPUT RETURN LOSS (S22) (V_{CC} = +3.3V)



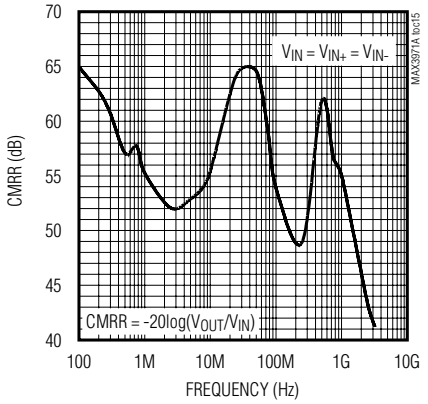
OUTPUT NOISE POWER (INPUT CONNECTED TO 50Ω TO GND)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



INPUT COMMON-MODE REJECTION RATIO vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	GNDIN+	Input Ground for Shielding Input Signal IN+. Not connected internally.
2	IN+	Noninverting Input Signal
3	IN-	Inverting Input Signal
4	GNDIN-	Input Ground for Shielding Input Signal IN-. Not connected internally.
5, 7, 9, 10	N.C.	No Connection. Leave unconnected.
6, 8, 11	GND	Ground
12, 15	V_{CC3}	Output Circuitry Power Supply
13	OUT-	Inverting Output of Amplifier
14	OUT+	Noninverting Output of Amplifier
16	DISABLE	When DISABLE is connected to V_{CC} or left floating, outputs are disabled. When DISABLE is connected to GND, outputs are enabled.
17	V_{CC2}	Power Supply to Circuitry other than Input and Output Circuits
18	CZ+	Filter Capacitor for Offset Correction. Connect CZ between pin 18 and pin 19. See the *Detailed Description* section.
19	CZ-	Filter Capacitor for Offset Correction. Connect CZ between pin 18 and pin 19. See the *Detailed Description* section.
20	V_{CC1}	Input Circuitry Power Supply
—	EP	Exposed Pad. Must be soldered to supply ground for proper electrical and thermal operation.

Detailed Description and Applications Information

Figure 1 is a functional diagram of the MAX3971A limiting amplifier. The signal path consists of an input buffer followed by a gain stage and output amplifier. A feedback loop provides offset correction by driving the average value of the differential output to zero.

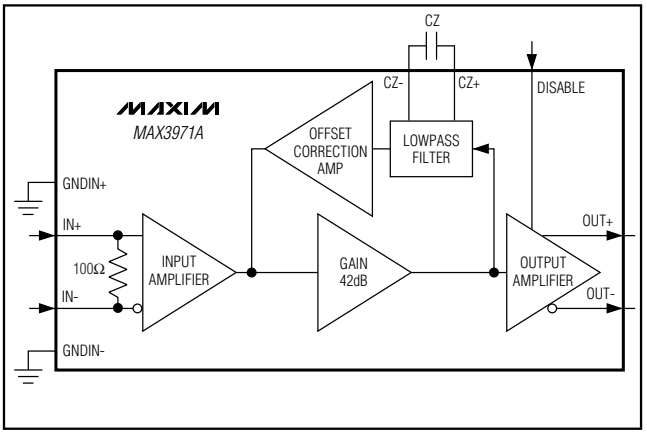


Figure 1. Functional Diagram

Gain Stage and Offset Correction

The limiting amplifier provides approximately 42dB gain. The large gain makes the amplifier susceptible to small DC offsets, which cause deterministic jitter. A low-frequency loop is integrated into the limiting amplifier to reduce output offset, typically to less than 2mV.

The external capacitor (CZ) is required for stability and to set the low-frequency cutoff for the offset correction loop. The time constant of the loop is set by the product of an equivalent 20kΩ on-chip resistor and the value of the off-chip capacitor (CZ). For stable operation, the minimum value of CZ is 0.01µF. To minimize pattern-dependent jitter, CZ should be as large as possible. For 10Gbps ethernet and SONET applications, the typical value of CZ is 0.1µF. Keep CZ close to the package to reduce parasitic inductance.

CML Input Circuit

The input buffer is designed to accept CML input signals such as the output from the MAX3970 transimpedance amplifier. An equivalent circuit for the input is shown in Figure 2. For lowest deterministic jitter in all operating conditions, AC-coupling capacitors are recommended on the input.

+3.3V, 10.7Gbps Limiting Amplifier

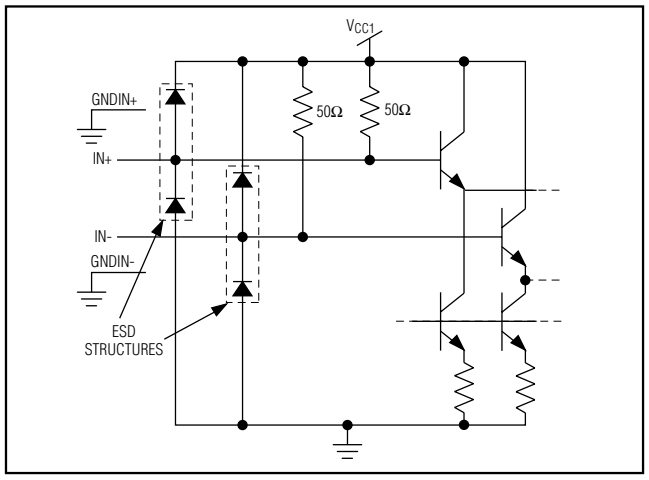


Figure 2. CML Input Equivalent Circuit

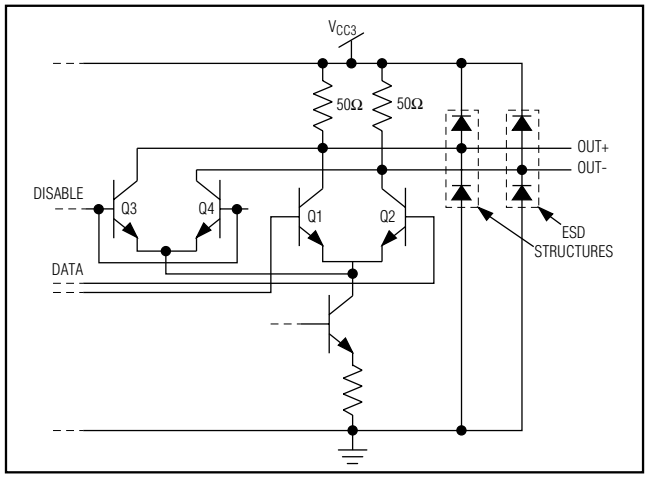


Figure 3. CML Output Equivalent Circuit

CML Output Circuit

An equivalent circuit for the output network is shown in Figure 3. It consists of a pair of 50Ω resistors connected to V_{CC} driven by the collectors of an output differential transistor pair (Q1 and Q2). The differential output signals are clamped by transistors Q3 and Q4 when the DISABLE input is high.

DISABLE Function

A logic signal can be applied to the DISABLE pin to squelch the output signal. When the output is disabled, an offset is added to the output, preventing the following stage from oscillating, if DC-coupled. See Figure 4 for the input stage of the DISABLE function.

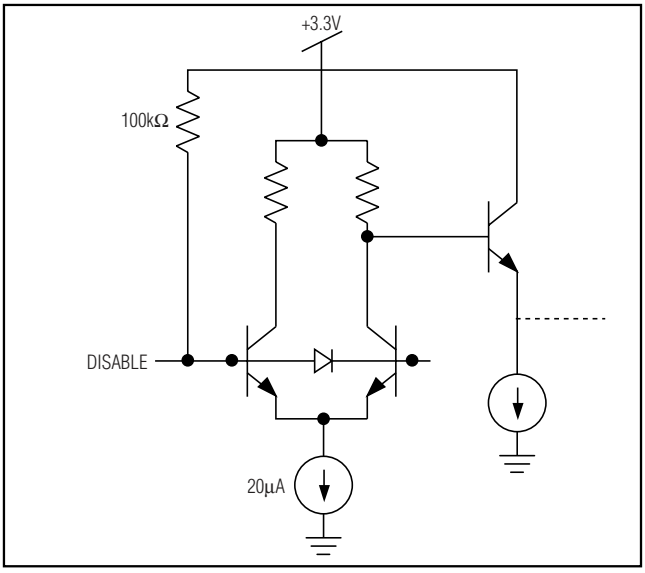


Figure 4. TTL Input Stage

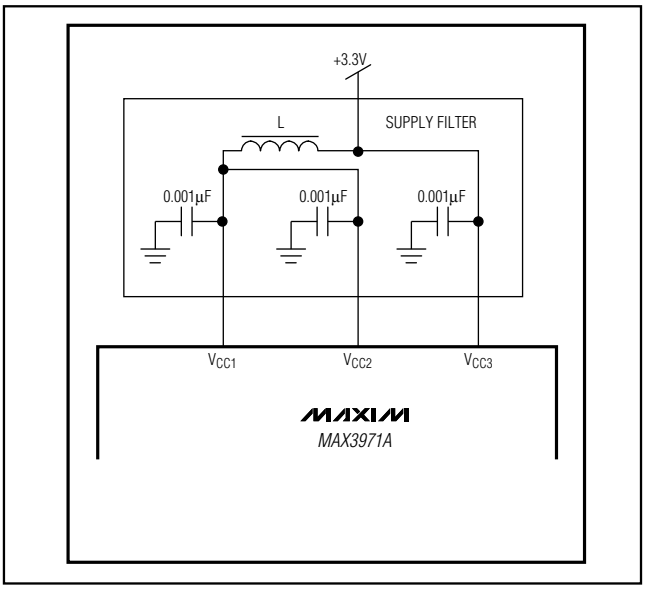


Figure 5. Power-Supply Filter

Layout Considerations

Circuit board layout and design can significantly affect the performance of the MAX3971A. Use good high-frequency techniques, including fixed-impedance transmission lines for the high-frequency data signal. Use a multilayer board with solid ground plane. Minimize the inductance between the MAX3971A and the ground plane.

The MAX3971A uses three power-supply pins (V_{CC1}, V_{CC2}, and V_{CC3}). The input circuitry of the MAX3971A is supplied by V_{CC1}. The output drivers have a separate supply (V_{CC3}), which usually has large pulsing currents. All other circuitry is powered by V_{CC2}. It is possible to simply connect the three pins together. However, using a supply filter ensures better isolation of the input circuitry. For optimal isolation, Figure 5 shows a possible supply-filtering circuit. Element L, a ferrite bead, provides isolation between a noisy V_{CC3} and a sensitive V_{CC1}.

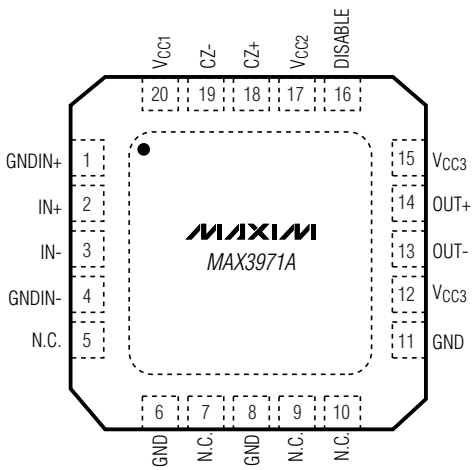
Chip Information

TRANSISTOR COUNT: 324

PROCESS: SiGe Bipolar

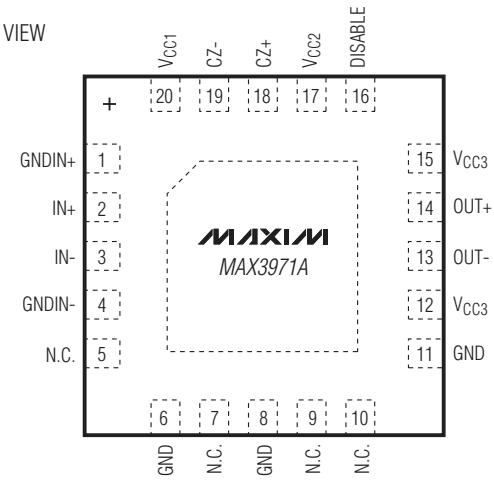
SUBSTRATE: Electrically Isolated

Pin Configurations



QFN
4mm x 4mm

THE EXPOSED PAD MUST BE SOLDERED TO GND FOR PROPER THERMAL AND ELECTRICAL PERFORMANCE.

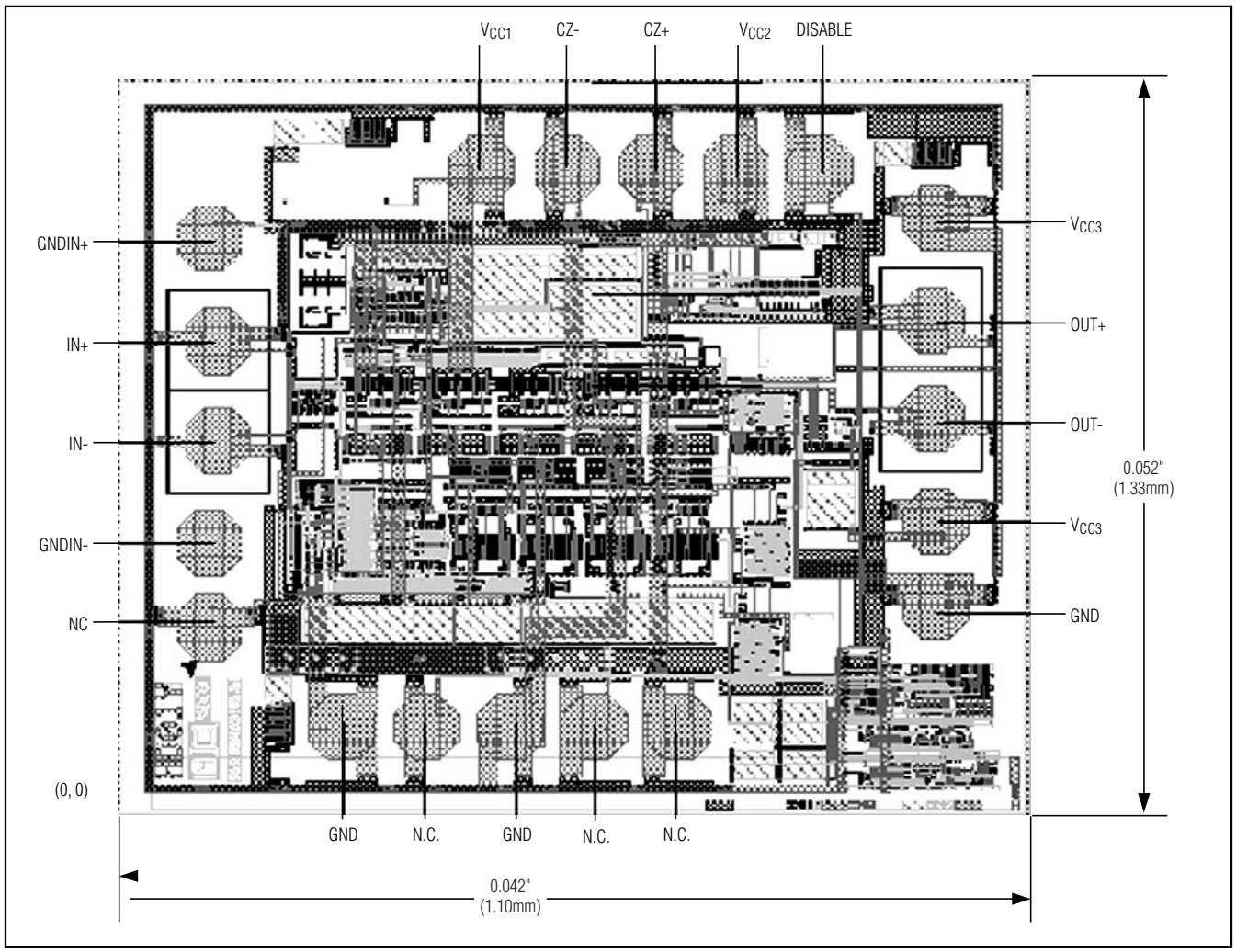


THIN QFN
4mm x 4mm

THE EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER THERMAL AND ELECTRICAL PERFORMANCE.

+3.3V, 10.7Gbps Limiting Amplifier

Chip Topography



Chip Topography (continued)

MAX3971A		
PAD NUMBER	X DIMENSION (µm)	Y DIMENSION (µm)
1	16	554
2	26	418
3	26	287
4	16	151
5	16	39
6	191	-92
7	303	-92
8	415	-92
9	527	-92
10	639	-92
11	978	67
12	978	179
13	974	315
14	974	446
15	978	582
16	825	647
17	713	647
18	601	647
19	489	647
20	377	647

- Pad dimensions:

  PASSIVATION OPENING: 94.4µm ×94.4µm

  METAL: 102.4µm ×102.4µm

- All measurements specify the lower left corner of the pad. Refer to Application Note H Fan-08.0: *Understanding Bonding Coordinates and Physical Die Size*.

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

Revision History

Rev 0; 4/02: Initial data sheet release.

Rev 1; 5/03: Added package code to *Ordering Information* and deleted EP references from *Ordering Information* (page 1); updated package drawing (page 10).

Rev 2; 2/07: Added thin QFN package (pages 1 and 7); removed package drawing.