19-5713; Rev 0; 12/10

MAX14811

Dual, Unipolar/Bipolar, High-Voltage Digital Pulsers with Fault Condition Management

General Description

The MAX14811 integrated circuit generates high-voltage, high-frequency unipolar or bipolar pulses from low-voltage logic inputs. The dual pulser features independent logic inputs, independent high-voltage pulser outputs with active clamps, and independent high-voltage supply inputs.

The device features fault condition management to protect the outputs. The outputs enter three-state if both INP_ and INN_ are logic-high. The device has a 9Ω output impedance for the high-voltage outputs and a 27Ω impedance for the active clamp. The high-voltage outputs are guaranteed to provide 2.0A (typ) output current. All the pulser outputs and clamp outputs have overvoltage protection.

The device uses three logic inputs per channel to control the positive and negative pulses and active clamp. Also included are two independent enable inputs. Disabling EN_ ensures the output MOSFETs are not accidentally turned on during fast power-supply ramping. This allows for faster ramp times and shorter delays between pulsing modes. A low-power shutdown mode reduces power consumption to less than 1µA. All digital inputs are CMOS compatible.

The device is available in a 7mm x 7mm, 56-pin TQFN exposed-pad package, and is specified over the 0°C to +70°C commercial temperature range.

Features

- **Fault Condition Management**
- **Highly Integrated, High-Voltage, High-Frequency Unipolar/Bipolar Pulser**
- **9Ω Output Impedance and 2.0A (typ) Output Current**
- **27Ω Active Clamp**
- **Pulser and Clamp Overvoltage Protection**
- **0 to +220V Unipolar or ±110V Bipolar Outputs**
- **Matched Rise/Fall Times and Matched Propagation Delays**
- **CMOS-Compatible Logic Inputs**
- **7mm x 7mm, 56-Pin TQFN Package**

Applications

Ultrasound Medical Imaging

Cleaning Equipment

Industrial Imaging/Flaw Detection

Piezoelectric Drivers

Test Equipment

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to: ***www.maxim-ic.com/MAX14811.related***

Dual, Unipolar/Bipolar, High-Voltage Digital Pulsers with Fault Condition Management

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{DD} Logic Supply Voltage Range .... -0.3V to +7V
$V_{CC\_}$ Output Driver Positive Supply Voltage Range...................................... -0.3V to +15V
$V_{EE\_}$ Output Driver Negative Supply Voltage Range..................................... -15V to +0.3V
$V_{PP\_}$ High Positive Supply Voltage Range .... -0.3V to +230V
$V_{NN\_}$ High Negative Supply Voltage Range...... -230V to +0.3V
V_{SS} Voltage Range .... ($V_{PP\_}$ - 230V) to $V_{NN\_}$
V_{PP1} - V_{NN1}, V_{PP2} - V_{NN2} Supply Voltage Range .... -0.6V to +230V
INP_, INN_, INC_, EN_, $\overline{SHDN}$ Logic Input Range.................................... -0.3V to (V_{DD} + 0.3V)
OP_, OCP_, ON_, OCN_ Voltage Range.................. (-0.3V + $V_{NN\_}$) to (+0.3V + $V_{PP\_}$)
CGN_ Voltage Range........... (-0.3V + $V_{NN\_}$) to (+15V + $V_{NN\_}$)
CGP_ Voltage Range .... (+0.3V + $V_{PP\_}$) to (-15V + $V_{PP\_}$)
CGC_ Voltage Range.. -15V to +15V
CDC_, CDP_, CDN_ Voltage Range .... -0.3V to $V_{CC\_}$
Peak Current Per Output Channel 3.0A
Continuous Power Dissipation (T_A = +70°C) (Note 1)
TQFN (derate 40mW/°C above +70°C) 3200mW
Operating Temperature Range .... 0°C to +70°C
Junction Temperature .... +150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Note 1: This specification is based on the thermal characteristic of the package, the maximum junction temperature, and the setup described by JESD51. The maximum power dissipation for the MAX14811 might be limited by the thermal protection included in the device.

Warning: The MAX14811 is designed to operate with high voltages. Exercise caution.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....25°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....0.8°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS*

(V_{DD} = +2.7V to +6V, $V_{CC\_}$= +4.75V to +12.6V, $V_{EE\_}$= -12.6V to -4.75V, $V_{NN\_}$= -200V to 0, $V_{PP\_}$ = 0 to ($V_{NN\_}$+ 200V), $V_{SS} \leq$ the lower of V_{NN1} or V_{NN2}, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY (V_{DD}, $V_{CC\_}$, $V_{EE\_}$, $V_{PP\_}$, $V_{NN\_}$)						
Logic Supply Voltage	V_{DD}		+2.7	+3	+6	V
Positive Drive Supply Voltage	$V_{CC\_}$		+4.75	+12	+12.6	V
Negative Drive Supply Voltage	$V_{EE\_}$		-12.6	-12	-4.75	V
High-Side Supply Voltage	$V_{PP\_}$		0		$V_{NN\_}$ + 220	V
Low-Side Supply Voltage	$V_{NN\_}$		-200		0	V
$V_{PP\_}$ - $V_{NN\_}$			0		+220	V
SUPPLY CURRENT (SINGLE CHANNEL)						
V_{DD} Supply Current	I_{DD}	$V_{INN\_}$ /$V_{INP\_}$ = 0V, $V_{\overline{SHDN}}$ = 0V			1	µA
		$V_{EN\_}$ = V_{DD}, $V_{\overline{SHDN}}$ = V_{DD}, $V_{INC\_}$ = 0V or V_{DD}, $V_{INN\_}$ = $V_{INP\_}$, f = 5MHz		100	200	µA

*The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.

ELECTRICAL CHARACTERISTICS* (continued)

(V_{DD} = +2.7V to +6V, $V_{CC\_}$ = +4.75V to +12.6V, $V_{EE\_}$ = -12.6V to -4.75V, $V_{NN\_}$ = -200V to 0, $V_{PP\_}$ = 0 to ($V_{NN\_}$ + 200V), $V_{SS} \leq$ the lower of V_{NN1} or V_{NN2}, $T_A = T_J = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CC\_}$ Supply Current	$I_{CC\_}$	$V_{\overline{SHDN}}$ = 0V, CH1 and CH2			1	mA
		$V_{EN\_} = V_{DD}$, $V_{\overline{SHDN}} = V_{DD}$, CH1 and CH2		130	200	
		$V_{EN\_} = V_{DD}$, $V_{\overline{SHDN}} = V_{DD}$, $V_{INC\_}$ = 0V or V_{DD}, $V_{INN\_} = V_{INP\_}$, f = 5MHz, $V_{CC\_}$ = 5V, V_{DD} = 3V, only one channel switching		15		
		$V_{EN\_} = V_{DD}$, $V_{\overline{SHDN}} = V_{DD}$, $V_{INC\_}$ = 0V or V_{DD}, $V_{INN\_} = V_{INP\_}$, f = 5MHz, $V_{CC\_}$ = 12V, V_{DD} = 3V, only one channel switching		36		
$V_{EE\_}$ Supply Current	$I_{EE\_}$	$V_{\overline{SHDN}}$ = 0V, CH1 and CH2			1	µA
		$V_{EN\_} = V_{DD}$, $V_{\overline{SHDN}} = V_{DD}$, CH1 and CH2			25	
		$V_{EN\_} = V_{DD}$, $V_{\overline{SHDN}} = V_{DD}$, $V_{INC\_}$ = 0V or V_{DD}, $V_{INN\_} = V_{INP\_}$, f = 5MHz, $V_{EE\_}$ = -5V, only one channel switching			200	
		$V_{EN\_} = V_{DD}$, $V_{\overline{SHDN}} = V_{DD}$, $V_{INC\_}$ = 0V or V_{DD}, $V_{INN\_} = V_{INP\_}$, f = 5MHz, $V_{EE\_}$ = -12V, only one channel switching			200	
$V_{PP\_}$ Supply Current	$I_{PP\_}$	$V_{\overline{SHDN}}$ = 0V, CH1 and CH2			1	µA
		$V_{EN\_} = V_{DD}$, $V_{\overline{SHDN}} = V_{DD}$, CH1 and CH2		90	160	
		$V_{EN\_} = V_{DD}$, $V_{\overline{SHDN}} = V_{DD}$, $V_{INC\_}$ = 0V or V_{DD}, $V_{INN\_} = V_{INP\_}$, f = 5MHz, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, no load, only one channel switching		9		mA
		$V_{EN\_} = V_{DD}$, $V_{\overline{SHDN}} = V_{DD}$, $V_{INC\_}$ = 0V or V_{DD}, $V_{PP\_}$ = +80V, $V_{NN\_}$ = -80V, pulse repetition frequency (PRF) = 10kHz, f = 10MHz, four periods, no load, only one channel switching		0.6		
$V_{NN\_}$ Supply Current	$I_{NN\_}$	$V_{\overline{SHDN}}$ = 0V, CH1 and CH2			1	µA
		$V_{EN\_} = V_{DD}$, $V_{\overline{SHDN}} = V_{DD}$, CH1 and CH2		40	80	
		$V_{EN\_} = V_{DD}$, $V_{\overline{SHDN}} = V_{DD}$, $V_{INC\_}$ = 0V or V_{DD}, $V_{INN\_} = V_{INP\_}$, f = 5MHz, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, no load, only one channel switching		9		mA
		$V_{EN\_} = V_{DD}$, $V_{\overline{SHDN}} = V_{DD}$, $V_{INC\_}$ = 0V or V_{DD}, $V_{PP\_}$ = +80V, $V_{NN\_}$ = -80V, pulse repetition frequency (PRF) = 10kHz, f = 10MHz, four periods, no load, only one channel switching		0.6		

**The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.*

ELECTRICAL CHARACTERISTICS* (continued)

(V_{DD} = +2.7V to +6V, $V_{CC\_}$ = +4.75V to +12.6V, $V_{EE\_}$ = -12.6V to -4.75V, $V_{NN\_}$ = -200V to 0, $V_{PP\_}$ = 0 to ($V_{NN\_}$ + 200V), $V_{SS} \leq$ the lower of V_{NN1} or V_{NN2}, $T_A = T_J = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (EN_, $\overline{SHDN}$, INN_, INP_, INC_)						
Low-Level Input Voltage	V_{IL}				0.25 x V_{DD}	V
High-Level Input Voltage	V_{IH}		0.75 x V_{DD}			V
Logic-Input Capacitance	C_{IN}			5		pF
Logic-Input Leakage (INC_, $\overline{SHDN}$, EN_ Only)	I_{IN}	V_{IN} = 0V or V_{DD}	-1		+1	µA
Pulldown Resistor (INN_, INP_ Only)	R_{PIN}		7	10	13	kΩ
OUTPUT (OUT_)						
OUT_ Output-Voltage Range	$V_{OUT\_}$	No load at OUT_	$V_{NN\_}$		$V_{PP\_}$	V
		100mA load	$V_{NN\_}$ + 2.5		$V_{PP\_}$ - 2.5	
Low-Side Small-Signal Output Impedance	R_{SOL}	$I_{ON\_}$ = -100mA, $V_{CC\_}$ = +12V ±5%, DC-coupled		9	17	Ω
		$I_{ON\_}$ = -100mA, $V_{CC\_}$ = +5V ±5%, DC-coupled		9.5	18	
High-Side Small-Signal Output Impedance	R_{HOS}	$I_{OP\_}$ = -100mA, $V_{CC\_}$ = +12V ±5%, DC-coupled		10.5	17	Ω
		$I_{OP\_}$ = -100mA, $V_{CC\_}$ = +5V ±5%, DC-coupled		12	18	
Low-Side Output Current	I_{OL}	$V_{CC\_}$ = +12V ±5%, $V_{OUT\_}$ - $V_{NN\_}$ = 100V	1.3	2.5		A
High-Side Output Current	I_{OH}	$V_{CC\_}$ = +12V ±5%, $V_{OUT\_}$ - $V_{PP\_}$ = 100V	1.3	2		A
Off-Output Capacitance	$C_{O(OFF)}$	OP_, ON_, OCP_ and OCN_ connected together, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V		45		pF
Off-Output Leakage Current	I_{LK}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $V_{EN\_}$ = 0V, $V_{OUT\_}$ = -100V to +100V	-1		+1	µA
Low-Side Signal-Clamp Output Impedance	R_{CLS}	$I_{OCN\_}$ = -100mA, DC-coupled, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$		22	50	Ω
		$I_{OCN\_}$ = -100mA, DC-coupled, $V_{CC\_}$ = +5V ±5%, $V_{EE\_}$ = $-V_{CC\_}$		24	65	
High-Side Signal-Clamp Output Impedance	R_{CHS}	$I_{OCP\_}$ = -100mA, DC-coupled, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$		28	50	Ω
		$I_{OCP\_}$ = -100mA, DC-coupled, $V_{CC\_}$ = +5V ±5%, $V_{EE\_}$ = $-V_{CC\_}$		38	65	
Low-Side Gate Short Impedance	R_{LSH}	$V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$, $I_{CGN\_}$ = 10mA, $V_{EN\_}$ = 0V			100	Ω
		$V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$, $I_{CGN\_}$ = 10mA, $V_{EN\_}$ = V_{DD}	5	7.5	10	kΩ

*The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.

ELECTRICAL CHARACTERISTICS* (continued)

(V_{DD} = +2.7V to +6V, $V_{CC\_}$ = +4.75V to +12.6V, $V_{EE\_}$ = -12.6V to -4.75V, $V_{NN\_}$ = -200V to 0, $V_{PP\_}$ = 0 to ($V_{NN\_}$ + 200V), $V_{SS} \leq$ the lower of V_{NN1} or V_{NN2}, $T_A = T_J = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-Side Gate Short Impedance	R_{HSH}	$V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$, $I_{CGP\_}$ = 10mA, $V_{EN\_}$ = 0V			100	Ω
		$V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$, $I_{CGP\_}$ = 10mA, $V_{EN\_}$ = V_{DD}	5	7.5	10	kΩ
THERMAL SHUTDOWN						
Thermal Shutdown	T_{HDN}	Junction temperature rising		150		°C
Thermal-Shutdown Hysteresis				20		°C
DYNAMIC CHARACTERISTICS (R_L = 100Ω, C_L = 100pF, unless otherwise noted.)						
Logic Input to Output Rise Propagation Delay	t_{PLH}	$V_{CC\_}$ = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, Figure 1		15		ns
Logic Input to Output Fall Propagation Delay	t_{PHL}	$V_{CC\_}$ = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, Figure 1		15		ns
Logic Input to Output Rise Propagation Delay	t_{POH}	$V_{CC\_}$ = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, Figure 1		15		ns
Logic Input to Output Fall Propagation Delay	t_{POL}	$V_{CC\_}$ = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, Figure 1		15		ns
Logic Input to Output Rise Propagation Delay Clamp	t_{PHO}	$V_{CC\_}$ = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, Figure 1		15		ns
Logic Input to Output Fall Propagation Delay Clamp	t_{PLO}	$V_{CC\_}$ = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, Figure 1		15		ns
OUT_ Rise Time (GND to $V_{PP\_}$)	t_{ROP}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$, Figure 1		9	20	ns
OUT_ Rise Time ($V_{NN\_}$ to GND)	t_{RNO}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$, Figure 1		17	35	ns
OUT_ Rise Time ($V_{NN\_}$ to $V_{PP\_}$)	t_{RNP}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$, Figure 1		10.5	35	ns
OUT_ Fall Time (GND to $V_{NN\_}$)	t_{FON}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$, Figure 1		9	20	ns
OUT_ Fall Time ($V_{PP\_}$ to GND)	t_{FPO}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$, Figure 1		17	35	ns
OUT_ Fall Time ($V_{PP\_}$ to $V_{NN\_}$)	t_{FPN}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$, Figure 1		10.5	35	ns
OUT_ Enable Time from EN_ (Figure 2)	t_{EN}	$V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$			100	ns
		$V_{CC\_}$ = +5V ±5%, $V_{EE\_}$ = $-V_{CC\_}$			150	
OUT_ Disable Time from EN_ (Figure 2)	t_{DI}	$V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$			100	ns
		$V_{CC\_}$ = +5V ±5%, $V_{EE\_}$ = $-V_{CC\_}$			150	
Clamp Enable Time from INC_ (Figure 3)	t_{EN-CL}	$V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$			100	ns
		$V_{CC\_}$ = +5V ±5%, $V_{EE\_}$ = $-V_{CC\_}$			150	

*The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.

ELECTRICAL CHARACTERISTICS* (continued)

(V_{DD} = +2.7V to +6V, $V_{CC\_}$ = +4.75V to +12.6V, $V_{EE\_}$ = -12.6V to -4.75V, $V_{NN\_}$ = -200V to 0, $V_{PP\_}$ = 0 to ($V_{NN\_}$ + 200V), $V_{SS} \leq$ the lower of V_{NN1} or V_{NN2}, $T_A = T_J = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clamp Disable Time from INC_ (Figure 3)	t_{DI-CL}	$V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$			100	ns
		$V_{CC\_}$ = +5V ±5%, $V_{EE\_}$ = $-V_{CC\_}$			150	
Short Enable Time from EN_ (Figure 4)	t_{EN-SH}	$V_{PP\_}$ = +12V, $V_{NN\_}$ = 0V, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$			1000	ns
		$V_{PP\_}$ = +5V, $V_{NN\_}$ = 0V, $V_{CC\_}$ = +5V ±5%, $V_{EE\_}$ = $-V_{CC\_}$			1000	
Short Disable Time from EN_ (Figure 4)	t_{DI-SH}	$V_{PP\_}$ = +12V, $V_{NN\_}$ = 0V, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = $-V_{CC\_}$			250	ns
		$V_{PP\_}$ = +5V, $V_{NN\_}$ = 0V, $V_{CC\_}$ = +5V ±5%, $V_{EE\_}$ = $-V_{CC\_}$			250	
INP_ to INN_ Fault Overlap Detection Time (Figure 5)	t_{OV}	V_{DD} = +3.3V ±5%	2			ns
Recovery Time from Fault Condition (Figure 6)	t_{REC}	V_{DD} = +3.3V, $V_{CC\_}$ = +12V ±5%		50	120	ns
Crosstalk		$V_{PP\_}$ = $V_{CC\_}$ = +5V, $V_{NN\_}$ = $V_{EE\_}$ = -5V, f = 5MHz		69		dB
2nd Harmonic Distortion	2HD	$V_{PP\_}$ = $-V_{NN\_}$ = 100V, f_{OUT} = 5MHz, $V_{CC\_}$ = 12V		-48		dB
RMS Output Jitter	t_J	$V_{CC\_}$ = 12V		9		ps

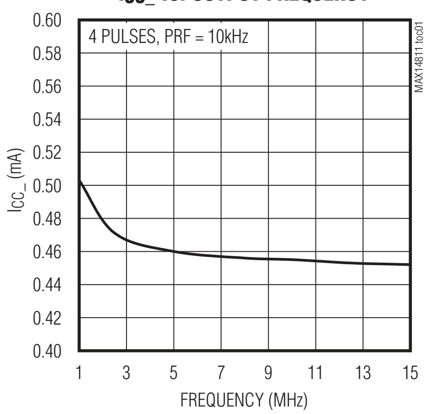
Note 3: All units are 100% production tested at T_A = +70°C. Specifications over operating temperature range are guaranteed by design.

The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.

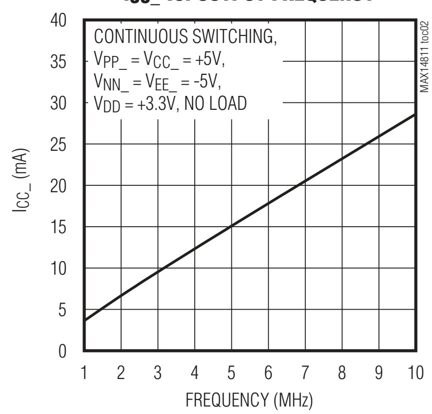
Typical Operating Characteristics

(V_{DD} = +3.3V, $V_{CC\_}$ = +12V, $V_{EE\_}$ = -12V, V_{SS} = -100V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $f_{OUT\_}$ = 5MHz, T_A = +25°C, unless otherwise noted.)

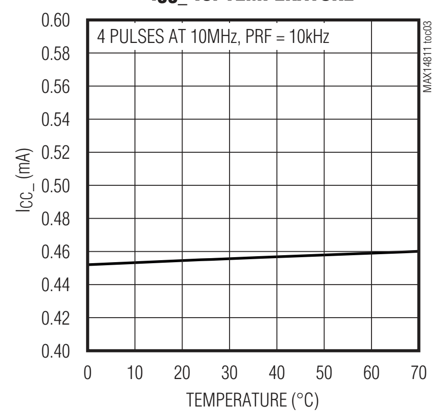
$I_{CC\_}$ vs. OUTPUT FREQUENCY



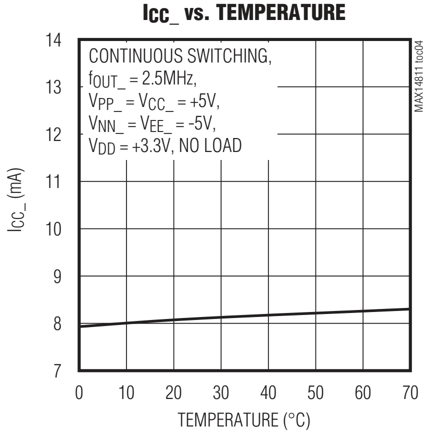
$I_{CC\_}$ vs. OUTPUT FREQUENCY



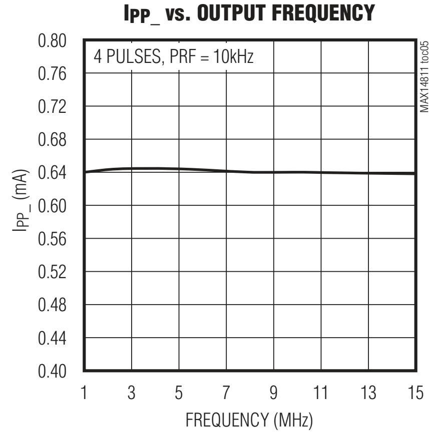
$I_{CC\_}$ vs. TEMPERATURE



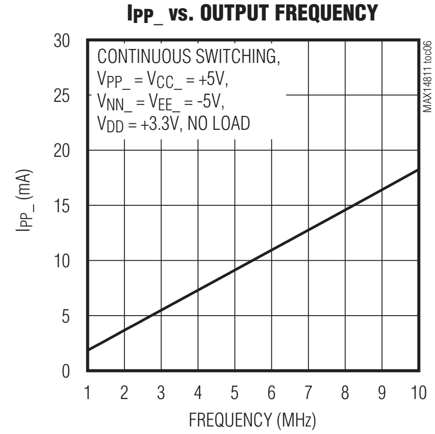
$I_{CC\_}$ vs. TEMPERATURE



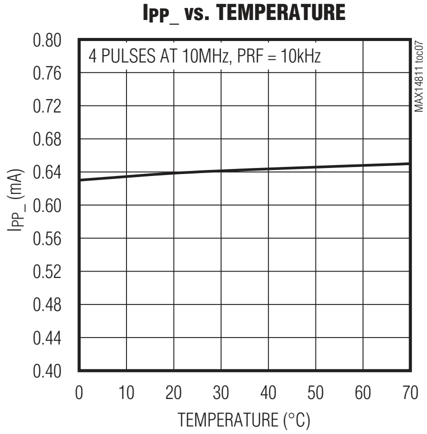
$I_{PP\_}$ vs. OUTPUT FREQUENCY



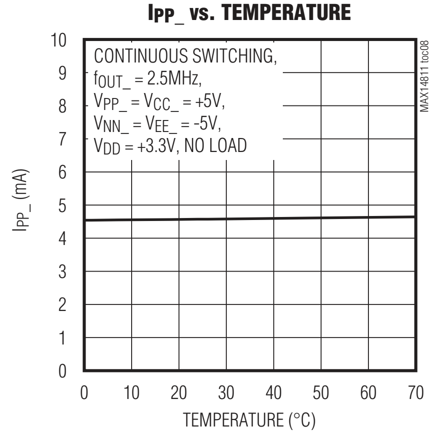
$I_{PP\_}$ vs. OUTPUT FREQUENCY



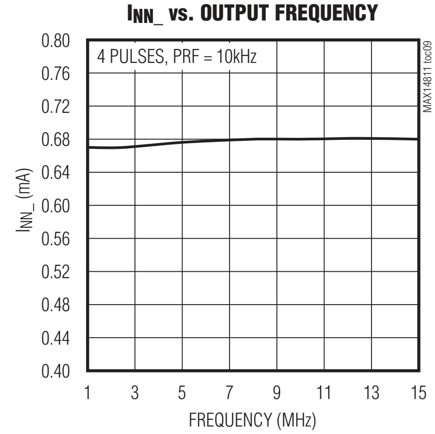
$I_{PP\_}$ vs. TEMPERATURE



$I_{PP\_}$ vs. TEMPERATURE



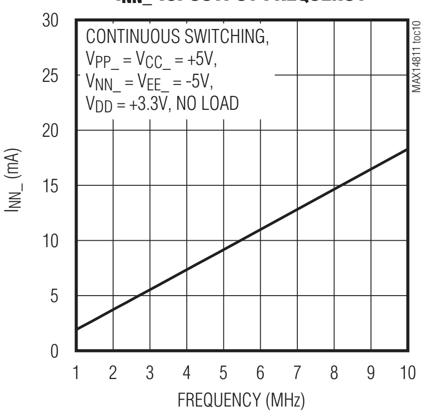
$I_{NN\_}$ vs. OUTPUT FREQUENCY



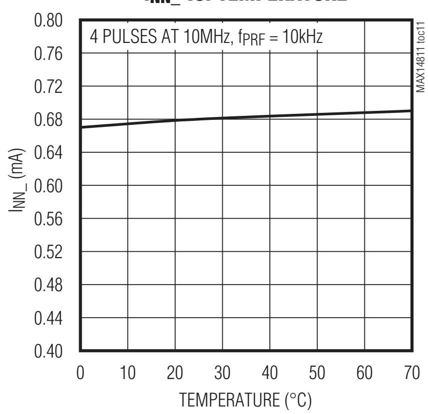
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, $V_{CC\_}$ = +12V, $V_{EE\_}$ = -12V, V_{SS} = -100V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $f_{OUT\_}$ = 5MHz, T_A = +25°C, unless otherwise noted.)

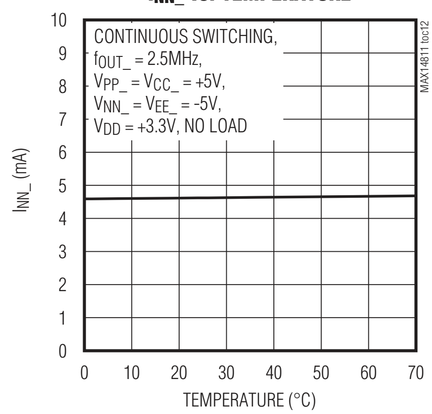
$I_{NN\_}$ vs. OUTPUT FREQUENCY



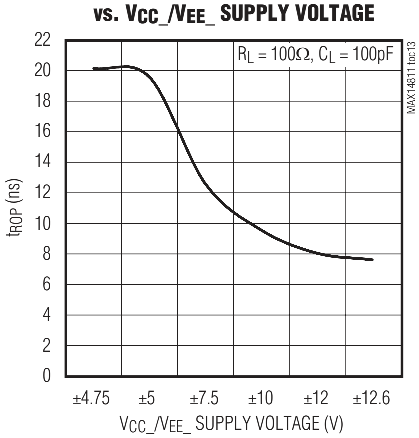
$I_{NN\_}$ vs. TEMPERATURE



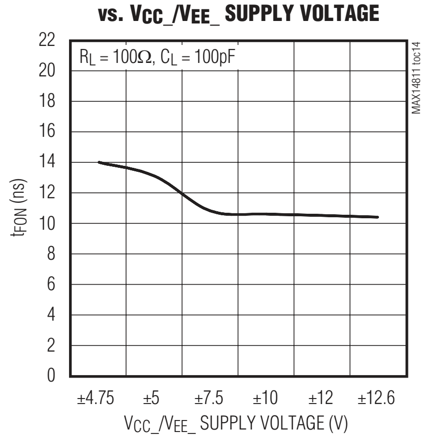
$I_{NN\_}$ vs. TEMPERATURE



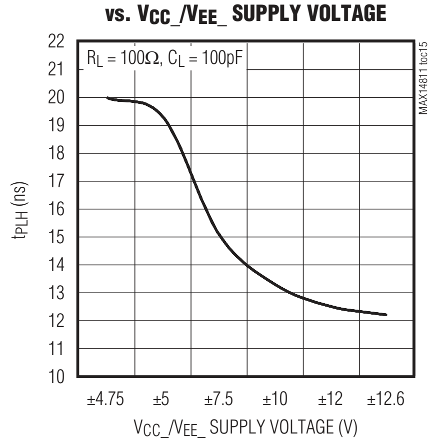
OUT_ RISE TIME (GND TO $V_{PP\_}$) vs. $V_{CC\_}/V_{EE\_}$ SUPPLY VOLTAGE



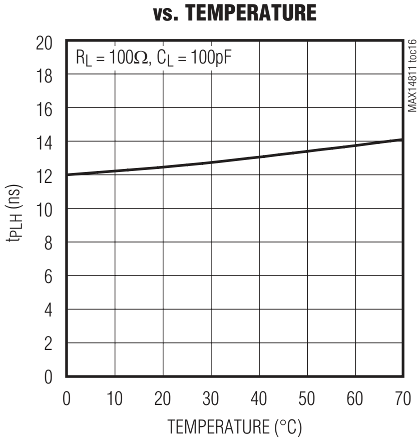
OUT_ FALL TIME (GND TO $V_{NN\_}$) vs. $V_{CC\_}/V_{EE\_}$ SUPPLY VOLTAGE



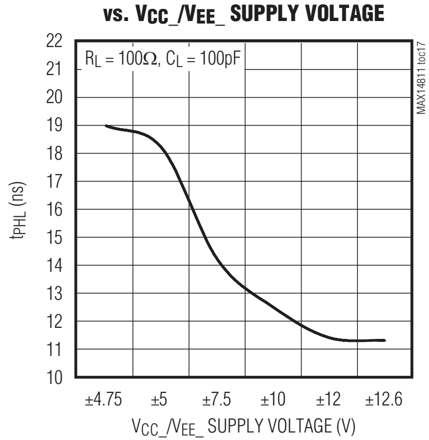
INP_-TO-OUT_ RISE PROPAGATION DELAY vs. $V_{CC\_}/V_{EE\_}$ SUPPLY VOLTAGE



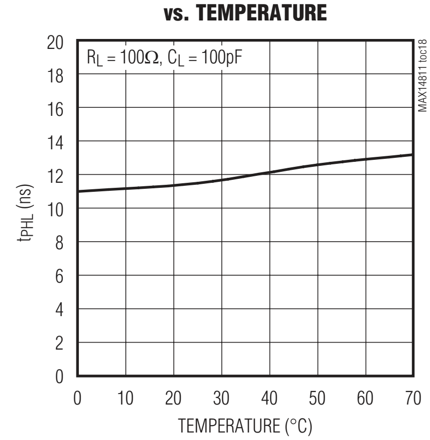
INP_-TO-OUT_ RISE PROPAGATION DELAY vs. TEMPERATURE



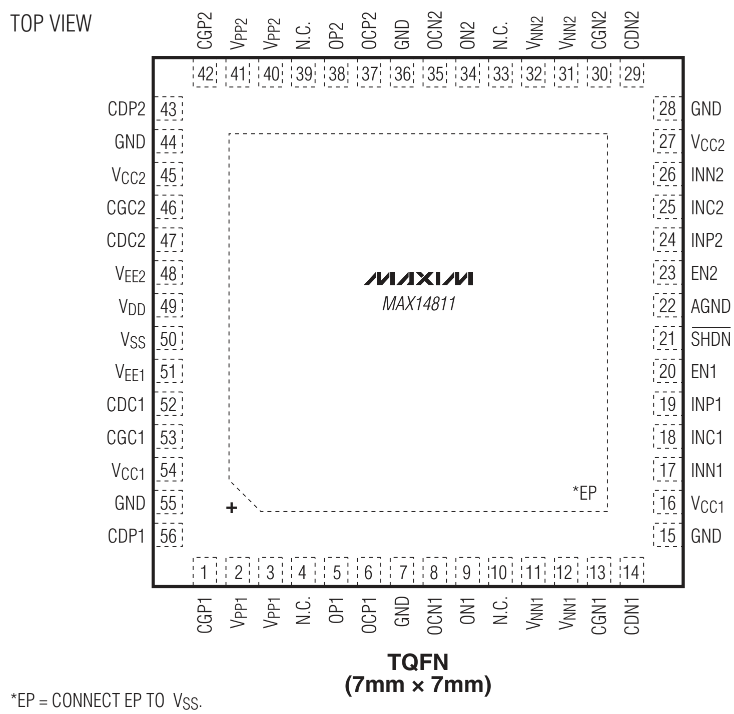
INP_-TO-OUT_ FALL PROPAGATION DELAY vs. $V_{CC\_}/V_{EE\_}$ SUPPLY VOLTAGE



INP_-TO-OUT_ FALL PROPAGATION DELAY vs. TEMPERATURE



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	CGP1	Channel 1 High-Side Gate Input. Connect a 1nF to 10nF capacitor between CDP1 and CGP1 as close as possible to the device.
2, 3	V_{PP1}	Channel 1 High-Side Positive Supply-Voltage Input. Bypass V_{PP1} to GND with a 0.1µF capacitor as close as possible to the device. Depending on the pulser lead, additional bypassing may be required (see the *Power Supplies and Bypassing* section).
4, 10, 33, 39	N.C.	No Connection. Not connected internally.
5	OP1	Channel 1 High-Side Drain Output
6	OCP1	Channel 1 High-Side Clamp Output
7, 15, 28, 36, 44, 55	GND	Ground
8	OCN1	Channel 1 Low-Side Clamp Output
9	ON1	Channel 1 Low-Side Drain Output
11, 12	V_{NN1}	Channel 1 High-Side Negative Supply-Voltage Input. Bypass V_{NN1} to GND with a 0.1µF capacitor as close as possible to the device. Depending on the pulser lead, additional bypassing may be required (see the *Power Supplies and Bypassing* section).

Pin Description (continued)

PIN	NAME	FUNCTION
13	CGN1	Channel 1 Low-Side Gate Input. Connect a 1nF to 10nF capacitor between CDN1 and CGN1 as close as possible to the device.
14	CDN1	Channel 1 Low-Side Driver Output. Connect a 1nF to 10nF capacitor between CDN1 and CGN1 as close as possible to the device.
16, 54	V_{CC1}	Channel 1 Gate-Drive Supply-Voltage Input. Bypass V_{CC1} to GND with a 0.1µF capacitor as close as possible to the device.
17	INN1	Channel 1 Low-Side Logic Input (Table 1). INN1 has a 10kΩ pulldown resistor.
18	INC1	Channel 1 Clamp Logic Input. Clamps OCP1 and OCN1 are turned on when INC1 is high and when INP1 and INN1 are low and $\overline{\text{SHDN}}$ and EN1 are high (Table 1).
19	INP1	Channel 1 High-Side Logic Input (Table 1). INP1 has a 10kΩ pulldown resistor.
20	EN1	Channel 1 Enable Logic Input. Drive EN1 high to enable OP1, ON1, OCN1, and OCP1. Pull EN1 low to turn on the gate-source short circuit (Table 1).
21	$\overline{\text{SHDN}}$	Active-Low Shutdown Logic Input (Table 1)
22	AGND	Analog Ground. AGND must be connected to common GND.
23	EN2	Channel 2 Enable Logic Input. Drive EN2 high to enable OP2, ON2, OCN2, and OCP2. Pull EN2 low to turn on the gate-source short circuit (Table 1).
24	INP2	Channel 2 High-Side Logic Input (Table 1). INP2 has a 10kΩ pulldown resistor.
25	INC2	Channel 2 Clamp Logic Input. Clamps OCP2 and OCN2 are turned on when INC2 is high and when INP2 and INN2 are low and $\overline{\text{SHDN}}$ and EN2 are high (Table 1).
26	INN2	Channel 2 Low-Side Logic Input (Table 1). INN2 has a 10kΩ pulldown resistor.
27, 45	V_{CC2}	Channel 2 Gate-Drive Supply-Voltage Input. Bypass V_{CC2} to GND with a 0.1µF capacitor as close as possible to the device.
29	CDN2	Channel 2 Low-Side Driver Output. Connect a 1nF to 10nF capacitor between CDN2 and CGN2 as close as possible to the device.
30	CGN2	Channel 2 Low-Side Gate Input. Connect a 1nF to 10nF capacitor between CDN2 and CGN2 as close as possible to the device.
31, 32	V_{NN2}	Channel 2 High-Side Negative Supply-Voltage Input. Bypass V_{NN2} to GND with a 0.1µF capacitor as close as possible to the device. Depending on the output, additional bypassing may be required (see the *Power Supplies and Bypassing* section).
34	ON2	Channel 2 Low-Side Drain Output
35	OCN2	Channel 2 Low-Side Clamp Output
37	OCP2	Channel 2 High-Side Clamp Ouput
38	OP2	Channel 2 High-Side Drain Ouput
40, 41	V_{PP2}	Channel 2 High-Side Positive Supply-Voltage Input. Bypass V_{PP2} to GND with a 0.1µF capacitor as close as possible to the device. Depending on the pulser lead, additional bypassing may be required (see the *Power Supplies and Bypassing* section).
42	CGP2	Channel 2 High-Side Gate Input. Connect a 1nF to 10nF capacitor between CDP2 and CGP2 as close as possible to the device.
43	CDP2	Channel 2 High-Side Driver Output. Connect a 1nF to 10nF capacitor between CDP2 and CGP2 as close as possible to the device.

Pin Description (continued)

PIN	NAME	FUNCTION
46	CGC2	Channel 2 High-Side Clamp Gate Input. Connect a 1nF to 10nF capacitor between CDC2 and CGC2 as close as possible to the device.
47	CDC2	Channel 2 High-Side Clamp Driver Output. Connect a 1nF to 10nF capacitor between CDC2 and CGC2 as close as possible to the device.
48	V_{EE2}	Channel 2 Negative Supply Input. $\|V_{EE2}\| \leq \|V_{CC2}\|$. Gate-drive supply voltage for the OCP2 clamp. Bypass V_{EE2} to GND with a 0.1µF capacitor as close as possible to the device.
49	V_{DD}	Logic Supply-Voltage Input. Bypass V_{DD} to GND with a 0.1µF capacitor as close as possible to the device. Depending on the pulser lead, additional bypassing may be required (see the *Power Supplies and Bypassing* section).
50	V_{SS}	Substrate Voltage. Connect V_{SS} to a voltage equal to or more negative than the more negative of V_{NN1} or V_{NN2}. Bypass V_{SS} to GND with a 0.1µF capacitor as close as possible to the device.
51	V_{EE1}	Channel 1 Negative Supply Input. $\|V_{EE1}\| \leq \|V_{CC1}\|$. Gate-drive supply voltage for the OCP1 clamp. Bypass V_{EE1} to GND with a 0.1µF capacitor as close as possible to the device.
52	CDC1	Channel 1 High-Side Clamp Driver Output. Connect a 1nF to 10nF capacitor between CDC1 and CGC1 as close as possible to the device.
53	CGC1	Channel 1 High-Side Clamp Gate Input. Connect a 1nF to 10nF capacitor between CDC1 and CGC1 as close as possible to the device.
56	CDP1	Channel 1 High-Side Driver Output. Connect a 1nF to 10nF capacitor between CDP1 and CGP1 as close as possible to the device.
—	EP	Exposed Pad. EP must be connected to V_{SS}. Do not use EP as the only V_{SS} connection for the device.

Detailed Description

The MAX14811 integrated circuit generates high-voltage, high-frequency unipolar or bipolar pulses from low-voltage logic inputs. The dual pulser features independent logic inputs, independent high-voltage pulser outputs with active clamps, and independent high-voltage supply inputs.

The device features fault condition management to protect the outputs. The outputs enter three-state if both INP_ and INN_ are logic-high. The device has a 9Ω output impedance for the high-voltage outputs and a 27Ω impedance for the active clamp. The high-voltage outputs are guaranteed to provide 2.0A (typ) output current. All the pulser outputs and clamp outputs have overvoltage protection.

The device uses three logic inputs per channel to control the positive and negative pulses and active clamp. Also included are two independent enable inputs. Disabling EN_ ensures the output MOSFETs are not accidentally turned on during fast power-supply ramping. This allows for faster ramp times and shorter delays between pulsing modes. A low-power shutdown mode reduces power consumption to less than 1µA. All digital inputs are CMOS compatible.

Logic Inputs (INP_, INN_, INC_, EN_, $\overline{\text{SHDN}}$)

The device has a total of nine logic-input signals. $\overline{\text{SHDN}}$ controls the power-up and power-down of the device. There are two sets of INP_, INN_, INC_, and EN_ signals: one for each channel. Each INP_ and INN_ input has a 10kΩ (typ) pulldown resistor. INP_ controls the on and off states of the high-side FET, INN_ controls the on and off states of the low-side FET, INC_ controls the active clamp, and EN_ controls the gate-to-source short. These signals give complete control of the output stage of each driver (see Table 1 for all logic combinations).

The device logic inputs are CMOS-logic-compatible and the logic levels are referenced to V_{DD} for maximum flexibility. The low 5pF (typ) input capacitance of the logic inputs reduces loading and increases switching speed.

Table 1. Truth Table

INPUTS					OUTPUTS			STATE
$\overline{\text{SHDN}}$	EN_	INP_	INN_	INC_	OP_	ON_	OCP_, OCN_	
0	X	X	X	X	High Impedance	High Impedance	High Impedance	Power-down, INP_/INN_ disabled, gate-source short disabled, clamp disabled.
1	0	X	X	X	High Impedance	High Impedance	High Impedance	Power-down, INP_/INN_ disabled, gate-source short enabled, clamp disabled.
1	1	0	0	0	High Impedance	High Impedance	High Impedance	Power-up, all inputs enabled, gate-source short disabled.
1	1	0	0	1	High Impedance	High Impedance	GND	Power-up, all inputs enabled, gate-source short disabled.
1	1	0	1	X	High Impedance	$V_{NN\_}$	High Impedance	Power-up, all inputs enabled, gate-source short disabled.
1	1	1	0	X	$V_{PP\_}$	High Impedance	High Impedance	Power-up, all inputs enabled, gate-source short disabled.
1	1	1	1	X	High Impedance	High Impedance	High Impedance	Fault condition if INP_ = 1 and INN_ = 1 for more than 5.5ns.

X = Don't care, 0 = Logic-low, 1 = Logic-high.

High-Voltage Output Protection

The device's high-voltage outputs feature an integrated overvoltage protection circuit that allows the user to implement multilevel pulsing by connecting the outputs of multiple pulser channels in parallel. Internal diodes in series with the ON_ and OP_ outputs prevent the body diode of the high-side and low-side FETs from switching on when a voltage greater than $V_{NN\_}$ or $V_{PP\_}$ is present on the output. See the *Functional Diagram*.

Active Clamps

The device features an active clamp circuit to improve pulse quality and reduce 2nd harmonic output. The clamp circuit consists of an n-channel (DC-coupled) and a p-channel (AC and DC delay coupled) high-voltage FETs that are switched on or off by the logic clamp input (INC_). The device features protected clamp devices, allowing the clamp circuit to be used in bipolar pulsing circuits (see the *Functional Diagram* and Figure 1). A diode in series with the OCN_ output prevents the body diode of the low-side FET from turning on when a voltage lower than GND is present. Another diode in series with the OCP_ output prevents the body diode of the high-side FET from turning on when a voltage higher than ground is present.

The user can connect the active clamp input (INC_) to a logic-high voltage and drive only the INP_ and INN_ inputs to minimize the number of signals used to drive the device. In this case, whenever both the INP_ and INN_ inputs are low and the INC_ input is high, the active clamp circuit pulls the output to GND through the OCP_ and OCN_ outputs (see Table 1 for more information).

Fault Protection

The device features fault protection management to protect the outputs. When INP_ and INN_ are both logic-high, the outputs (OP_, ON_, OCP_, and OCN_) enter a high-Z state.

Power-Supply Ramping and Gate-Source Short Circuit

The device includes a gate-source short circuit that is controlled by the enable input (EN_). When $\overline{\text{SHDN}}$ is high and EN_ is low, a 60Ω switch shorts together the gate and source of the high-side output FET. At the same time, a similar switch shorts the gate and source of the low-side output FET (Table 1). The gate-source short circuit prevents accidental turn-on of the output FETs due to the ramping voltage on $V_{PP\_}$ and $V_{NN\_}$, and allows for faster ramping rates and smaller delay times between pulsing modes.

Shutdown Mode

$\overline{\text{SHDN}}$ is common to both channel 1 and channel 2 and powers up or down the device. Drive $\overline{\text{SHDN}}$ low to power down all internal circuits (except the clamp circuits). When $\overline{\text{SHDN}}$ is low, the device is in the lowest power state (1µA) and the gate-source short circuit is disabled. The device takes 1µs (typ) to become active when $\overline{\text{SHDN}}$ is disabled.

Thermal Protection

A thermal shutdown circuit with a typical threshold of +150°C prevents damage due to excessive power dissipation. When the junction temperature exceeds T_J = +150°C, all outputs are disabled. Normal operation typically resumes after the IC's junction temperature drops below +130°C.

Applications Information

AC-Coupling Capacitor Selection

The value of all AC-coupling capacitors (between CDP_ and CGP_ and between CDN_ and CGN_) must be between 1nF and 10nF. The voltage rating of the capacitor must be at least as high as $V_{PP\_}$. Place the capacitors as close as possible to the device. Because INP_ and part of INC_ are AC-coupled to the output devices, they cannot be driven high indefinitely when the device is active.

Power Dissipation

The device's power dissipation consists of three major components caused by the current consumption from $V_{CC\_}$, $V_{PP\_}$, and $V_{NN\_}$. The sum of these components ($P_{VCC\_}$, $P_{VPP\_}$, and $P_{VNN\_}$) must be kept below the maximum power-dissipation limit. See the *Typical Operating Characteristics* section for more information on typical supply currents vs. switching frequencies. The device consumes most of the supply current from $V_{CC\_}$ supply to charge and discharge internal nodes such as the gate capacitance of the high-side FET (C_P) and the low-side FET (C_N). Neglecting the small quiescent supply current and a small amount of current used to charge and discharge the capacitances at the internal gate clamp FETs, the power consumption can be estimated as follows:

$$P_{VCC\_} = [(C_N \times V_{CC\_}^2 \times f_{IN}) + (C_P \times V_{CC\_}^2 \times f_{IN})] \times (BRF \times BTD)$$

$$f_{IN} = f_{INN\_} = f_{INP\_}$$

where $f_{INN\_}$ and $f_{INP\_}$ are the switching frequencies of the inputs $\overline{INN\_}$ and $\overline{INP\_}$, respectively, and where BRF is the burst repetition frequency and BTD is the burst time duration. The typical value of the gate capacitances of the power FET are C_N = 0.2nF, C_P = 0.4nF. For an output load that has a resistance of R_L and capacitance of C_L, the power dissipation can be estimated as follows (assume square-wave output and neglect the resistance of the switches):

$$P_{VPP\_} = \left[(C_O + C_L) \times f_{IN} \times (V_{PP\_} - V_{NN\_})\right]^2 + \left[\frac{V_{PP\_}{}^2}{R_L} \times \frac{1}{2}\right] \times (BRF \times BTD)$$

where C_O is the device's output capacitance.

Power Supplies and Bypassing

The device operates from independent supply voltage sets (only V_{DD} and V_{SS} are common to both channels). The logic input circuit operates from a +2.7V to +6V single supply (V_{DD}). The level-shift driver dual supplies, $V_{CC\_}/V_{EE\_}$ operate from ±4.75V to ±12.6V.

The $V_{PP\_}/V_{NN\_}$ high-side and low-side supplies are driven from a single positive supply up to +220V, from a single negative supply up to -200V, or from ±110V dual supplies. Either $V_{PP\_}$ or $V_{NN\_}$ can be set at 0V. Bypass each supply input to ground with a 0.1µF capacitor as close as possible to the device.

Depending on the load of the pulser, additional bypassing may be needed to keep the output of $V_{PP\_}$ and $V_{NN\_}$ stable during output transitions. For example, with C_{OUT} = 100pF and R_{OUT} = 100Ω load, additional 10µF (typ) capacitor is recommended. V_{SS} is the substrate voltage and must be connected to a voltage equal to or more negative than the more negative voltage of V_{NN1} or V_{NN2}.

Exposed Pad and Layout Concerns

The device provides an exposed pad (EP) underneath the TQFN package for improved thermal performance. The EP is internally connected to V_{SS}. Connect EP to V_{SS} externally and do not run traces under the package to avoid possible short circuits. To aid heat dissipation, connect EP to a similarly sized pad on the component side of the PCB. This pad should be connected through to the solder-side copper by several plated holes to a large heat-spreading copper area to conduct heat away from the device.

The device's high-speed pulser requires low-inductance bypass capacitors to their supply inputs. High-speed PCB trace design practices are recommended. Pay particular attention to minimize trace lengths and use sufficient trace width to reduce inductance. Use of surface-mount components is recommended.

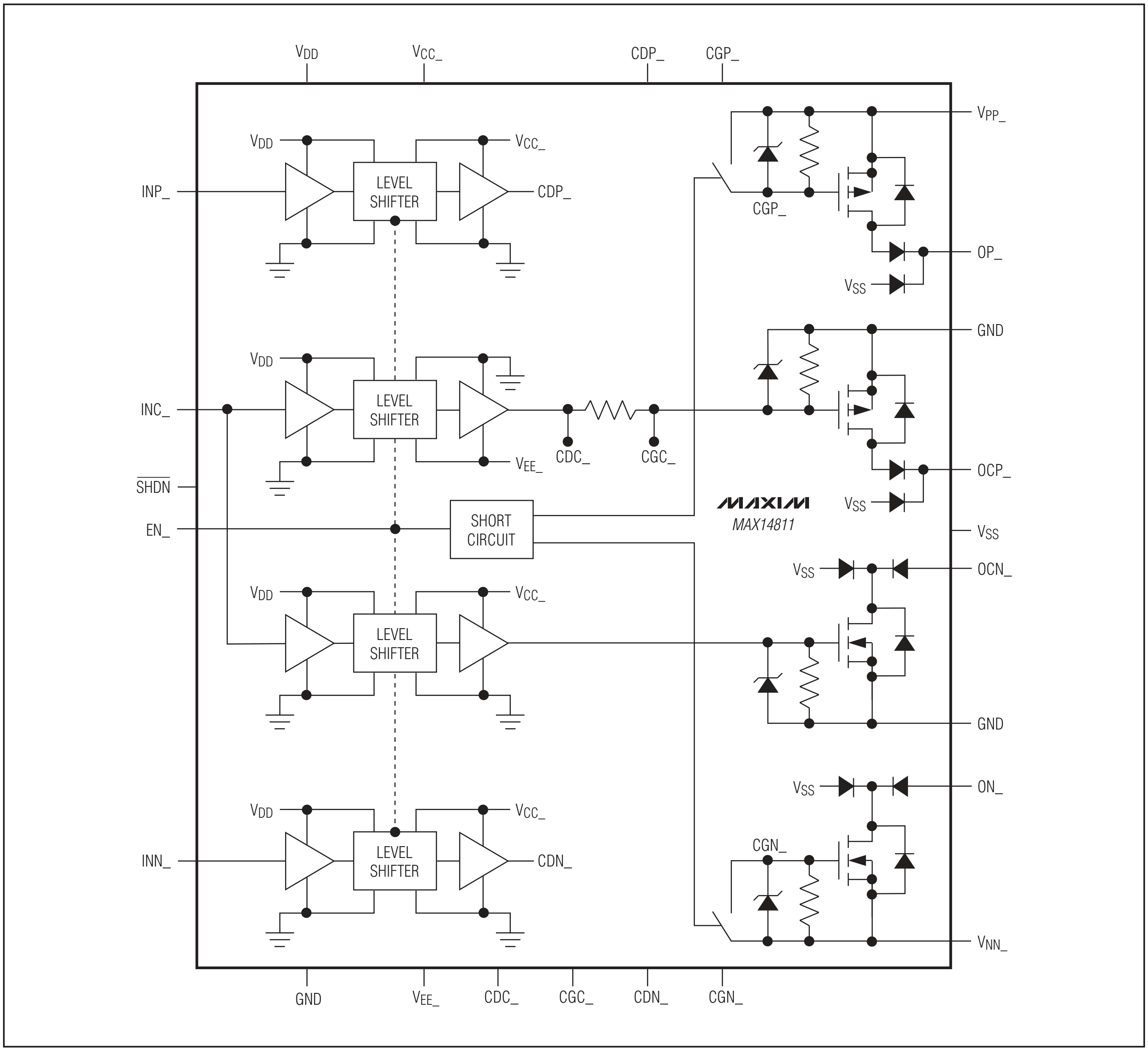
Supply Sequencing

V_{SS} must be lower than or equal to the more negative voltage of V_{NN1} or V_{NN2} at all times. No other power-supply sequencing is required for the device.

Typical Applications Circuit

Figure 7 shows the MAX14811 in a bipolar pulsing application.

Functional Diagram



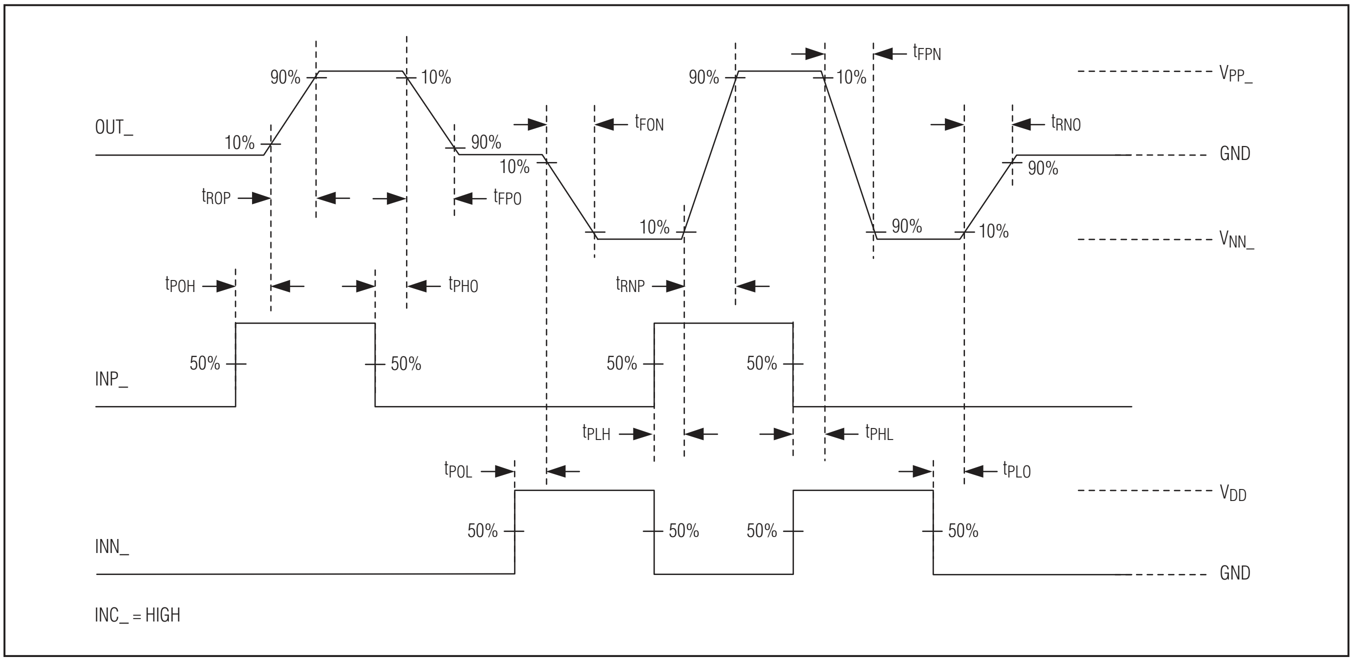


Figure 1. Detailed Timing (R_L = 100Ω, C_L = 100pF)

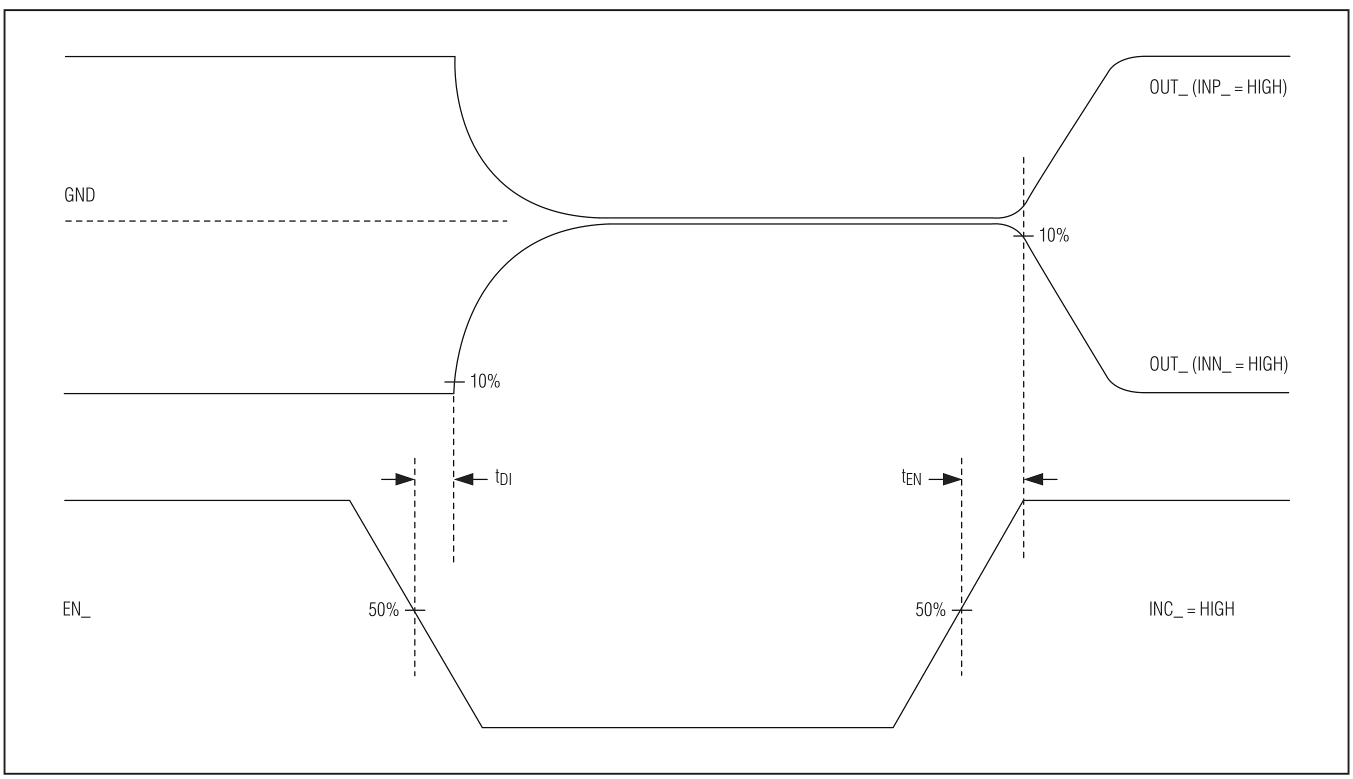


Figure 2. Enable Timing (R_L = 100Ω, C_L = 100pF)

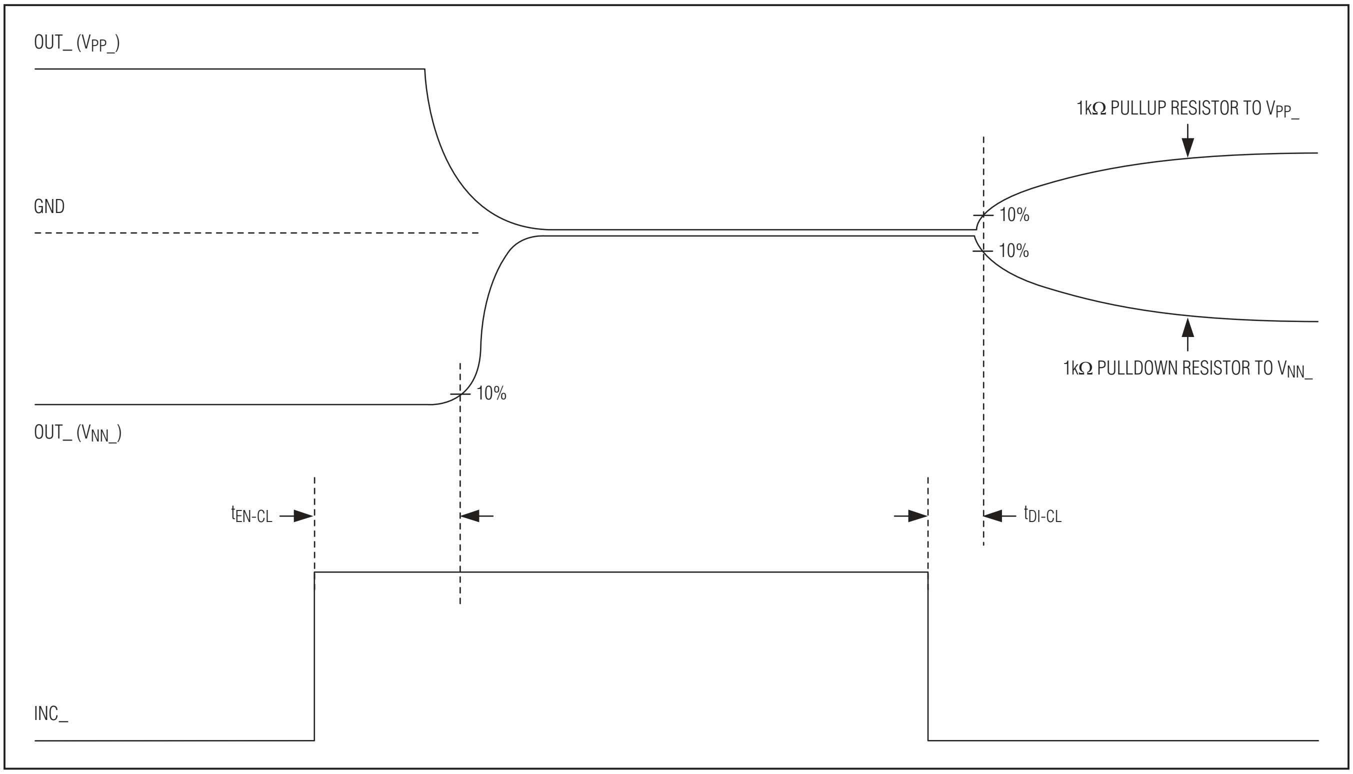


Figure 3. Active Clamp Timing (R_L = 100Ω, C_L = 100pF)

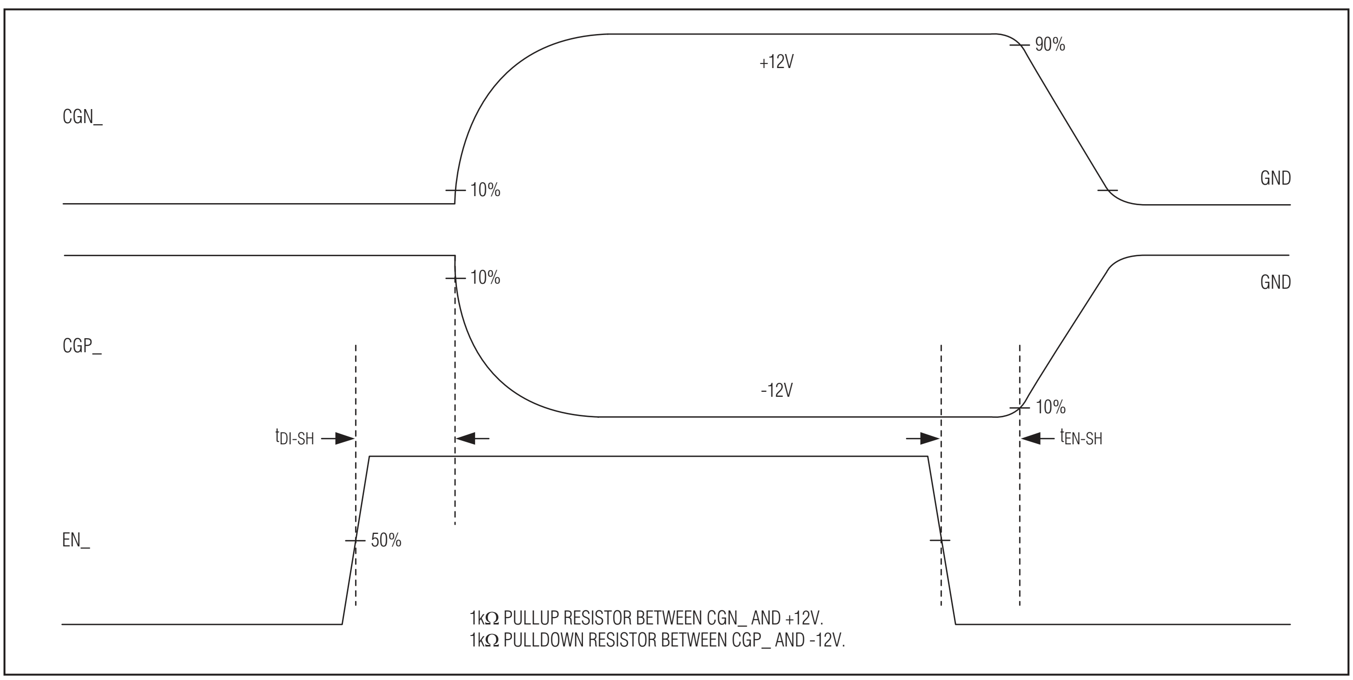


Figure 4. Short-Circuit Timing (R_L = 100Ω, C_L = 100pF)

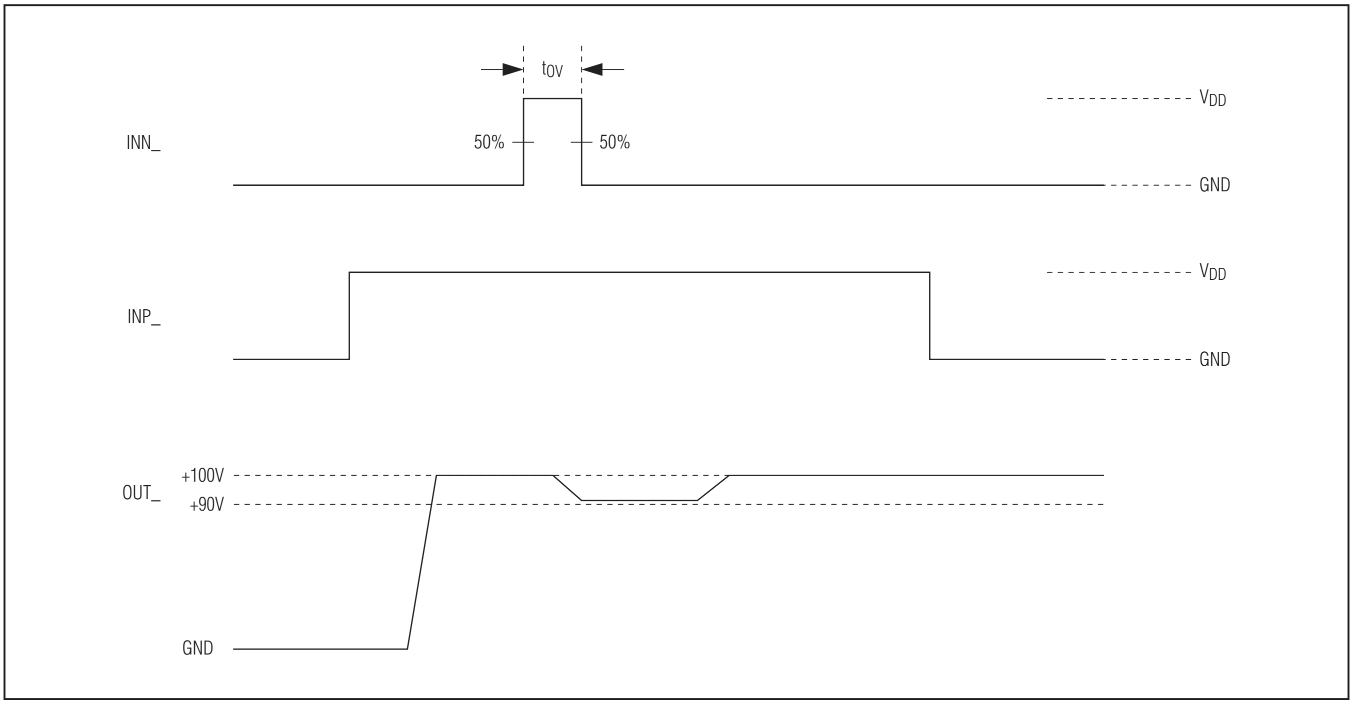


Figure 5. INP_ to INN_ Fault Overlap Detection Timing

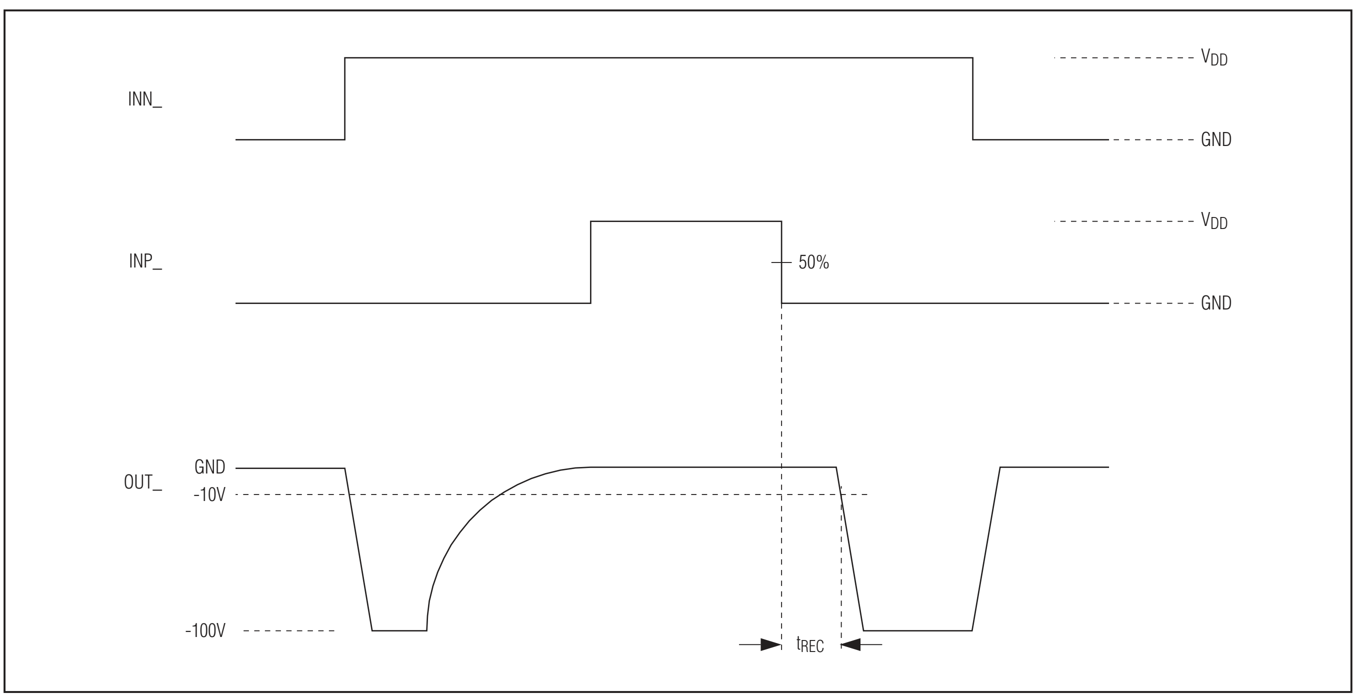


Figure 6. Recovery from Fault Condition Timing

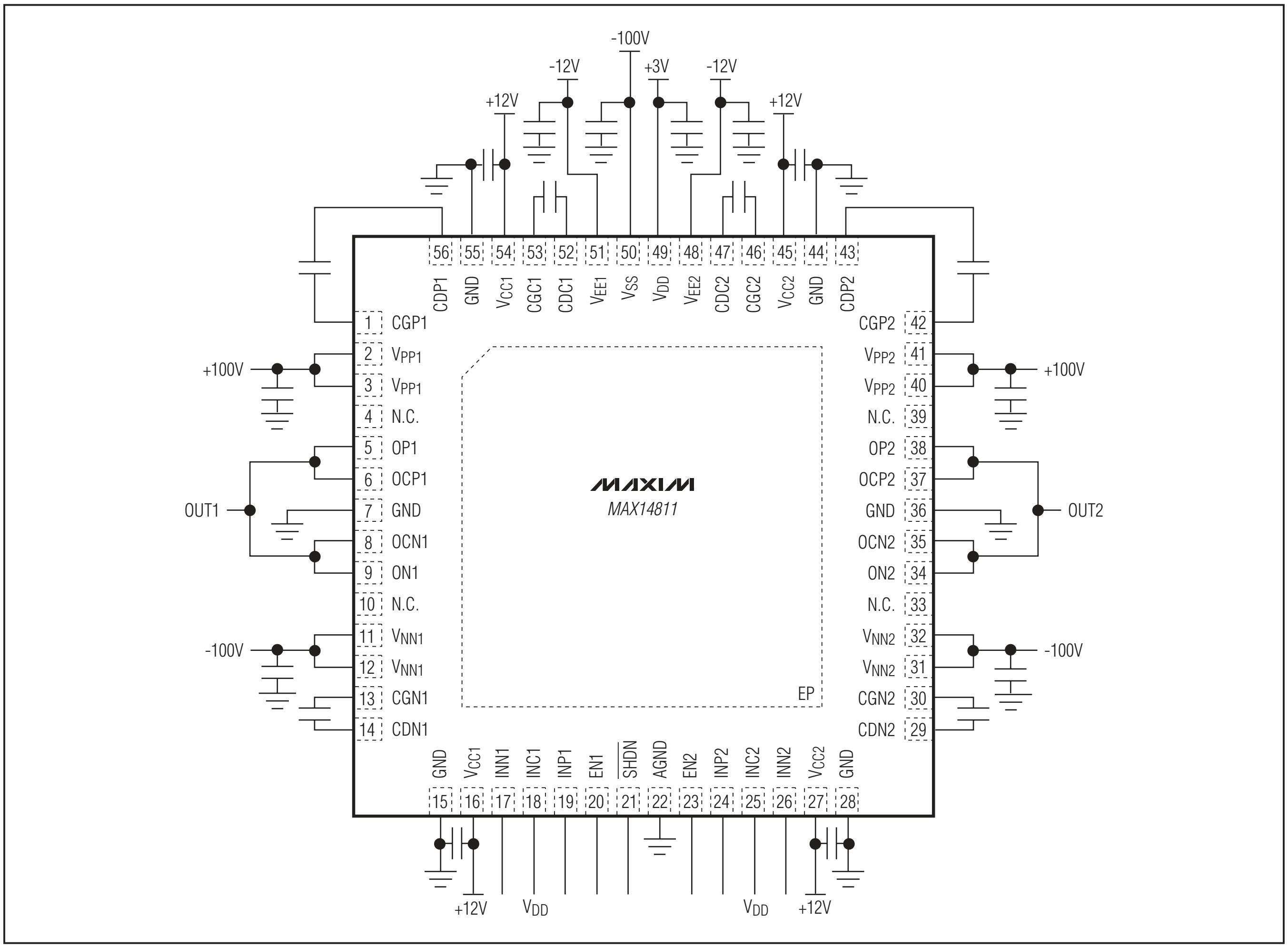


Figure 7. Dual Bipolar Pulsing, ±100V, GND

Ordering Information

PART	TEMP RANGE	PROTECTED OUTPUTS	OUTPUT CURRENT (A)	PIN-PACKAGE
MAX14811CTN+	0°C to +70°C	OCP_, OCN_, OP_, ON_	2.0	56 TQFN-EP*

+*Denotes a lead(Pb)-free/RoHS-compliant package.*
**EP = Exposed pad.*

Warning: The MAX14811 is designed to operate with high voltages. Exercise caution.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
56 TQFN-EP	T5677+1	**21-0144**	**90-0042**

Dual, Unipolar/Bipolar, High-Voltage Digital Pulsers with Fault Condition Management

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—