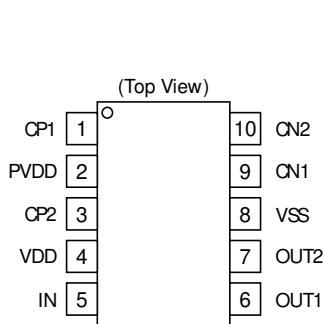
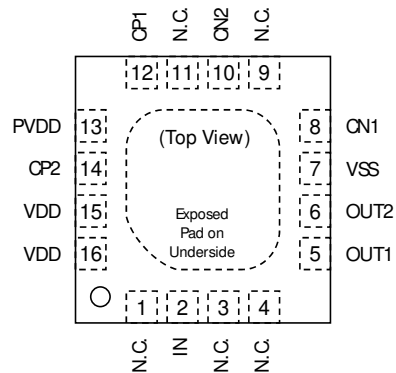




## ■ PIN CONFIGURATIONS



NJW1280RB2  
TVSP10



NJW1280MG2  
EQFN16-G2

SYMBOL	PIN NO.		DESCRIPTION
	MSOP10 (TVSP10)	EQFN16-G2	
N.C.	-	1, 3, 4, 9, 11	-
CP1	1	12	Capacitor Connection Terminal
PVDD	2	13	Charge Pump Output Terminal
CP2	3	14	Capacitor Connection Terminal
VDD	4	15, 16	Power Supply Terminal
IN	5	2	Input Terminal
OUT1	6	5	Output Terminal 1
OUT2	7	6	Output Terminal 2
VSS	8	7	VSS Terminal
CN1	9	8	Capacitor Connection Terminal
CN2	10	10	Capacitor Connection Terminal

Exposed Pad: Connect the Exposed Pad on land of float, or GND

## ■ PRODUCT NAME INFORMATION



## ■ ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJW1280MG2 (TE1)	EQFN16-G2	Yes	Yes	Sn2Bi	1280	6.5	3000
NJW1280RB2 (TE1)	MSOP10 (TVSP10)	Yes	Yes	Sn2Bi	1280	19	2000

## ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V_{DD}$	6.0	V
Input Voltage	$V_{IN}$	-0.3 to $V_{DD}+0.3$	V
Power Dissipation ( $T_a = 25^\circ\text{C}$ ) EQFN16-G2 MSOP10 (TVSP10)	$P_D$	2layer / 4layer 520 / 1400 <sup>(1)</sup> 520 / 730 <sup>(2)</sup>	mW
Storage Temperature	$T_{stg}$	-40 to 150	$^\circ\text{C}$

(1) 2-Layer: Mounted on glass epoxy board (101.5 mm × 114.5 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4) with exposed pad.

4-Layer: Mounted on glass epoxy board (101.5 mm × 114.5 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4) with exposed pad.

(For 4-layer: Applying 99.5 mm × 99.5 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)

(2) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).

4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4), internal Cu area: 74.2 mm × 74.2 mm.

## ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Supply Voltage	$V_{DD}$		2.0 to 5.5	V
Operating Temperature	$T_{opr}$		-40 to 105	$^\circ\text{C}$

**■ ELECTRICAL CHARACTERISTICS**

 (T<sub>a</sub> = 25°C, VDD = 3V, C1 = C2 = 220nF, C<sub>OUT</sub> = 100nF, C<sub>PIEZO</sub> = 30nF, F<sub>IN</sub> = 4kHz, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Charge Pump Output Voltage 1	V <sub>PVDD1</sub>	PVDD terminal (C <sub>PIEZO</sub> = No Load, I <sub>PVDD</sub> = -9mA) <sup>(3)</sup>	8	-	9	V
Charge Pump Output Voltage 2	V <sub>PVDD2</sub>	PVDD terminal, VDD = 5V (C <sub>PIEZO</sub> = No Load, I <sub>PVDD</sub> = -15mA) <sup>(3)</sup>	13.5	-	15	V
Piezo Driver Output Voltage 1	V <sub>OUT1</sub>	Differential Output (OUT1, OUT2)	16.2	18	-	V <sub>PP</sub>
Piezo Driver Output Voltage 2	V <sub>OUT2</sub>	Differential Output (OUT1, OUT2), VDD = 5V	27	30	-	V <sub>PP</sub>
Operating Current 11	I <sub>DD11</sub>	C <sub>PIEZO</sub> = No Load	-	3.5	7	mA
Operating Current 12	I <sub>DD12</sub>	C <sub>PIEZO</sub> = No Load, VDD = 5V	-	4.5	9	mA
Operating Current 21	I <sub>DD21</sub>	Differential application	-	16.5	-	mA
Operating Current 22	I <sub>DD22</sub>	Differential application, VDD = 5V	-	27.5	-	mA
Shutdown Current 1	I <sub>SD1</sub>	IN = 0V <sup>(4)</sup>	-	-	0.5	μA
Shutdown Current 2	I <sub>SD2</sub>	IN = 0V, VDD = 5V	-	-	1	μA
Input Signal Frequency Range	F <sub>IN</sub>	Waveform = Rectangular Pulse	0.2	4	6	kHz
Internal Switching Frequency	F <sub>OSC</sub>		0.3	0.6	1.2	MHz
Turn-On Time	T <sub>ON</sub>	From IN signal High to the OUT1 signal high	-	2	4	ms
Shutdown Delay Time	T <sub>OFF</sub>	DIN = H -> L to PVDD OFF	6	15	30	ms
Output Wave Rise Time	T <sub>R</sub>	OUT1, OUT2, 10% to 90%	-	16	-	μs
Output Wave Fall Time	T <sub>F</sub>	OUT1, OUT2, 90% to 10%	-	10	-	μs

(3) It does not guarantee the use of any method other than the use of the application circuit.

 (4) IN has been low at least T<sub>OFF(max)</sub>.

**■ INPUT TERMINAL CHARACTERISTICS** (T<sub>a</sub> = 25°C, VDD = 3V, unless otherwise specified)

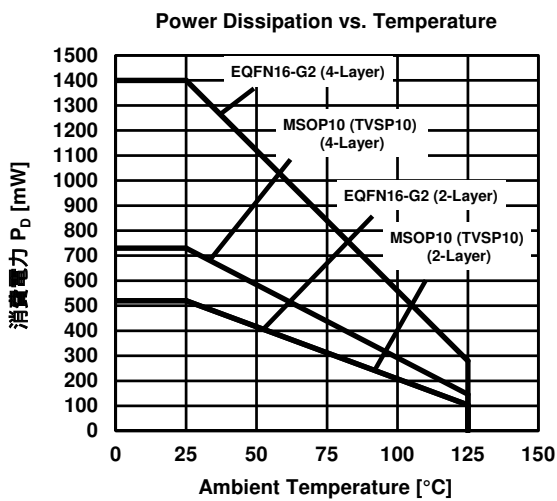
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
High Level Input Voltage 1	V <sub>IH1</sub>	IN terminal	1.6	-	VDD	V
Low Level Input Voltage 1	V <sub>IL1</sub>	IN terminal	0	-	0.4	V
High Level Input Current	I <sub>IH</sub>	IN terminal, IN = 3V	-	3	4	μA
Low Level Input Current	I <sub>IL</sub>	IN terminal, IN = 0V	-	-	1	μA

## ■ THERMAL CHARACTERISTICS

PACKAGE	SYMBOL	VALUE	UNIT
Junction-to-ambient		2layer / 4layer	
EQFN16-G2	$\theta_{ja}$	239.4 / 89.8 <sup>(5)</sup>	°C/W
MSOP10 (TVSP10)		240.3 / 171.6 <sup>(6)</sup>	

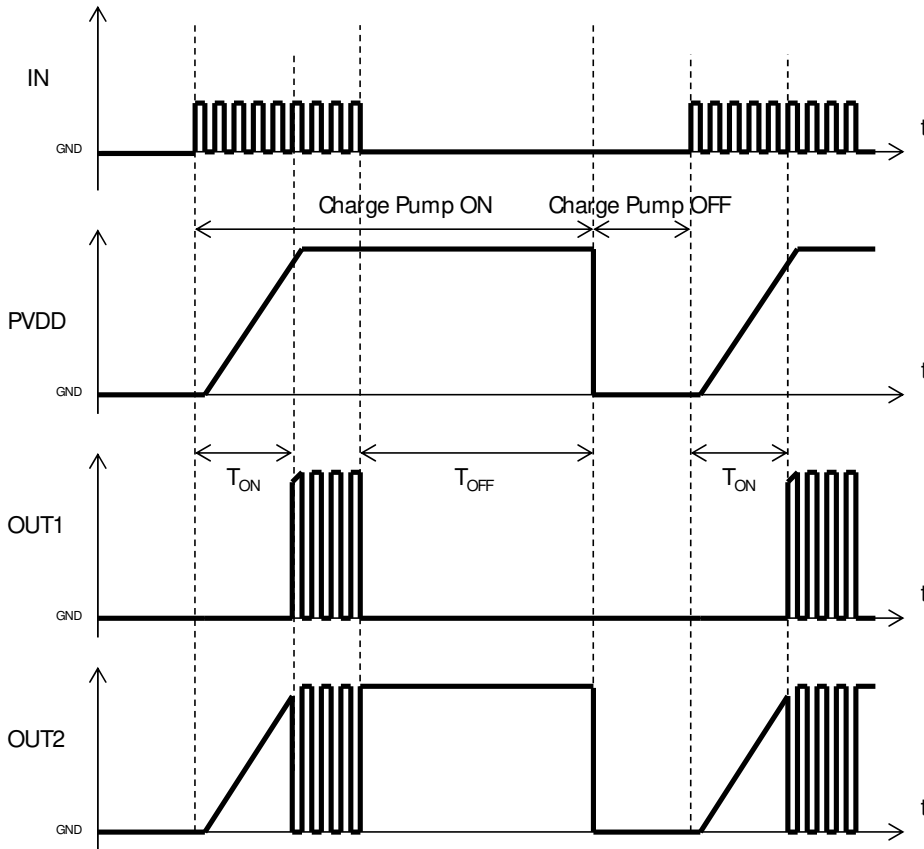
- (5) 2-Layer: Mounted on glass epoxy board (101.5 mm × 114.5 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4) with exposed pad.  
 4-Layer: Mounted on glass epoxy board (101.5 mm × 114.5 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4) with exposed pad.  
 (For 4-layer: Applying 99.5 mm × 99.5 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)
- (6) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).  
 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4), internal Cu area: 74.2 mm × 74.2 mm.

## ■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

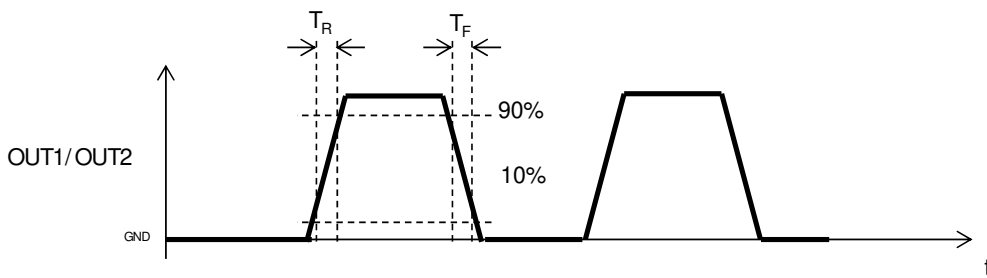


## ■TIMING CHART

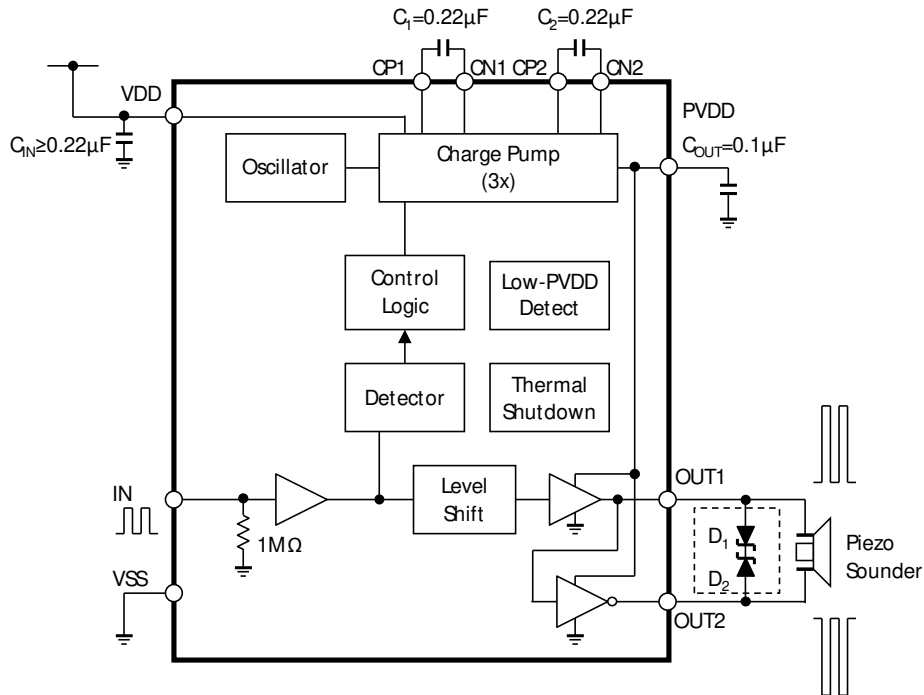
$T_{ON} / T_{OFF}$



$T_R / T_F$

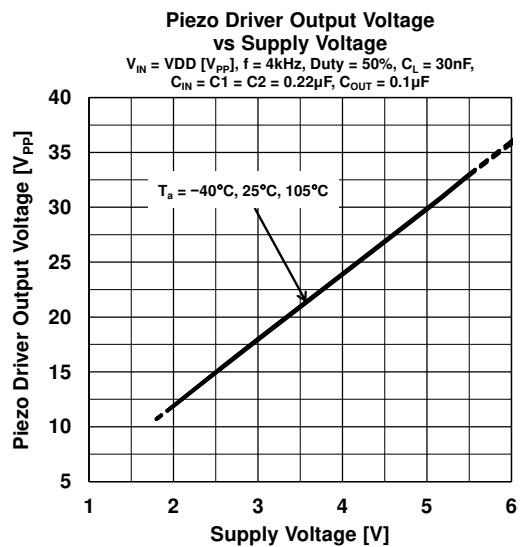
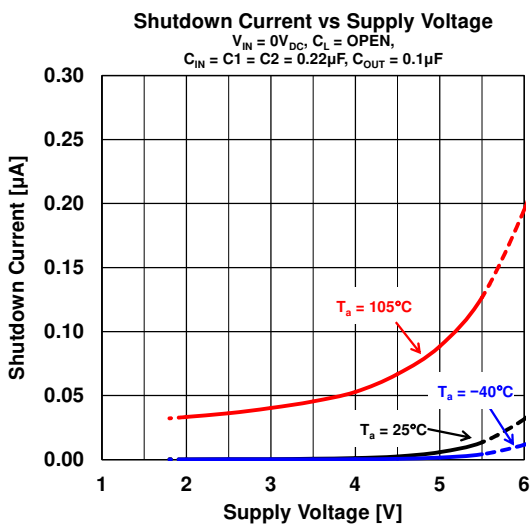
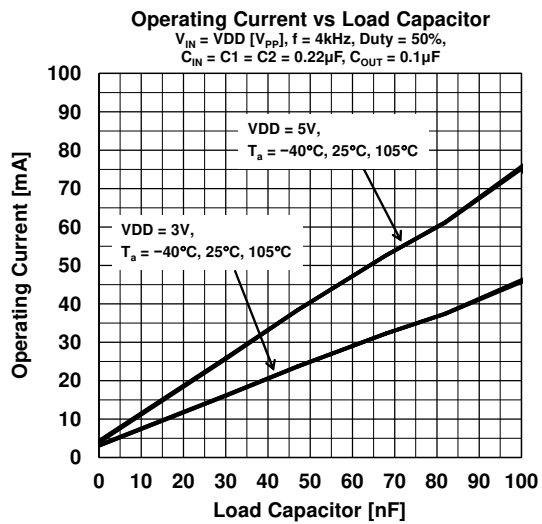
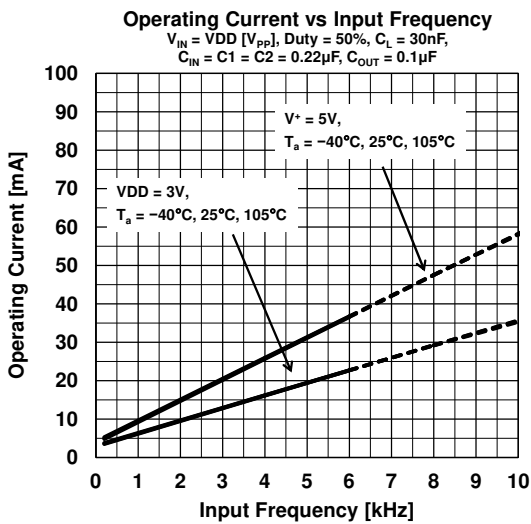
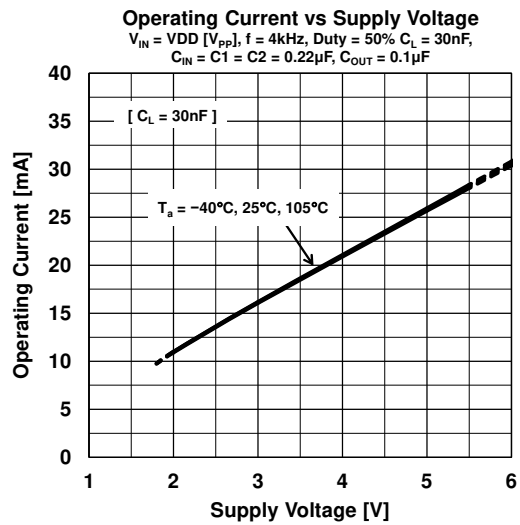
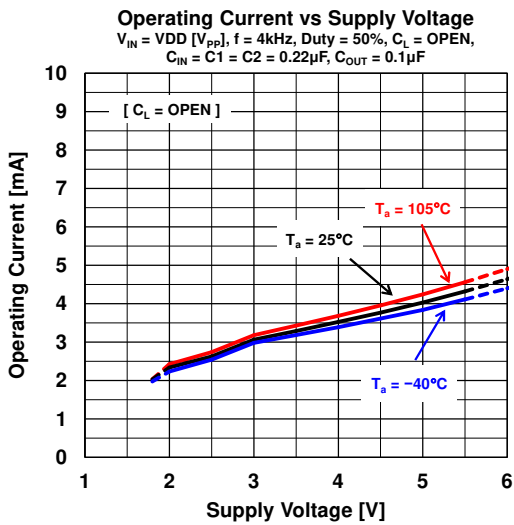


## ■ APPLICATION CIRCUIT



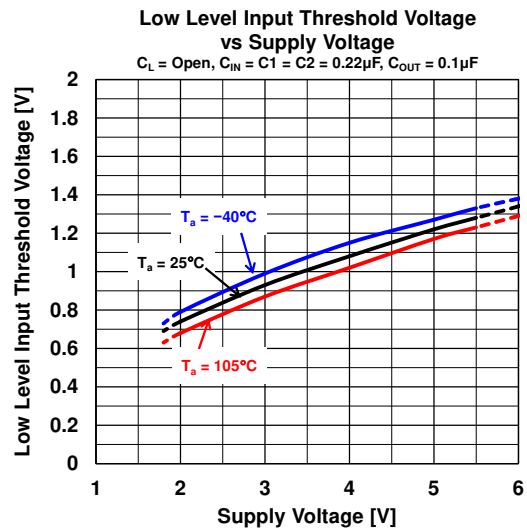
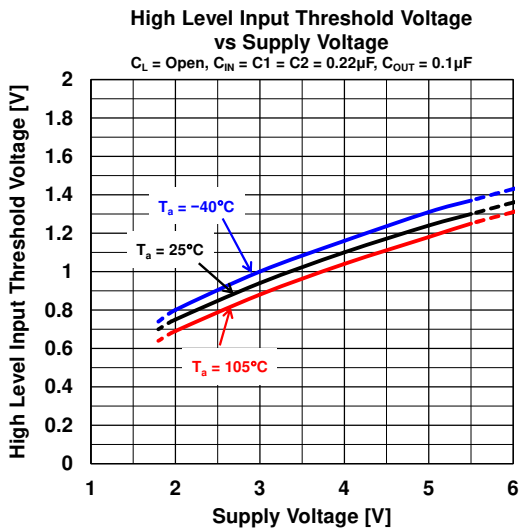
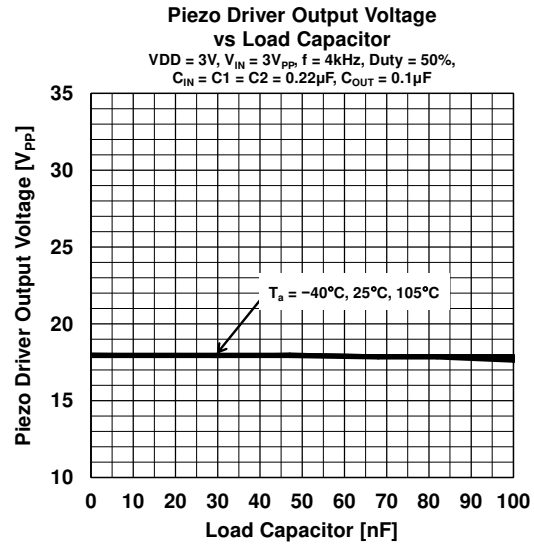
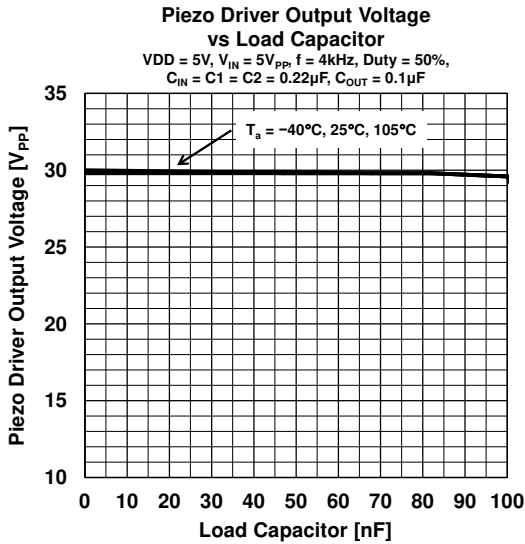
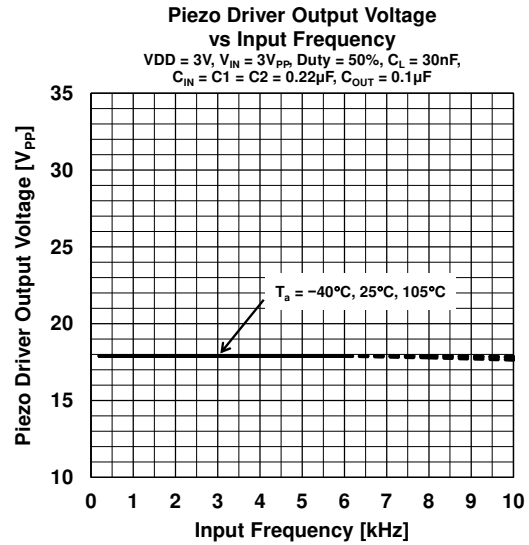
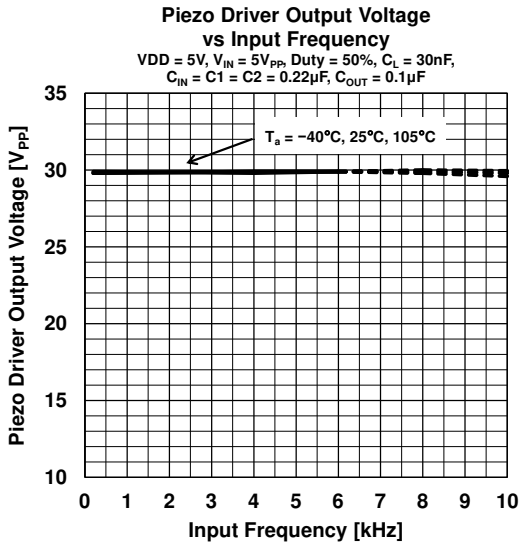
When a thermal shock or mechanical shock is applied to the piezo-sounder, an electric charge (surge voltage) is generated on the piezoelectric diaphragm, which may permanent damage the IC. As a protection example against this surge voltage, consider using a zener diode ( $D_1$ ,  $D_2$ ) between the OUT1 and OUT2 pins. Use the zener voltage higher than  $VDD \times 3$  and not exceeding 20V.

## ■ TYPICAL CHARACTERISTICS

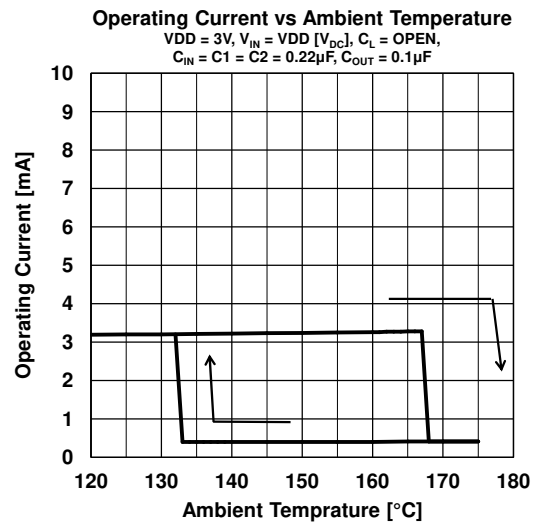
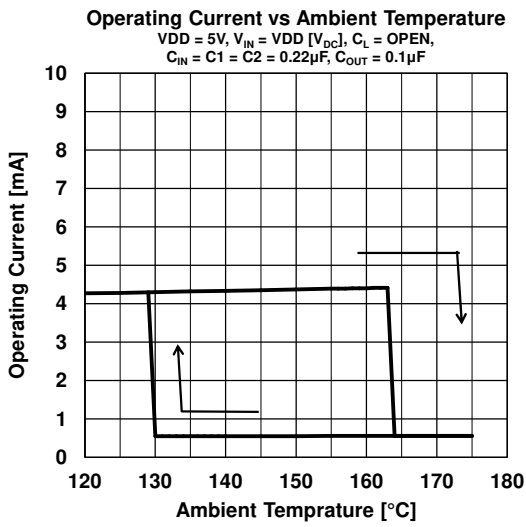




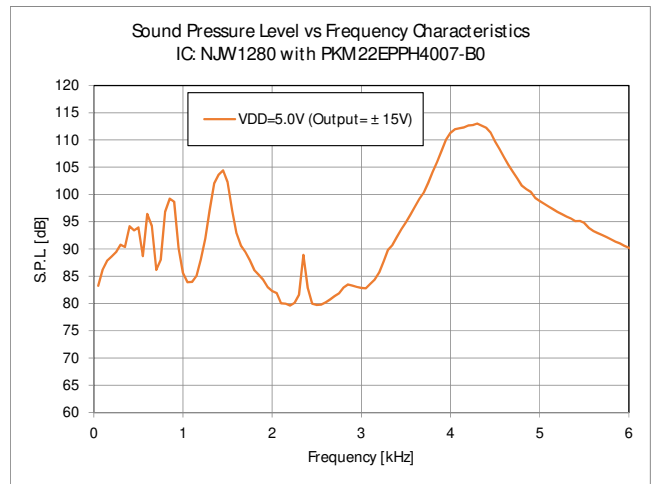
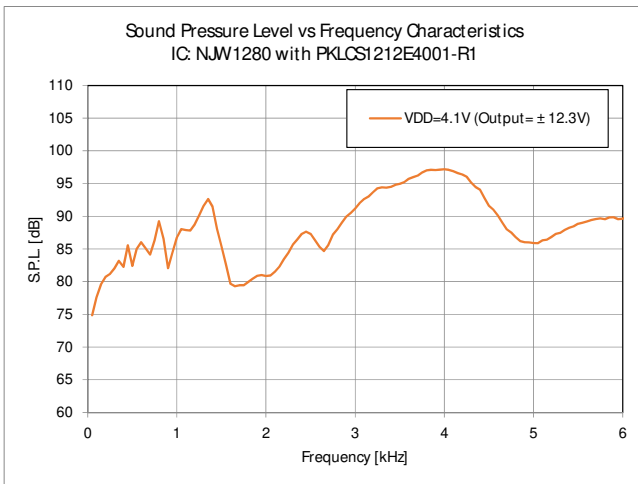
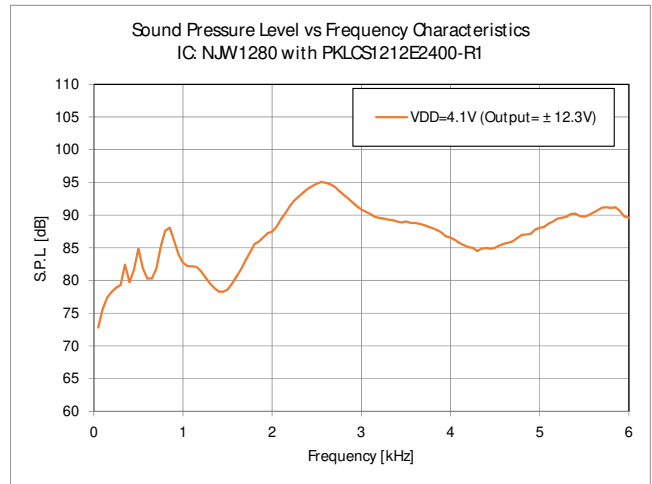
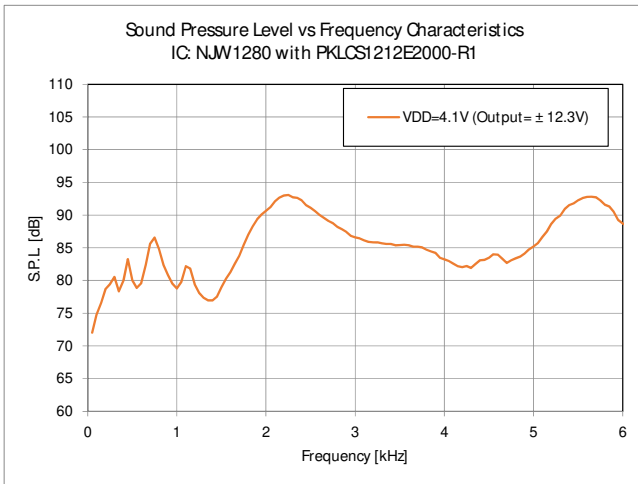
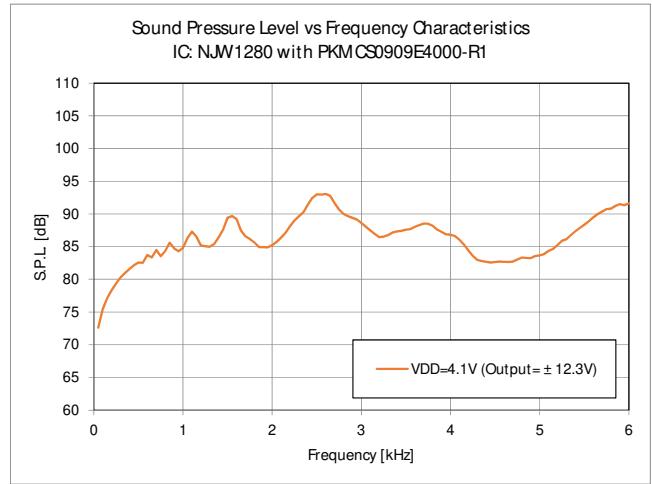
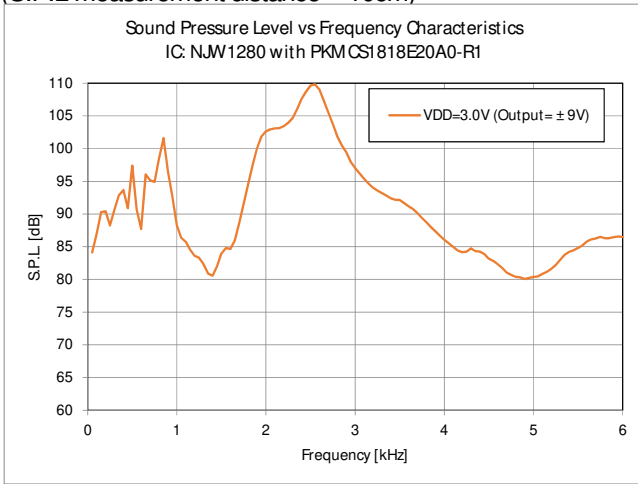
## ■ TYPICAL CHARACTERISTICS



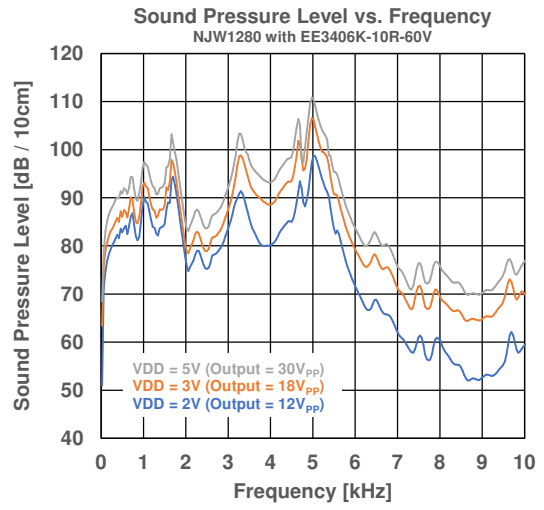
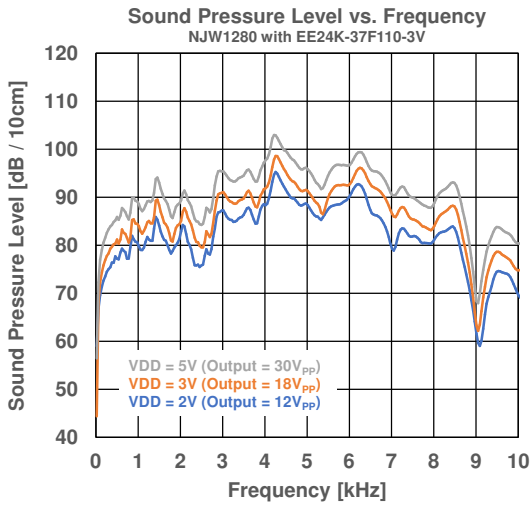
## ■ TYPICAL CHARACTERISTICS



■ MURATA MANUFACTURING PIEZO-SOUNDER RECOMMENDED PARTS EVALUATION RESULT  
 (S.P.L measurement distance = 10cm)



■ NJ COMPONENTS PIEZO-SOUNDER RECOMMENDED PARTS EVALUATION RESULT  
 (S.P.L measurement distance = 10cm)



**■ PRECAUTIONS FOR USE****1. Power Supply**

Use a stable power supply to operate the IC stably. Furthermore, please design so that unexpected abnormal overcurrent does not flow more than necessary to prevent the IC breakdown and the spread of the effects.

**2. Inductive Load**

If your design includes an inductive load, the IC malfunction or breakdown caused by the current resulting from the inrush current at ON or the current resulting from the back electromotive force at OFF. Incorporate a protection circuit into the design to prevent these. The IC breakdown may cause smoke or ignition.

**3. External Parts**

Carefully select external parts (such as power supply decoupling capacitor, charge pump flying capacitor and charge pump store capacitor), load components (such as a piezo-sounder) taking into consideration absolute maximum ratings, characteristics variation by temperature and leakage current characteristics.

In particular, if the leakage current of the input or the capacitor used in the negative feedback circuit is large, a DC voltage will be generated at the output of the IC, and overcurrent will cause deterioration of the IC or speaker, and even smoke or ignition due to a failure there is.

**4. Auxiliary Functions**

The Piezo-sounder Driver IC have the auxiliary functions which suppress breaking themselves under unexpected abnormal conditions. These auxiliary functions are not guarantee as they operate over absolute maximum ratings. It is essential to design as the auxiliary functions do not operate. Do not design depending on the auxiliary functions.

**4.1 Thermal Shutdown (TSD) Circuit**

The thermal shutdown circuit is a suspension circuit of IC's operation to prevent the junction temperature endlessly increase under unexpected abnormal conditions. The IC will return to operate under normal junction temperature.

The thermal shutdown function is not guarantee as it operates over temperature of absolute maximum ratings. Depending on the method of use and usage conditions may cause the thermal shutdown circuit to not operate properly or the IC breakdown before operation.

**4.2 Current Limit Circuit**

The current limit circuit limits output current to below a constant value to prevent output current endlessly increase under unexpected abnormal conditions.

Depending on the method of use and usage conditions such as exceeding absolute maximum ratings may cause the current limit circuit to not operate properly or the IC breakdown before operation.

## APPLICATION NOTE

The NJW1280 is a switching driver with 3times charge pump for piezo-sounder. It can drive outputs up to 30V<sub>PP</sub> from 5V supply. When not operating (no signal), the built-in input signal detection circuit automatically switches to the shutdown mode (0.5 μA max. at V<sub>DD</sub>=3V) to reduce battery consumption and realize a long service life of the set.

### 1. Operating Principle

The NJW1280 has the built-in oscillator, charge pump, control logic, detector for auto shutdown, level shifter, Low-PVDD detection, and Thermal shutdown. (Fig.1)

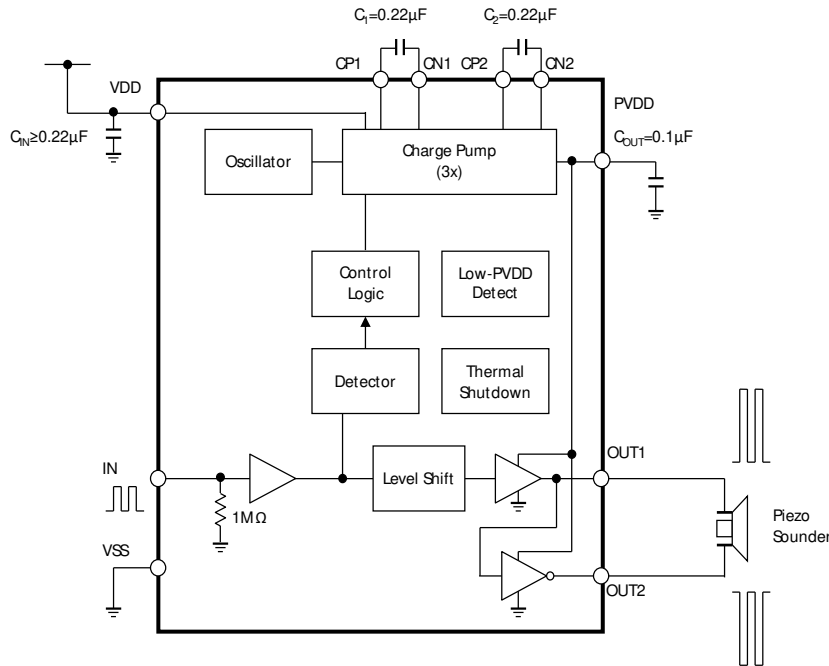


Fig.1 NJW1280 Function Block Diagram and application circuit

## 2. External Parts

### 2-1. Parts List

Table 1 is a list of external parts for application circuits. Please refer to the table and make a decision after evaluation according to the application to be used.

Table 1 List of External Parts

Part No.	Quantity	Voltage	Value	Description	Use in application
C <sub>1</sub> , C <sub>2</sub>	2	≥ 3 × V <sub>DD</sub>	0.22μF	X7R ceramic capacitor	Charge pump flying capacitor
C <sub>OUT</sub>	1	≥ 9 × V <sub>DD</sub>	0.1μF	X7R ceramic capacitor	Charge pump store capacitor
C <sub>IN</sub>	1	≥ 3 × V <sub>DD</sub>	≥ 0.22μF	X7R ceramic capacitor	Power supply decoupling

### 2-2. Flying Capacitor (C<sub>1</sub>, C<sub>2</sub>)

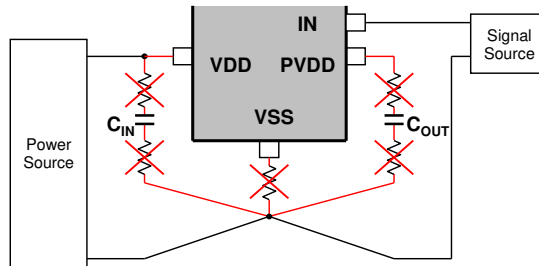
C<sub>1</sub>, C<sub>2</sub> are flying capacitors that carry charges in the charge pump circuit. Use capacitors with a low-ESR (ex. ceramic capacitors) and good temperature characteristics, and place them as closed to the IC as possible to minimize wiring resistance, capacitance, and inductance (Fig. 2)



Fig. 2 Flying Capacitor

### 2-3. Store Capacitor (C<sub>OUT</sub>)

C<sub>OUT</sub> is a capacitor that stores the pumped charge and stabilizes the charge pump output. Use capacitors with a low-ESR (ex. ceramic capacitors) and good temperature characteristics, and place them as close to the IC as possible to minimize wiring resistance, capacitance, and inductance (Fig. 3)



**Fig. 3 Store capacitor, Coupling Capacitor**

### 2-4. Coupling Capacitor of Power Supply

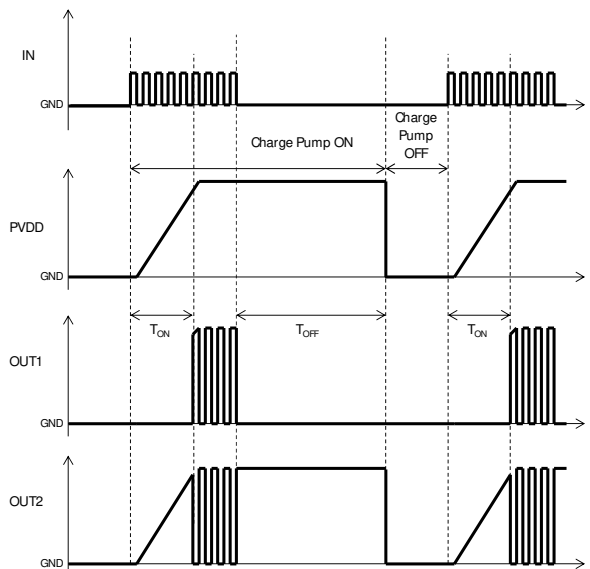
It stabilizes the VDD line. Please decide the capacity according to your system. Use capacitors with low ESR (ex. ceramic capacitors) and good temperature characteristics, and place them as close to the IC as possible to minimize wiring resistance, capacitance, and inductance. (Fig. 3) Also, connecting an electrolytic capacitor with large capacitance in parallel will make the operation of the NJW 1280 more stable.

## 3. Operation and Usage

NJW1280 detects the input signal and switches active mode and shutdown mode automatically. When inputting a signal to the IN terminal, the operation starts and turn active mode. When no signal to the IN terminal in a certain period of time, the operation stops and turns shutdown mode.

### 3-1. Operation Sequence

Fig. 4 shows the sequence from operation start to stop. NJW1280 starts in the shutdown state when the supply turned on, then when it detects the rise of the input signal, turns active mode after Turn-On Time (T<sub>ON</sub> = 2ms typ.). Also, during the T<sub>ON</sub> period, the Charge Pump Output Terminal (PVDD) will gradually start up (**soft start**), and no signal be output at this period. Soft start suppresses the inrush current at startup and prevents system shutdown due to a sudden voltage drop in small capacity batteries such as coin batteries. After the T<sub>ON</sub> period, when NJW1280 detects the rise of the input signal, the signal is output. When the input signal is in the Low state and elapses the Shutdown Delay Time (T<sub>OFF</sub> = 15ms typ.), the IC turns shutdown mode.



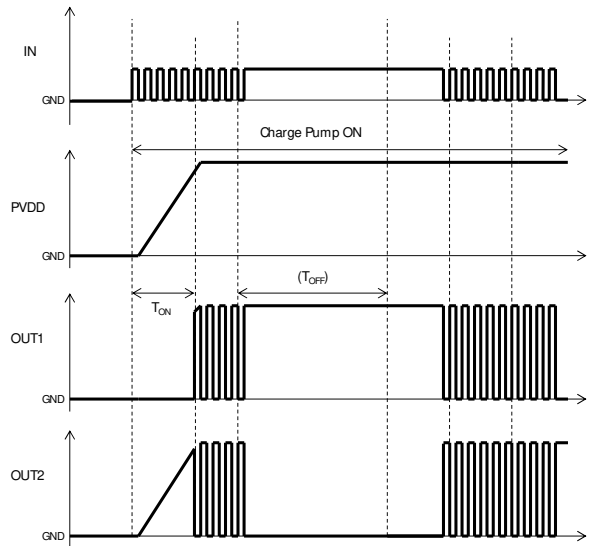
**Fig.4 Operation Sequence**

Soft start does not prevent system shutdown with any combination of batteries or buzzers. Please make a sufficient evaluation under the conditions of use.

### 3-2. Operation in Intermittent Signal

When inputting an intermittent signal, the period of no signal may exceed  $T_{OFF}$ . When the IC enters the shutdown state, no signal is output during the  $T_{ON}$  period when the signal is input again, so the head of the output signal will be missing. In this case, as shown in Fig. 5, if the input signal is held at the High level in the no signal period, the NJW 1280 does not count the  $T_{OFF}$  period and does not enter the shutdown state.

However, when supplying DC voltage to the piezo-sounder, there is a possibility that it will have some effect on the piezo-sounder. Therefore, if you can think of a way of supplying DC voltage, please check with the piezo-sounder manufacturer you use.

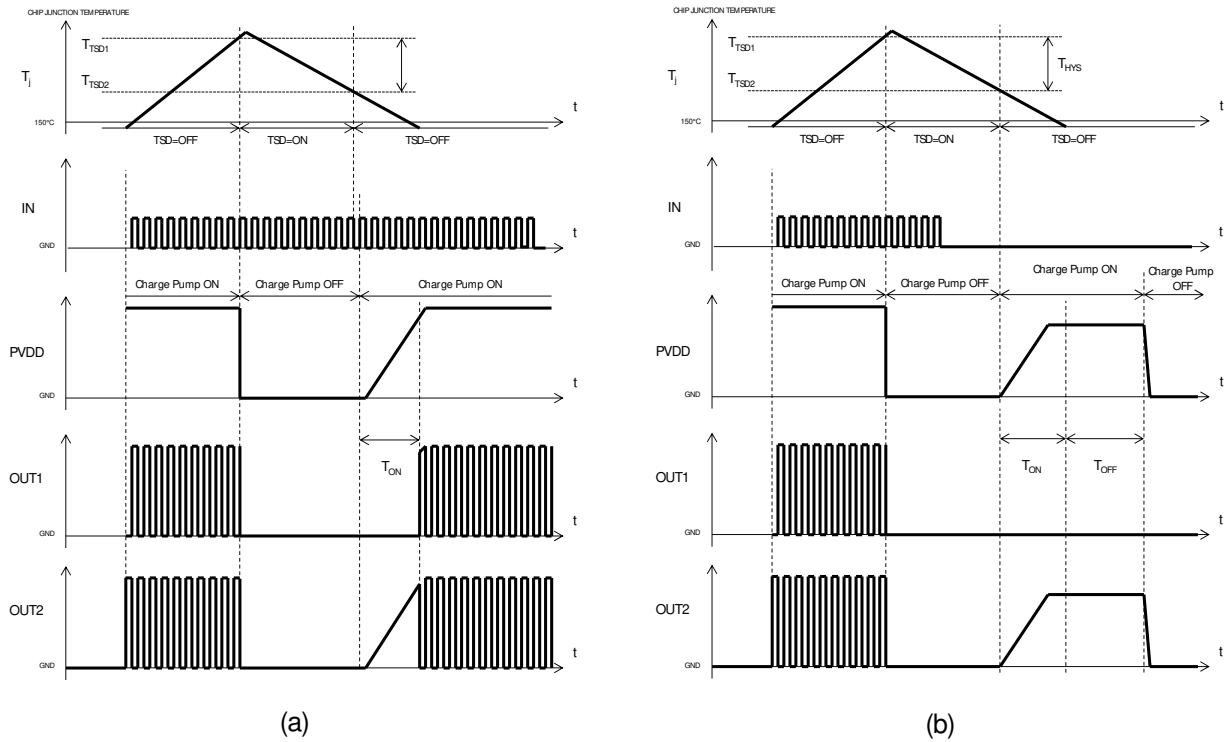


**Fig. 5 Output countermeasure sequence**



### 3-3. Thermal Shutdown (TSD) Function

Fig. 6 shows the thermal shutdown function (hereinafter, TSD function) stops the charge pump circuit and output circuit when the junction temperature  $T_j$  of NJW1280 exceeds  $T_{slg}$  and further exceeds  $T_{TSD1}$ . When  $T_j$  drops below  $T_{TSD2}$ , NJW1280 restarts to active mode after a soft start [Fig. 6 (a)]. When the input signal is stopped while the TSD function is ON, the TSD function is OFF and the IC returns to active mode after a soft start, but shuts down after the  $T_{OFF}$  period [Fig. 6 (b)].



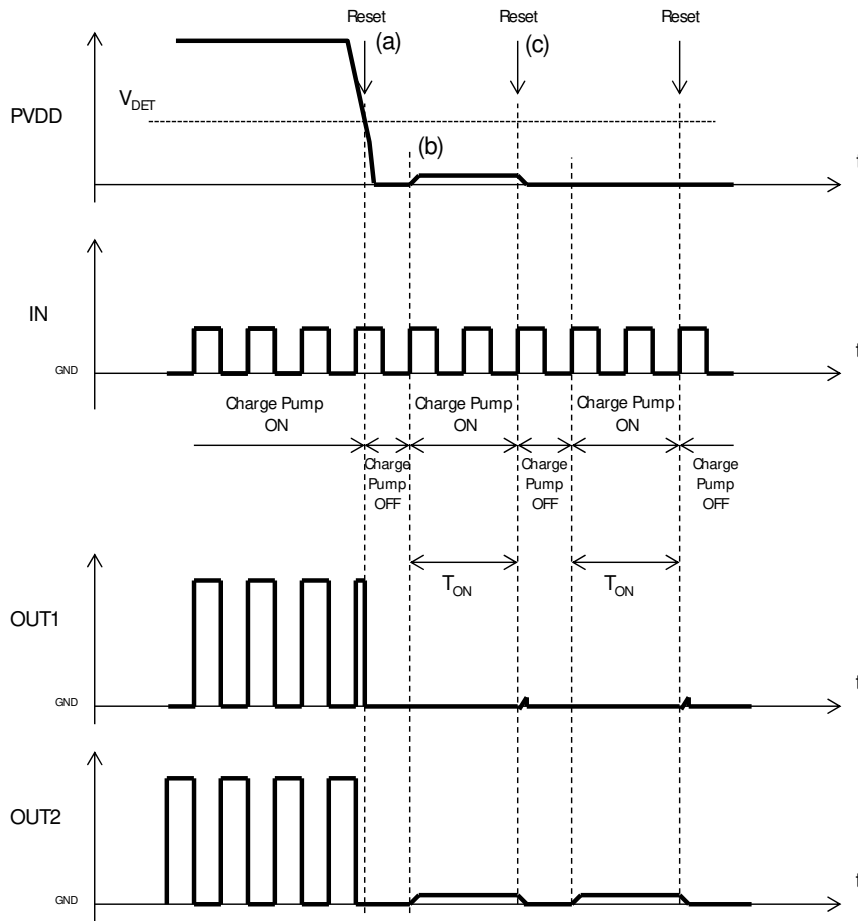
**Fig. 6 Thermal Shutdown operation sequence**

The TSD function is not guaranteed because it exceeds the maximum rating. It is an auxiliary function to the last. Please make a redundant design that the TSD does not work. Do not perform set design using this function.

### 3-4. Low-PVDD Detection Circuit

The Low-PVDD detection circuit resets the IC when the PVDD terminal voltage falls below the voltage  $V_{DET} \approx 1.5 \times V_{DD}$  for some reason. Detection voltage depends on  $V_{DD}$  voltage.

Figure 7 shows the operation of the Low-PVDD detection function. When the PVDD voltage drops below  $V_{DET}$  while the NJW1280 is in active mode, the NJW1280 switches to shutdown mode and stops the charge pump circuit and output (a). When the input signal is detected in this state, the IC restarts from the soft start (b), but if PVDD stayed below  $V_{DET}$  even after  $T_{ON}$ , IC shutdowns again due to Low-PVDD detection (c). This situation continues until the cause of the voltage drop at the PVDD terminal is eliminated.



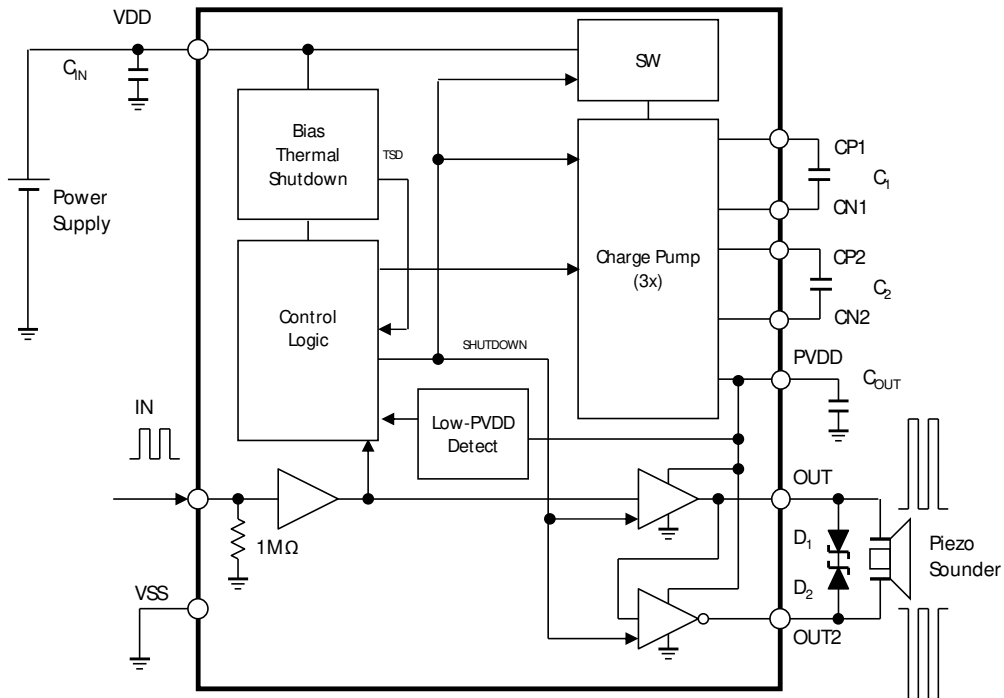
**Fig.7 Low-PVDD detection operation sequence**

This function is an auxiliary function. Please make safety design so that this function does not work. Also, do not do set design using this function.

**4. Surge Voltage From Piezo-Souder**

When a thermal shock or mechanical shock is applied to the piezo-souder, an electric charge (surge voltage) is generated on the piezoelectric diaphragm, which may permanent damage the IC.

As a protection example against this surge voltage, consider using a zener diode ( $D_1$ ,  $D_2$ ) between the OUT1 and OUT2 terminals as shown in Fig. 8 (For details, see the application note of the piezo-souder under consideration.). Use the zener voltage higher than  $VDD \times 3$  and not exceeding 20V.



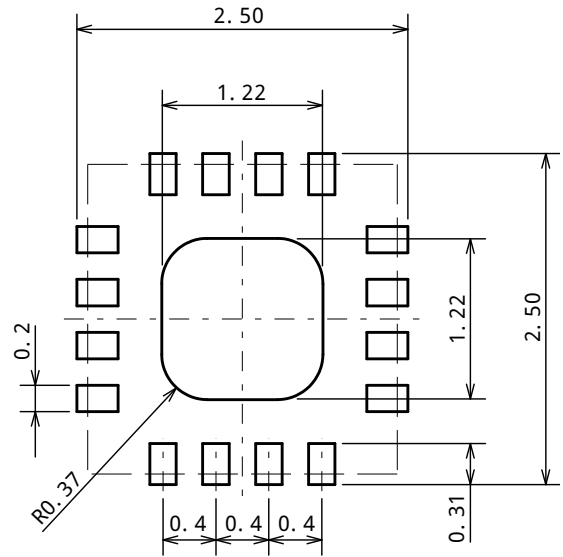
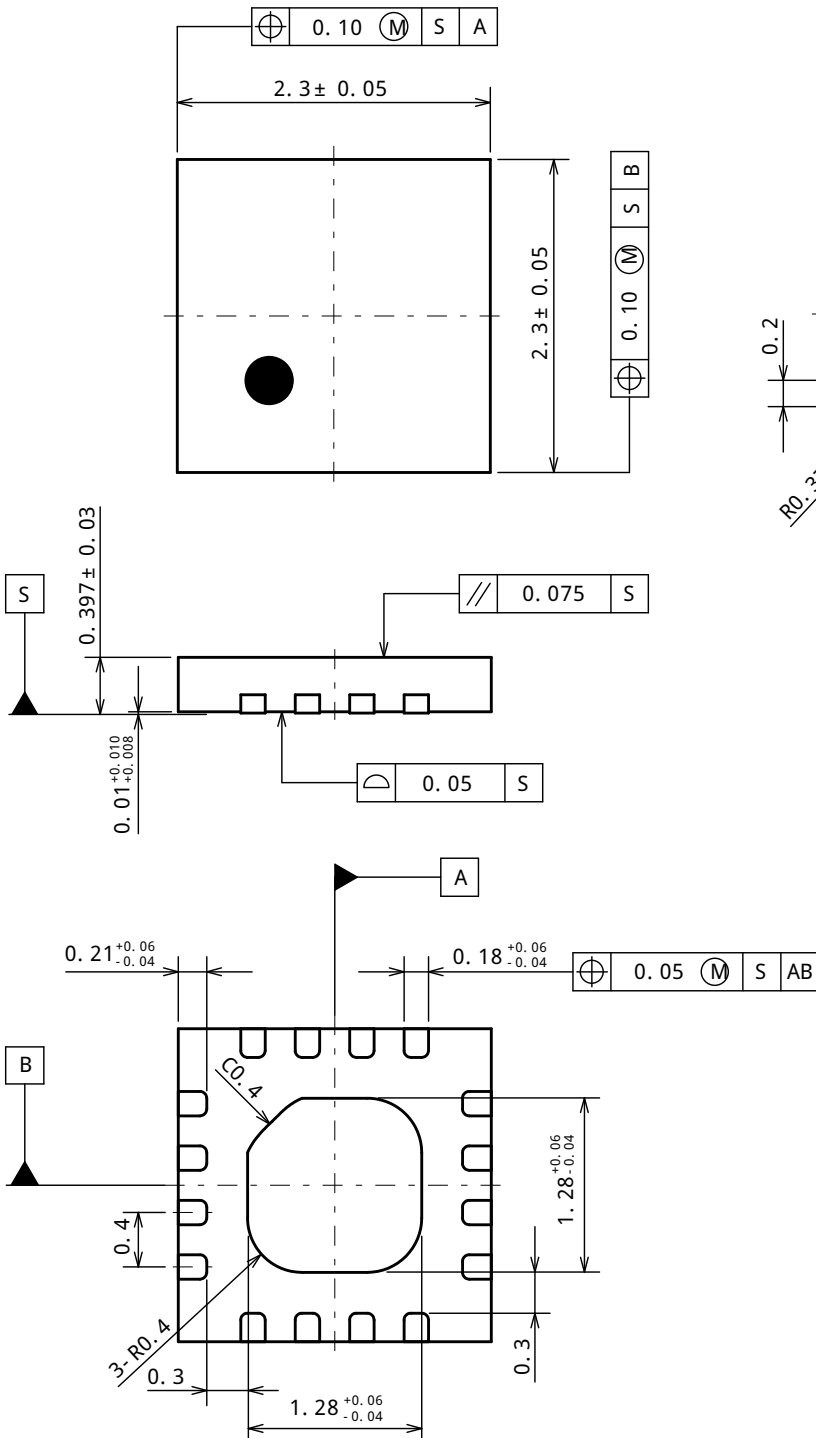
**Fig. 8 Example of application circuit**

## EQFN16-G2

Unit: mm

### ■ PACKAGE DIMENSIONS

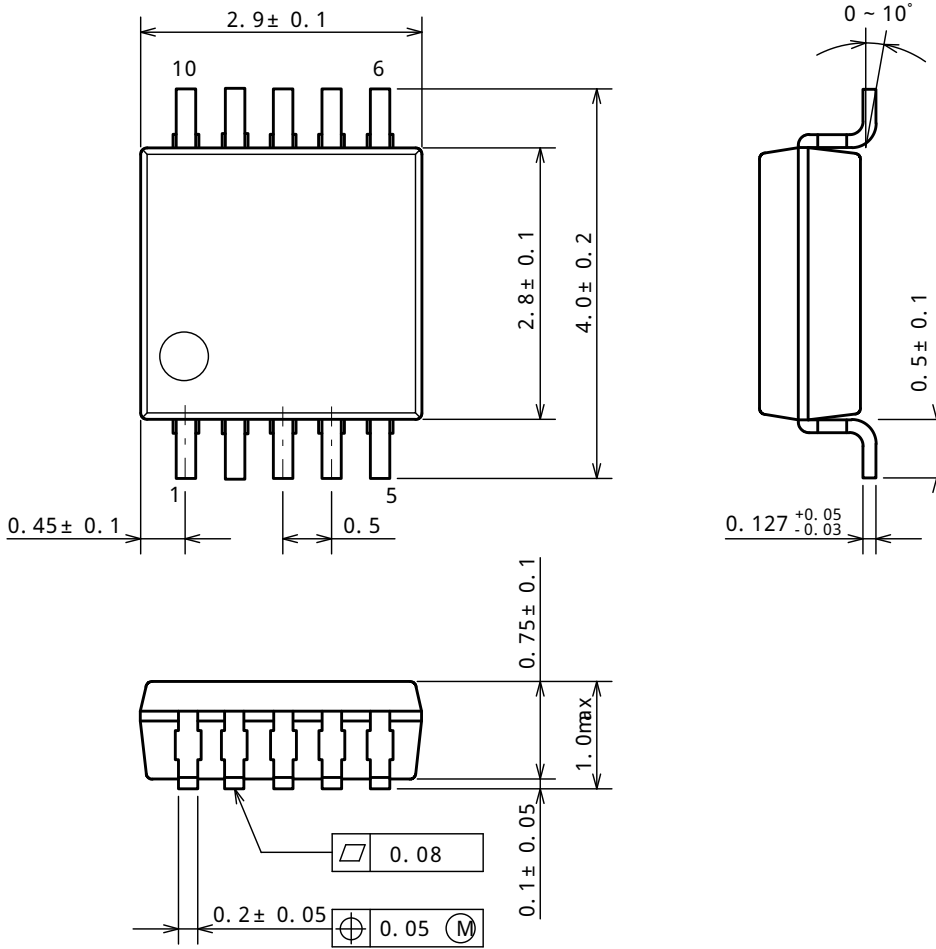
### ■ EXAMPLE OF SOLDER PADS DIMENSIONS



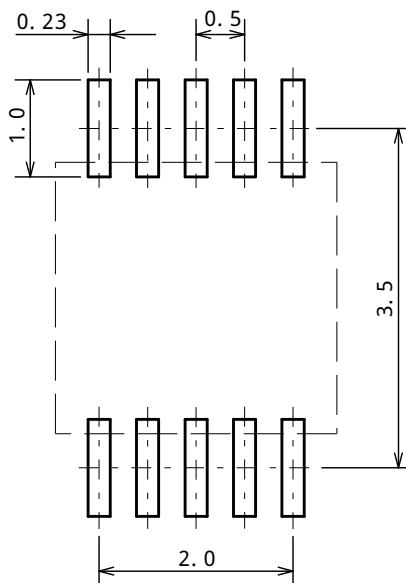
## MSOP10 JEDEC MO-187-DA/THIN TYPE

Unit: mm

### ■ PACKAGE DIMENSIONS



### ■ EXAMPLE OF SOLDER PADS DIMENSIONS

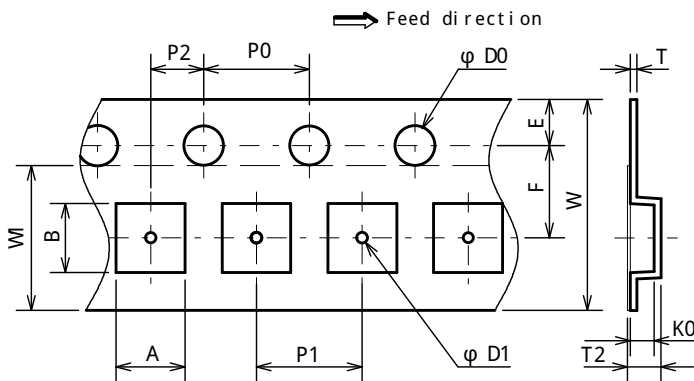


## EQFN16-G2

### PACKING SPEC

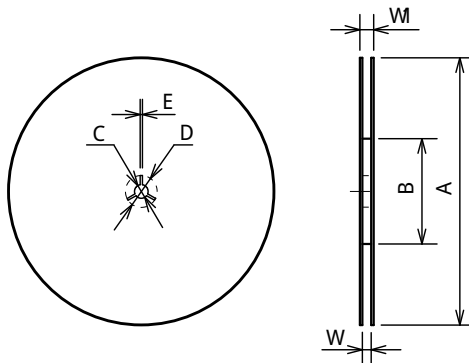
Unit: mm

#### TAPING DIMENSIONS



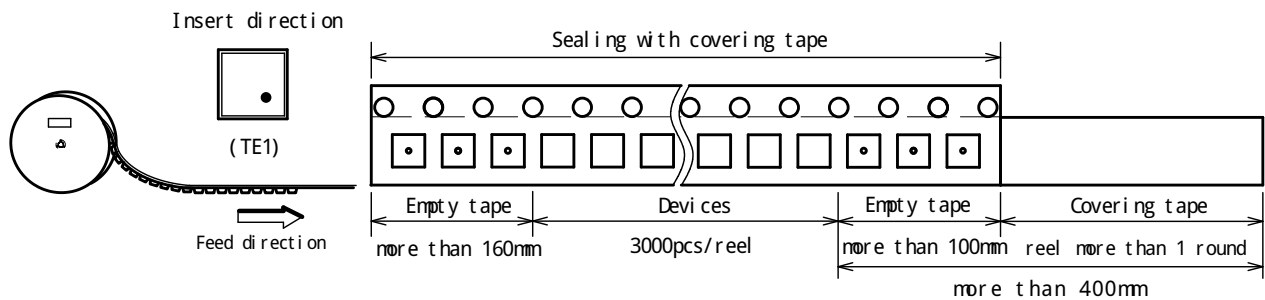
SYMBOL	DI MENSION	REMARKS
A	2.55± 0.05	BOTTOM DI MENSION
B	2.55± 0.05	BOTTOM DI MENSION
D0	1.5 <sup>+0.1</sup> <sub>0</sub>	
D1	0.5± 0.1	
E	1.75± 0.1	
F	3.5± 0.05	
P0	4.0± 0.1	
P1	4.0± 0.1	
P2	2.0± 0.05	
T	0.25± 0.05	
T2	1.00± 0.07	
K0	0.65± 0.05	
W	8.0± 0.2	
Wf	5.5	THICKNESS 0.1max

#### REEL DIMENSIONS

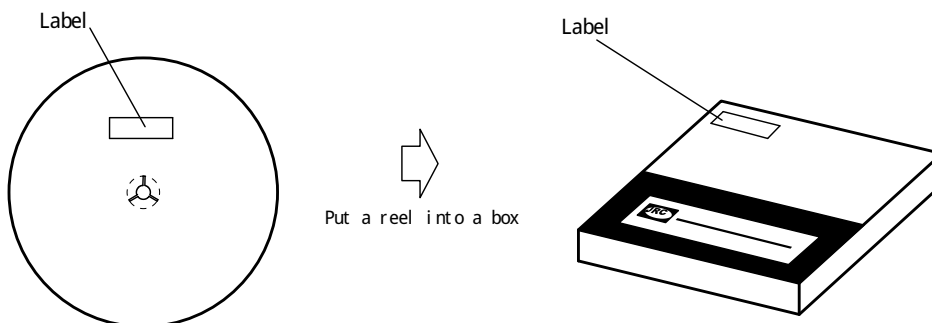


SYMBOL	DI MENSION
A	φ 180 <sup>0</sup> <sub>-1.5</sub>
B	φ 60 <sup>+1</sup> <sub>0</sub>
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	9 <sup>+0.3</sup> <sub>0</sub>
Wf	1.2

#### TAPING STATE



#### PACKING STATE

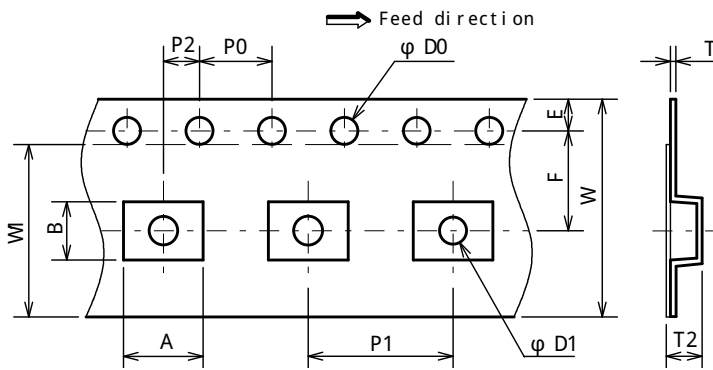


## MSOP10 MEET JEDEC MO-187-DA/THIN TYPE

### PACKING SPEC

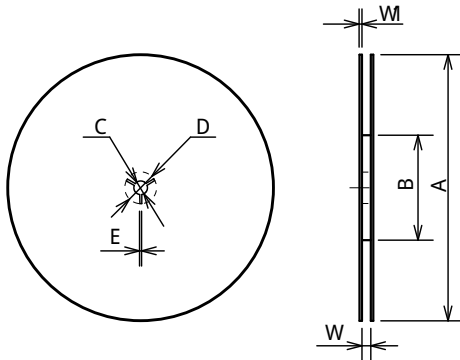
Unit: mm

#### TAPING DIMENSIONS



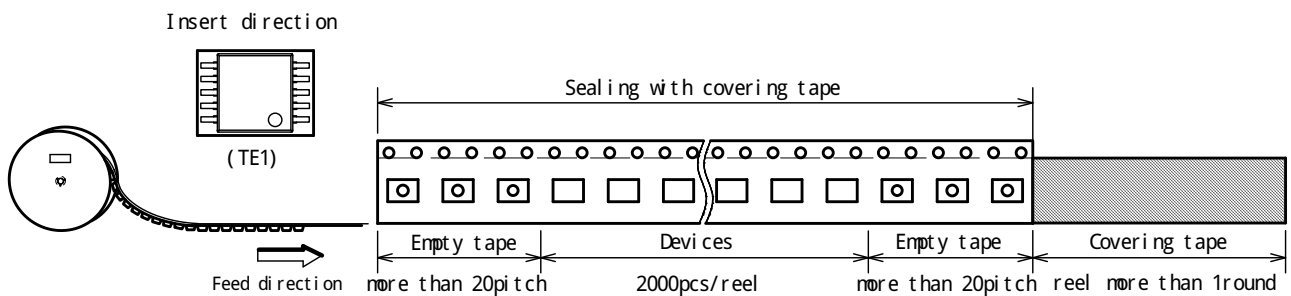
SYMBOL	DI MENSION	REMARKS
A	4.4	BOTTOM DI MENSION
B	3.2	BOTTOM DI MENSION
D0	1.5 <sup>+0.1</sup> <sub>0</sub>	
D1	1.5 <sup>+0.1</sup> <sub>0</sub>	
E	1.75± 0.1	
F	5.5± 0.05	
P0	4.0± 0.1	
P1	8.0± 0.1	
P2	2.0± 0.05	
T	0.3± 0.05	
T2	1.75 (MAX.)	
W	12.0± 0.3	
W1	9.5	THICKNESS 0.1max

#### REEL DIMENSIONS

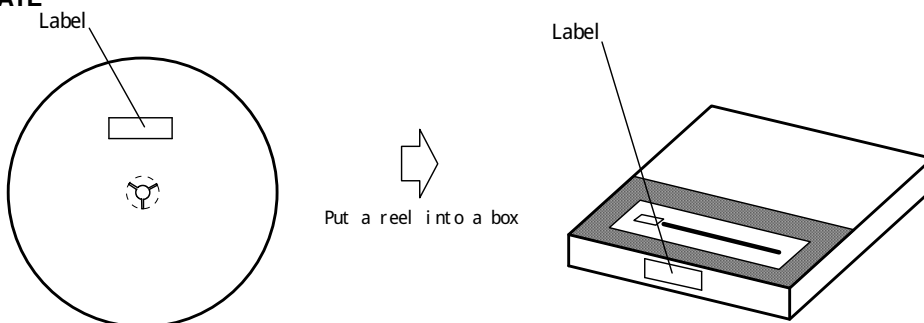


SYMBOL	DI MENSION
A	φ 254± 2
B	φ 100± 1
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	13.5± 0.5
W1	2.0± 0.2

#### TAPING STATE

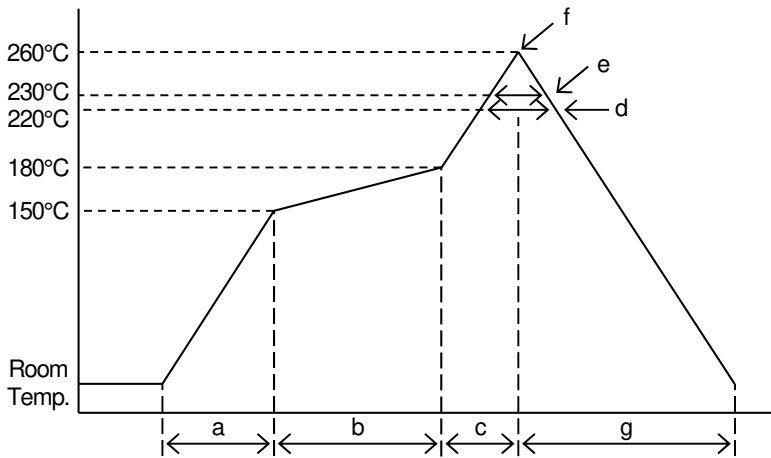


#### PACKING STATE



## ■ RECOMMENDED MOUNTING METHOD

### INFRARED REFLOW SOLDERING PROFILE



a	Temperature ramping rate	1 to 4°C/s
b	Pre-heating temperature	150 to 180°C
	Pre-heating time	60 to 120s
c	Temperature ramp rate	1 to 4°C/s
d	220°C or higher time	shorter than 60s
e	230°C or higher time	shorter than 40s
f	Peak temperature	lower than 260°C
g	Temperature ramping rate	1 to 6°C/s

The temperature indicates at the surface of mold package.

## ■ REVISION HISTORY

DATE	REVISION	CHANGES
September 28, 2020	Ver.3.8	Changed datasheet format. Updated operation sequence on Application note. Added Piezo-sounder matching data on typical Characteristics.



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