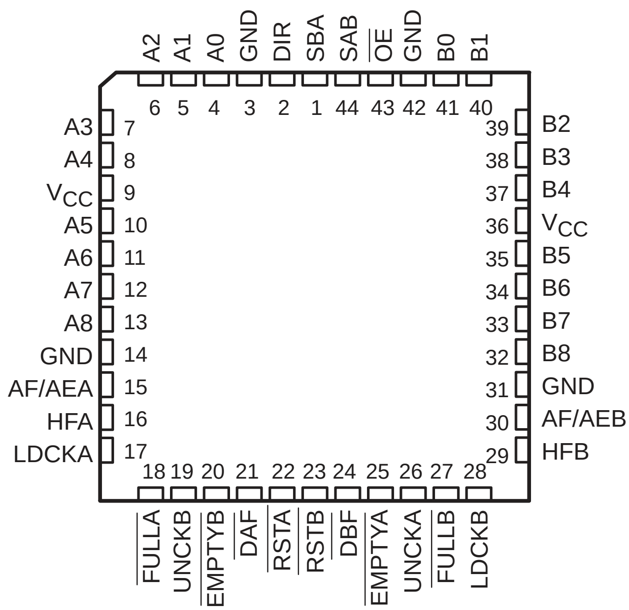
- **Independent Asynchronous Inputs and Outputs**
- **Low-Power Advanced CMOS Technology**
- **Bidirectional**
- **1024 Words by 9 Bits Each**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Empty, Full, and Half-Full Flags**
- **Access Times of 25 ns With a 50-pF Load**
- **Data Rates From 0 to 50 MHz**
- **Fall-Through Times of 23 ns Max**
- **High Output Drive for Direct Bus Interface**
- **3-State Outputs**
- **Available in 44-Pin PLCC (FN) Package**

FN PACKAGE
(TOP VIEW)



description

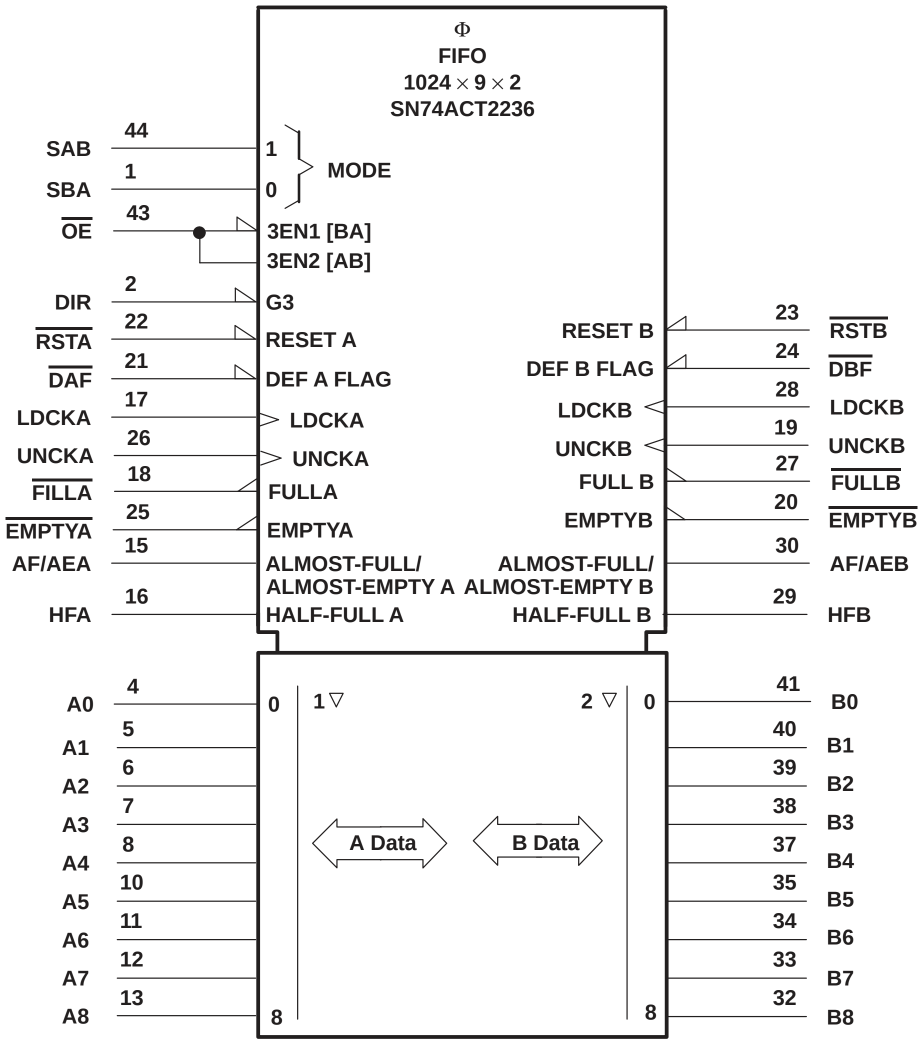
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT2236 is arranged as two 1024 by 9-bit FIFOs for high speed and fast access times. It processes data at rates from 0 to 50 MHz with access times of 25 ns in a bit-parallel format.

The SN74ACT2236 consists of bus-transceiver circuits, two 1024 × 9 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enable $\overline{\text{OE}}$ and DIR inputs are provided to control the transceiver functions. The select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 shows the five fundamental bus-management functions that can be performed with the SN74ACT2236.

The SN74ACT2236 is characterized for operation from 0°C to 70°C.

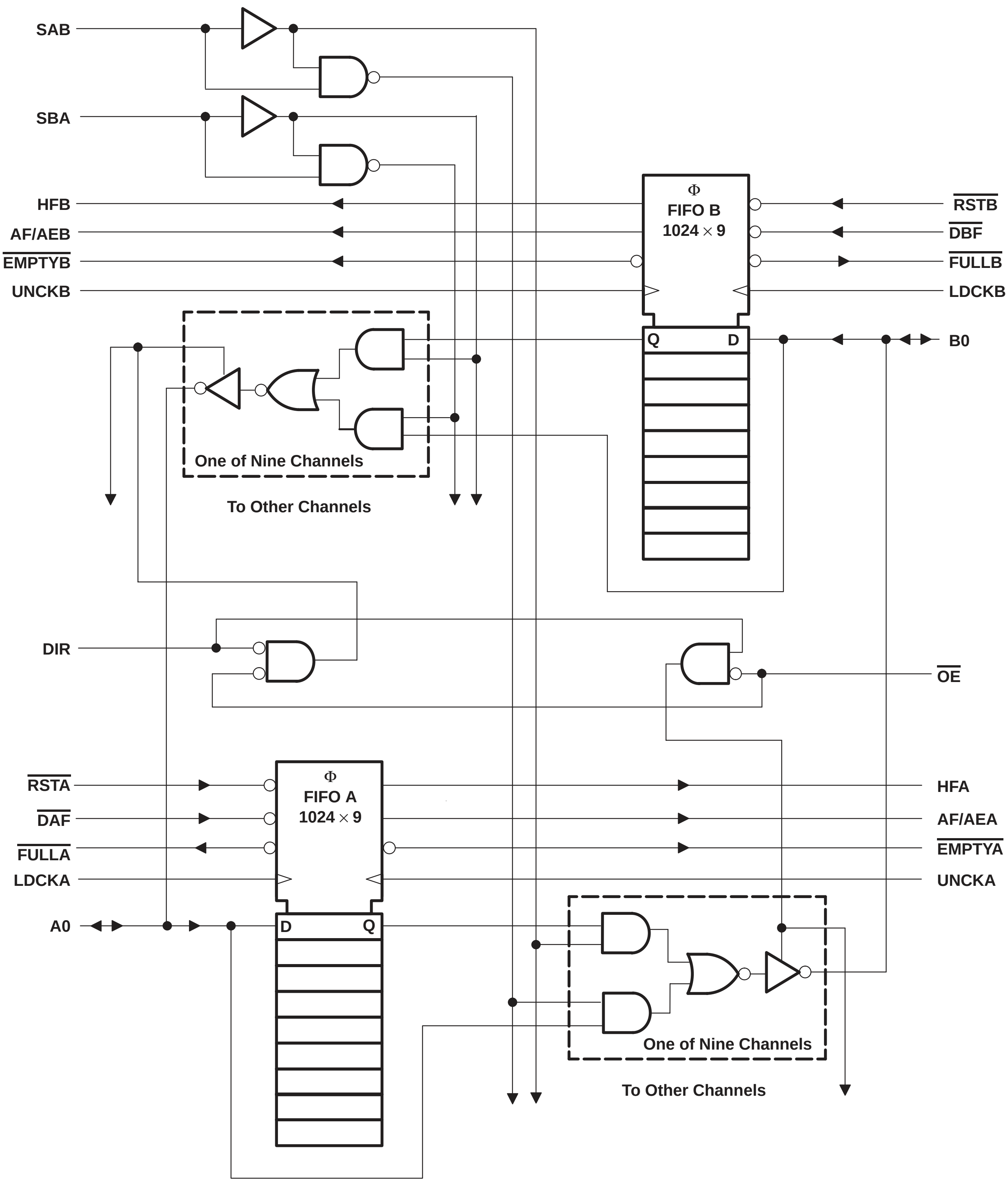
For more information on this device family, see the application report *1K × 9 × 2 Asynchronous FIFOs SN74ACT2235 and SN74ACT2236* in the 1996 *High-Performance FIFO Memories Designer's Handbook*, literature number SCAA012A.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AEA, AF/AEB	15, 30	O	Almost full/almost empty flags. The almost-full/almost-empty A flag (AF/AEA) is defined by the almost-full/almost-empty offset value for FIFO A (X). AF/AEA is high when FIFO A contains X or less words or 1024 − X words. AF/AEA is low when FIFO A contains between X + 1 or 1023 − X words. The operation of the almost-full/almost-empty B flag (AF/AEB) is the same as AF/AEA for FIFO B.
A0 − A8	4 − 8, 10 − 13	I/O	A data inputs and outputs
B0 − B8	32 − 35, 37 − 41	I/O	B data inputs and outputs
$\overline{\text{DAF}}$, $\overline{\text{DBF}}$	21, 24	I	Define-flag inputs. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value on A0 − A8 as the almost-full/almost-empty offset value for FIFO A (X). The high-to-low transition of $\overline{\text{DBF}}$ stores the binary value of B0−B8 as the almost-full/almost-empty offset value for FIFO B (Y).
$\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$	20, 25	O	Empty flags. $\overline{\text{EMPTYA}}$ and $\overline{\text{EMPTYB}}$ are low when their corresponding memories are empty and high when they are not empty.
$\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$	18, 27	O	Full flags. FULLA and FULLB are low when their corresponding memories are full and high when they are not full.
HFA, HFB	16, 29	O	Half-full flags. HFA and HFB are high when their corresponding memories contain 512 or more words, and low when they contain 511 or less words.
LDCKA, LDCKB	17, 28	I	Load clocks. Data on A0−A8 is written into FIFO A on a low-to-high transition of LDCKA. Data on B0 − B8 is written into FIFO B on a low-to-high transition of LDCKB. When the FIFOs are full, LDCKA and LDCKB have no effect on the data residing in memory.
DIR, $\overline{\text{OE}}$	2, 43	I	Enable inputs. DIR and $\overline{\text{OE}}$ control the transceiver functions. When OE is high, both A0 − A8 and B0 − B8 are in the high-impedance state and can be used as inputs. With $\overline{\text{OE}}$ low and DIR high, the A bus is in the high-impedance state and B bus is active. When both $\overline{\text{OE}}$ and DIR are low, the A bus is active and the B bus is in the high-impedance state.
$\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$	22, 23	I	Reset. A reset is accomplished in each direction by taking $\overline{\text{RSTA}}$ and $\overline{\text{RSTB}}$ low. This sets $\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$, $\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$, and AF/AEB high. Both FIFOs must be reset upon power up.
SAB, SBA	1, 44	I	Select-control inputs. SAB and SBA select whether real-time or stored data is transferred. A low level selects real-time data, and a high level selects stored data. Eight fundamental bus-management functions can be performed as shown in Figure 1.
$\overline{\text{UNCKA}}$, $\overline{\text{UNCKB}}$	19, 26	I	Unload clocks. Data in FIFO A is read to B0 − B8 on a low-to-high transition of UNCKB. Data in FIFO B is read to A0 − A8 on a low-to-high transition of UNCKB. When the FIFOs are empty, $\overline{\text{UNCKA}}$ and $\overline{\text{UNCKB}}$ have no effect on data residing in memory.

programming procedure for AF/AEA

The almost-full/almost-empty flags (AF/AEA, AF/AEB) are programmed during each reset cycle. The almost-full/almost-empty offset value FIFO A (X) and for FIFO B (Y) are either a user-defined value or the default values of X = 256 and Y = 256. Below are instructions to program AF/AEA using both methods. AF/AEB is programmed in the same manner for FIFO B.

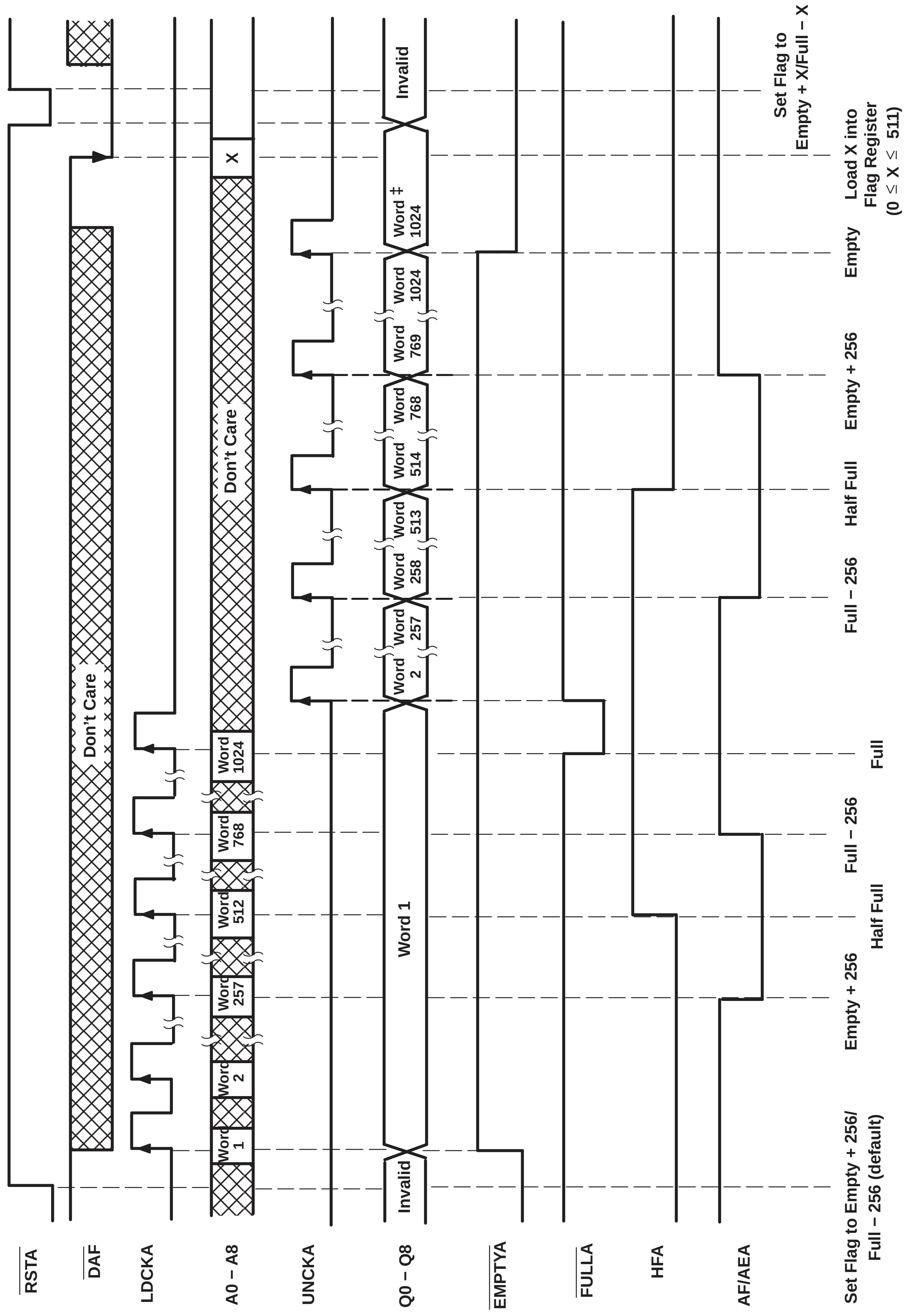
user-defined X

Take $\overline{\text{DAF}}$ from high to low. This stores A0 thru A8 as X.
If $\overline{\text{RSTA}}$ is not already low, take $\overline{\text{RSTA}}$ high.
With $\overline{\text{DAF}}$ held low, take $\overline{\text{RSTA}}$ high. This defines the AF/AEA flag using X.
To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low.

default X

To redefine the AF/AE flag using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.

timing diagram for FIFO A†



† Operation of FIFO B is identical to that of FIFO A.
‡ Last valid data stays on outputs when FIFO goes empty due to a read.

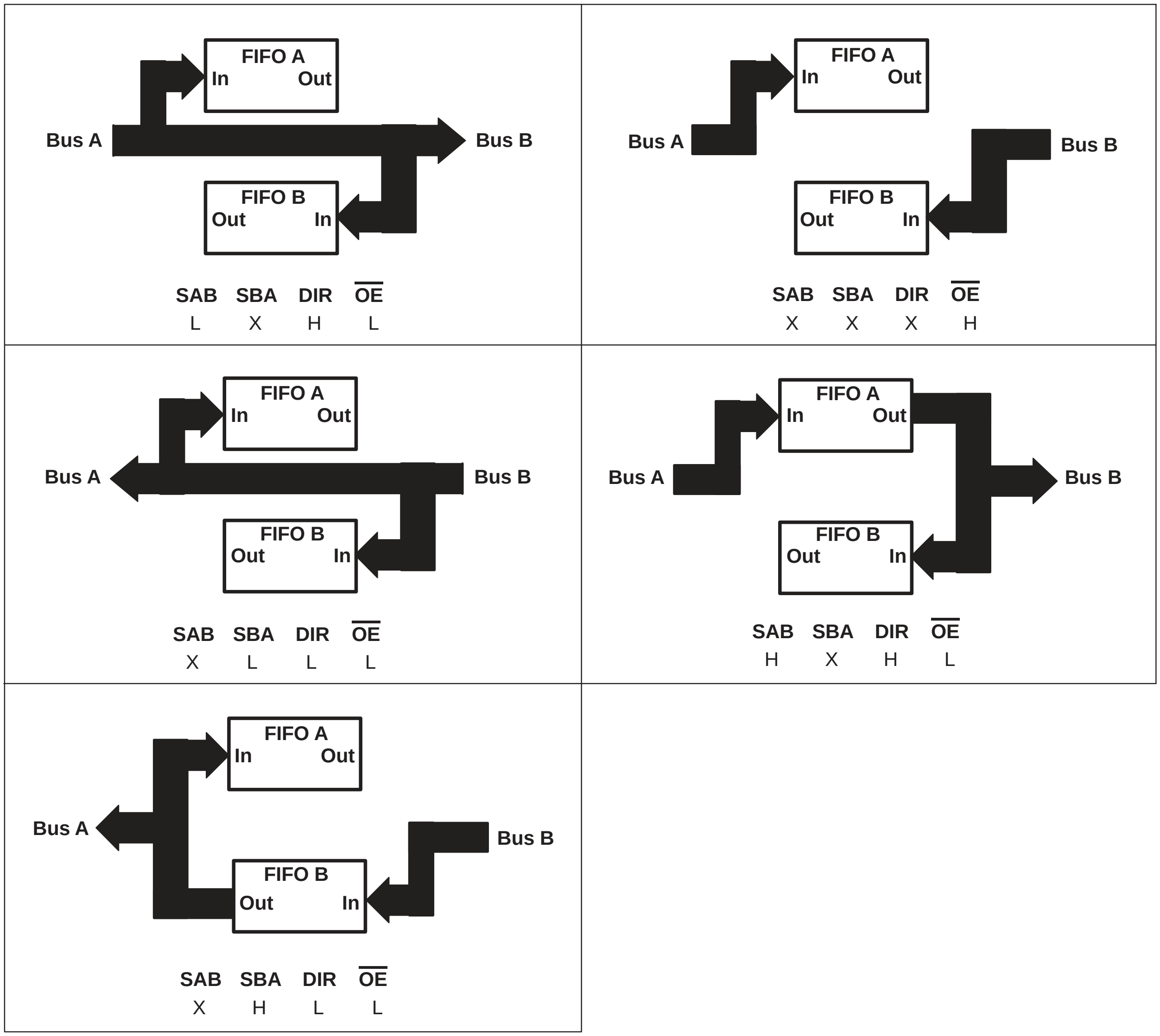


Figure 1. Bus-Management Functions

SELECT-MODE CONTROL TABLE

CONTROL		OPERATION	
SAB	**SBA**	**A BUS**	**B BUS**
L	L	Real-time B to A bus	Real-time A to B bus
L	H	FIFO B to A bus	Real-time A to B bus
H	L	Real-time B to A bus	FIFO A to B bus
H	H	FIFO B to A bus	FIFO A to B bus

OUTPUT-ENABLE CONTROL TABLE

CONTROL		OPERATION	
DIR	**$\overline{OE}$**	**A BUS**	**B BUS**
X	H	Input	Input
L	L	Output	Input
H	L	Input	Output

Figure 1. Bus-Management Functions (Continued)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage: Control inputs . . . . 7 V
I/O ports . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . 5.5 V
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Maximum junction temperature, T_J . . . . 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			′ACT2236-20		′ACT2236-30		′ACT2236-40		′ACT2236-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current	A or B ports		−8		−8		−8		−8	mA
		Status flags		−8		−8		−8		−8	
I_{OL}	Low-level output current	A or B ports		16		16		16		16	mA
		Status flags		8		8		8		8	
f_{clock}	Clock frequency	LDCKA or LDCKB		50		33		25		16.7	MHz
		UNCKA or UNCKB		50		33		25		16.7	
t_w	Pulse duration	$\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ low	20		20		25		25		ns
		LDCKA or LDCKB low	8		10		14		20		
		LDCKA or LDCKB high	8		10		14		20		
		UNCKA or UNCKB low	8		10		14		20		
		UNCKA or UNCKB high	8		10		14		20		
		$\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ high	10		10		10		10		
t_{su}	Setup time	Data before LDCKA or LDCKB↑	4		4		5		5		ns
		Define AF/AE: D0−D8 before $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$↓	5		5		5		5		
		Define AF/AE: $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$↓ before $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	7		7		7		7		
		Define AF/AE (default): $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ high before $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	5		5		5		5		
		$\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ inactive (high) before LDCKA or LDCKB↑	5		5		5		5		
t_h	Hold time	Data after LDCKA or LDCKB↑	1		1		2		2		ns
		Define AF/AE: D0−D8 after $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$↓	0		0		0		0		
		Define AF/AE: $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ low after $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	0		0		0		0		
		Define AF/AE (default): $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ high after $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	0		0		0		0		
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = − 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	I/O ports	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	$V_I = V_{CC}$ or 0				±5	μA
I_{OZ}		V_{CC} = 5.5 V,	$V_O = V_{CC}$ or 0				±5	μA
I_{CC}‡		$V_I = V_{CC}$ − 0.2 V or 0				10	400	μA
ΔI_{CC}§	DIR, $\overline{OE}$	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2	mA
	Other inputs						1	
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I_{CC} tested with outputs open.
§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	′ACT2236-20			′ACT2236-30		′ACT2236-40		′ACT2236-60		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK		50			33		25		16.7		MHz
	UNCK		50			33		25		16.7		
t_{pd}	LDCK↑, LDCKB↑	B or A	8		23	8	23	8	25	8	27	ns
t_{pd}	UNCKA↑, UNCKB↑	B or A	10	17	25	10	25	10	35	10	45	ns
t_{PLH}	LDCK↑, LDCKB↑	$\overline{EMPTYA}$, $\overline{EMPTYB}$	4		15	4	15	4	17	4	19	ns
t_{PHL}	UNCKA↑, UNCKB↑	$\overline{EMPTYA}$, $\overline{EMPTYB}$	2		17	2	17	2	19	2	21	ns
t_{PHL}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	$\overline{EMPTYA}$, $\overline{EMPTYB}$	2		18	2	18	2	20	2	22	ns
t_{PHL}	LDCK↑, LDCKB↑	$\overline{FULLA}$, $\overline{FULLB}$	4		15	4	15	4	17	4	19	ns
t_{PLH}	UNCKA↑, UNCKB↑	$\overline{FULLA}$, $\overline{FULLB}$	4		15	4	15	4	17	4	19	ns
t_{PLH}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	$\overline{FULLA}$, $\overline{FULLB}$	2		15	2	15	2	17	2	19	ns
t_{PLH}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	AF/AEA, AF/AEB	2		15	2	15	2	17	2	19	ns
t_{PLH}	LDCK↑, LDCKB↑	HFA, HFB	2		15	2	15	2	17	2	19	ns
t_{PHL}	UNCKA↑, UNCKB↑	HFA, HFB	4		19	4	19	4	21	4	23	ns
t_{PHL}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	HFA, HFB	1		15	1	15	1	17	1	19	ns
t_{pd}	SAB or SBA¶	B or A	1		11	1	11	1	13	1	15	ns
t_{pd}	A or B	B or A	1		11	1	11	1	13	1	15	ns
t_{pd}	LDCK↑, LDCKB↑	AF/AEA, AF/AEB	2		19	2	19	2	21	2	23	ns
t_{pd}	UNCKA↑, UNCKB↑	AF/AEA, AF/AEB	2		19	2	19	2	23	2	23	ns
t_{en}	DIR, $\overline{OE}$	A or B	2		12	2	12	2	14	2	16	ns
t_{dis}	DIR, $\overline{OE}$	A or B	1		10	1	10	1	12	1	14	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per 1K bits	Outputs enabled	C_L = 50 pF, f = 5 MHz	71	pF
		Outputs disabled		57	

TYPICAL CHARACTERISTICS

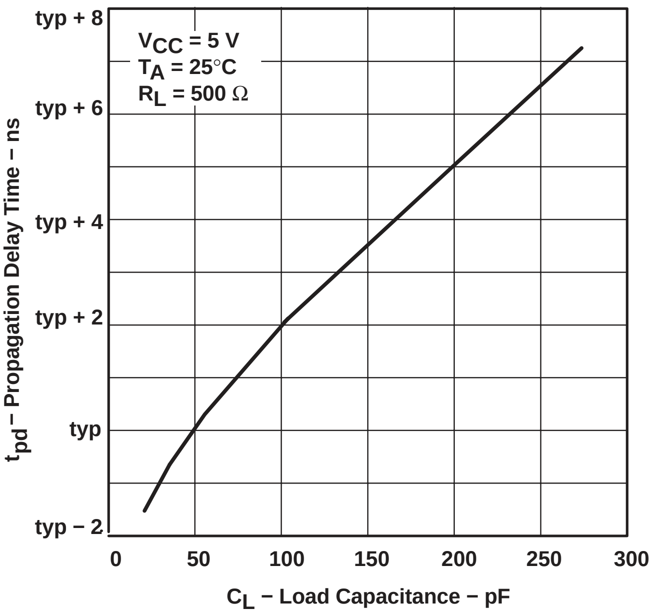


Figure 2

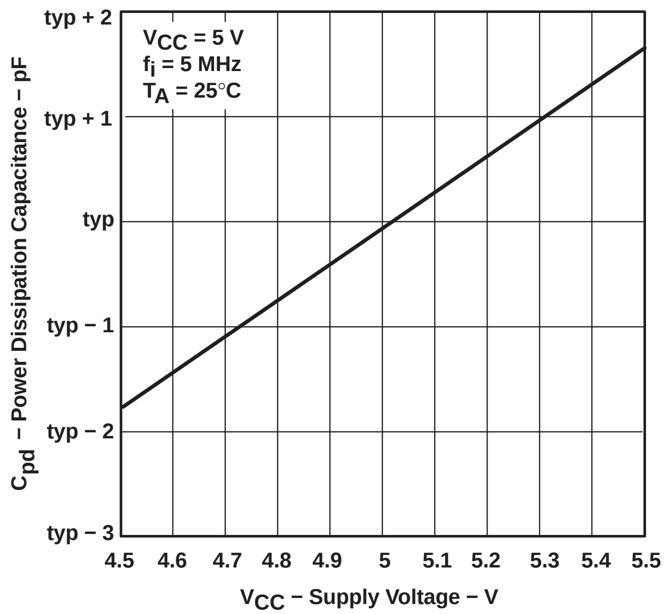


Figure 3

calculating power dissipation

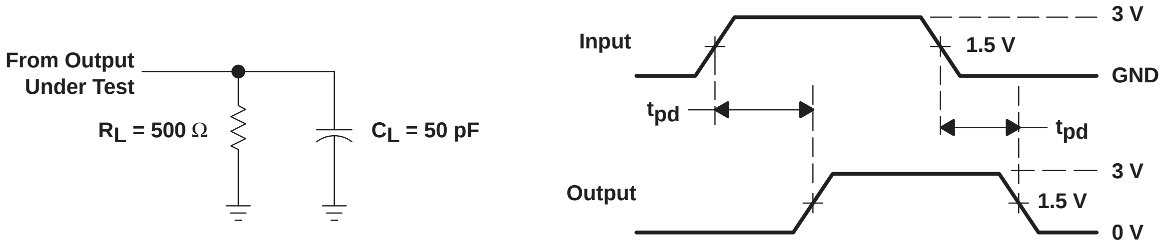
The maximum power dissipation (P_T) can be calculated by:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

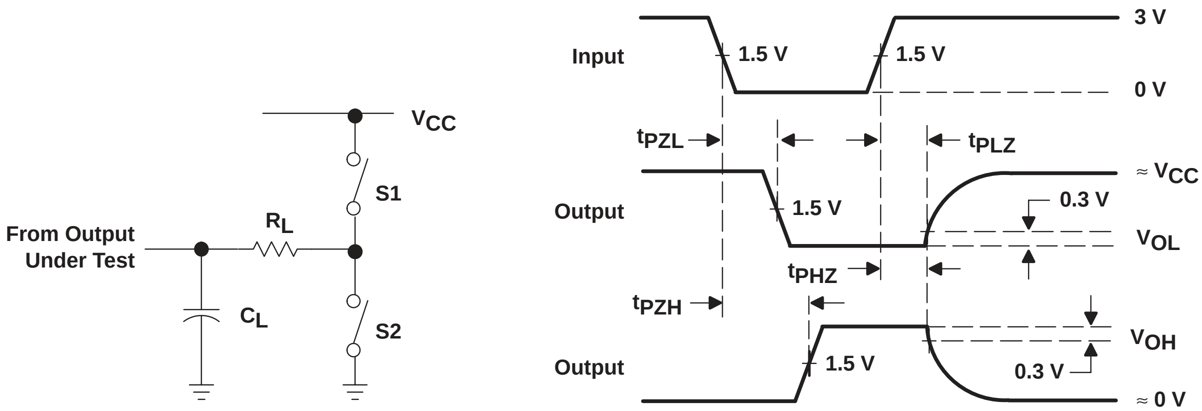
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 4. Standard CMOS Outputs (All Flags)



LOAD CIRCUIT

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

PARAMETER		R_L	C_L †	S1	S2
t_{en}	t_{PZH}	500 Ω	50 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		−	50 pF	Open	Open

† Includes probe and test-fixture capacitance

Figure 5. 3-State Outputs (A0−A8, B0−B8)

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74ACT2236-20FN	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI
SN74ACT2236-30FN	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI
SN74ACT2236-40FN	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI
SN74ACT2236-60FN	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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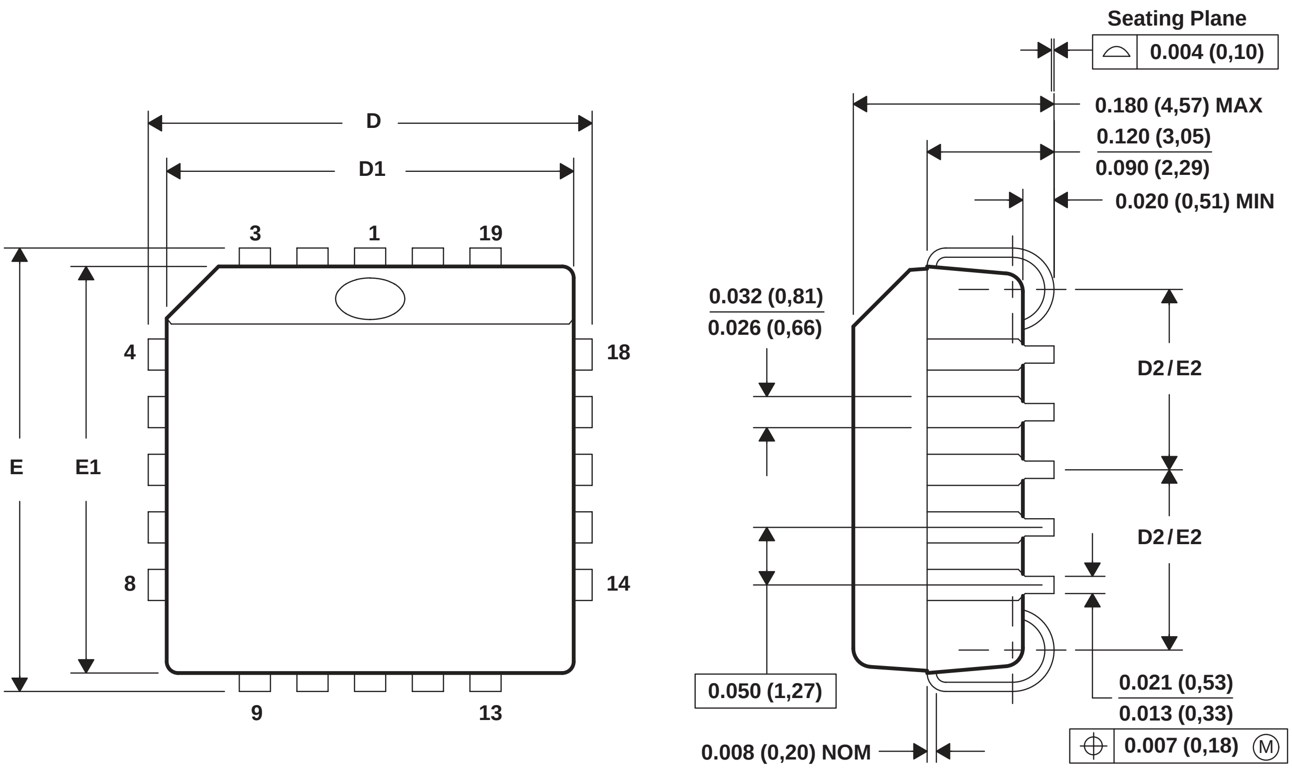
MPLC004A – OCTOBER 1994

FN (S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D / E		D1 / E1		D2 / E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018